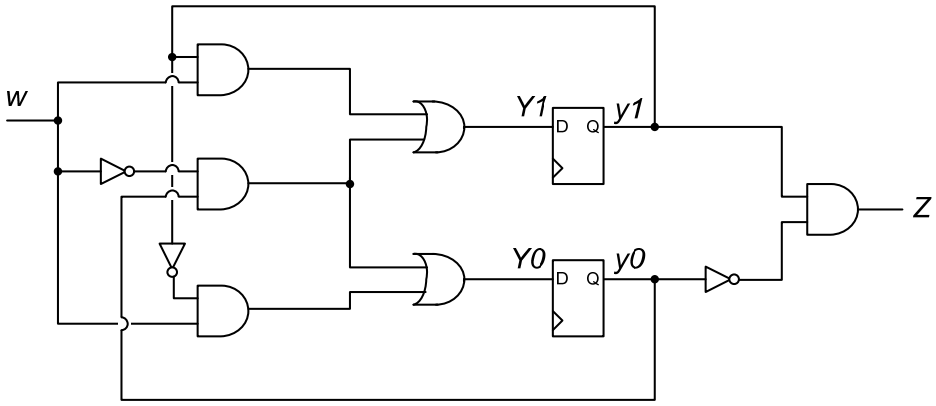
UNIVERSITY OF BRITISH COLUMBIA
ELECTRICAL AND COMPUTER ENGINEERING
CPEN 311: Digital Systems Design

Practice Assignment 3: Timing

This assignment will NOT be handed in. Answers will be posted.

1. Consider the following circuit. The clock connections to the flip-flops are not shown (both flip-flops are clocked by the same clock).



Assume the following:

Delay of each logic gate: 1 ns
Set up time of each flip-flop: 0.2 ns
Hold time of each flip-flop: 0 ns
Maximum Clk-to-Q delay of each flip-flop: 0.5 ns
Minimum Clk-to-Q delay of each flip-flop: 0.1 ns

a) What is the maximum frequency of the clock in this circuit (in Mhz) ?
b) Suppose the hold time is not 0. What is the largest value for the hold time for which this circuit will still function properly?
c) Write a synthesizable VHDL specification of the above circuit using a single process and no "port map"s.

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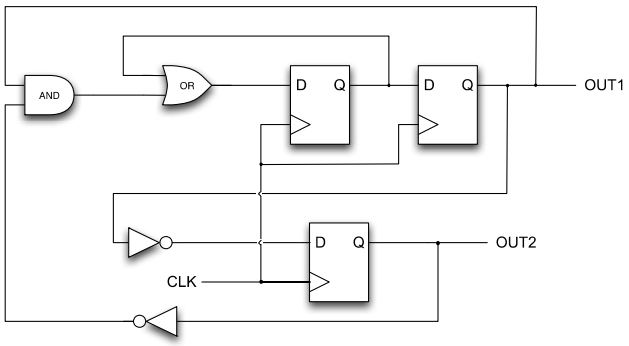
2. Consider the following circuit:



Assume the following:

- Delay of each inverter: 0.6 ns
- Delay of each AND and OR gate: 1 ns
- Set up time of each flip-flop: 0.3 ns
- Hold time of each flip-flop: 0.2 ns
- Maximum Clk-to-Q delay of each flip-flop: 0.5 ns
- Minimum Clk-to-Q delay of each flip-flop: 0 ns

Answer the following questions:

a) What is the maximum frequency of this circuit (in Mhz) ?
b) Suppose the minimum Clk-to-Q delay is not 0 ns. What is the smallest value of the minimum Clk-to-Q delay such that there is no hold time violation in this circuit?

3. Suppose a high-end microprocessor is to run at 2Ghz (remember than 2Ghz = 2000 Mhz). Further, suppose the delay of each logic gate is 0.08 ns. Assume the set-up, hold, and Clk-to-Q times of all flip flops are 0. What is the maximum number of gates that can appear in the critical path of this circuit? (note: all the numbers in this question are realistic, and the answer has a huge effect on the logic design of high-end microprocessors… you'll learn more about this in CPEN 411 if you take it).

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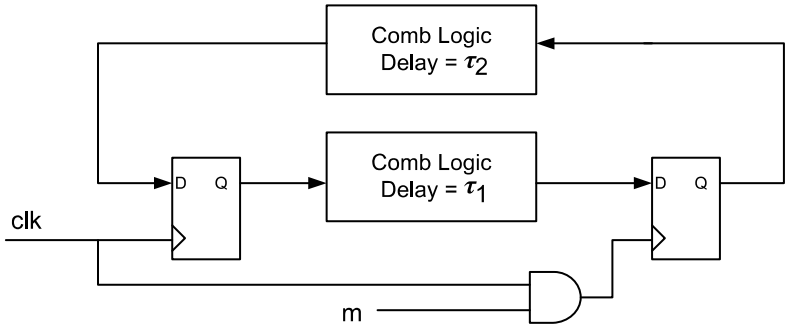
4. Consider the following circuit. Note that the second flip-flop's clock input is derived from the clock signal and input signal m (so the clock only goes high when m is high).



Assume the following:

Set up time of each flip-flop: 0.3 ns
Hold time of each flip-flop: 0.2 ns
Maximum Clk-to-Q delay of each flip-flop: 0.5 ns
Minimum Clk-to-Q delay of each flip-flop: 0.25 ns
Delay of the AND gate: 1 ns

Suppose we want to run this circuit at 100 Mhz. Answer the following questions:

a) What is the *maximum* possible value of τ_1 that the circuit is guaranteed to work correctly at 100 Mhz? Show your work. If there is no maximum, write ∞.

b) What is the *maximum* possible value of τ_2 for the circuit to work correctly at 100 Mhz? Show your work. If there is no maximum, write ∞.

c) What is the *minimum* possible value of τ_1 for the circuit to work correctly at 100 Mhz? Show your work. If there is no minimum, write 0.

d) What is the *minimum* possible value of τ_2 for the circuit to work correctly at 100 Mhz? Show your work. If there is no minimum, write 0.