Altera DE0 Companion Board
for ELEC 371 Laboratory Activity

Technical design and initial implementation by
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This document provides a description of the Altera DE0 Companion Board that was designed, implemented, and demonstrated by three graduates of Queen's University as their capstone undergraduate project during the 2014-2015 academic session in the Department of Electrical and Computer Engineering. The purpose of the Altera DE0 Companion Board is to enhance learning in the course *ELEC 371 Microprocessor Interfacing and Embedded Systems*.

The graduates responsible for the design of the board have agreed to provide their intellectual property for educational use in undergraduate engineering courses at Queen's University, and their contribution is acknowledged in this document and through text printed on the hardware.

This document has been prepared by Dr. Naraig Manjikian for reference purposes to provide students in ELEC 371 with relevant details for laboratory work. The technical basis of this document is the circuit schematic generated by the designers of the Companion Board, and additional documentation from vendors of the chips used on the Companion Board.

The source of funding to enable the fabrication of custom printed-circuit boards and the purchase of components for populating fabricated boards is the Better Equipment Donation fund of the Queen's University Engineering Society that represents undergraduate students in the Faculty of Engineering and Applied Science.

The completion of the effort to produce boards for laboratory use also relied on contributions from technical staff members, namely Roy Campsall for final assembly of boards and components, and Steve Humphrey and Gary Neff for logistics related to boards/components.

Background: Since 2012, laboratory activity in ELEC 371 has relied on the Altera DE0 board with a programmable logic chip in which a computer system can be embedded. The DE0 board is also used in laboratory activity for two prerequisite courses, *ELEC 271 Digital Systems* and *ELEC 274 Computer Architecture*. The purchase of a large number of DE0 boards for laboratory activity in all three courses was supported in part by the Better Equipment Donation fund of the Engineering Society. The DE0 board provides a common platform for practical learning of digital logic, computer organization, and hardware interfacing with the benefits of low per-board cost and the simplicity of a single USB cable connection to an attached computer for both power and communication.

The DE0 board provides digital interfaces such as switches, pushbuttons, individual LEDs, and seven-segment LED displays, but it lacks analog interfacing features. The DE0 Companion Board is designed to be connected to the Altera DE0 board and provide additional interfacing capabilities, primarily analog input/output but also a connector for a standard servomotor that uses pulse-width-modulated (PWM) digital signalling.

Due the manner in which Altera Corp. has designed boards and embedded computer systems for educational use in university-level engineering courses, the Companion Board can, in fact, be connected to several of the DE*x* boards, namely the DE0, DE1, and DE2 products. The computer systems that are embedded into the programmable logic chip in these boards are compatible with each other, and the parallel ports that are associated with the physical connectors have the same address and pin assignments. Despite this broader compatibility, this document will emphasize the use of the Companion Board with the Altera DE0 board because the DE0 board is presently the only board that is used in the laboratory activity for ELEC 371 (and also the prerequisite courses ELEC 271 and ELEC 274).

Design Features: The Companion Board connects to the Altera DE0 board through a 40-pin ribbon cable. A parallel port interface enables the computer system embedded in the programmable logic chip on the DE0 board to access the circuitry on the Companion Board. The Companion Board includes the following features:

- analog input from a photoresistor
- analog input from a potentiometer
- analog inputs from a three-axis accelerometer to sense physical orientation
- analog output to an LED to control its brightness
- digital PWM output for servomotor control (relying on an external battery pack for power to the motor)

There are also connection points on the Companion Board for five additional analog inputs and three additional analog outputs.

There are three chips that provide analog-to-digital-conversion (ADC) capability. Only one chip is active at any time to provide conversion results as a digital value between 0 and 255 to correspond to a voltage input between 0 and 3.3 volts. The digital value from the active ADC chip is available as an input from the Companion Board to the DE0 board. To increase the total number of possible analog input sources from only three (one per chip) to a maximum of 12, analog multiplexer chips allow one of four different voltage inputs to be selected as the analog input to each ADC chip. Software must select both the multiplexed analog input and the active ADC chip to specify which of the 12 possible sources is desired for conversion.

There is one chip that provides digital-to-analog-conversion (DAC) capability. This chip accepts a digital value between 0 and 255 and provides a corresponding output voltage between 0 and 3.3 volts on one of four output pins. Software must specify which output pin should be affected.

The physical connector on the Companion Board for servomotor control has three lines: ground, power, and PWM. The ground line is common with the Companion Board. The power line, however, relies solely on external battery pack so that the motor power is distinct from the power for the chips on the board. The PWM control line is directly connected to one of the *data* lines of the 40-pin connection to the DE0 board. It is therefore the software executing on the embedded computer system in the programmable logic chip that must control the 0 or 1 setting on the appropriate parallel port bit to obtain a proper PWM signal for a connected servomotor. (A custom hardware interface in the programmable logic chip could also be designed to produce the PWM signal without direct reliance on software, and a custom computer system could also be designed to use such a custom hardware interface.)

Hardware Interface of Companion Board: The interface between the DE0 board and the Companion Board is a 40-pin connection for *power* (5V, 3.3V, ground) and *data* (32 bits). A parallel ribbon cable is connected between two 40-pin headers on the boards. ***This document assumes that header JP1 on the DE0 board is used (i.e., the leftmost expansion header).*** Although the second expansion header could be used, JP1 is the recommended and expected connector in the discussion that follows.

On the DE0 side, the 32 *data* lines indicated above are directly and permanently connected to 32 specific pins of the programmable logic chip. On the Companion Board side, these *data* lines are distributed individually or in groups to different chips for control, status, and data.

Within the programmable logic chip, the Altera-provided DE0 Basic Computer and DE0 Media Computer both provide the same JP1 parallel port interface beginning at address 0x10000060 with four 32-bit registers for input/output data, pin direction control, pin interrupt masking, and pin edge-detect control. Software that executes on the embedded computer system can read and write the parallel port registers for control, status, and data interactions with the Companion Board. (In fact, any custom embedded computer or any pure hardware implemented as custom logic within the chip can interact with the Companion Board, provided that the interaction uses the 32 relevant pins of the logic chip in a manner that conforms to the design and operation of the hardware on the Companion Board.)

The Companion Board uses the 32 *data* lines from the DE0 board in the manner shown in the schematic view of Figure 1 that reflects the physical connector. The corresponding 32 data bits of the embedded parallel port are shown in an abstract form in Figure 2 that is more convenient for guiding the development of software. Figure 2 also indicates the data direction for each line.

Companion board usage	Port/power usage	JP1 header pins		Port/power usage	Companion board usage
––	––	1	2	D0	ADC_data_bit0
––	––	3	4	D1	ADC_data_bit1
ADC_data_bit2	D2	5	6	D3	ADC_data_bit3
ADC_data_bit4	D4	7	8	D5	ADC_data_bit5
ADC_data_bit6	D6	9	10	D7	ADC_data_bit7
––	5V	11	12	GND	––
ADC_read_n	D8	13	14	D9	(unused D9)
(unused D10)	D10	15	16	D11	ADC_done0_n
ADC_done1_n	D12	17	18	D13	ADC_done2_n
––	––	19	20	D14	DAC_data_bit0
––	––	21	22	D15	DAC_data_bit1
DAC_data_bit2	D16	23	24	D17	DAC_data_bit3
DAC_data_bit4	D18	25	26	D19	DAC_data_bit5
DAC_data_bit6	D20	27	28	D21	DAC_data_bit7
––	3.3V	29	30	GND	––
DAC_select0	D22	31	32	D23	DAC_select1
DAC_write_n	D24	33	34	D25	ADC_select0
ADC_select1	D26	35	36	D27	MUX_select1
MUX_select0	D28	37	38	D29	(unused D29)
(unused D30)	D30	39	40	D31	servo

Figure 1: Physical pins of the JP1 header on the DE0 board and their usage

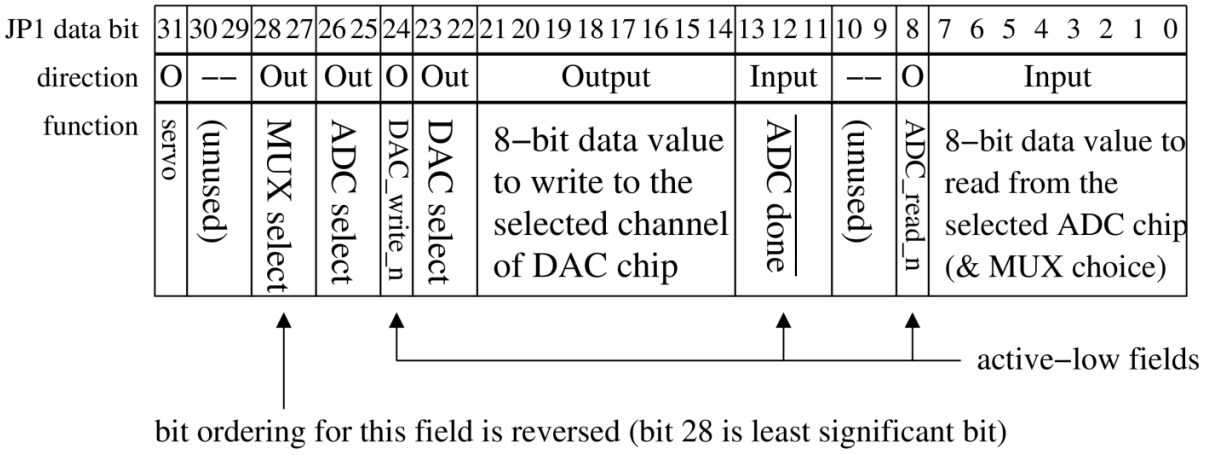

Figure 2: Usage of JP1 data bits for Companion Board

In software, the initialization code of a program that uses the Companion Board must configure the parallel pin data directions as indicated in Figure 2. Because of the design of the Companion Board, that configuration must remain unchanged as the main code of the program executes.

Three of the fields in Figure 2 are identified as being active-low. The software that uses the Companion Board must be coded in a manner that reflects this mode of operation.

In the discussion that follows, the interpretation of *input* and *output* direction is from the perspective of the DE0 board and the software that executes on the computer system embedded in the programmable logic chip. Figure 2 reflects these input and output directions.

All accesses to the 32-bit data register of the parallel port in the embedded computer system must be done appropriately to involve only the subset of bits that are relevant to a particular interaction without affecting other bits. AND/OR operations must be used along with shift operations to isolate the relevant subset of bits to be read or modified.

The fields shown in Figure 2 are described below.

- *ADC_data*: 8-bit input data obtained from analog-to-digital conversion (ADC); depends on the selected ADC chip and the selected input to that chip through analog multiplexer configuration
- *ADC_select*: 2-bit field with three valid binary settings (00, 01, 10) to select one of the three ADC chips on the Companion Board for the next conversion
- *MUX_select*: 2-bit field with four valid binary settings (00, 01, 10, 11) to select the voltage source for the selected ADC chip through analog multiplexing; not all of the multiplexer inputs have a connected source; Figure 2 indicates that the bit ordering for this field is reversed, and software must be prepared accordingly
- *ADC_read_n*: active-low control line that initiates conversion for the selected ADC chip; must be kept low during conversion to allow determination of completion and to make converted digital value available as an input from the Companion Board
- *ADC_done_n*: 3-bit active-low field with each bit dedicated to one of the three ADC chips; software must check for a low value on the bit corresponding to the selected chip to determine when the conversion has been completed
- *DAC_data*: 8-bit output data provided to the Companion Board for digital-to-analog conversion (DAC); the value determines the voltage for the selected DAC channel
- *DAC_select*: 2-bit field with four valid binary settings (00, 01, 10, 11) to select one of four output channels of the DAC chip for the next conversion (the LED is channel 0)
- *DAC_write_n*: active-low control line for conversion of the selected DAC channel; if this bit is kept low, the DAC chip operates in a ‘transparent’ mode where the selected voltage output changes shortly after any change in the output data provided on the *DAC_data* lines; on the other hand, a ‘latched’ mode can be utilized where a low-to-high transition captures the current *DAC_data* value, and the voltage output for the selected channel changes and then remains stable to correspond to the latched data

The combination of the *ADC_select* and *MUX_select* fields allows for up to 12 different sources to be selected for analog-to-digital conversion. For the present version of the Companion Board design, however, only 10 of the 12 possible sources are directly accessible by software. Five of these 10 accessible sources are actually connection points on the Companion Board to external voltage sources for future expansion. Figure 3 summarizes the necessary bit settings for *ADC_select* and *MUX_select* to correspond to the 10 accessible voltage sources. As stated earlier in this document, the bit ordering for the *MUX_select* is reversed in the hardware, but Figure 3 indicates the necessary bit settings for direct use by software (i.e., do not reorder the given bit values; apply them *directly as given in Figure 3* to the *MUX_select* field in the same manner as other fields).

Feature	MUX_select	ADC_select
accelerometer x−axis	0 0	0 0
<unavailable>	0 1	
external input	1 0	
external input	1 1	
accelerometer y−axis	0 0	0 1
<unavailable>	0 1	
external input	1 0	
external input	1 1	
accelerometer z−axis	0 0	1 0
photoresistor	0 1	
potentiometer	1 0	
external input	1 1	

Figure 3: *ADC_select* and *MUX_select* bit settings for different analog sources

References: The following documents served as the basis for information in this document.

David King, Brendan Montgomery, and Matt Sippert, *ELEC 490/498 Final Report: Companion Board for Altera DEx*, Department of Electrical and Computer Engineering, Queen's University, March 2015. (The circuit schematic in this document was the primary reference.)

Texas Instruments, *ADC0820-N 8-Bit High Speed µP Compatible A/D Converter with Track/Hold Function*, March 2013. (The primary reference was Figure 4 in this document that indicates the timing characteristics and the active-low mode of operation for the various signals.)

Texas Instruments, *TLC7226C/TLC7226I/TLC7226M Quadruple 8-bit Digital-to-Analog Converters*, April 2009. (The primary reference was Table 2 in this document that indicates the active-low nature of the write control signal, and also the difference between operating the chip in latched and transparent modes.)