



THOMAS KOETTING

Computer Engineering Student at the University of Kansas

Computer Engineering Junior with hands-on Verilog RTL, FPGA, and PCB/SPICE labs; grounded in CMOS/VLSI and computer architecture. NSF STEM Scholars research; IEEE KU. Targeting Spring/Summer 2026 hardware/semiconductor design internship.

EDUCATION

CONTACT

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UNIVERSITY OF KANSAS
Aug 2024 - May 2027

BS in Computer Engineering

B.S. in Computer Engineering in progress; interests in electronics design, VLSI/digital systems, and semiconductor fundamentals. Active IEEE KU Chapter member.

Cumulative GPA: 3.70

JOHNSON COUNTY
COMMUNITY COLLEGE
Aug 2022 - May 2024

No Degree Commitment

Completed transfer coursework in engineering/CS and was selected for the NSF JCCC STEM Scholars program. Conducted a research project applying game-theory models to web interaction; summary PDF linked on portfolio. Was selected for honor roll 3/4 semesters.

PROJECTS

- Used Vivado to implement Verilog RTL on a Xilinx FPGA dev board: created XDC pin/timing constraints, ran synthesis & place-and-route, generated bitstreams, and verified on hardware (switches/LEDs/UART); met timing constraints.
- Built self-checking testbenches with Verilator for independent Verilog modules; wrote small C/Makefile harnesses, generated waveform traces for debug, and iterated until functional correctness.
- Wrote both high-level behavioral and low-level structural Verilog: parameterized modules (generate/for), clean FSMs (always_ff/case), correct nonblocking sequential logic, and simple gate-level compositions.
- Performed FPGA bring-up and board I/O integration: debounced inputs, synchronized resets, and validated peripheral behavior with simple test firmware/patterns.
- Prototyped on breadboard and soldered through-hole/basic SMD components; did rework and continuity checks; followed basic ESD and inspection practices.

WORK EXPERIENCE

- Processed ~30–100 transactions/day (deposits, withdrawals, cashier's checks, wires) with 100% adherence to bank policies; balanced a \$6k-12k drawer with little to no discrepancies over ~28 months.
- Verified IDs and monitored transactions to meet BSA/AML, CIP, and Reg CC requirements; flagged suspicious activities and followed escalation procedures
- Recognized as 3rd best part-time teller bank wide (out of 20+ branches) two years in a row
- Cross-trained new tellers on cash balancing, transaction codes, and compliance checklists

SKILLS

- **HDL & EDA:** Verilog (RTL/testbenches), Vivado, Verilator, GTKWave
- **EE Tools:** LTspice/Ngspice, oscilloscopes, logic analyzers, basic PCB rework
- **Programming:** C, Python
- **Concepts:** FSMs, synchronization/debouncing, CMOS/VLSI basics
- **Other:** LaTeX