TPS7B82-Q1 300mA、高電圧、超低 I_Q、低ドロップアウト・レギュレータ

1 特長

- 車載アプリケーション用に AEC-Q100 認定取得済み
  - 温度グレード 1:–40℃ ≤ T_A ≤ 125℃
  - 温度グレード 0:–40℃ ≤ T_A ≤ 150℃
- 広い接合部温度範囲:
  - グレード 1:–40℃ ≤ T_J ≤ 150℃
  - グレード 0:–40℃ ≤ T_J ≤ 165℃
- 低い静止電流 I_Q
  - シャットダウン時 I_Q:300nA
  - 軽負荷時:2.7µA (標準値)
  - 軽負荷時:5µA (最大値)
- 3V～40V の広い V_{IN} 入力電圧範囲、最大 45V の過渡電圧に対応
- 最大出力電流:300mA
- 2% の出力電圧精度
- 最大ドロップアウト電圧:固定 5V 出力バージョンで、負荷電流 200mA 時に 700mV
- 低 ESR (0.001Ω～5Ω) のセラミック出力コンデンサ (1µF～200µF) で安定
- 2.5V、3.3V、5V の固定出力電圧
- パッケージ
  - 8 ピン HVSSOP、$R_{\theta JA}$ = 63.9℃/W
  - 6 ピン WSON、$R_{\theta JA}$ = 72.8℃/W
  - 5 ピン TO-252、$R_{\theta JA}$ = 31.1℃/W
  - 14 ピン HTSSOP、$R_{\theta JA}$ = 52.0℃/W

2 アプリケーション

- 車載ヘッド・ユニット
- テレマティクス制御ユニット
- ヘッドライト
- 車体制御モジュール
- インバータおよびモータ制御

3 概要

車載用のバッテリ接続アプリケーションでは、消費電力を削減し、バッテリ駆動時間を延長するため、静止電流 (I_Q) が低いことが重要です。常時オンのシステムには超低静止電流 I_Q が不可欠です。

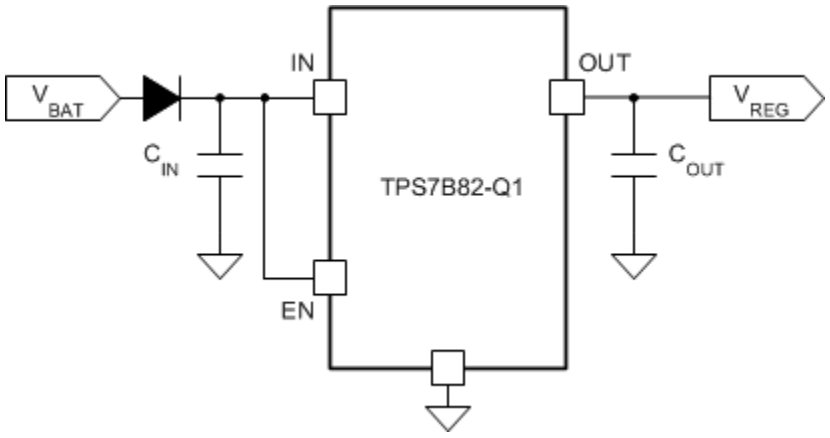
TPS7B82-Q1 は低ドロップアウトのリニア・レギュレータであり、3V～40V の広い入力電圧範囲 (45V の負荷ダンプ保護) で動作するよう設計されています。TPS7B82-Q1 は最低 3V で動作するため、コールド・クランクおよび始動 - 停止状態の間も動作を継続できます。軽負荷時の標準静止電流がわずか 2.7µA なので、スタンバイ・システムのマイクロコントローラ (MCU) や CAN/LIN トランシーバの電源として最適なソリューションです。

このデバイスには、短絡および過電流保護機能が内蔵されています。このデバイスは –40℃～+125℃の周囲温度、–40℃～+150℃の接合部温度で動作します。また、このデバイスは高放熱パッケージを採用しているため、デバイスの電力消費が大きくても持続的に動作できます。これらの特長から、このデバイスは各種の車載アプリケーションの電源として設計されていると言えます。

製品情報(1)

部品番号	パッケージ	本体サイズ (公称)
TPS7B82-Q1	HVSSOP (8)	3.00mm × 3.00mm
	WSON (6)	2.00mm × 2.00mm
	TO-252 (5)	6.10mm × 6.60mm
	HTSSOP (14)	5.00mm × 4.40mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



代表的なアプリケーション回路図

Table of Contents

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision H (March 2021) to Revision I (August 2021) **Page**

- Changed I_Q parameter maximum specifications from *3.5 µA* to *5 µA* and from *4.5 µA* to *6.5 µA* in the *Electrical Characteristics: Grade 0 Options* table ... 6
- Changed $V_{(Load-Reg)}$ parameter maximum specification from *10 mV* to *20 mV* in the *Electrical Characteristics: Grade 0 Options* table ... 6
- Changed V_{OUT} parameter test condition from *40 V* to *14 V* in the *Electrical Characteristics: Grade 0 Options* table ... 6

Changes from Revision G (July 2020) to Revision H (March 2021) **Page**

- ドキュメントに PWP (HTSSOP) パッケージを追加 ... 1
- 「*特長*」セクションにグレード 0 の情報を追加 ... 1
- 「*特長*」セクションから熱抵抗の箇条書き項目を削除 ... 1
- 「*パッケージ*」の*箇条書き*の TO-252 の箇条書き副項目の $R_{\theta JA}$ 定格を 38.8°C/W から 31.1°C/W に変更 ... 1
- Added grade 0 information to *junction temperature* parameter in *Absolute Maximum Ratings* ... 4
- Added grade 0 information to *Recommended Operating Conditions* table ... 4
- Added *grade 1 options* to condition statement of *Electrical Characteristics* table ... 5
- Added *Electrical Characteristics: Grade 0 Options* table ... 6

5 Pin Configuration and Functions

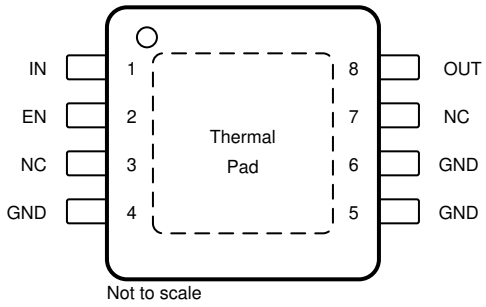


図 5-1. DGN Package, 8-Pin HVSSOP PowerPAD™, Top View

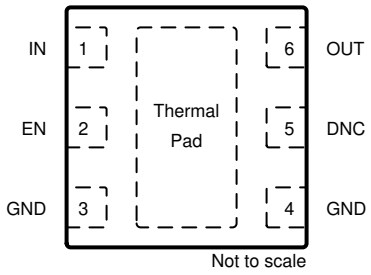


図 5-2. DRV Package, 6-Pin WSON PowerPAD™, Top View

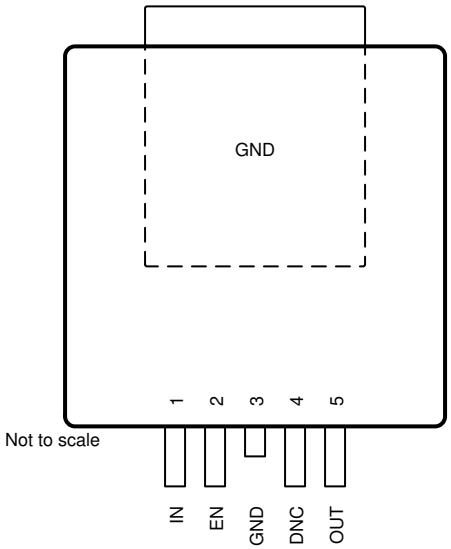


図 5-3. KVU Package, 5-Pin TO-252, Top View

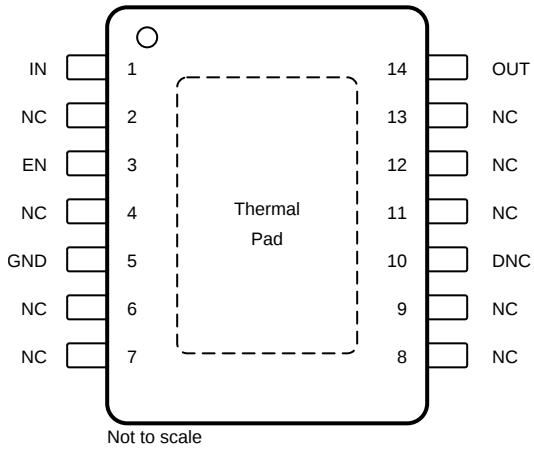


図 5-4. PWP Package, 14-Pin HTSSOP, Top View

NC – No internal connection

表 5-1. Pin Functions

PIN					I/O	DESCRIPTION
NAME	NO.					
	DGN	DRV	KVU	PWP		
DNC	—	5	4	10	—	Do not connect to a biased voltage. Tie this pin to ground or leave floating.
EN	2	2	2	3	I	Enable input pin
GND	4, 5, 6	3,4	3, TAB	5	—	Ground reference
IN	1	1	1	1	I	Input power-supply pin
NC	3, 7	—	—	2, 4, 6, 7, 8, 9, 11, 12, 13	—	Not internally connected
OUT	8	6	5	14	O	Regulated output voltage pin
Thermal pad					—	Connect the thermal pad to a large-area GND plane for improved thermal performance.

6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
V_{IN}	Unregulated input(3)	–0.3	45	V
V_{EN}	Enable input(3)	–0.3	V_{IN}	V
V_{OUT}	Regulated output	–0.3	7	V
T_J	Junction temperature (grade 1)	–40	150	°C
	Junction temperature (grade 0)	–40	165	
T_{stg}	Storage temperature range	–40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND.
(3) Absolute maximum voltage, withstand 45 V for 200 ms.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1) HBM ESD classification level H2		±2000	V
		Charged-device model (CDM), per AEC Q100-011 CDM ESD classification level C3B	Corner pins (1, 4, 5, and 8)	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Unregulated input voltage	3	40	V
V_{EN}	Enable input voltage	0	V_{IN}	V
C_{OUT}	Output capacitor requirements(1)	1	200	µF
ESR	Output capacitor ESR requirements(2)	0.001	5	Ω
T_A	Ambient temperature (grade 1)	–40	125	°C
	Ambient temperature (grade 0)	–40	150	
T_J	Junction temperature (grade 1)	–40	150	°C
	Junction temperature (grade 0)	–40	165	

(1) The output capacitance range specified in the table is the effective value.
(2) Relevant equivalent series resistance (ESR) value at f = 10 kHz.

6.4 Thermal Information

THERMAL METRIC[1]		TPS7B82-Q1				UNIT
		DGN (HVSSOP)	DRV (WSON)	KVU (TO-252)	PWP (HTSSOP)	
		8 PINS	6 PINS	5 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	63.9	72.8	31.1	52.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	50.2	85.8	39.9	48.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22.6	37.4	9.9	28.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.8	2.7	4.2	2.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	22.3	37.3	9.9	28.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	12.1	13.8	2.8	10.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics: Grade 1 Options

V_{IN} = 14-V, 10-µF ceramic output capacitor, grade 1 options, T_J = –40°C to +150°C, over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE AND CURRENT (IN)							
V_{IN}	Input voltage			$V_{OUT(NOM)}$ + $V_{(Dropout)}$		40	V
$I_{(SD)}$	Shutdown current	EN = 0 V			0.3	1	µA
$I_{(Q)}$	Quiescent current	V_{IN} = 6 V to 40 V, EN ≥ 2 V, I_{OUT} = 0 mA	DRV and KVU packages		1.9	3.5	µA
			DGN package		1.9	5	
		V_{IN} = 6 V to 40 V, EN ≥ 2 V, I_{OUT} = 0.2 mA	DRV and KVU packages		2.7	4.5	
			DGN package		2.7	6.5	
$V_{(IN, UVLO)}$	V_{IN} undervoltage detection	Ramp V_{IN} down until the output turns OFF				2.7	V
		Hysteresis			200		mV
ENABLE INPUT (EN)							
V_{IL}	Logic-input low level					0.7	V
V_{IH}	Logic-input high level			2			V
REGULATED OUTPUT (OUT)							
V_{OUT}	Regulated output	V_{IN} = V_{OUT} + $V_{(Dropout)}$ to 40 V, I_{OUT} = 1 mA to 300 mA	DRV and KVU packages	–1.5%		1.5%	
			DGN package	–2%		2%	
$V_{(Line-Reg)}$	Line regulation	V_{IN} = 6 V to 40 V, I_{OUT} = 10 mA				10	mV
$V_{(Load-Reg)}$	Load regulation	V_{IN} = 14 V, I_{OUT} = 1 mA to 300 mA	DRV and KVU packages			10	mV
			DGN package			20	

6.5 Electrical Characteristics: Grade 1 Options (continued)

V_{IN} = 14-V, 10-µF ceramic output capacitor, grade 1 options, T_J = –40°C to +150°C, over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$V_{(Dropout)}$	Dropout voltage(1)	$V_{OUT(NOM)}$ = 5 V	I_{OUT} = 300 mA	DRV and KVU packages		630	1170	mV
				DGN package			1000	
			I_{OUT} = 200 mA	DRV and KVU packages		420	780	
				DGN package		400	700	
			I_{OUT} = 100 mA	DRV and KVU packages		210	390	
				DGN package		200	350	
		V_{OUT} = 3.3 V	I_{OUT} = 300 mA	DRV and KVU packages		730	1350	
				DGN package			1250	
			I_{OUT} = 200 mA	DRV and KVU packages		475	900	
				DGN package			850	
			I_{OUT} = 100 mA				450	
I_{OUT}	Output current	V_{OUT} in regulation			0		300	mA
$I_{(CL)}$	Output current limit	V_{OUT} short to 90% × V_{OUT}			310	510	690	mA
PSRR	Power-supply ripple rejection	$V_{(Ripple)}$ = 0.5 V_{PP}, I_{OUT} = 10 mA, frequency = 100 Hz, C_{OUT} = 2.2 µF				60		dB
OPERATING TEMPERATURE RANGE								
$T_{(SD)}$	Junction shutdown temperature					175		°C
$T_{(HYST)}$	Hysteresis of thermal shutdown					20		°C

(1) Dropout is not valid for the 2.5-V output because of the minimum input voltage limits.

6.6 Electrical Characteristics: Grade 0 Options

V_{IN} = 14-V, 10-µF ceramic output capacitor, grade 0 options (PWP package), T_J = –40°C to +165°C, over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE AND CURRENT (IN)						
V_{IN}	Input voltage		$V_{OUT(NOM)}$ + $V_{(Dropout)}$		40	V
$I_{(SD)}$	Shutdown current	EN = 0 V		0.3	1	µA
$I_{(Q)}$	Quiescent current	V_{IN} = 6 V to 40 V, EN ≥ 2 V, I_{OUT} = 0 mA		1.9	5	
		V_{IN} = 6 V to 40 V, EN ≥ 2 V, I_{OUT} = 0.2 mA		2.7	6.5	µA
$V_{(IN, UVLO)}$	V_{IN} undervoltage detection	Ramp V_{IN} down until the output turns OFF			2.7	V
		Hysteresis		200		mV
ENABLE INPUT (EN)						
V_{IL}	Logic-input low level				0.7	V
V_{IH}	Logic-input high level		2			V
REGULATED OUTPUT (OUT)						
V_{OUT}	Regulated output	V_{IN} = V_{OUT} + $V_{(Dropout)}$ to 14 V, I_{OUT} = 1 mA to 300 mA	–1.5%		1.5%	

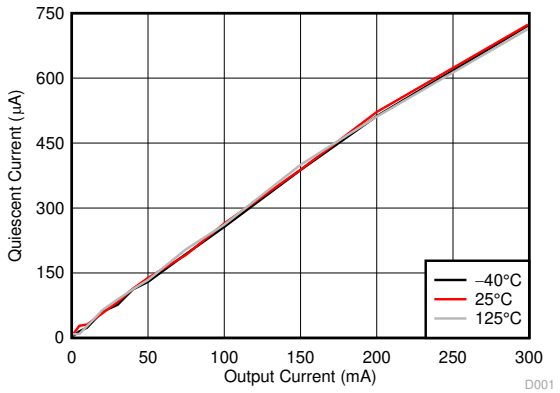
6.6 Electrical Characteristics: Grade 0 Options (continued)

V_{IN} = 14-V, 10-µF ceramic output capacitor, grade 0 options (PWP package), T_J = –40°C to +165°C, over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(Line-Reg)}$	Line regulation	V_{IN} = 6 V to 40 V, I_{OUT} = 10 mA				10	mV
$V_{(Load-Reg)}$	Load regulation	V_{IN} = 14 V, I_{OUT} = 1 mA to 300 mA				20	mV
$V_{(Dropout)}$	Dropout voltage(1)	$V_{OUT(NOM)}$ = 5 V	I_{OUT} = 300 mA		630	1170	mV
			I_{OUT} = 200 mA		420	780	
			I_{OUT} = 100 mA		210	390	
		V_{OUT} = 3.3 V	I_{OUT} = 300 mA		730	1350	
			I_{OUT} = 200 mA		475	900	
			I_{OUT} = 100 mA			450	
I_{OUT}	Output current	V_{OUT} in regulation		0		300	mA
$I_{(CL)}$	Output current limit	V_{OUT} short to 90% × V_{OUT}		310	510	690	mA
PSRR	Power-supply ripple rejection	$V_{(Ripple)}$ = 0.5 V_{PP}, I_{OUT} = 10 mA, frequency = 100 Hz, C_{OUT} = 2.2 µF			60		dB
OPERATING TEMPERATURE RANGE							
$T_{(SD)}$	Junction shutdown temperature				185		°C
$T_{(HYST)}$	Hysteresis of thermal shutdown				20		°C

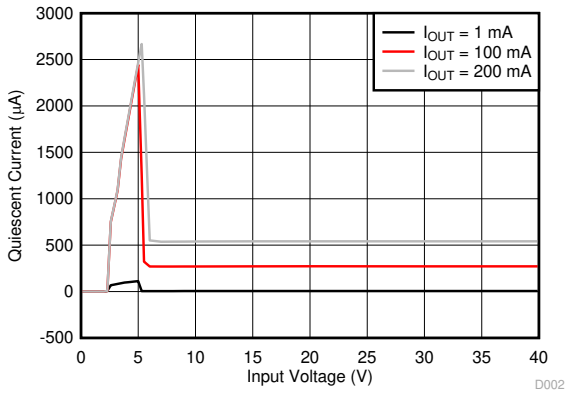
6.7 Typical Characteristics

V_{IN} = 14 V, V_{EN} ≥ 2 V, T_J = –40°C to 150°C (unless otherwise noted)



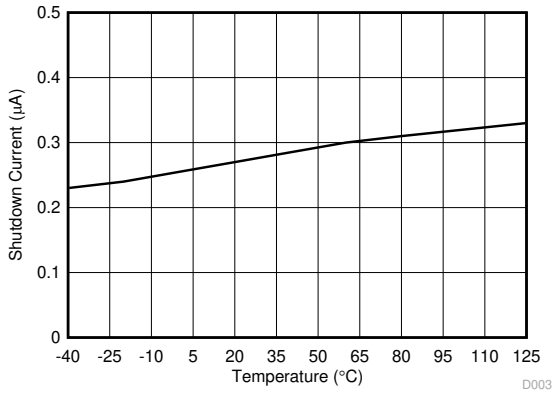
V_{OUT} = 5 V

図 6-1. Quiescent Current vs Output Current



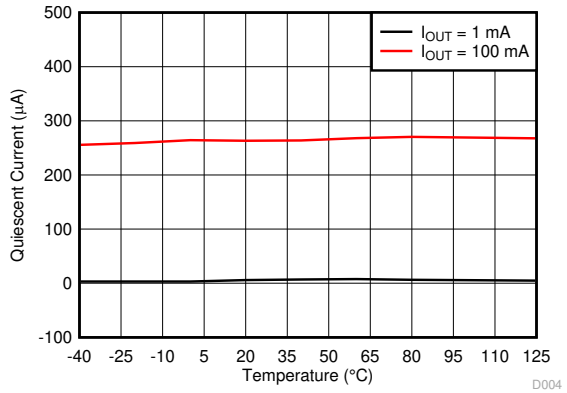
V_{OUT} = 5 V

図 6-2. Quiescent Current vs Input Voltage



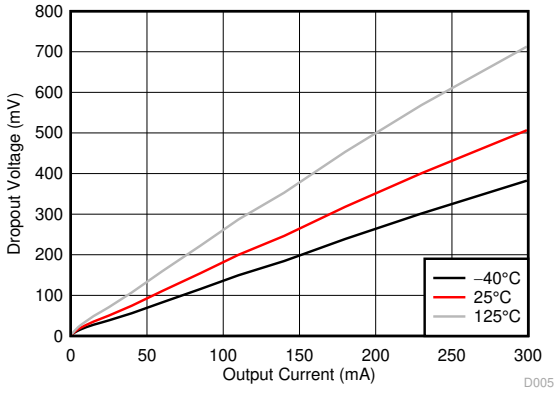
V_{EN} = 0 V

図 6-3. Shutdown Current vs Ambient Temperature



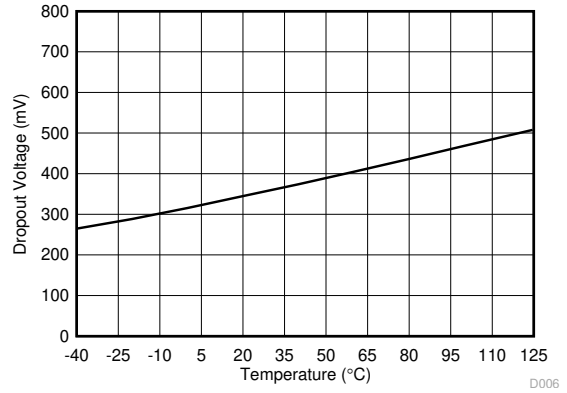
V_{OUT} = 5 V

図 6-4. Quiescent Current vs Ambient Temperature



V_{IN} = 5 V, 5-V fixed output, $V_{(Dropout)} = V_{IN} – V_{OUT}$

図 6-5. Dropout Voltage vs Output Current

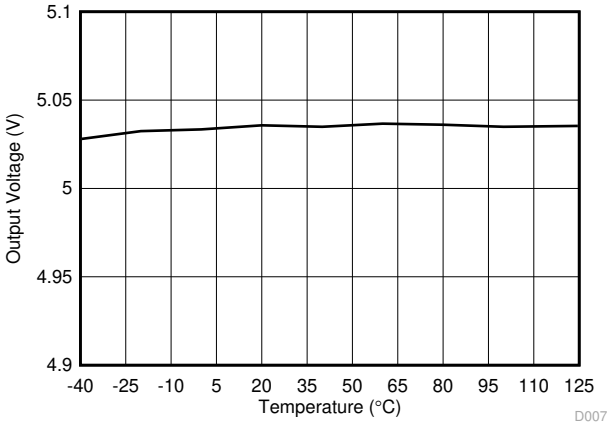


V_{IN} = 5 V, 5-V fixed output, $V_{(Dropout)} = V_{IN} – V_{OUT}$

図 6-6. Dropout Voltage vs Ambient Temperature

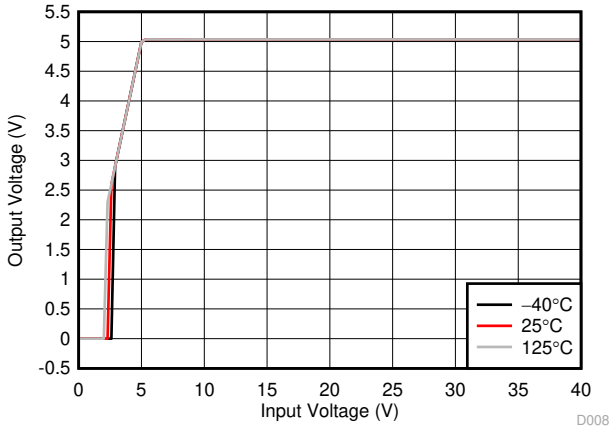
6.7 Typical Characteristics (continued)

V_{IN} = 14 V, V_{EN} ≥ 2 V, T_J = –40°C to 150°C (unless otherwise noted)



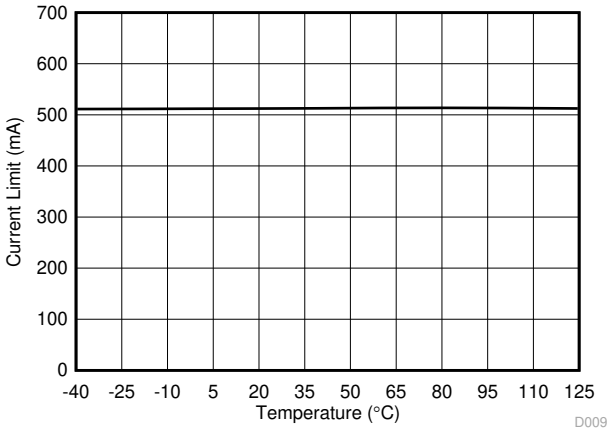
V_{OUT} = 5 V

図 6-7. Output Voltage vs Ambient Temperature



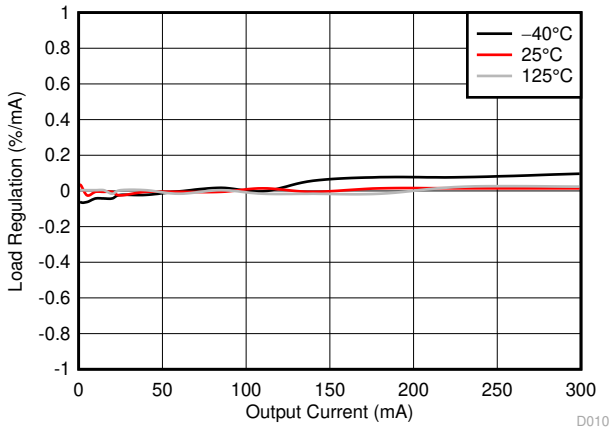
V_{OUT} = 5 V, I_{OUT} = 1 mA

図 6-8. Output Voltage vs Input Voltage



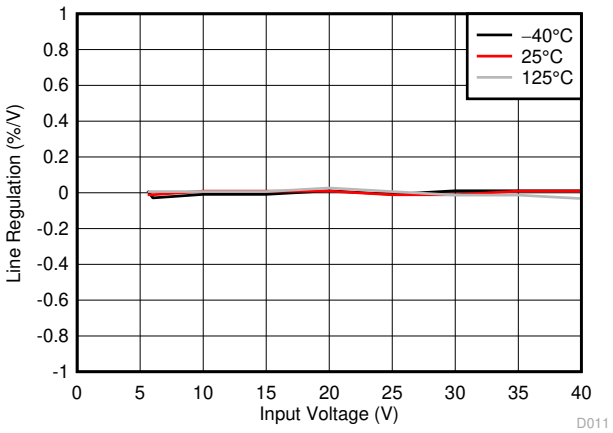
V_{IN} = 14 V, V_{OUT} is shorted to 90% × V_{OUT}

図 6-9. Output Current Limit vs Ambient Temperature



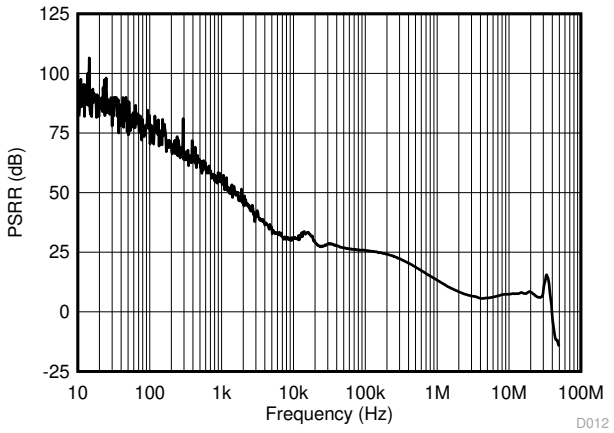
V_{OUT} = 5 V

図 6-10. Load Regulation



V_{OUT} = 5 V, I_{OUT} = 10 mA

図 6-11. Line Regulation

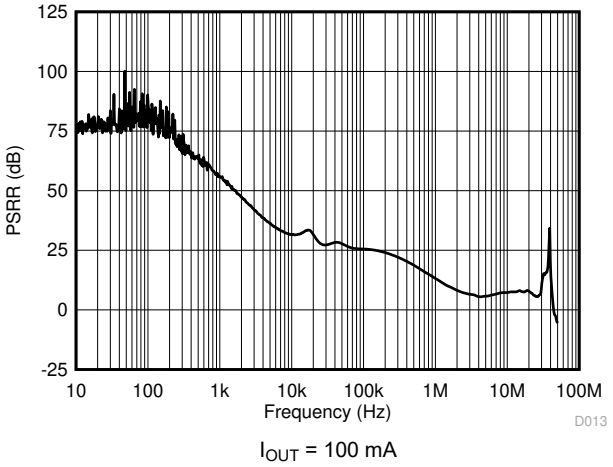


I_{OUT} = 10 mA

図 6-12. PSRR vs Frequency

6.7 Typical Characteristics (continued)

V_{IN} = 14 V, V_{EN} ≥ 2 V, T_J = –40°C to 150°C (unless otherwise noted)



I_{OUT} = 100 mA

図 6-13. PSRR vs Frequency

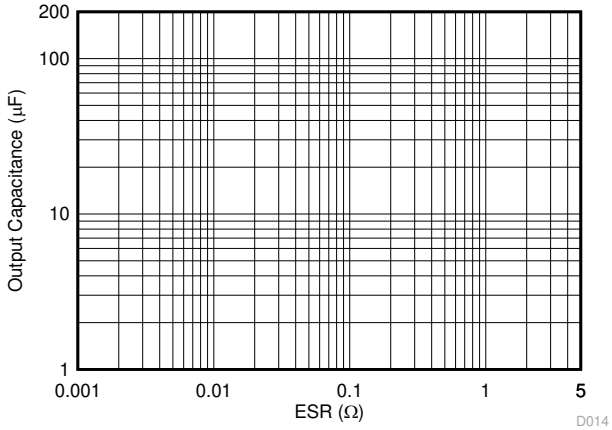


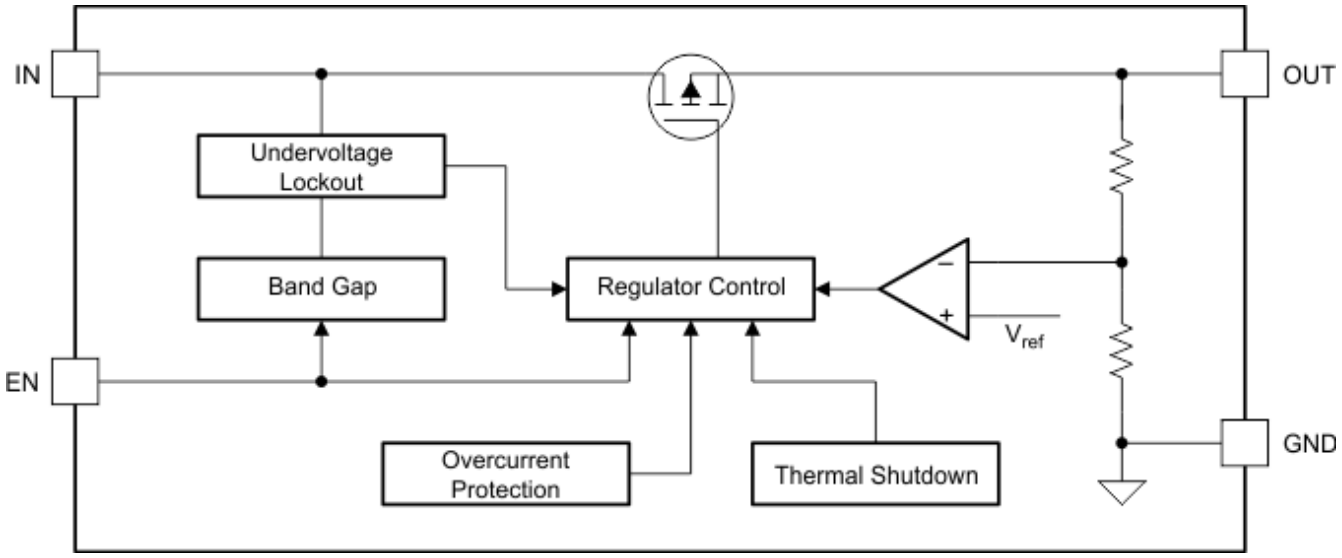
図 6-14. Output Capacitance vs ESR Stability

7 Detailed Description

7.1 Overview

The TPS7B82-Q1 is a 40-V, 300-mA low-dropout (LDO) linear regulator with ultra-low quiescent current. This voltage regulator consumes only 3 µA of quiescent current at light load, and is designed for the automotive always-on application.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Device Enable (EN)

The EN pin is a high-voltage-tolerant pin. A high input activates the device and turns the regulation ON. Connect this pin to an external microcontroller or a digital circuit to enable and disable the device, or connect to the IN pin for self-bias applications.

7.3.2 Undervoltage Shutdown

This device has an integrated undervoltage lockout (UVLO) circuit to shut down the output if the input voltage (V_{IN}) falls below an internal UVLO threshold ($V_{(UVLO)}$). This threshold limit ensures that the regulator does not latch into an unknown state during low-input-voltage conditions. If the input voltage has a negative transient that drops below the UVLO threshold and recovers, the regulator shuts down and powers up with a normal power-up sequence when the input voltage is above the required level.

7.3.3 Current Limit

This device features current-limit protection to keep the device in a safe operating area when an overload or output short-to-ground condition occurs. This limit protects the device from excessive power dissipation. For example, during a short-circuit condition on the output, fault protection limits the current through the pass element to $I_{(LIM)}$ to protect the device from excessive power dissipation.

7.3.4 Thermal Shutdown

This device incorporates a thermal shutdown (TSD) circuit as a protection from overheating. For continuous normal operation, the junction temperature must not exceed the TSD trip point. The junction temperature exceeding the TSD trip point causes the output to turn off. When the junction temperature falls below the TSD trip point minus thermal shutdown hysteresis, the output turns on again.

7.4 Device Functional Modes

7.4.1 Operation With V_{IN} Lower Than 3 V

The device normally operates with input voltages above 3 V. The device can also operate at lower input voltages; the maximum UVLO voltage is 2.7 V. At input voltages below the actual UVLO voltage, the device does not operate.

7.4.2 Operation With V_{IN} Larger Than 3 V

When V_{IN} is greater than 3 V, if V_{IN} is also higher than the output set value plus the device dropout voltage, V_{OUT} is equal to the set value. Otherwise, V_{OUT} is equal to V_{IN} minus the dropout voltage.

8 Application and Implementation

Note

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

The TPS7B82-Q1 is a 300-mA, 40-V low-dropout linear regulator with ultra-low quiescent current. The PSpice transient model is available for download on the product folder and can be used to evaluate the basic function of the device.

8.2 Typical Application

図 8-1 shows a typical application circuit for the TPS7B82-Q1. Different values of external components can be used, depending on the end application. An application may require a larger output capacitor during fast load steps to prevent a large drop on the output voltage. Use a low-ESR ceramic capacitor with a dielectric of type X5R or X7R.

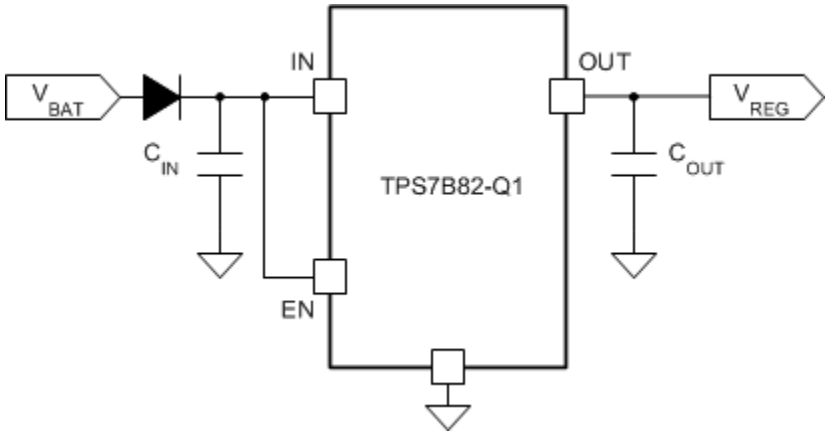


図 8-1. TPS7B82-Q1 Typical Application Schematic

8.2.1 Design Requirements

For this design example, use the parameters listed in 表 8-1.

表 8-1. Design Requirements Parameters

PARAMETER	VALUE
Input voltage range	3 V to 40 V
Output voltage	5 V or 3.3 V
Output current	300 mA maximum

8.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
- Output voltage
- Output current

8.2.2.1 Input Capacitor

Although an input capacitor is not required for stability, good analog design practice is to connect a 10-µF to 22-µF capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple rejection, and PSRR. The voltage rating must be greater than the maximum input voltage.

8.2.2.2 Output Capacitor

To ensure the stability of the TPS7B82-Q1, the device requires an output capacitor with a value in the range from 1 µF to 200 µF and with an ESR range between 0.001 Ω and 5 Ω. Select a ceramic capacitor with low ESR to improve the load transient response.

8.2.3 Application Curve

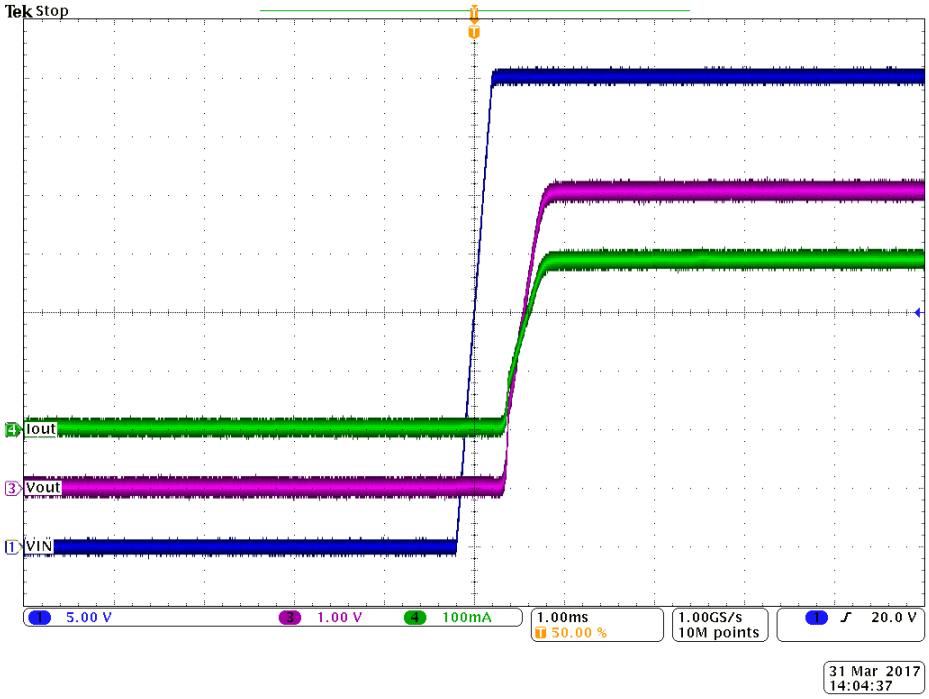


図 8-2. TPS7B82-Q1 Power-Up Waveform (5 V)

9 Power Supply Recommendations

The device is designed to operate from an input voltage supply range from 3 V to 40 V. This input supply must be well regulated. If the input supply is located more than a few inches from the TPS7B82-Q1, add a capacitor with a value greater than or equal to 10 µF with a 0.1-µF bypass capacitor in parallel at the input.

10 Layout

10.1 Layout Guidelines

For LDO power supplies, especially high-voltage and large output current supplies, layout is an important step. If layout is not carefully designed, the regulator can fail to deliver enough output current because of thermal limitation. To improve the thermal performance of the device, and to maximize the current output at high ambient temperature, spread the copper under the thermal pad as far as possible and place enough thermal vias on the copper under the thermal pad. 図 10-1 shows an example layout.

10.2 Layout Example

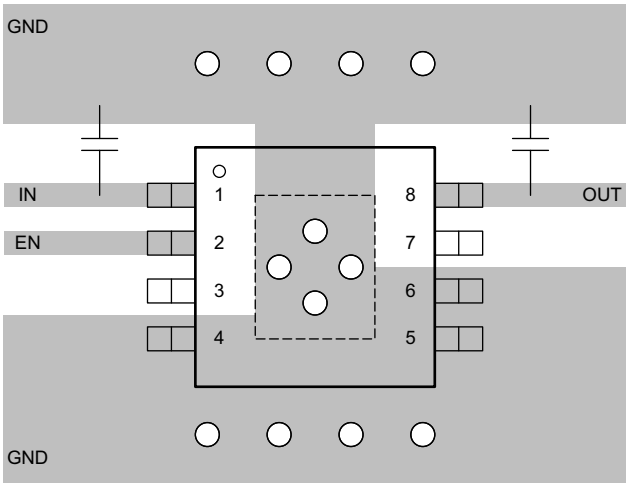


図 10-1. TPSB82-Q1 Example Layout Diagram

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

11.3 Trademarks

PowerPAD™ and TI E2E™ are trademarks of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated device. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7B8225QDGNRQ1	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 150	1QFX	Samples
TPS7B8233EPWPRQ1	ACTIVE	HTSSOP	PWP	14	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 150	7B8233E	Samples
TPS7B8233QDGNRQ1	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 150	1GGX	Samples
TPS7B8233QDRVRQ1	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	1ORH	Samples
TPS7B8233QKVURQ1	ACTIVE	TO-252	KVU	5	2500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 150	7B8233Q1	Samples
TPS7B8250EPWPRQ1	ACTIVE	HTSSOP	PWP	14	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 150	7B8250E	Samples
TPS7B8250QDGNRQ1	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 150	19TX	Samples
TPS7B8250QDRVRQ1	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	1UFH	Samples
TPS7B8250QKVURQ1	ACTIVE	TO-252	KVU	5	2500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 150	7B8250Q1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

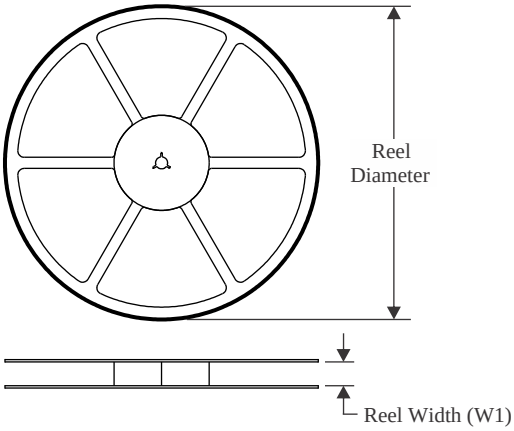
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

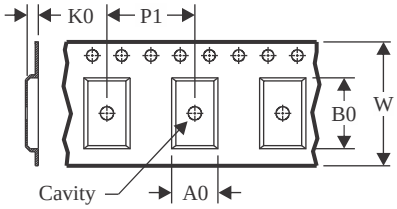
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

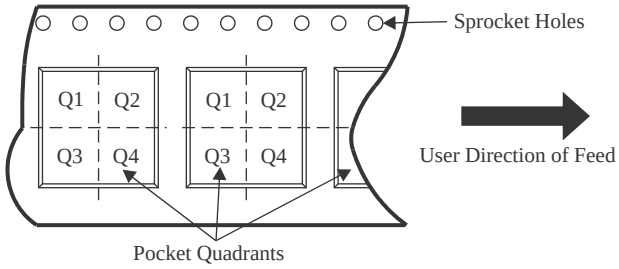


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

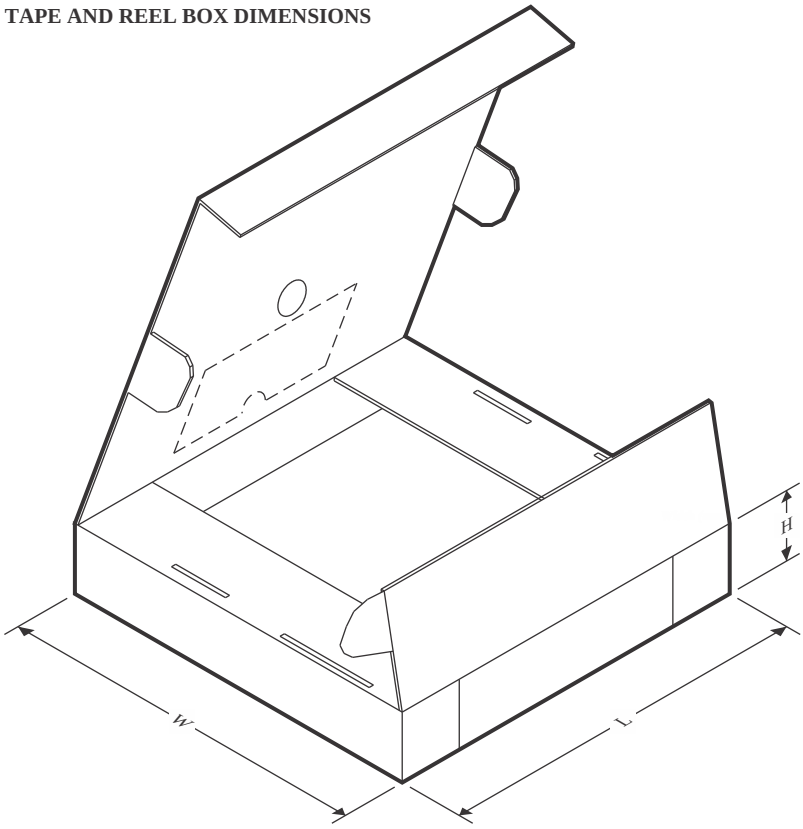
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7B8225QDGNRQ1	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS7B8233EPWPRQ1	HTSSOP	PWP	14	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS7B8233QDGNRQ1	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS7B8233QDRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS7B8233QKVURQ1	TO-252	KVU	5	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TPS7B8250EPWPRQ1	HTSSOP	PWP	14	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS7B8250QDGNRQ1	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS7B8250QDRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS7B8250QKVURQ1	TO-252	KVU	5	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS

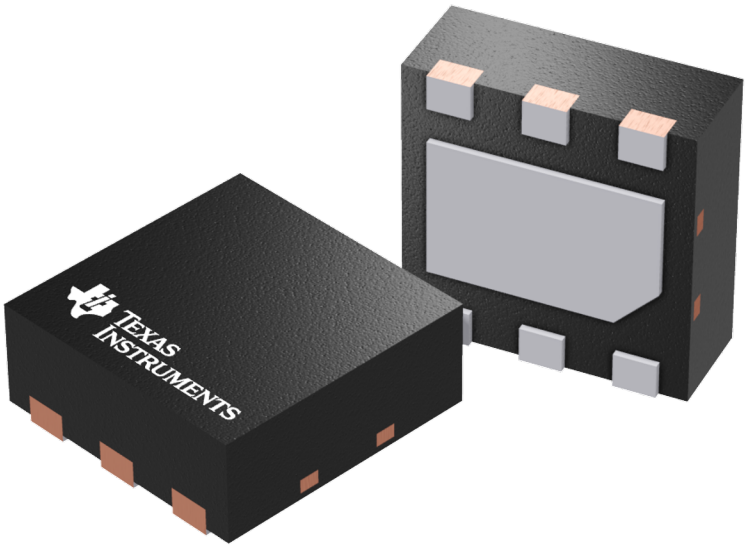


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7B8225QDGNRQ1	HVSSOP	DGN	8	2500	366.0	364.0	50.0
TPS7B8233EPWPRQ1	HTSSOP	PWP	14	2500	356.0	356.0	35.0
TPS7B8233QDGNRQ1	HVSSOP	DGN	8	2500	366.0	364.0	50.0
TPS7B8233QDRVRQ1	WSON	DRV	6	3000	210.0	185.0	35.0
TPS7B8233QKVURQ1	TO-252	KVU	5	2500	340.0	340.0	38.0
TPS7B8250EPWPRQ1	HTSSOP	PWP	14	2500	356.0	356.0	35.0
TPS7B8250QDGNRQ1	HVSSOP	DGN	8	2500	366.0	364.0	50.0
TPS7B8250QDRVRQ1	WSON	DRV	6	3000	210.0	185.0	35.0
TPS7B8250QKVURQ1	TO-252	KVU	5	2500	340.0	340.0	38.0

DRV 6 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



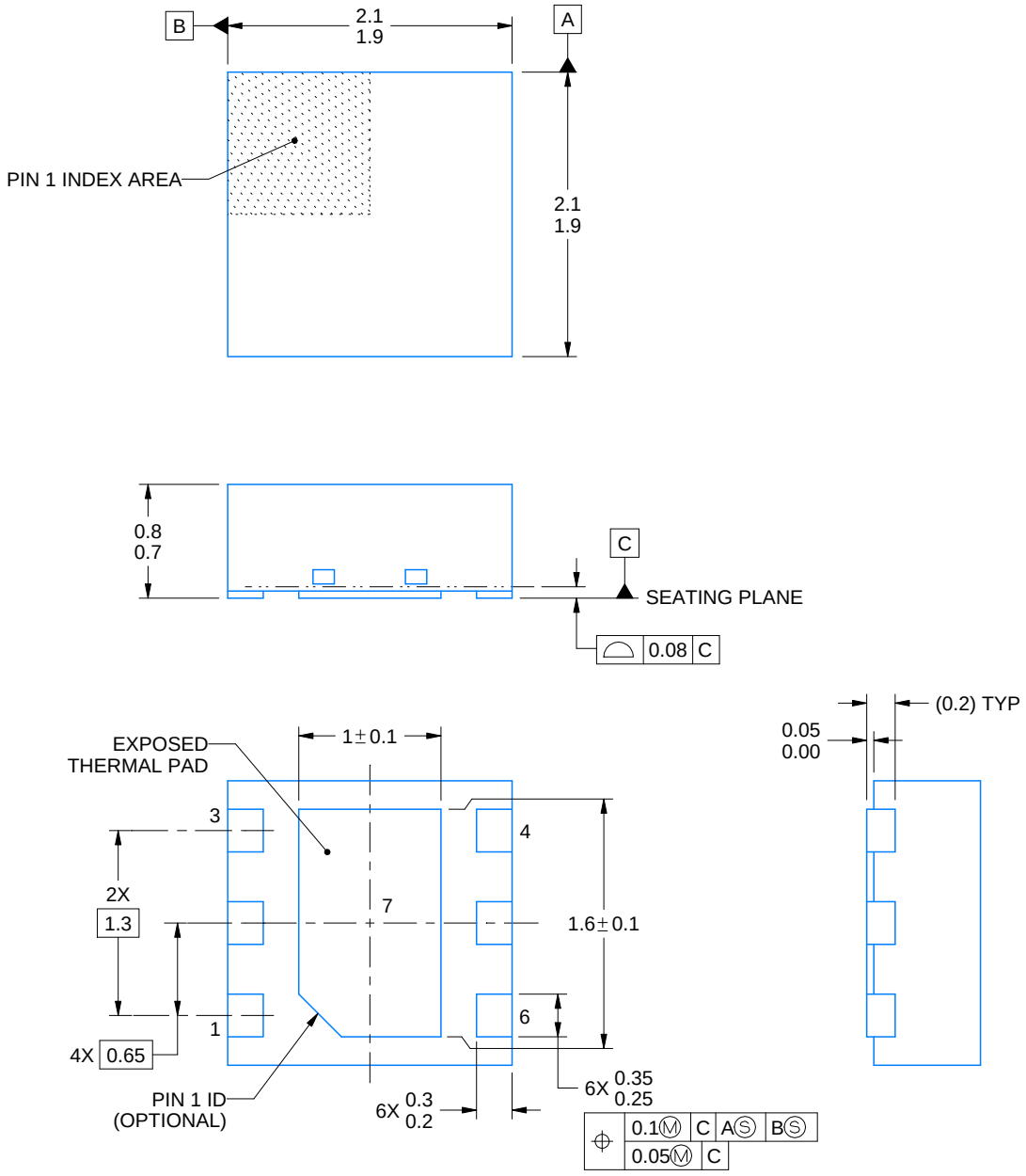
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DRV0006A

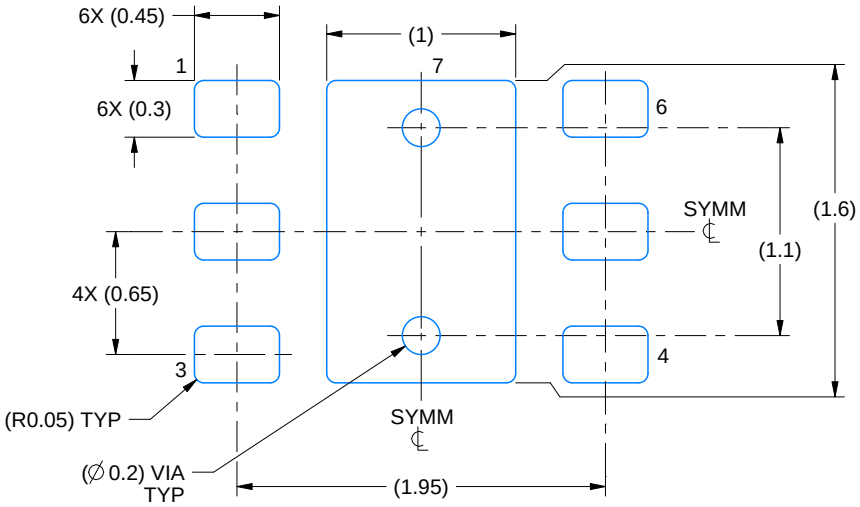
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

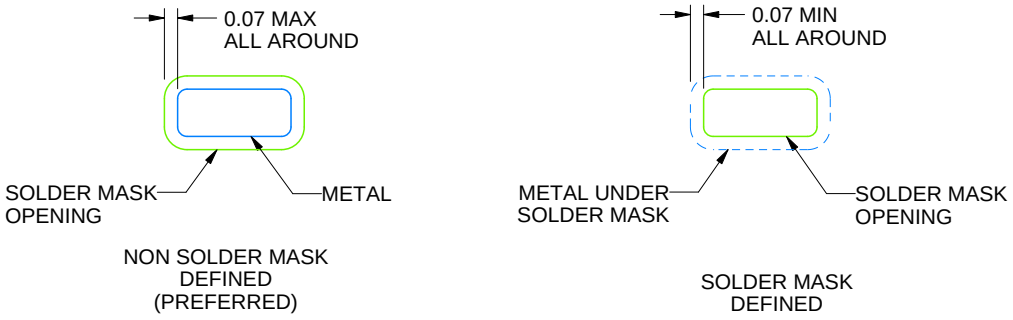


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:25X



SOLDER MASK DETAILS

4222173/B 04/2018

NOTES: (continued)

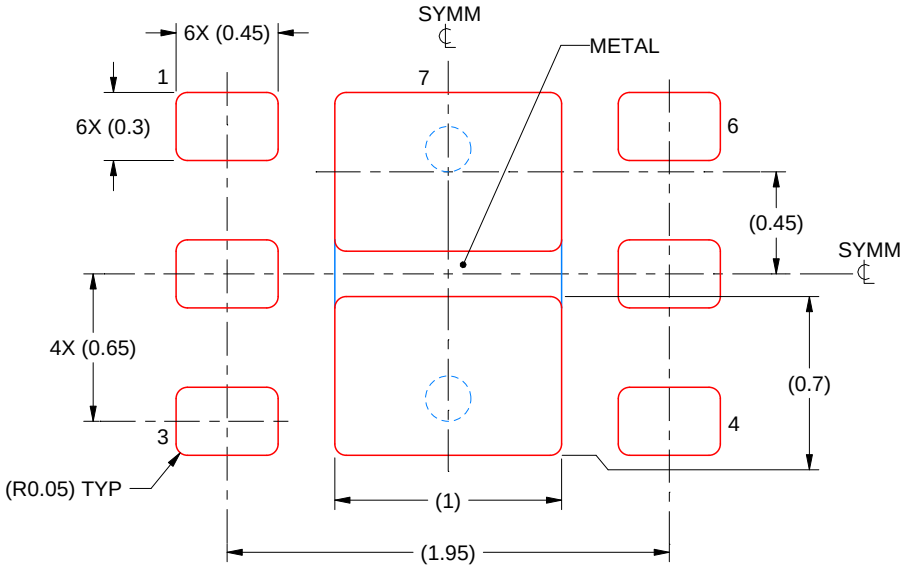
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

EXAMPLE STENCIL DESIGN

DRV0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

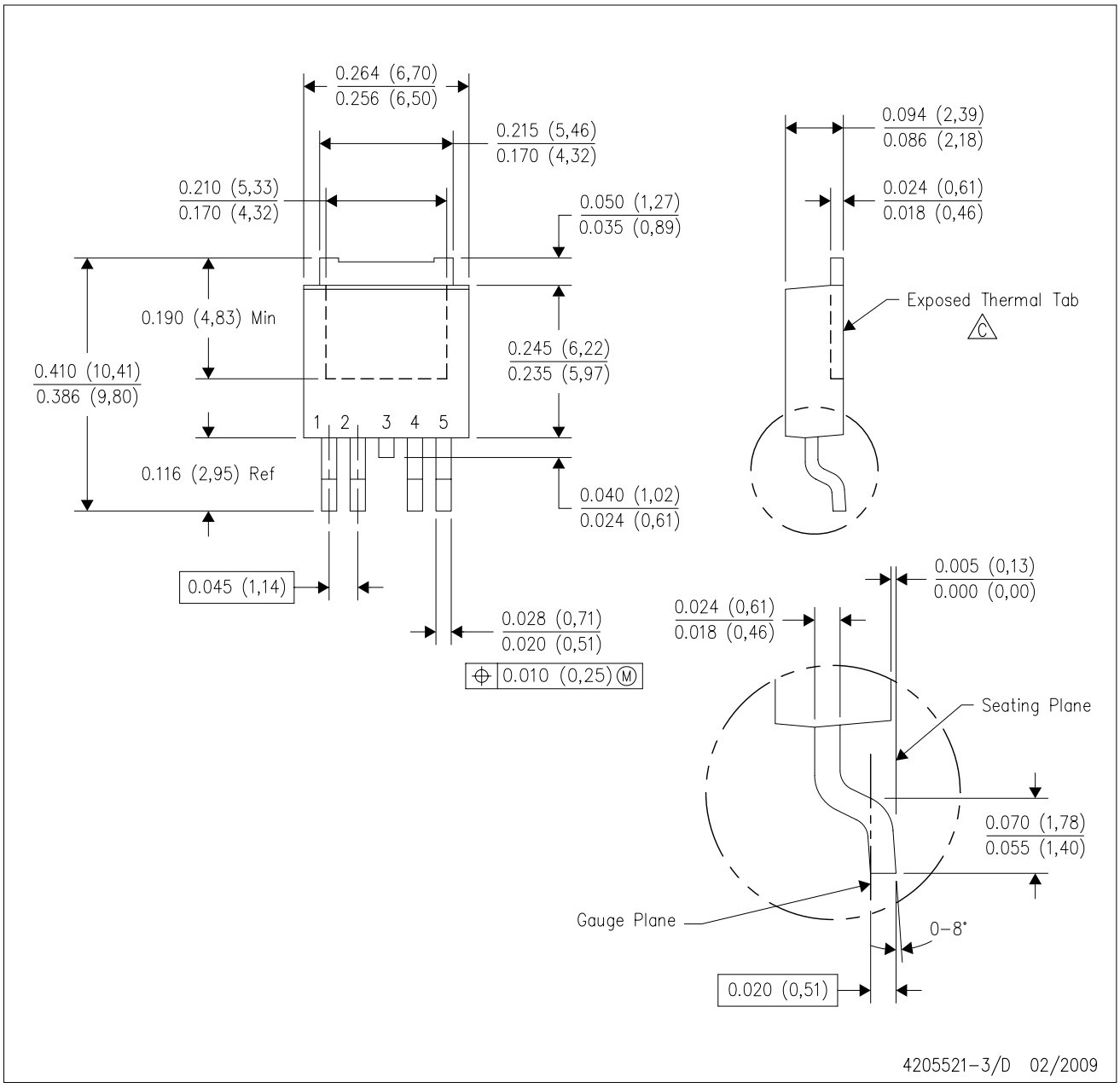
EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4222173/B 04/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

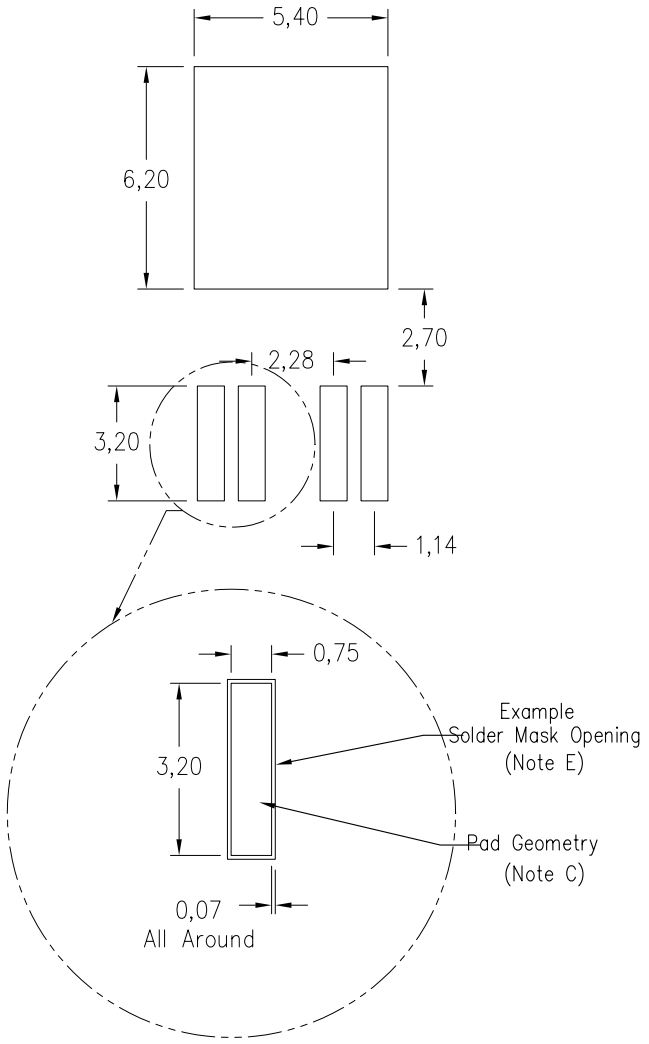
KVU (R–PSFM–G5) PLASTIC FLANGE–MOUNT PACKAGE



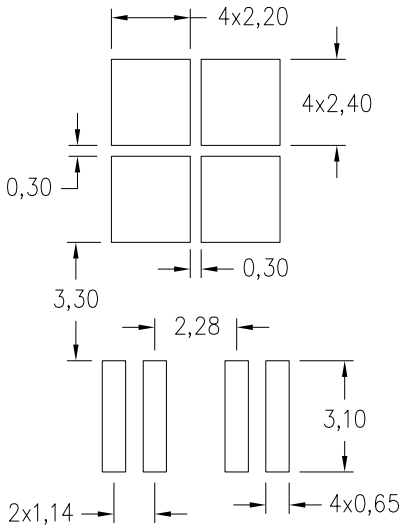
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. The center lead is in electrical contact with the exposed thermal tab.
D. Body Dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.006 (0,15) per side.
E. Falls within JEDEC TO–252 variation AD.

KVU (R–PSFM–G5) PLASTIC FLANGE MOUNT PACKAGE

Example Board Layout



Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).



63% solder coverage on center pad

4211592–3/B 03/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–SM–782 is an alternate information source for PCB land pattern designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

GENERIC PACKAGE VIEW

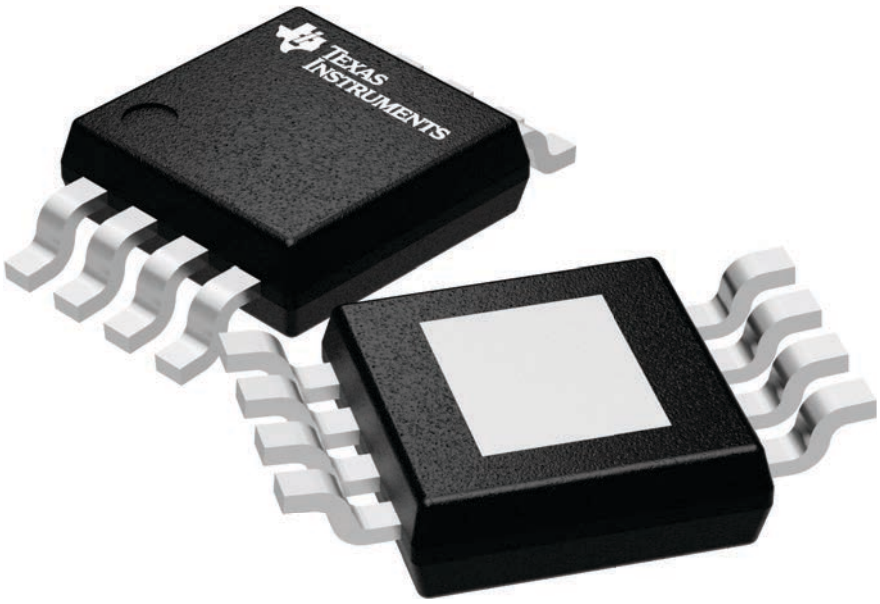
DGN 8

PowerPAD VSSOP - 1.1 mm max height

3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

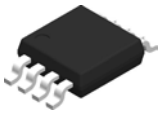
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225482/A

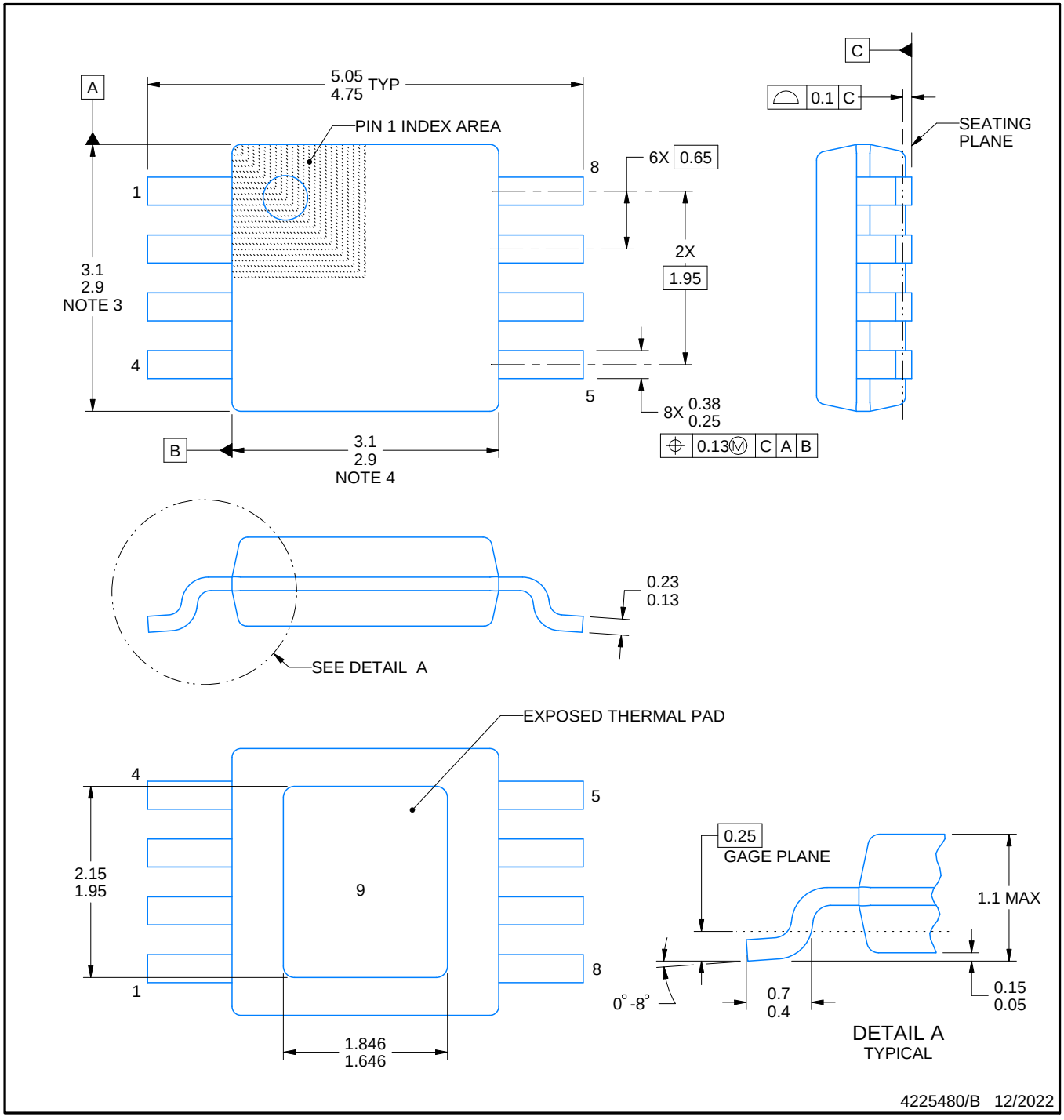
PACKAGE OUTLINE

DGN0008G



PowerPAD™ VSSOP - 1.1 mm max height

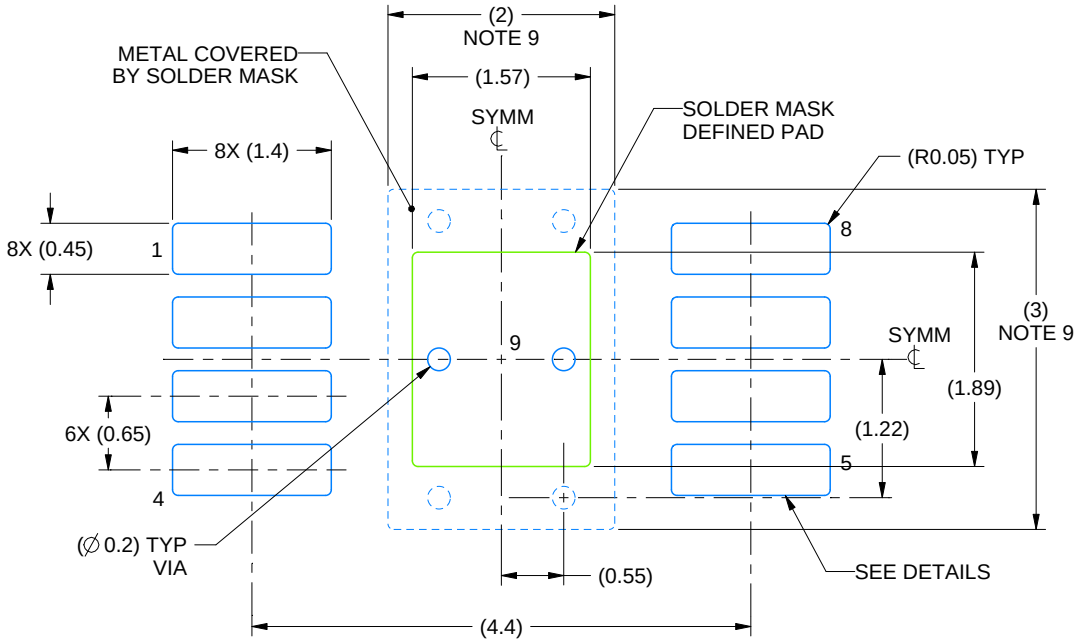
SMALL OUTLINE PACKAGE



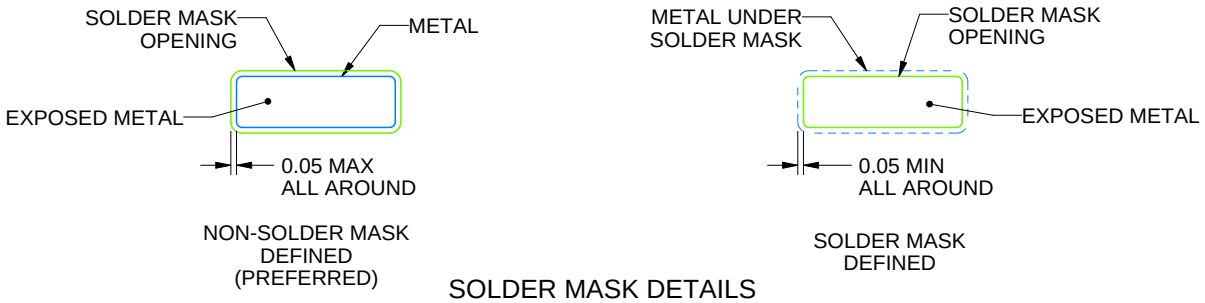
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

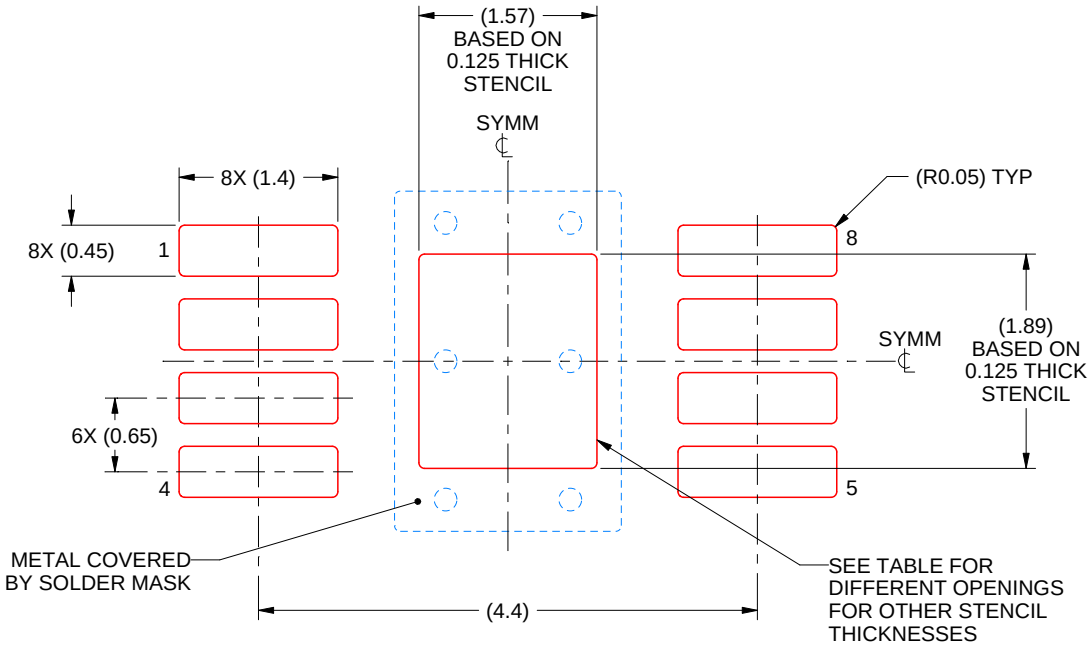


SOLDER MASK DETAILS

4225480/B 12/2022

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

4225480/B 12/2022

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

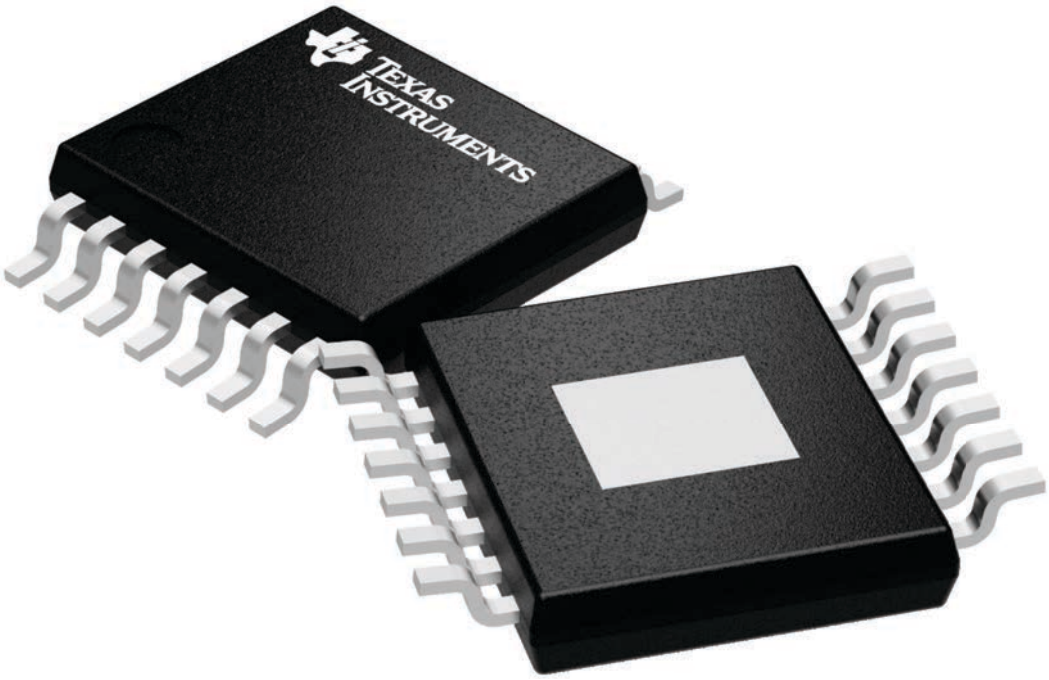
PWP 14

PowerPAD TSSOP - 1.2 mm max height

4.4 x 5.0, 0.65 mm pitch

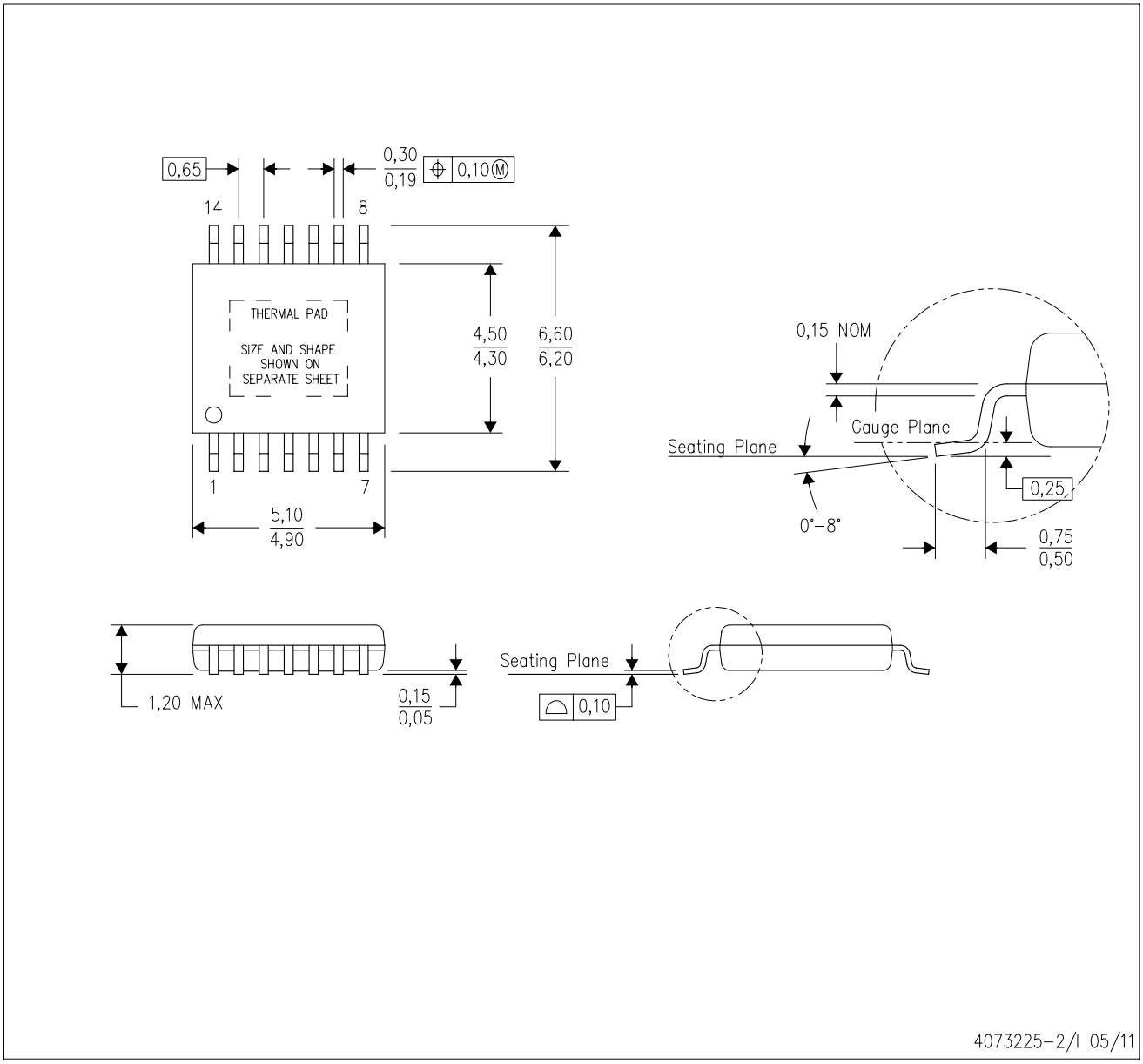
PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224995/A

PWP (R–PDSO–G14) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

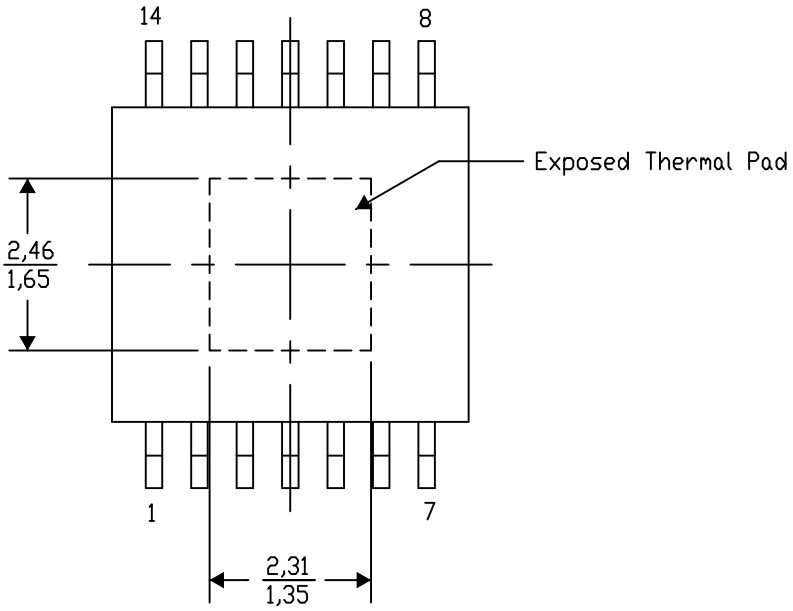
PWP (R–PDSO–G14) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

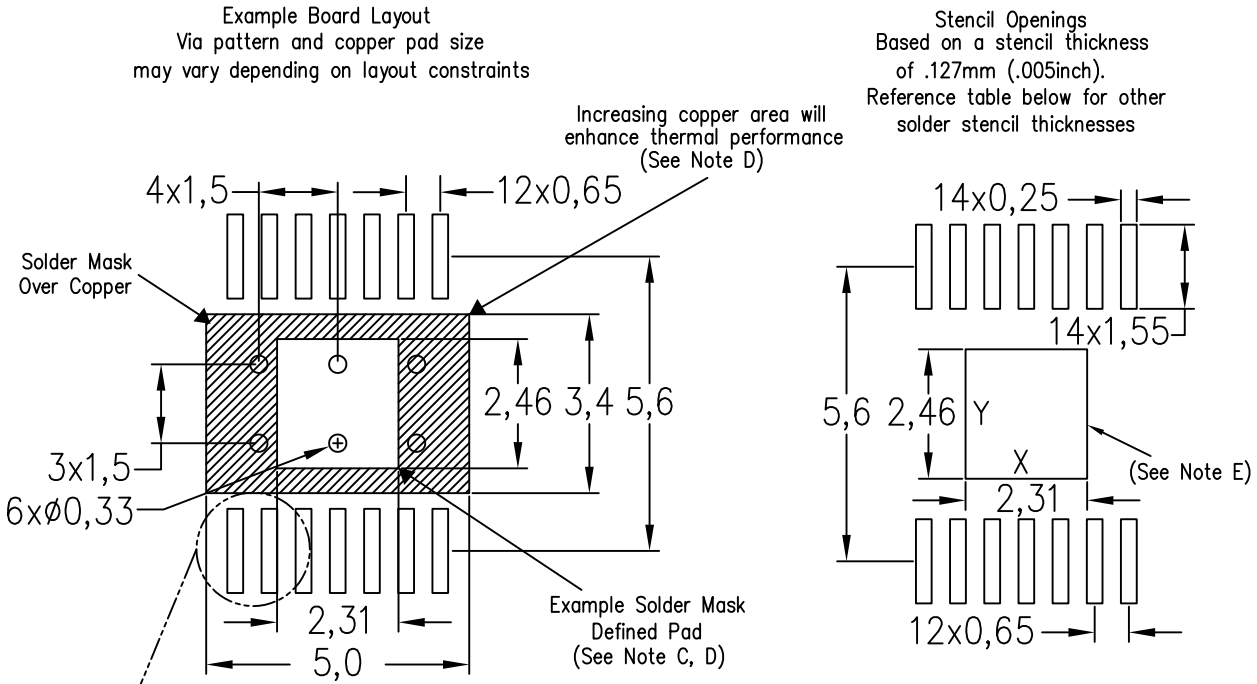
Exposed Thermal Pad Dimensions

4206332–2/AO 01/16

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G14) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.5	2.65
0.127mm	2.31	2.46
0.152mm	2.15	2.3
0.178mm	2.05	2.15

4207609–2/W 09/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス· デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、TI の販売条件、または ti.com やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265