Hamming SEC-DAED and Extended Hamming SEC-DED-TAED codes through selective shortening and bit placement

Alfonso Sánchez-Macián, *Member, IEEE*, Pedro Reviriego, *Member, IEEE*, and Juan Antonio Maestro, *Member, IEEE*

***Abstract*— Radiation particles can impact registers or memories creating soft errors. These errors can modify more than one bit causing a Multiple Cell Upset (MCU) which consists of errors in registers or memory cells physically close. These MCUs can affect a single word, producing adjacent bit errors. Hamming codes are commonly used to protect memories or registers from soft errors. However, when multiple errors occur a Hamming code may not detect them. In this letter, Single Error Correction Double Adjacent Error Detection (SEC-DAED) Hamming codes are presented for 16, 32 and 64-bit words. Additionally, Single Error Correction Double Error Detection Triple Adjacent Error Detection (SEC-DED-TAED) codes based on Extended Hamming are presented as well. The enhanced detection is achieved by performing a selective shortening and reordering of the Hamming matrix so adjacent errors result in a syndrome that does not match that of any single error. These codes will help in the detection of MCUs in SRAM memory designs.**

***Index Terms*— Hamming codes, Multiple Cell Upsets (MCUs), error correction codes, memory.**

I. Introduction

Hamming codes were presented in 1950 [1] and they have been widely used since then. One application is the protection against soft errors [2] produced by a radiation particle hitting SRAM memory cells or a register and changing the value stored in them. To avoid this data corruption issue, one option is to use Error Correction Codes (ECCs) [3],[4] which are already used in memories for reliability purposes. Single Error Correction (SEC) codes are utilized when low delay is required. SEC codes have a minimum distance of three. This means that double errors can be mistaken for a single error and miscorrected. This problem can be overcome by using Single Error Correction Double Error Detection (SEC-DED) codes, with a distance of four, so they are preferred in memory applications [3].

Dealing with manufacturing errors in SRAM memories is out of the scope of this paper. These errors can be solved by using spare rows and columns as in [5].

Hamming codes are one example of these SEC codes. A SEC-DED code can be created by extending a Hamming code with a parity bit covering all bits [1].

A radiation particle can upset more than one memory cell or register causing multiple errors [6]. This is called a Multiple Cell Upset [7]. Memory cells affected by a MCU are physically close and in many cases adjacent [8]. Several adjacent bits of a particular word can be upset. SEC and SEC-DED codes would not be able to detect the error, and could even miscorrect the word into a different valid one producing Silent Data Corruption (SDC) which can lead to an incorrect system behavior and further data corruption.

In this letter, specific matrices for Single Error Correction Double Adjacent Error Detection (SEC-DAED) Hamming codes are presented. They will provide a code capable of correcting single errors and detecting double-adjacent errors. Additionally, Single Error Correction Double Error Detection Triple Adjacent Error Detection (SEC-DED-TAED) codes are generated from an Extended Hamming code.

The rest of the letter is organized as follows section II presents related work. In section III the SEC-DAED Hamming codes are introduced. Then in section IV the SEC-DED-TAED are presented. The proposed codes are validated by simulation in section V and finally conclusions are included in section VI.

II. Related Work

There are different options for SEC-DED codes that reduce slightly the implementation cost [9] or the miscorrection probability for triple errors [10]. Optimal SEC-DAED codes organized in bytes of size b were mathematically modeled in [11]. Selective reordering has been proposed to reduce the miscorrection of double errors in SEC codes and triple errors in SEC-DED codes [12]. The paper in [13] presents SEC-DEC-DAEC, so the approach is similar to the second part of this letter, but focusing on correcting double-adjacent errors instead of detecting triple-adjacent errors. In [14] a code and implementation to correct single errors, double-adjacent and

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A. Sánchez-Macian, P. Reviriego and J.A. Maestro are with Universidad Antonio de Nebrija, C/Pirineos, 55, E-28040, Madrid, Spain, (phone: +34 914521100; fax: +34 914521110; email: {asanchep,previrie, jmaestro}@nebrija.es).

triple-adjacent errors and double-almost-adjacent errors are presented based on a previous patent. It requires 7 check bits for a 16-bit data word, i.e. one additional bit more per word than an Extended Hamming code. The work presented in following sections uses standard codes and selects appropriate check matrices for them in order to obtain SEC-DAED and SEC-DED-TAED codes. The main advantage of having data words with a length corresponding to a power of 2 is that shortening can be optimized and combined with bit placement strategies due to the existence of many possible combinations, as presented in next sections.

III. SEC-DAED Hamming Codes

In [12], enhanced detection of double and triple adjacent errors using Hamming codes was presented by reordering the code bits when a lexicographic matrix was used. This letter continues that work and presents Hamming Matrices for 16-bit, 32-bit and 64-bit data words that provide single error correction and double-adjacent error detection. This is achieved by applying a selective shortening and reordering strategy.

Hamming codes are characterized by the following parameters (for any positive integer m≥3) [15]:

$$\begin{aligned} n &= 2^m - 1 \\ k &= n - m \\ d_{\min} &= 3 \end{aligned} \tag{1}$$

where n is the block size, m the parity check bits, k the number of information bits and d_{min} the minimum distance of the code.

For a 16-bit data word (k=16), shortening is applied to a (31, 26) Hamming code, producing a (21, 16) SEC code. Thus, 10 columns can be removed from the original matrix. The shortening process chosen for this letter is as follows:

- Fill the first 16 columns with the odd-weight values to maximize double error detection. A double error affecting any of these columns will produce an even-weight syndrome. So, it will not correspond to any of these columns.
- Sort those columns trying to minimize the different even-weight syndromes generated. Adjacent-errors on these 16 columns produce 15 syndromes. The goal is to maximize the coincidences between these syndrome values.
- The remaining 5 columns need to be filled by even-weight values. However, an adjacent error produced in the transition between the last odd-weight column and the first even-weight value would produce a miscorrection as it corresponds to a different existing odd-weight column. So a specific odd-weight column will be selected and removed from the matrix to provide for the identified odd-weight syndrome.
- The 5 columns plus the removed one (6 in total) are filled with even-weight values placing them in the appropriate order and excluding those which coincide with a previous double-adjacent error syndrome.

The same approach is used for 32-bit and 64-bit data words. Using the procedure described above, matrices (2), (3) and (4) are generated.

$$\begin{pmatrix} 0&1&0&1&0&1&0&\mathbf{1}&0&\mathbf{1}&\mathbf{1}&\mathbf{0}&1&\mathbf{0}&1&0&0&0&0&1 \\ 1&1&1&1&1&1&0&0&\mathbf{1}&0&\mathbf{0}&\mathbf{0}&\mathbf{0}&\mathbf{0}&0&\mathbf{0}&1&1&0&1&0&1 \\ 1&1&1&0&0&0&1&1&\mathbf{0}&1&\mathbf{0}&\mathbf{0}&\mathbf{0}&\mathbf{0}&1&\mathbf{0}&0&0&1&0&1&0 \\ 1&0&0&1&1&0&1&1&\mathbf{0}&0&\mathbf{1}&\mathbf{0}&\mathbf{0}&\mathbf{1}&0&\mathbf{0}&1&1&1&0&0&0 \\ 0&0&1&0&1&1&1&0&\mathbf{0}&1&\mathbf{0}&\mathbf{0}&\mathbf{1}&\mathbf{1}&0&\mathbf{0}&1&0&0&1&1&0 \end{pmatrix} \tag{2}$$

$$\begin{pmatrix} 1&1&1&1&1&1&1&1&1&1&1&1&1&0&1&\mathbf{0}&0&1&\mathbf{0}&0&0&0&\mathbf{0}&0&0&0&0&0&0&\mathbf{1}&\mathbf{0}&\mathbf{0}&1&0&0&0&1&1&1 \\ 1&0&1&1&0&1&1&0&1&1&0&0&1&0&\mathbf{0}&\mathbf{1}&\mathbf{0}&\mathbf{0}&1&1&\mathbf{0}&\mathbf{0}&1&0&1&0&1&0&\mathbf{0}&\mathbf{0}&\mathbf{1}&0&0&0&0&1&1&1 \\ 0&1&1&0&1&0&1&1&1&0&1&1&0&1&\mathbf{0}&\mathbf{1}&\mathbf{0}&\mathbf{0}&1&0&\mathbf{1}&\mathbf{0}&1&0&1&1&0&1&\mathbf{0}&\mathbf{0}&\mathbf{0}&1&1&0&0&1&1&0 \\ 0&1&1&0&1&1&0&0&1&0&0&1&1&1&\mathbf{1}&\mathbf{1}&\mathbf{0}&\mathbf{0}&1&1&\mathbf{0}&\mathbf{1}&1&0&0&1&1&0&\mathbf{0}&\mathbf{0}&\mathbf{0}&1&0&1&0&1&0&1 \\ 0&1&0&1&0&0&1&1&1&0&0&1&1&0&\mathbf{0}&\mathbf{1}&\mathbf{1}&\mathbf{0}&1&0&\mathbf{1}&\mathbf{0}&0&0&1&1&1&1&\mathbf{0}&\mathbf{0}&\mathbf{0}&1&1&1&1&0&0&0 \\ 1&1&1&0&0&0&1&0&1&0&1&0&1&1&\mathbf{0}&\mathbf{1}&\mathbf{0}&\mathbf{0}&1&0&\mathbf{1}&\mathbf{0}&1&1&1&0&1&1&\mathbf{1}&\mathbf{0}&\mathbf{0}&0&1&0&0&0&0&1 \end{pmatrix} \tag{3}$$

The parity bit columns (those that have a single one) are emphasized using bold face.

IV. SEC-DED-TAED Extended Hamming Codes

A similar approach can be applied to Extended Hamming Codes adding the Triple-Adjacent Error detection capability. Extending Hamming codes include an additional parity bit over the whole word. If we consider initially only the original Hamming matrix, selective shortening is, this time, performed by taking into account the weight properties of columns being added. The objective is to get an even-weight syndrome for any triple-adjacent error. To fulfill this goal, columns are arranged placing them with the following weight order (odd odd even odd odd even … and so on).

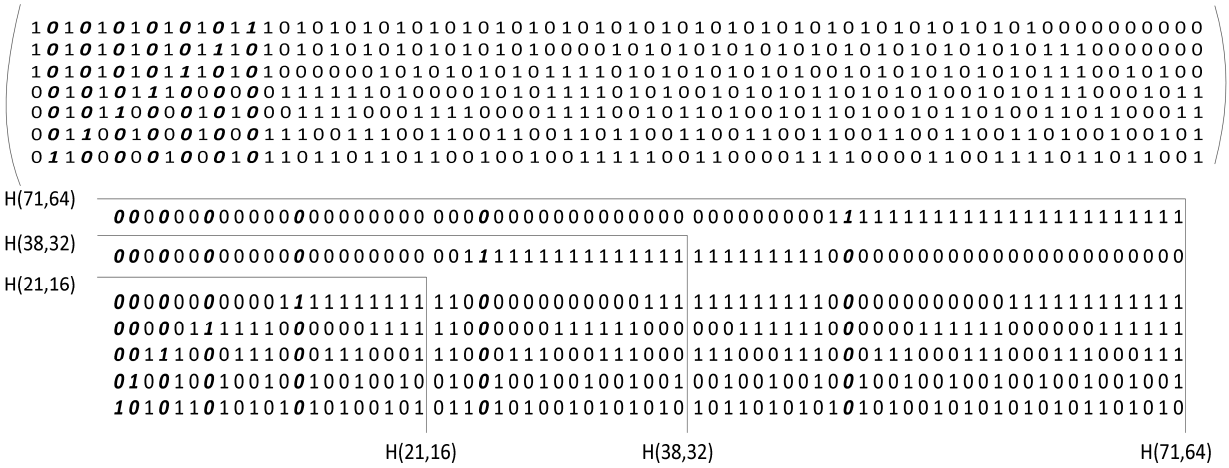
An algorithm is designed to place the smallest available column value with the expected weight for a specific position. It excludes the previously selected columns and, if the expected weight is even, it also ignores those values that result from the combination of any previous consecutive three columns.

The result is a set of matrices where any three adjacent columns produce a value not included in the same matrix, so a triple-adjacent error is detected. Additionally, considering 16, 32 and 64-bit data words, the m-1 rows of the first (k/2 + m-1) columns for these check matrices correspond to the matrix of (k/2) data bits.

The matrices for (21,16), (38,32) and (71,64) codes, which do not consider the parity bit yet, are shown in (5).

The additional parity bit is easily generated as the combination of all bits and checked by comparing it to the parity of the code word excluding the bit itself. This process can be done independently or matrices can be modified. Considering the first option, double errors in the message (not affecting the parity bit) are detected because they will produce a Hamming Syndrome different from zero with no error in the recalculation of the parity bit.

All triple-adjacent errors are detected due to the special configuration of the check matrix, except the one affecting the additional parity bit and its two adjacent code word bits.



(4)

(5)

To detect this error, the additional parity bit is placed prepending the less significant bit. Any error affecting the two first bits of the code word will be always detected because they produce a syndrome (with a value of 3) which is not a valid column value. Thus, a miscorrection is never performed. So if the parity bit is affected too, it will be detected by the previous condition without any additional modification.

V. Validation

A simulation has been performed to validate all the possible error combinations in the different cases. The results are shown in Tables I and II.

TABLE I. SUMMARY OF RESULTS SEC-DAED

Code	Percentage of double errors detected		
	Double-adjacent errors	Double non-adjacent errors	Total double errors
Hamming(21,16)	100%	30,47%	40%
Hamming(38,32)	100%	49,93%	55,19%
Hamming(71,64)	100%	66,96%	69,82%

TABLE II. SUMMARY OF RESULTS SEC-DED-TAED

Code	Percentage of triple errors detected		
	Triple-adjacent errors	Triple non-adjacent errors	Total triple errors
Hamming(22,16)	100%	34,61%	35,91%
Hamming(39,32)	100%	40,37%	40,77%
Hamming(72,64)	100%	41,90%	42,02%

Apart from detecting all the consecutive errors, the SEC-DAED codes presented can also detect between 30 and 67% of double non-adjacent errors. Considering SEC-DED-TAED codes, they can detect between 34 and 42% of triple non-adjacent errors.

VI. Conclusions

In this letter, parity check matrices to implement SEC-DAED Hamming codes and SEC-DED-TAED in Hamming codes have been presented. The result is achieved by selectively shortening the matrices so adjacent errors produce a syndrome that does not match any of those that correspond to a single error. The proposed scheme does not require any additional circuitry. The memory area, power and speed will be the same as with the traditional bit placement. It can help in the detection of adjacent errors which are the ones usually caused by Multiple Cell Upsets (MCUs) in SRAM memories.

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