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Implementation of Error Correction Techniques in Memory Applications

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Abstract— **As the technology scales down, various soft errors in SRAM memories occurs due to which the single cell and multiple cell upsets are formed. Error correction codes such as the first technique (7,4) hamming code, where 7 denotes total code word, four refers to data bits and 3 parity bits were implemented and verified its encoding and decoding process. But it is only useful for single bit error detection and also correction, which has been the main drawback of this hamming code. So, the second technique implemented was the extended hamming code (8,4) or SEC-DED code ("Single Error Correction-Double Error Detection"). This code has an extra bit and used for correction of single error and also detection of double error. But correction of double error doesn't happen in SEC-DED code. So, the extension of (8,4) SEC-DED code was (14,8) SEC-DED-DAEC ("Single Error Correction-Double Error Detection-Double Adjacent Error Correction") code where 14 denotes total code word, 8 data bits, six parity bits which can be used for correction of single error, detection of double error and also correction of double adjacent error was proposed in this work. These techniques related Encoding and Decoding processes were studied and all the simulation results were verified and implemented by using Verilog Coding in Xilinx ISE 14.7 tool. This proposed SEC-DED-DAEC method was also implemented in memory application and its output is verified. The double error detection was adjacently corrected by using this method and the complexity was decreased. The advantage of the proposed technique is it has the ability to detect and correct errors adjacently up to 2 bits.**

Keywords— **Multiple cell upsets, Error Detection and Correction codes, SRAM memories, (7,4) Hamming Code, SEC-DED code (Single Error Correction-Double Error Detection), SEC-DED-DAEC code (Single Error Correction-Double Error Detection-Double Adjacent Error Correction), Xilinx ISE, Verilog Coding.**

I. INTRODUCTION

As there is a huge demand for increase in the functionality, power reduction, transistor dimensions and operating voltages, CMOS technology scales down. The demand for the functionality of a chip has caused an increase in the memory applications. To accomplish the demand for increase of chip storage capability, embedded memories are designed and used with minimum sizes that is around 14 to 16 nm technology. Scaling of technology and reduction in the supply voltages can make memory cells become more sensitive to radiation factors. This issue is specifically occurred in memories. Various soft errors are induced due to radiation which in turn leads to reliability issues.

Soft errors occur when neutrons from the alpha particles emit from the packaging material of the chip. The transients appearing at the nodes of the circuits corrupt the data which is stored in the memories. When this corrupts single data bit it is called single bit upset, similarly when multiple cells are corrupted it is called as multiple cell upsets. These only corrupt the data but don't damage the whole device so they are called as soft errors. Additionally, as the bit cell density increases, several adjacent cells are also being corrupted and causing many multiple bit and multiple cell upsets.

The main motivation of this research is to detect these types of errors and also correct these errors so that the data transmission and receiving will be the same even though there is interference of noise through channel.

The main objective of this research work is the extension of SEC-DED code to SEC-DED-DAEC code and the double error which is detected is adjacently corrected.

II. LITERATURE REVIEW

When technology scales down, soft errors were increased so that in order to reduce these error correction codes like SEC-DED code by using area efficient was discussed in [1] and hamming code based algorithm which can detect random and burst errors [2] was used in quantum system application. Error Detection and Correction of various multiple bit random and burst errors were proposed in [3] by using diagonal hamming code technique. In the case of spectrum sensing and allocation application, data transmission needs to be efficient so parity check hamming code was proposed in [4] along with necessary encoding and decoding blocks. Due to various multiple errors, different low redundant error correction codes like matrix code based on hamming code and column line code were proposed in [5]. Especially in the case of memories error correction in both data and parity up to 3 bits based on 3D parity check code was proposed in [6]. Horizontal-Vertical diagonal hamming was proposed in [7] for detection and correction of multiple bit errors. Decimal and parity matrix codes were the proposed error correction codes in order to overcome multiple cell upsets in [8]. Ultrafast Error Correction codes were proposed in [9] in order to reduce the delay but with high redundancy. Error Correction codes that correct single and double adjacent errors SEC-DAEC code was proposed in [10]. SEC-DED-DAEC code with optimized decoding was proposed in [11] to reduce multiple cell upsets. In [12] SEC-DAED and SEC-DED-TAED codes were presented for the

detection of upsets in memory designs. New codes which provided basic SEC-DED and DAEC, scalable error correction was presented in [13]. In [14] low complexity multi bit error correction codes were proposed with low cost and high reliability. Soft error rates will increase when technology scaling took place in memories as mentioned in [15].

K. Rahul and S. Yachareni proposed that when the technology scaled down, SRAM bit cells will be increased in the IC. This will cause an increase in the number of soft errors. Here they used SEC-DED ("Single Error Correction Double Error Detection") code and other methods like word interleaving, column muxing so as to reduce these errors. They also proposed area efficient (72,64) and (39,32) codes without adding any extra parity bit which can be used for the detection of adjacent three-bit errors and correction of adjacent two-bit errors. Similarly, they even proposed an area efficient (73,64) and (40,32) codes with one extra parity in order to detect and also correct two bit, three bit adjacent errors [1].

X. Zhong and G. Jin presented the technique for quantum distribution application. In this one should share the state of the quantum to another via channel known as quantum channel. Yet, due to some external factors there might be a change in the quantum state during transmission so this would cause an error in the actual key at receiver end. A method based on the Hamming code was proposed, verified in this particular application. This algorithm could be adapted to various bit error rates by changing the length coding. By incorporating the key interleaving algorithm this would be able correct random as well as burst errors in the actual key [2].

G. M. Sai, K. M. Avinash, L. S. G. Naidu, M. S. Rohith and M. Vinodhini presented that soft errors were occurred in memories due to variations in the voltage or other induced external radiations. The diagonal hamming code based on multiple bit error technique was proposed for the detecting errors up to 8 bits and correcting up to 5 bits. Some combinations of random errors like 6 and 7 bits, burst errors of 8 bits were corrected. They have achieved high code rate with lesser area, delay compared with other methods [3].

Subhasri. G and Radha. N presented spectrum sensing and allocation were performed due to that it might cause interferences and also occurrence of error in the original data. Data transmission process need to be efficient for both error detection and also correction methods. These were implemented based on the parity checking and hamming code methods. Encoder block was used for parity bits calculation based on hamming code for the input data. Decoder block was used for calculation of syndrome bits. Those blocks were developed in Xilinx tool (ISE) [4].

J. Gracia-Morán, L. J. Saiz-Adalid, D. Gil-Tomás and P. J. Gil-Vicente presented the faults occurred due to SRAM systems when the technology was scaled down and also the density on the chip raised. So, there might be a chance of the occurrence of single cell and Multiple Cell Upsets(MCU). An ideal solution was usage of error correction codes. These codes should have good error coverage and redundancy. Encoding and decoding processes should be efficient with respect to area and power. In this, matrix code technique incorporated Hamming code and parity check codes to detect and also correct some MCUs. CLC was a matrix modified technique which was based on extended Hamming and parity checking codes. They also presented low redundant codes which were able to correct the upsets with reduction in area and power. These codes improved error coverage in memory compared with other codes [5].

S. Tambatkar, S. N. Menon, V. Sudarshan, M. Vinodhini and N. S. Murty presented that data present in memory and buffer need both error detecting and correcting codes. Errors may occur due to supply variations, noise and radiation. These can be temporary or permanent. So, a method based on the three-dimensional parity checking code was proposed. In encoder circuit the data bits have arranged in the form of matrix. The parity bits were calculated for all the elements in rows, columns and diagonals. The parity bits error detection, correction was performed by using Hamming code. In the decoder syndrome calculation technique was used for detecting, correcting of errors in the input data. This 3-D code has corrected up to 3 data bits and Hamming code corrected up to 3 parity bits. So, this method was used for detection and correction in both data and parity bits. This has achieved higher reliability when compared with the other methods [6].

P. Raha, M. Vinodhini and N. S. Murty suggested that due to various external radiations, soft errors were created which in turn lead to many critical issues. In order to rectify these soft errors, Single ECC was mainly used for detection, correction of single error. But this SEC method was somewhat inefficient. So, "Horizontal Vertical Parity and Diagonal Hamming" code was suggested for detecting errors till 8 bits and correcting errors up to 1-bit, 2-bit, different combinations of 3, 4 and 5bit errors. The main intent was to incorporate both encoder and decoder circuits so that they would be effective in detection and also correction of the errors. These circuits used 3 parity sets out of which first one was horizontal, second was vertical and the last was grouped diagonal parities. When the analysis was performed by using this technique, code rate achieved was higher compared with the existing ones [7].

S. Manoj and C. Babu proposed a novel approach to overcome various multiple cell upsets by incorporating error correction coding techniques. The matrix computer codes based on the hamming code have been proposed for the protection of computer storage. The main problem was that they were able to correct the double errors and also the error correction capacity was not improved in all the cases. Decimal matrix coding and Parity matrix coding were the two error correction coding techniques which were an improvement of matrix-based codes. These were based on the decimal algorithm which had lesser delay so that the reliability of the memory would be enhanced. An error reuse technique was used in order to reduce the area without causing any disturbance to both encoder and decoder circuits. These were compared with the other error correction techniques [8].

III. ERROR CORRECTING CODES IN MEMORIES

A. Communication Channel

In conventional communication systems, data is transmitted by using space as a medium over a communication channel. During transmission, data is

originated from the source. Data compression encoding for source takes place for an effective transfer of data. Channel encoding takes place for the reliable transmission of data and lastly modulation phenomenon for propagation of data in the channel. Then data can be sent in spatial domain. During transmission, data may be corrupted due to induction of noise. So, the received output data is demodulated and that is usually done by using decoding process.

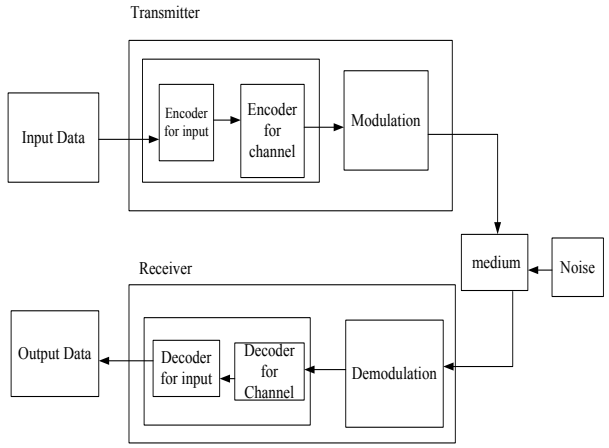

Fig 1: Block Diagram of Communication Channel

B. Memory System

This communication channel model is used for memory systems applications. Instead of spatial transmission, it takes place with respect to the time it is present in the cell of a memory. When write operation takes place the data comes from the input data bus and it is channel encoded by code and then stored by using the write circuit of memory. So, the data in memory travels and may be susceptible to external induced noise for example cosmic particles. When read request is activated, data is then demodulated by using the read circuit of the memory. Then channel can be decoded by using the necessary error correction codes. When error handling process is finished, then the data is placed on the output data bus of the memory.

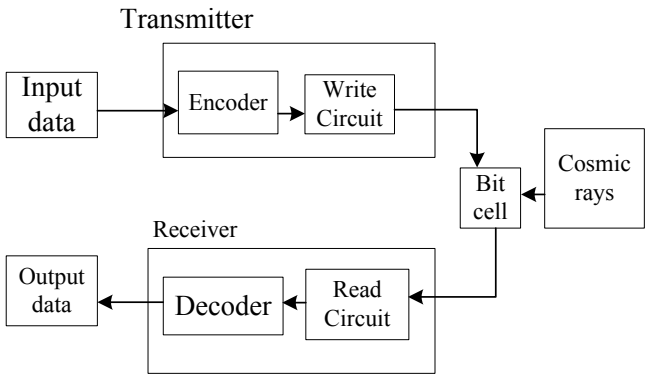

Fig 2: Block Diagram of Memory System

IV. ERROR CORRECTION TECHNIQUES

A. Error Detection and Correction Codes

The parity check bit generator is a combinational circuit which is present at the transmitter side, it accepts original data as an input and generates the parity bit as output for that original data. The transmitter used for transmitting the original data with parity bits. These parity bits are even and odd. In the Even parity number of one's are even and similarly in the odd parity number of one's are odd. The Code word is generated using LCPC code (Low Complexity Parity Check). This not only has low complexity but also has the low memory requirement. Syndrome calculation is a very efficient process of decoding in the case of noisy channel. It also has least distance decoding process with minimized look up table.

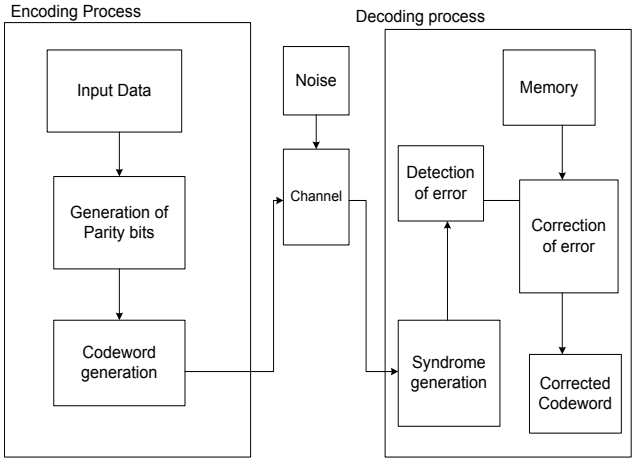

Fig 3: Block Diagram of Error Detection and Correction Codes

B. Basic Coding Process

A (d,b) error correction code has a d-bit word as input and b-bit word as output. The input word d is a vector of k bits vector which is used to represent the original data. And b is an n bits vector and (n−k) are usually the redundant bits added to the input word which are called as parity bits. When this code word b is transmitted across a channel it produces the received word. The error vector (e) is used to model the error which is interfered due to the channel noise. If error is not present then e equals to 0 or else e equals to 1. The received word is obtained by performing the XOR operation of code word (b) and error vector (e).

C. Hamming Code

These are linear correction codes generally used in telecommunication and memory applications. These are used for 1 bit error detection and correction with lesser redundancy. Here (7,4) hamming code is presented. Where 7 denotes the total code word and 4 refers data bits and 7-4=3 represents the parity bits to be added to the data bits. The drawback of this code is it can be used only for single bit error detection and correction [2].

In this Hamming Code Encoding process, there are 3 parity bits P1, P2, P4 and 4 data bits D1, D2, D3, D4 and the total encoded code word consists of 7 bits those are concatenation of P1, P2, D1, P4, D2, D3, D4 bits. The parity expressions are given as follows,

P1=D1^D2^D4
P2=D1^D3^D4
P4=D2^D3^D4 (1)

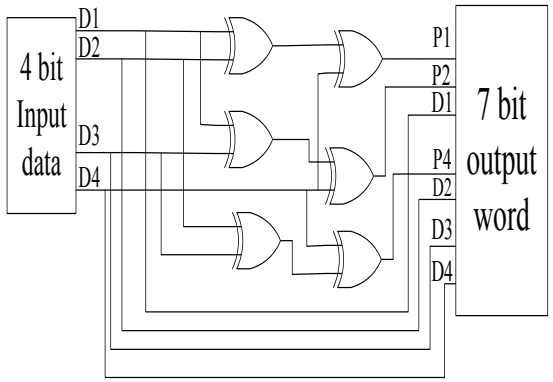

Fig 4: Hamming Code Encoder diagram

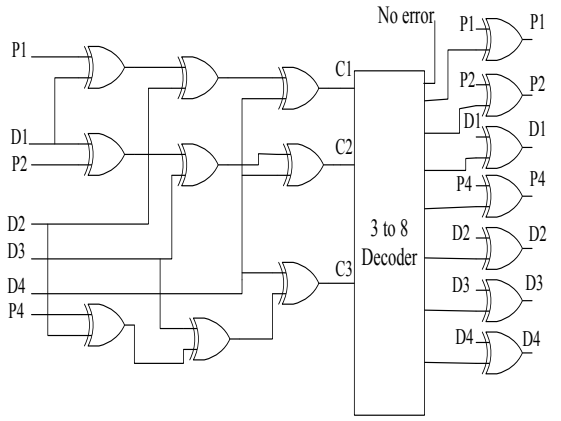

Fig 5: Hamming Code Decoder diagram

In this Decoder process, there are 3 check bits C1, C2, C3 and 4 data bits, 3 parity bits similar to that of encoder. It has 3 to 8 decoder which takes three inputs as check bits and generates 8 outputs out of which one is no error signal and remaining undergoes XOR operation with all the data and parity bits. The check bits expressions are given as follows.

C1=D1^D2^D4^P1
C2=D1^D3^D4^P2
C3=D2^D3^D4^P4 (2)

C. SEC-DED Code

Hamming codes are extended for the purpose of single error correction and double error detection. So, these are known as SEC–DED ("Single Error Correction Double Error Detection") or extended hamming code [1]. These require an extra bit for double error detection. It is calculated as even parity for the whole encoded output. By adding an extra bit that is for example d7, the (7,4) Hamming code is converted into another form of code known as (8,4) SEC–DED code [5]. d7 is an extra bit can be wriiten as follows:

$$d7 = d0 \oplus d1 \oplus d2 \oplus d3 \oplus d4 \oplus d5 \oplus d6 \quad (3)$$

That is the XOR operation of all the bits. In this the decoding process is used for checking two conditions one is the parity of the received word while the other syndrome calculation.

Table I Operation table of SEC-DED Code

Syndrome from hamming sh	Syndrome from parity sp	Operation
0	0	No Error is present
0	1	Correction of Single Error in entire received word
1	0	Detection of double error but not Corrected
1	1	Single error Correction at sh bits

V. PROPOSED WORK SEC-DED-DAEC CODE TECHNIQUE

The proposed code is defined as a linear block code. This code block diagram has two parts one is encoding and the other is decoding. In the encoding process, the encoded code word transmission takes place through a channel there may be occurrence of external noise or error. In the decoder, detection and correction of errors takes place in the received code word. The (14, 8) SEC-DED-DAEC ("Single Error Correction Double Error Detection Double Adjacent Error Correction") code refers to total code word that is 14 and the data equal to 8. The main blocks of these suggested codes are

1. Parity check generator
2. Syndrome generator and
3. Look up tables

In the proposed code, the number of redundant bits added are 14-8=6 bits. The major advantage by using this code is it has lesser complexity when compared with the other existing codes.

Here the novelty of the proposed research is the extension of SEC-DED code to SEC-DED-DAEC code which is used for single error correction, double error detection and double adjacent error correction. And also using this technique in Memory application and also providing an example for this technique.

A. Rules for H-matrix:

The H-matrix for suggested code has been developed using below conditions.

1. All the columns should be both distinct and non zero.

2. All columns of data should have weight as 3.

3. The XOR sum of 2 columns shouldn't be equal to the remaining columns.

4. And the XOR sum of any two adjacent columns must be both distinct and also non-zero.

The first condition mentioned is used for correction of single error. The detection of double error is performed by the conditions 1-3. The Double Adjacent Error Correction property is verified by using all the above conditions mentioned.

B. SEC-DED-DAEC Encoder

In this Encoder, the parity check expressions are as follows.

$$p1 = d[8]^d[6]^d[3]^d[2]$$
$$p2 = d[7]^d[6]^d[5]^d[4]^d[2]$$
$$p3 = d[8]^d[7]^d[4]^d[2]^d[1]$$
$$p4 = d[8]^d[5]^d[3]^d[1]$$
$$p5 = d[7]^d[5]$$
$$p6 = d[6]^d[4]^d[3]^d[1] \quad (5)$$

The Encoded output is the concatenation of all the 8 data bits and 6 parity bits.

$$Output = \{d1,d2,d3,d4,d5,d6,d7,d8,p1,p2,p3,p4,p5,p6\} \quad (6)$$

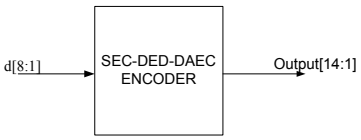

Fig 6: SEC-DED-DAEC Code Encoder Diagram

C. SEC-DED-DAEC Decoder

In the decoding process there are 6 syndrome check bits given as follows

s1=encode[14]^encode[12]^encode[9]^encode[8]^encode[6]
s2=encode[13]^encode[12]^encode[11]^encode[10]^encode[8]^encode[5]
s3=encode[14]^encode[13]^encode[10]^encode[8]^encode[7]^encode[4]
s4=encode[14]^encode[11]^encode[9]^encode[7]^encode[3]
s5= encode[13]^encode[11]^encode[2]
s6=encode[12]^encode[10]^encode[9]^encode[7]^encode[1] (7)

The Error Correction Block is used for checking single error (SE), double error (DE) and uncorrected error (UE).

The features of this decoder are it has [14:1] Encoded output data given as an input to the syndrome generator which provides 6 syndrome or check bits. And these are given as input to the Error Correction Block and generated outputs as SE-single error, DE-double error, UE-uncorrected error and out given to XOR logic where XOR operation takes place between out and encoded data so it finally provides the decoded output.

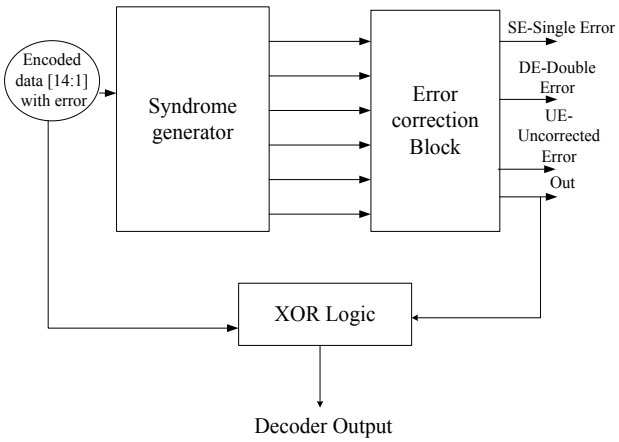

Fig 7: SEC-DED-DAEC Code Decoder Diagram

VI. SIMULATION RESULTS

All these Error Correction code techniques simulation results are verified by using Verilog Coding in Xilinx ISE 14.7 tool.

A. Hamming Code Encoder

In this Hamming Code Encoding process, there are 3 Parity bits are p1,p2,p3 and 4 data bits.

p1=data[0]^data[1]^data[3]
p2=data[0]^data[2]^data[3]
p3=data[1]^data[2]^data[3] (8)

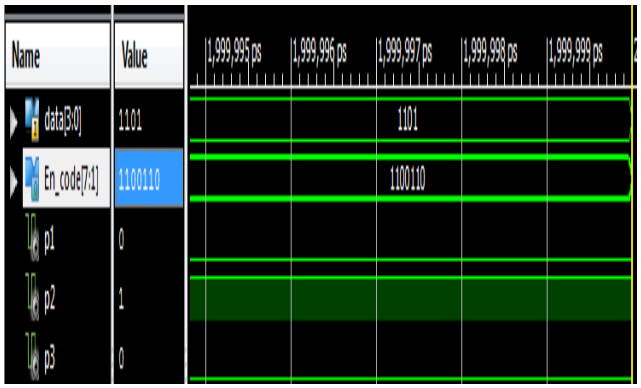

Fig 8: Hamming Code encoder output

In Fig 8 the output encode is obtained by combining all the four data bits and three parity bits. Here input data data[3:0]=1101 and the p1,p2,p3 are obtained by above parity expressions hence the encoded output Encode[7:1]=1100110.

B. Hamming Code Decoder

In this Decoder process, there are 3 check bits c[0], c[1],c[2].

c[0]=En_code[1]^En_code[3]^En_code[5]^En_code[7]
c[1]=E_ncode[2]^En_code[3]^En_code[6]^En_code[7]
c[2]=En_code[4]^En_code[5]^En_code[6]^En_code[7] (9)

In Fig 9 the encoded output obtained from Fig 8 Encode [7:1] =1100110 is introduced with 1 bit error in the first position that is 1100111 and given as an input to the hamming code decoder so 1 bit error detection and correction took place as a result decoded output Decode

[7:1] =encoded output Encode [7:1] =1100110. So, encoded output and decoded output are same so error detection and correction took place for 1 bit by using hamming code.

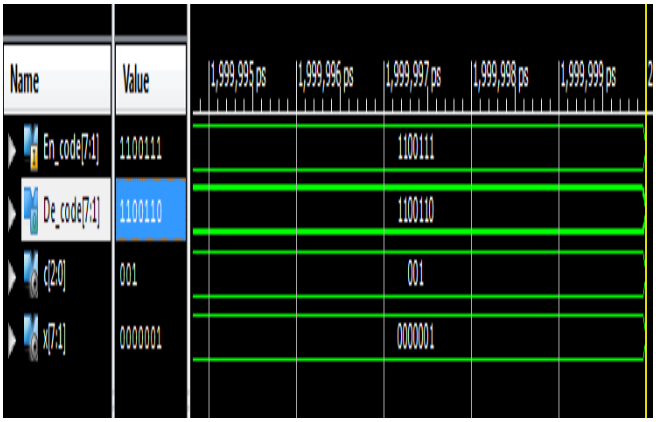

Fig 9: Hamming Code Decoder output for input=1100111

C. SEC-DED Code Encoder

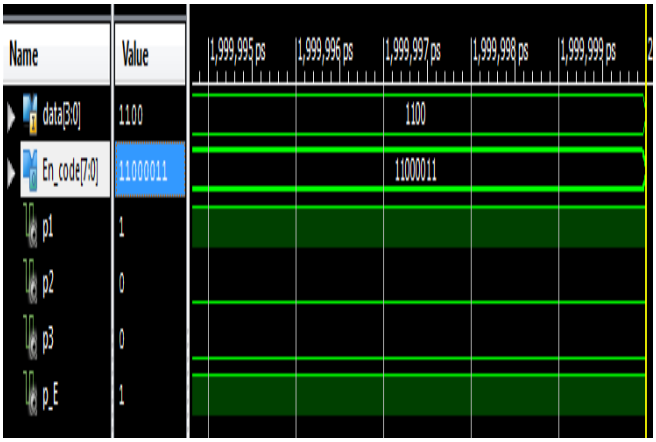

Fig 10: SEC-DED encoder output

In Fig 10 p_E=1 this SEC-DED code is an extension of the (7,4) hamming code so the extra bit for used for this code that is calculated by doing XOR operation of all the data and parity bits. Here 3 Parity bits p1,p2 and p3 are calculated based on the above mentioned hamming code equations. In this result p1=1, p2=0,p3=0 and the input data that is data [3:0]=1100, the encoded output is combination of all the data and parity bits hence Encode [7:0]=11000011.

D. SEC-DED Code Decoder

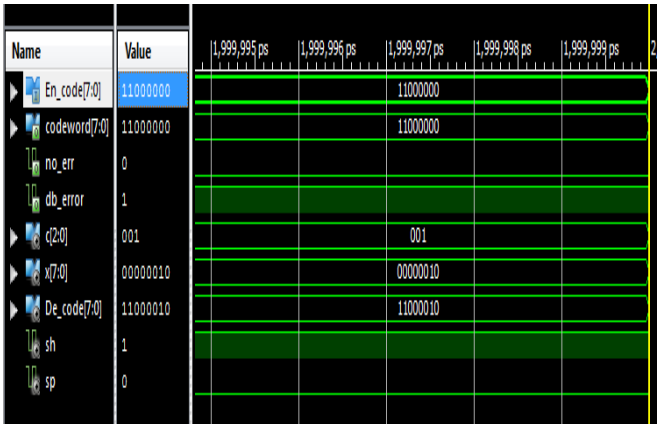

Fig 11: SEC-DED Decoder output when sh=1 and sp=0

In Fig 11 there are 3 check bits c[0], c[1] and c[2] which are calculated based on the hamming code expressions. And based on syndrome from hamming code (sh) and syndrome from parity (sp) different operations takes place. When sh=1 and sp=0 detection of double error takes place that is db=1. When Encoded output=11000011 is introduced with 2 errors at last two positions that is 11000000 and given as input to decoder double error detection db=1 takes place and single error correction also takes place.

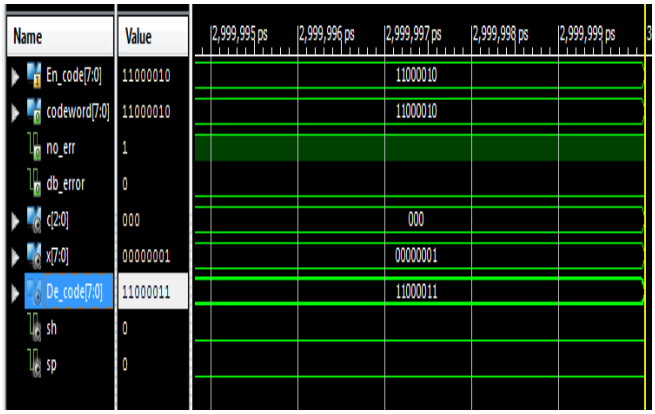

Fig 12: SEC-DED Decoder output when sh=0 and sp=0

In Fig 12 the encoded output=11000011 is introduced with an error in last position that is 11000010 and given as an input to the decoder. When sh=0 and sp=0 there is no error=1 and decoded output=encoded output=11000011.

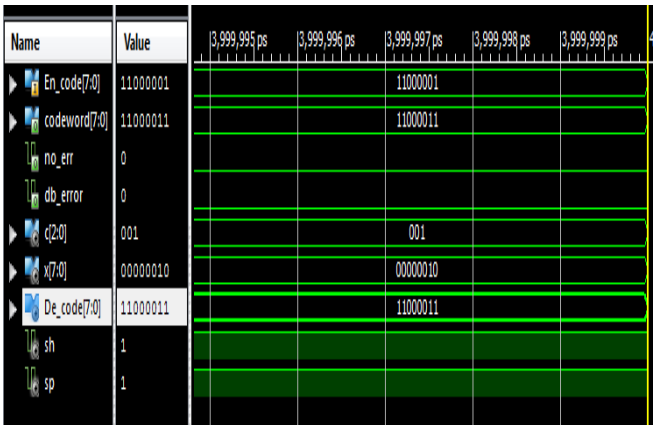

Fig 13: SEC-DED Decoder output when sh=1 and sp=1

In Fig 13 the encoded output =11000011 is given error in the last but one position that is 11000001. When sh=1 and sp=1 correction of single error takes place so that the decoded output=encoded output=11000011.

E. Proposed SEC-DED-DAEC Code Encoder

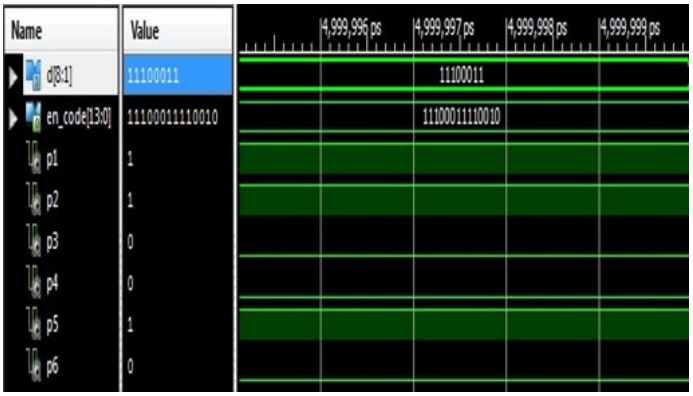

Fig 14: SEC-DED-DAEC Encoder output

In Fig 14 input data [8:1] =11100011 and by using the above parity equation (5) the output encoded data is obtained by performing concatenation of all the eight data bits and six parity bits. So, the encoded output [13:0] =11100011110010.

F. Proposed SEC-DED-DAEC Code Decoder

In Fig 15 the encoded output [13:0] = 11100011110010 is introduced with 2 errors in the first two positions that is 00100011110010 and given as an input for the decoder so that the double error detection and also correction took place DE=1 and OUT [14:1] represented the error positions which are present in the given encoded input data. Therefore, the decoded output [14:1] and encoded output [14:1] obtained were same values that is =11100011110010.

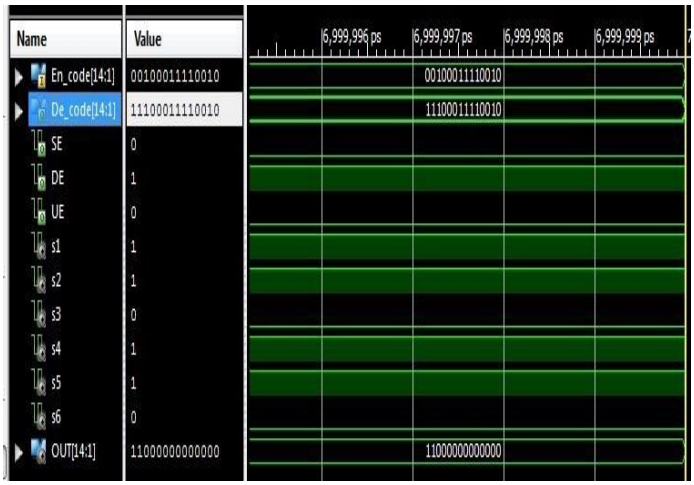

Fig 15: SEC-DED-DAEC Decoder output

VII. SEC-DED-DAEC CODE EXAMPLE

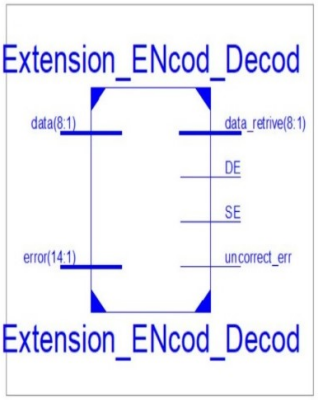

Fig 16: SEC-DED-DAEC Schematic Diagram

In Fig 16 this schematic diagram has data [8:1] and error [14:1] as input signals. It has outputs such as data retrieval of 8 bits [8:1], DE-Double Error, SE-Single Error and uncorrected error.

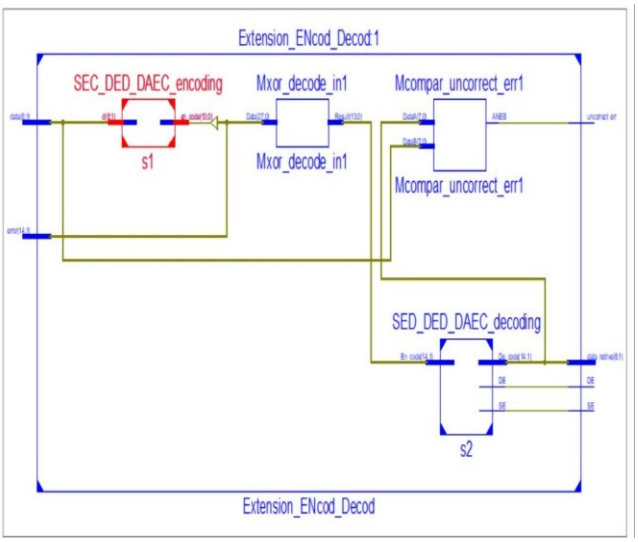

Fig 17: SEC-DED-DAEC Architecture Diagram

This architecture diagram has SEC-DED-DAEC Encoding and Decoding blocks. Along with that comparator for error correction block and XOR logic as shown in Fig 17.

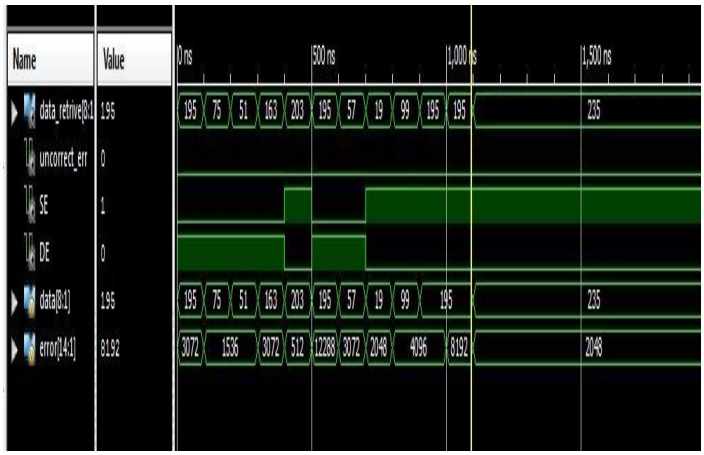

Fig 18: SEC-DED-DAEC Code Simulation Result

In this simulation result, the input data [8:1] and data retrieved [8:1] are both same at all instants even though there is occurrence of error. And single error signal SE=1, uncorrected error=0, DE=0, error has different values [14:1] at different values of data but irrespective of those different error values input data and data retrieved are both same as shown in Fig 18.

VIII. PROPOSED CODE IN MEMORY APPLICATION

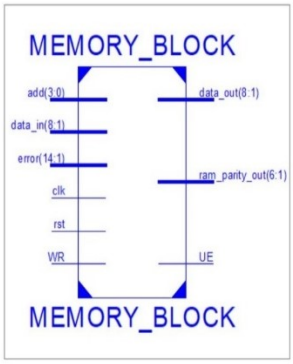

Fig 19: Memory Block Schematic Diagram

In Fig 19 Memory block Schematic Diagram has inputs as add [3:0], data input [8:1], error [14:1], clock-clk, reset-rst, write-WR and outputs has data out [8:1], ram parity out [6:1] and UE-Uncorrected Error.

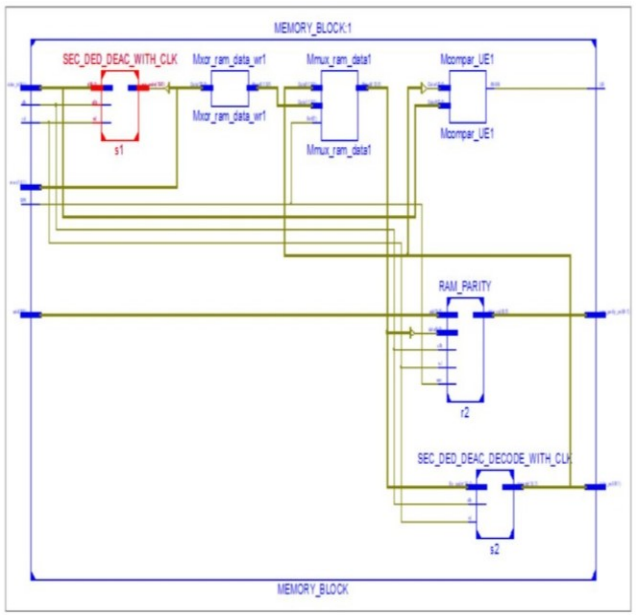

Fig 20: Memory Architecture Diagram

In Fig 20 Memory Architecture Diagram has SEC-DED-DAEC-CLK,SEC-DED-DAEC-DECODE-CLK, mux_ram_data1, compar_UE1, xor_ram_data_wr1 and RAM_PARITY.

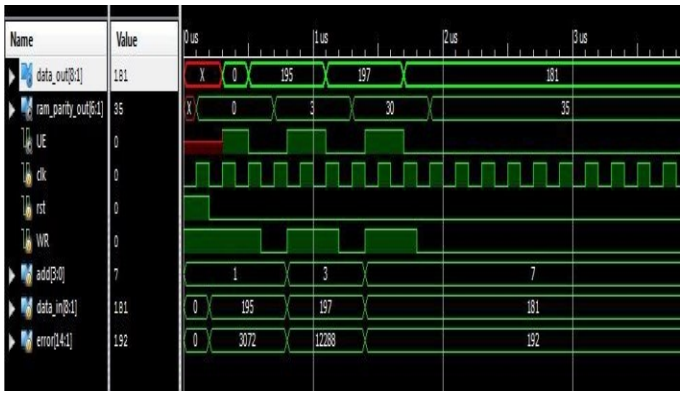

Fig 21: Simulation Result for Memory Application

In Fig 21 Simulation Result the data in [8:1] and data out [8:1] are same even though there is occurrence of different error [14:1] values at different values of data and by using this memory application we can store the obtained data out values. So, the data retrieval and also data storage took place even though there is occurrence of different values of errors hence data out and data in obtained are the same values in this memory application.

Table II Simulation Results

Code Technique	Encoder input	Encoder Output	Decoder Input	Decoder output
Hamming code	1101	1100110	1100111	1100110
SEC-DED code	1100	11000011	11000000	11000010 sh=1, sp=0
			11000010	11000011 sh=0, sp=0
			11000001	11000011 sh=1,sp=1

SEC-DED-DAEC code	11100011	111000111 10010	001000111 10010	111000111 10010

IX. CONCLUSION

As the technology scales down, various soft errors in SRAM memories were occurred due to which the single cell and multiple cell upsets were formed. Error Correction Codes such as the first technique (7,4) hamming code where 7 denotes total code word, four refers to data bits and 3 parity bits was implemented and verified its encoding and decoding processes. But it was useful only for single bit error detection and also correction which has been the main drawback of this hamming code. So, the second technique implemented was extended hamming code (8,4) or SEC-DED code ("Single Error Correction-Double Error Detection"). This code had an extra bit and used for correction of single error and also detection of double error. But correction of double error doesn't happen in SEC-DED code. So, the extension of (8,4) SEC-DED code was (14,8) SEC-DED-DAEC ("Single Error Correction-Double Error Detection-Double Adjacent Error Correction") code where 14 denotes total code word, 8 data bits, six parity bits which can be used for correction of single error, detection of double error and also correction of double adjacent error was proposed in this work. These techniques related Encoding and Decoding processes were studies and all the simulation results were verified and implemented by using Verilog Coding in Xilinx ISE 14.7 tool. This proposed SEC-DED-DAEC method was also implemented in Memory application and verified its output. The double error detection was adjacently corrected by this method and the complexity was decreased. The advantage of this proposed technique was it can able to detect and correct errors adjacently and limitation was there may be occurrence of multiple errors so this can be the further scope of this work. In this work presented error detection and correction up to 2 bits.

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