Error Detection and Correction Using RP SEC-DED

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Abstract— Error correcting codes are widely used to protect memories from radiation induced soft errors. With the advancement of the technology node, soft errors affect more than one bit in memory, as the circuitry is closely packed on a smaller area. Single Error Correction and Double Error Detection (SEC-DED) codes ensures that the contents of the memory gets rectified if corrupted. The Reduced Parity SEC-DED (RP SEC-DED) architecture that uses three blocks of SEC-DED is proposed here that detects six error bits and correct double bit error in first and second block and single bit error in the third SEC-DED block using 15-bits of parity. The input data word is assumed to be of 32-bits. The architecture is implemented using Verilog Hardware Description Language (HDL) in Xilinx Vivado® Design Suite V14.7. The comparative analysis is carried out to determine the number of parity bits used, area, power consumption, delay and the total number of logic gates used with the help of Cadence® Genus™ Synthesis Solution Version 17.2 tool at 45 nm technology with supply voltage of 1 V. The comparative analysis shows that there is a decrease in the number of parity bits used by 4 bits, 14.99% of decrease in area, 3.20% drop in power consumption, 18.48% reduction in delay and reduction of 39 logic gates used in the proposed RP SEC-DED architecture over the existing SEC-DED with DS based Architecture.

Keywords—error detection, error correction, parity, memories, soft errors, Single Error Correction-Double Error Detection (SEC-DED), Hamming code.

I. INTRODUCTION

The growth of modern communication systems has been primarily led by the development in error correcting codes. Traditionally, Single-Error Correction (SEC) was used to correct an error in a single memory cell but as technology scales down, the probability of multiple error is increased and there is a need to detect and correct multiple errors rather than single error. Electronic circuits started the use of Error Correcting Codes (ECCs), with the aim to protect the data. Various applications have different design requirements which led to different architectures for ECC. In most of the architectures, the decoding latency is a major issue which influences the algorithms and architecture for encoder and decoder to be efficient. Parallel decoders were used for double error correction, but these decoders are much more complex and have larger area, power consumption and delay compared to Single Error Correction and Double Error Detection (SEC-DED) codes [1]. The delay introduced due to the encoder and decoder must be of a small fraction to ensure that the correction speed of error correcting code is not effected.

The complexity in the architecture of the encoder and decoder depends on the size of the memory. To support correction capability for large capacity of memory, the complex decoder may constitute for small area overhead as compared to small capacity of memory. For memory, the data bits are 2^n, where n is equal to 1,2,3,…, n. In this work 32-bit data is used, as most of the communication Protocol used for reliable transmission such as Serial Peripheral Interface (SPI) and Peripheral Component Interconnect (PCI) use 32-bit data.

The main problem with error correcting codes is the requirement of number of redundant bits, codes such as Orthogonal Latin Squares [2] have higher number of redundant bits than other ECC codes. However, the number of redundant bits in Orthogonal Latin Square method are reduced by Extended Orthogonal Latin Square codes (EOLS) [5]. Redundant bits are appended along with data bits to detect and correct the errors encountered during transmission. The capacity of the memory relies on the number of redundant bits (parity bits) [9]. Higher number of redundant bits increases the detection ability [11] at the cost of increase in area and delay. As it is known in the era of 5G technology where data communication is paramount, the accuracy and security of data are most important. Thus, with the advancement in technology, there is a need for more powerful Error Correcting Codes to detect and correct more than single bit error with minimum number of parity bits so as to reduce the area consumption. In this work, an architecture with Reduced Parity SEC-DED (RP SEC-DED) is proposed. The comparative analysis of proposed architecture is carried out with respect to the existing SEC-DED with Difference Set Architecture [1] to determine the number of parity bits used, area, power consumption, delay and the total number of logic gates used. A typical application of this method is to enhance edge computing on embedded platforms as demonstrated in [12] and use cloud to enable seamless data communication in 5G technology.

The paper organisation shows literature survey on ECC architectures in Section II, Section III describes the proposed Reduced Parity SEC-DED (RP SEC-DED) in detail. Section IV conveys the simulation results and comparative analysis followed by conclusion and future scope in Section V.

II. LITERATURE REVIEW FOR ECC ARCHITECTURE

A Double Error Correction (DEC) code for 32-bit input data word that allows faster decoding of the encoded input compared to existing codes is discussed in [1]. A DEC code has been derived from a combination of Single Error Correction-Double Error Detection (SEC-DED) code and Difference Set (DS) code. This method has demonstrated that with less number of parity bits, an input can be encoded successfully in lieu of slightly complex decoding logic. The fault detection and correction coverage using matrix code, is studied as better option than Reed-Muller and Hamming code method [3]. To detect multiple errors in a 32-bit data word, the matrix code combines both Hamming code and parity code. The data is arranged in the matrix format, vertical and horizontal check bits are added for each column and row for SEC-DED. It is understood that matrix code method requires more parity bits that increases the storage area of bits [3].

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Horizontal-Vertical-Diagonal (HVD) method indicates that the fault correction coverage is 100% for 3-bit upsets [4]. The code rate i.e. the number of data bits to number of bits in code word of HVD method is specified as better than BCH and Golay codes [4]. The HVD method appends parity bits in row, column and two diagonals on a data part that leads to more number of parity bits. Diagonal parity bits increases the error detection ability as compared to matrix code method. Extended Orthogonal Latin Square (EOLS) codes divides data into multiple groups provided each data bit participates in at most one of the parity bits [5]. Extended OLS codes are preferred where the data block sizes are not a power of two. Most of the applications uses the data block with power two, limiting the use of extended OLS codes.

Modified Bose, Ray- Chaudhuri, Hocquenghem (BCH) decoder shows 30% of reduction in its architecture complexity as compared to the conventional BCH decoder architecture [6]. It is perceived that the delay incurred in this architecture is more due to the usage of four cascaded modules in the decoder block. A new error correction codes to correct 5-bit adjacent errors is discussed in [7]. A Parity check matrix of size (25, 16), (42, 32) and (75, 64) was used to perform the encoding and decoding operation which lead to increase in the number of error correction and improvements in power consumption compared to Quadruple Adjacent Error Correction method. The modified architecture of the Triple Modular Redundancy with Single Error Correcting (SEC) codes and Double Error Detecting (DEC) codes explained in [8] can detect up to two and four errors with improvements in area, power consumption and delay compared to the existing Triple Modular Redundancy technique with Single Error Correcting codes that can detect only two errors.

Ultrafast codes have been presented in [13] with an objective to achieve fast encoding and decoding operations. The number of parity bits used are same as that of the data bits i.e both are of 8 bits. Ultrafast codes were enhanced to obtain SEC-xAEC-DED for multiple adjacent error correction maintaining the parity bits of Ultrafast codes. Using these codes, the speed of 64-bit data words is increased by 160%. A method to reduce the complexity of adjacent error correcting decoder is discussed in [14]. The compact expressions obtained by Karnaugh map are used to design the existing SEC-DED-DAEC and SEC-DED-TAEC codes decoders with reduced number of logic gates. An area efficient ECC (72, 64) and ECC (39, 32) code as proposed in [15] can detect adjacent 3-bit error and correct adjacent 2-bit error without any extra parity bit. ECC (73, 64) and ECC (40, 32) code is also proposed in [15] which can detect and correct both adjacent 2-bit and 3-bit errors with one extra parity bit. With optimized syndrome calculation, ECC (73, 64) reduces the number of two input XOR gates by 30% as compared to SEC-DED code.

III. Proposed Architecture for Reduced Parity SEC-DED (RP SEC-DED)

An architecture for Reduced Parity SEC-DED (RP SEC-DED) that uses three blocks of SEC-DED is proposed to detect six error bits and correct double bit error in first and second block and single bit error in the third block using 15-bits of parity. The first two SEC-DED blocks can detect four bits of error and correct the same four bits. The third SEC-DED block can detect two bits of error and can correct only one bit. The architecture is implemented using Verilog in Xilinx Vivado® Design Suite V14.7. The analysis is carried out in terms of number of parity bits used, area, power consumption, delay and total number of logic gates used with the help of Cadence® Genus™ Synthesis Solution Version 17.2 tool. The input data word is assumed to be of 32-bits. This approach is highly useful in the design of memories protecting them from various soft errors that can inhibit their optimal operation.

The primer as an introduction to the proposed RP SEC-DED architecture is discussed below. Any information source has a sequence of binary bits as logic '0' or logic '1' as its output. In case of block coding, the message is divided into fixed size of blocks to which redundant bits called as parity bits are appended. For an (n, k) block code, there are 2^k distinct messages. Hamming code is a type of block code.

The encoder for any block code is complicated due to the huge number of gates corresponding to the values of k and n, since the encoder is supposed to store 2^k different code words which can be of a length up to n-bits. A given binary block code can be decisively linear only if the mod-2 sum of any two given code words forms another valid code word. Any linear block code possess the systematic structure if it is of the form as shown in Fig. 1.

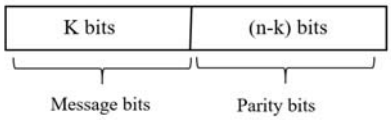


Fig. 1. Structure of a general Linear block code

A. Hamming Code

Hamming code is a linear block code which is able to detect two-bit errors and correct single-bit error. The encoding process of a Hamming code block consists of two steps as detailed below:

1) Calculating the total number of parity bits: During the transmission of a message, if n is the output of the encoder and p refers to the number of message bits, the number of parity bits to be added can be decided by using equation (1).

$$2^p \geq n + p + 1 \quad (1)$$

2) Calculating the values of each parity bit and positioning them: The parity bits are placed at the positions of power of 2 such as 1, 2, 4, 6, 8, 16 etc as shown in Table I. There are two configurations for encoding and detection of errors. When the total number of parity bits appended to the message bits is an even number then it is called as even parity else odd parity.

TABLE I. Parity and Data bit Position in A Hamming Code

Bit	D_3	D_2	D_1	P_2	D_0	P_1	P_0
Position	7	6	5	4	3	2	1

The parity bits are calculated using equation (2), (3) and (4):

$$P_2 = D_3 \oplus D_2 \oplus D_1 \quad (2)$$

$$P_1 = D_3 \oplus D_2 \oplus D_0 \quad (3)$$

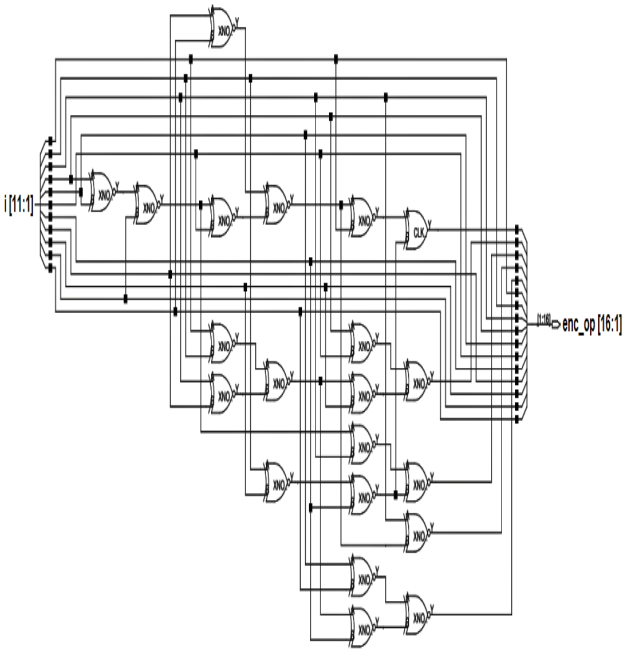
$$P_0 = D_3 \oplus D_1 \oplus D_0 \quad (4)$$

For the decoding of the Hamming code, parity bits are checked for odd parity and is compared with the parity at the encoder. If the parity matches then there is no error else an error is detected. For error correction, the decimal value of the recomputed parity bits at the receiver end is calculated and the corresponding bit is corrected.

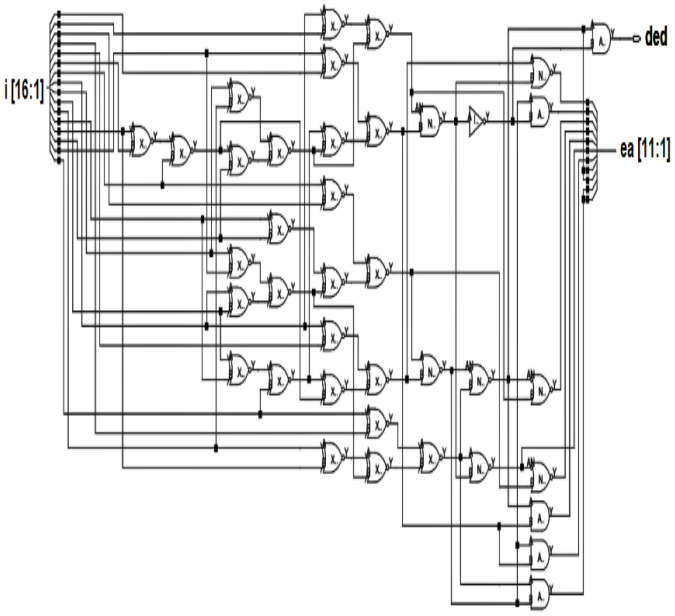
For any Hamming code, the minimum hamming distance is three. Hence, Hamming code is used to correct single error only. The difference between single and double bit error cannot be detected by the hamming code decoder and may cause miscorrection. To overcome this problem of hamming code, extra parity bit is appended so that the minimum hamming distance is four and the decoder can now differentiate between single and double bit error and perform Single Error Correction and Double Error Detection (SEC-DED).

B. Single Error Correction and Double Error Detection (SEC-DED) Code for the proposed RP SEC-DED method

SEC-DED code can be used for block sizes equal to the power of two. The number of XOR gates used in the encoder corresponds to the number of ones in the generator matrix of SEC-DED code. Hence, the encoder can be formed with the help of generator matrix. A hamming code of (15, 11) can be made a SEC-DED code by adding one extra parity bit to form a (16, 11) SEC-DED code with hamming distance of four. The error detection and correction capability increases with increase in the hamming distance. The parity check (H) matrix selected to implement the SEC-DED block satisfies the following two conditions.



(a)



(b)

Fig. 2. (a) Schematic diagram of a (16, 11) SEC-DED Encoder Architecture (b) Schematic diagram of a (16, 11) SEC-DED Decoder Architecture

1. The columns of parity check matrix (H) are linearly independent, the sum of two columns is nonzero and is not equal to the third column.

2. The column vectors of parity check matrix (H) is nonzero and are distinct.

The encoder block for (16, 11) SEC-DED is shown in Fig. 2 (a). The same block has been used (3 in number) in the proposed RP SEC-DED Encoder Architecture as shown in Fig. 3. The generator matrix G of a (16, 11) SEC-DED code is used to encode the information data into the code word. Hamming code is based on the basis of G matrix. G matrix is a combination of identity I and parity matrix P and it can be formed by the equation (5). The parity bits are denoted by r.

$$G_{k\times n} = [I_{k\times k} | P_{k\times r}] \quad (5)$$

The parity check matrix of (16, 11) SEC-DED code is used to decode and to correct the code word. The parity check matrix is the combination of negative value of transpose of parity matrix and identity matrix and can be formed by the equation (6).

$$H_{r\times n} = [-P^T_{k\times r} | I_{r\times r}] \quad (6)$$

The relation between the Generator matrix and parity check matrix is given by equation (7).

$$G * H^T = 0 \quad (7)$$

The SEC-DED decoder is designed in such a way that it has k number of AND gates with each gate having (n-k) inputs. Syndrome is computed at the decoder end by comparing the recomputed parity bits against the parity bits at the encoder end [10]. The main characteristics of SEC-DED code are SEC-DED codes can correct single bit errors and detect double bit errors, the block size must be equal to

the power of two, and the delay introduced due to the encoder and decoder is medium.

The proposed RP SEC-DED encoder architecture is as shown in Fig. 3. It consists of three (16, 11) SEC-DED blocks. Each of the SEC-DED block has five parity bits, resulting into total 15-bits of parity in the architecture. The first block has p_{1a}, p_{2a}… p_{5a} parity bits. The second block has p_{1b}, p_{2b}… p_{5b} and the third block has p_{1c}, p_{2c}… p_{5c} as parity bits. The 32-bit input data word has been divided into three blocks. Input to the first and second block is of 11-bits each i.e. i_1, i_2… i_{11} and i_{12}, i_{13}… i_{22} respectively. The input to the third block consists of first 10-bits as i_{23}, i_{24}… i_{32} and appended with the 11th bit as 0.

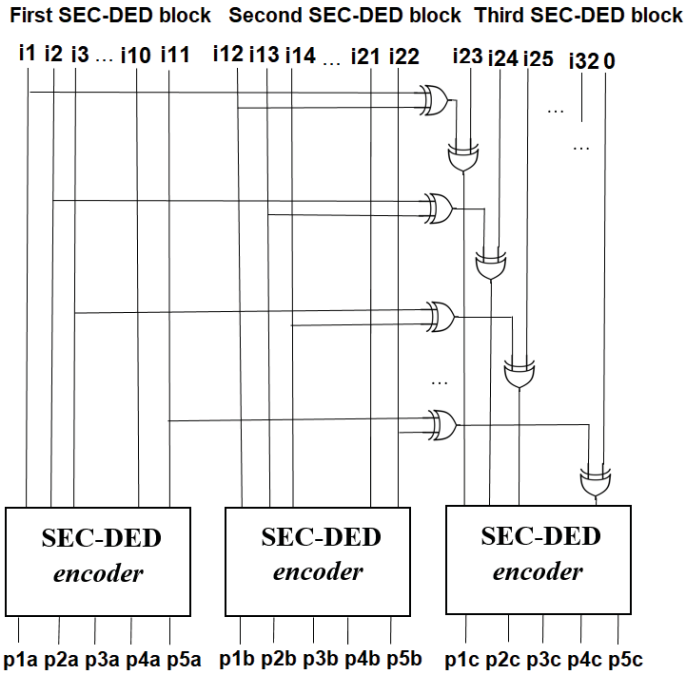


Fig. 3. Proposed RP SEC-DED Encoder architecture.

For detection and correction of error in the 32-bit data word the error correction signals for the first, & second and third SEC-DED blocks are e1a, e2a,…, e11a, & e1b, e2b,…, e11b and e1c, e2c,…, e11c respectively. These signals are generated by the decoding architecture of the proposed method and these signals are shown in the decoder given in Fig 4.

For double error correction, the correction signals from the third block are needed along with additional logic. The (16, 11) SEC-DED block for Decoder shown in Fig. 2 (b), has been used (3 in number) in the proposed RP SEC-DED Decoder Architecture as shown in Fig. 4. If Double Error Detected (DED) signal in Fig. 4, is not activated that indicates a single bit error. Single bit error is corrected with the help of the correction signals from the first and second block, if one bit of error is present in the first and second block. If Double Error Detected (DED) signal is activated, it indicates that there is double bit error present. The correction signal from the third block is used to perform the correction. The correction signals of the third SEC-DED block will be activated and can be used to correct two bits.

If the error is present in the third block then to correct this, the correction procedure is complex than the error correction of first and second block. As the third SEC-DED decoder block has inputs from the XOR of the bits from the first, second and third SEC-DED blocks, the correction signal of the third SEC-DED block may be activated by error on first, second or third block. The i23 bit of the third block would be correct if there is an error on bit i1 and i12. The correction logic of the data bits in the third block is described below:

- If any of the two Double Error Detected (DED) signals from the first and second SEC-DED block is activated, correction is not made because the third block has no errors during this case. The correction of the input data bits in the third block is made, when the XOR of the correction signals from the first and second blocks along with the input of the third block is logic ‘1’.
- The correction signals from the first and second block can be used to ensure that there is no miscorrection in the third block. For example the error present in the data bit i1 would activate the correction signals e1a and e1c which results the output of the XOR to be zero and bit i23 is not corrected.
- A double bit error on i1 and i23 would activate the e1a correction signal only. Hence, the output of XOR gate is logic ‘1’ and bit i23 is corrected.

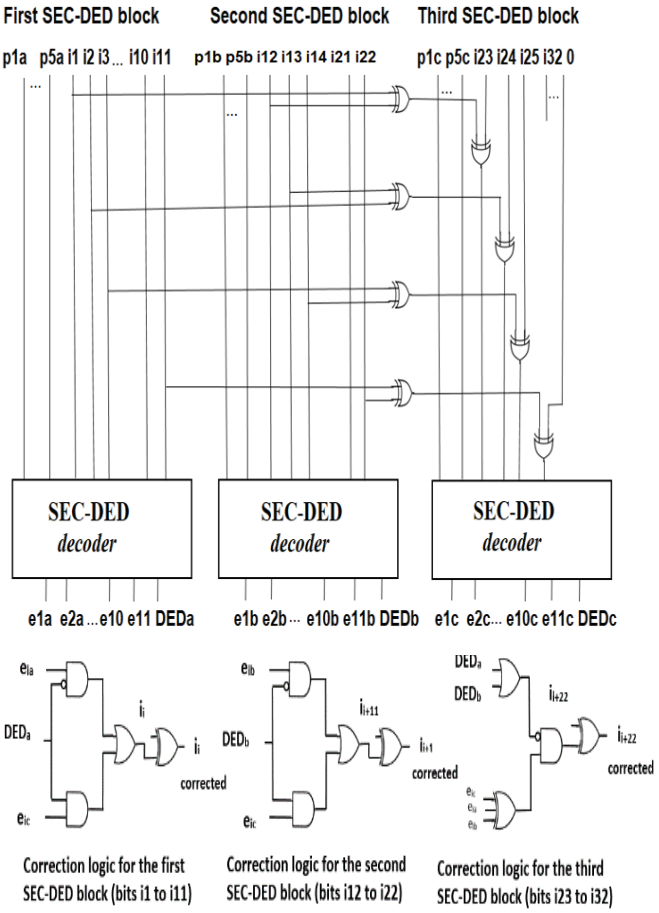


Fig. 4. Proposed RP SEC-DED Decoder architecture

By using the proposed decoding logic, that uses 15 parity bits to correct the error, double error correction is achieved in first and second block with the help of correction signals from third block which in turn corrects one bit of error. As a result, six error bits can be detected and double bit error in

first and second block and single bit error in the third SEC-DED block can be corrected by the proposed RP SEC-DED architecture for Encoder and Decoder. The number of parity bits used in proposed RP SEC-DED architecture uses 4 less number of parity bits as compared to SEC-DED architecture from [1], where use of 19 parity bits is studied.

IV. Simulation Results and Analysis

The Reduced Parity SEC-DED (RP SEC-DED) architecture that uses three blocks of SEC-DED is proposed to detect six error bits and correct double bit error in first and second block and single bit error in the third SEC-DED block using 15-bits of parity. The input data word is assumed to be of 32-bits. The first two SEC-DED blocks can detect four bits of error and correct the same four bits. The third SEC-DED block can detect two bits of error and can correct only one bit.

The architecture is implemented using Verilog Hardware Description Language (HDL) in Xilinx Vivado® Design Suite V14.7. The comparative analysis is carried out in terms of parity bits used, area, power consumption, delay and total number of logic gates used using Cadence® Genus™ Synthesis Solution Version 17.2 tool at 45nm technology with supply voltage of 1 V.

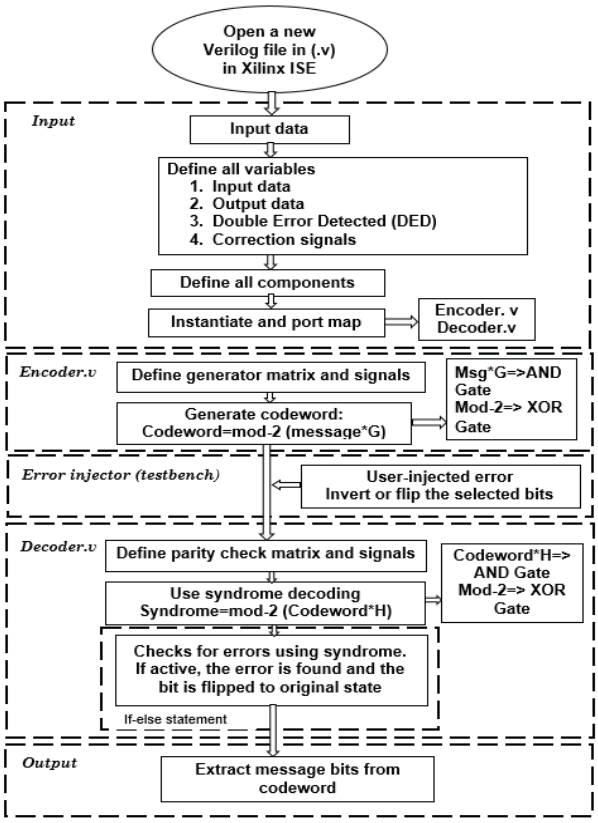


Fig. 5. Flow-chart for data activity in the proposed RP SEC-DED architecture for Encoder and Decoder

The entire data path that shows the activity of data through various blocks of the proposed RP SEC-DED is manifested in the form of a flow chart as shown in Fig. 5.

The output of the encoder module is of n-bits in length. The errors were injected in the written test bench to verify the functionality of the proposed architecture. The result is the extracted message bits from the code word. The output of encoder and decoder block should match to ensure that if at all there was an error in the information message sent is detected and corrected by the proposed architecture.

Fig. 6. (a) Functionality of proposed RP SEC-DED Encoder Architecture (b) Functionality of proposed RP SEC-DED Decoder Architecture for first block of SEC-DED (similar functionality is observed for second block of SEC-DED) and (c) Functionality of proposed RP SEC-DED Decoder Architecture for third block of SEC-DED

The functionality of the proposed architecture of RP SEC-DED encoder, decoder for first and third block is depicted in Fig. 6 (a), (b) and (c) respectively. The 32-bits input data and the corresponding encoded output is shown in Fig. 6 (a). The output of the first SEC-DED decoder block for double error correction can be obtained as Fig. 6. (b), which is observed as same for the second block of SEC-DED. Fig. 6 (c) shows the correction of error present in third SEC-DED block. The inputs are i1, i2, i3 and i1_c, i2_c, i3_c are the outputs of the architecture. As an example, the input sample, error sample and the received output for one of the simulated case for the proposed RP SEC-DED architecture is stated here. The assumed 32-bits of input data is "10111100101111100000111100110011" which is divided

among three (16, 11) SEC-DED encoder blocks. The input data for first, second and third SEC-DED encoder blocks are "10111100101", "11110000011" and "1100110011" respectively. The third SEC-DED block input gets appended with one bit of logic '0' as per the proposed architecture, resulting into the 11-bits of input to the third SEC-DED block as "11001100110". The data after the error gets injected to the encoded output which is of 16-bits from first block is "0111110010110110", and the corrected decoder output received for the first block is "10111100101" with DEDa signal as logic '1' for double error. The simulation is carried out for 100 ns.

TABLE II. COMPARATIVE ANALYSIS OF PROPOSED RP SEC-DED ARCHITECTURE AND SEC-DED WITH DS BASED ARCHITECTURE FROM [1]

Parameters	SEC-DED with DS based Architecture [1]	Proposed RP SEC-DED Architecture	% Improvement in Proposed RP SEC-DED Architecture over SEC-DED with DS based Architecture
Parity Bits	19	15	21.05%
Area (um^2)	742.379	631.101	14.99%
Power (uW)	160.805	155.654	3.20%
Delay (ps)	1688	1376	18.48%
Total number of Logic Gates used	220	181	17.72%

A comparative analysis is carried out for the proposed RP SEC-DED architecture with the existing SEC-DED with DS based architecture [1] with respect to number of parity bits used, area, power consumption, delay and total number of gates used as shown in Table II. Both architectures were implemented using Verilog HDL and verified for their functionality using 32-bit data word. The comparison shows that there is a decrease in the number of parity bits by 4-bits, 14.99% of decrease in area, 3.20% drop in power consumption, 18.48% reduction in delay and reduction of 39 logic gates used in the proposed RP SEC-DED architecture over SEC-DED with DS based Architecture from [1].

V. CONCLUSION AND FUTURE SCOPE

Single Error Correction Double Error Detection (SEC-DED) codes are used to ensure that the contents of the memory are not corrupted. SEC-DED can correct one bit error and rectify soft errors in memories. There is a need to detect more than one bit for efficient and reliable transmission. The Reduced Parity SEC-DED (RP SEC-DED) architecture that uses three blocks of SEC-DED is proposed to detect six error bits and correct double bit error in first and second block and single bit error in the third SEC-DED block using 15-bits of parity. The input data word is assumed to be of 32-bits. The first two SEC-DED blocks can detect four bits of error and correct the same four bits. The third SEC-DED block can detect two bits of error and can correct only one bit of error. The architecture is implemented using Verilog Hardware Description Language (HDL) in Xilinx Vivado® Design Suite V14.7. The comparative analysis is carried out to determine the number of parity bits used, area, power consumption, delay and the total number of logic gates used with the help of Cadence® Genus™ Synthesis Solution Version 17.2 tool at 45nm technology with supply voltage of 1 V. The comparison shows that there is a decrease in the number of parity bits by 4-bits, 14.99% of decrease in area, 3.20% drop in power consumption, 18.48% reduction in delay and reduction of 39 logic gates used in the proposed RP SEC-DED architecture over existing SEC-DED with DS based Architecture. As a future work, an optimized design of parity check matrix can be constructed so as to have multiple bit error detection and correction.

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