Rambus

INTERFACE IP
White Paper

Data Center Evolution: The Leap to 64 GT/s Signaling with PCI Express 6.1

Introduction

The PCI Express® (PCIe®) specification has served as the interconnect of choice in computing for nearly two decades. Its ongoing improvements in bandwidth and power efficiency have met the industry's demands for a high-speed, low-latency and scalable interconnect solution. Delivering performance and cost effectiveness, PCIe technology has been adopted across a broad landscape of data-intensive markets including data center, AI/ML, HPC, automotive, IoT, defense and aerospace.

From the introduction of PCIe 3.0 in 2010 onward, each new generation of the standard has offered double the signaling rate of its predecessor. PCIe 3.0 saw a significant change to the protocol with the move from 8b/10b to highly efficient 128b/130b encoding.

The following chart shows the evolution of the PCIe specification over time:

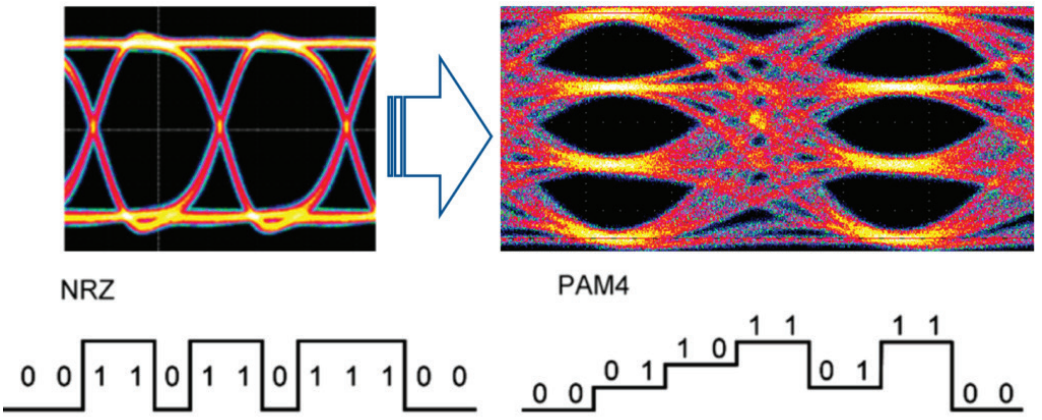
PCIe Specifications	Data Rate per Lane	Encoding	x16 Bandwidth (GB/s)	Specification Ratification Year
1.x	2.5	8b/10b	4	2003
2.x	5	8b/10b	8	2007
3.x	8	128b/130b	15.75	2010
4.0	16	128b/130b	31.5	2017
5.0	32	128b/130b	63	2019
6.x	64	PAM4/FLIT	128	2022

The PCIe 6.0 specification, released in 2022, doubled the signaling rate to 64 gigatransfers per second (GT/s) and did so with some of the most fundamental changes yet seen by the standard. PCIe 6.0 has since evolved to version 6.1 of the specification.

Features and Innovations

PAM4 Signaling

On the electrical layer, PCIe 6.1 uses PAM4 signaling ("Pulse Amplitude Modulation with four levels"). PAM4 signaling combines two bits per clock cycle for four amplitude levels (00, 01, 10, 11) vs. PCIe 5.0, and earlier generations, which used NRZ ("Non-Return-to-Zero" also known as "Pulse Amplitude Modulation with two levels") modulation with one bit per clock cycle and two amplitude levels (0, 1).



Comparison of NRZ modulation and PAM4 modulation

Forward Error Correction (FEC)

There are always trade-offs, however, and the transition to PAM4 signal encoding introduces a significantly higher Bit Error Rate (BER) vs. NRZ. You can see from the images above, if the maximum voltage level is the same, the voltage margin (eye opening) between levels is much smaller with PAM4.

This prompted the adoption of a Forward Error Correction (FEC) mechanism to mitigate the higher error rate inherent in PAM4. PCIe 6.1 adopts an FEC that is sufficiently lightweight to have minimal impact on latency. It works in conjunction with strong CRC (Cyclic Redundancy Check) to minimize the Link Retry probability. This new FEC feature targets an added latency of under 2ns.

FLIT Mode

PCIe 6.1 uses FLIT mode, where packets are organized in Flow Control Units of fixed sizes, as opposed to variable sizes in past PCIe generations. The initial reason for introducing FLIT mode was that error correction requires working with fixed size packets; however, FLIT mode also simplifies data management at the controller level and results in higher bandwidth efficiency, lower latency, and smaller controller footprint.

With fixed-size packets, the framing of packets at the Physical Layer is no longer needed yielding a 4-byte savings for every packet. FLIT encoding also does away with the 128B/130B encoding and DLLP (Data Link Layer Packets) overhead from previous PCIe specifications. This results in a significantly higher TLP (Transaction Layer Packet) efficiency, especially for smaller packets.

L0p Mode

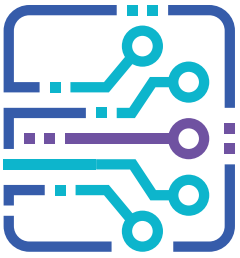
A final innovation to highlight in this paper is the introduction of a new Low Power State or L0p mode. L0p enables traffic to run on a reduced number of lanes to save power. L0p maintains at least one active lane at all times to ensure uninterrupted traffic flow. The link always trains in the highest possible width and can modulate down (and back up again) as needed by the traffic. One of the upshots as a trade off between power savings and complexity is that PCIe 6.1 only supports x1, x2, x4, x8 and x16 links. Support for x3, x5, x12, etc. and the huge (and rarely if ever implemented) x32 width have been dropped.

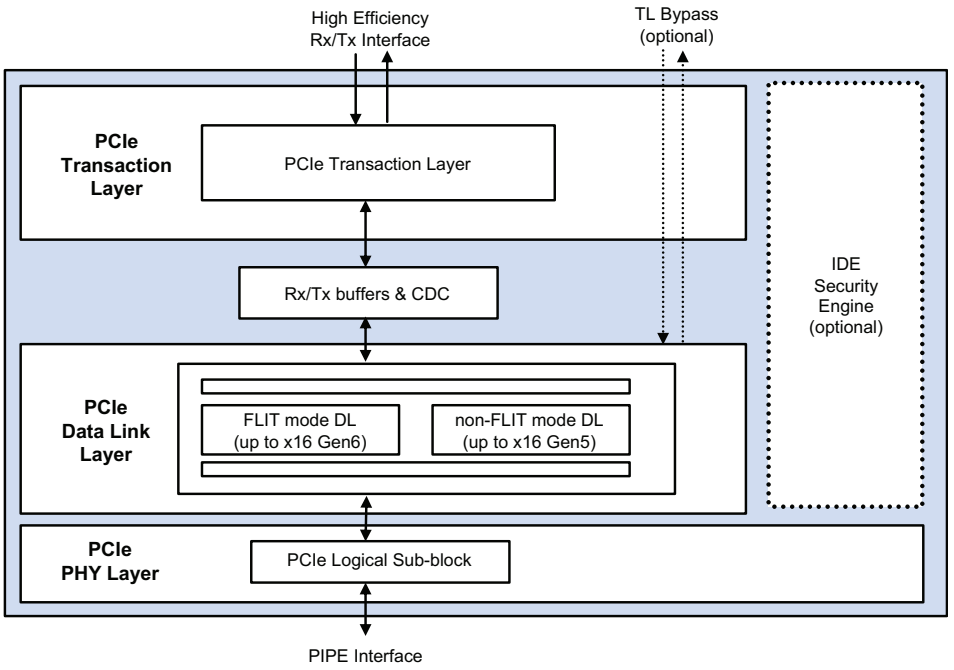
Rambus PCIe 6.1 Controller IP

The Rambus PCIe 6.1 Controller is designed to help customers take advantage of the key new features and innovations offered by PCIe 6.1. This IP solution builds on the successful track record of hundreds of Rambus customers who have successfully deployed Rambus PCIe IP in their ASIC, SoC and FPGA designs.

The **Rambus PCIe 6.1 Controller** is a low-power, area-optimized, silicon IP core designed with a system-oriented approach to maximize flexibility and ease of integration. It supports the PCIe 6.1 specification, including 64 GT/s data rates, PAM4 signaling, FLIT mode, and L0p power mode, and is backward compatible to the PCIe 5.0, 4.0 and 3.1/3.0 specifications. The Controller is built on flexible architecture models and can be tailored to meet the unique requirements of specific customer use cases.

The Rambus PCIe 6.1 Controller exposes a highly efficient transmit (Tx) and receive (Rx) interface with configurable bus widths. The IP can be configured to support endpoint, root port, switch port, and dual-mode topologies, allowing for a variety of use models. The provided Graphical User Interface (GUI) Wizard allows designers to tailor the IP to their exact requirements, by enabling, disabling, and adjusting a vast array of parameters. For applications that require state of-the-art security, the Rambus PCIe 6.1 controller offers an integrated IDE (Integrity and Data Encryption) security engine as an optional extra. Rambus also provides integration and validation of the PCIe 6.1 Controller with the customer's choice of PCIe 6.1 PHY.





PCIe 6.1 Controller Block Diagram

Controller highlights include:

- Optimized for high-bandwidth efficiency at data rates up to 64 GT/s
- Scalable data path
- Advanced PIPE modes and port bifurcation
- Supports multiple virtual channels
- (VCs) in FLIT and non-FLIT modes
- Supports Endpoint, Root-Port, Dual-mode, Switch port configurations
- Advanced RAS features
- Optional IDE security with AES-GCM encryption, decryption and authentication

For more information, visit
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