EECE 277
FPGA Design

Fall 2014, Dr. William H. Robinson

Laboratory Assignment One

Due: *Friday, September 12, 2014 at the beginning of class*

OBJECTIVE

The purpose of the assignment is to familiarize you with the EDA tools used in the course (Quartus II and ModelSim-Altera) and the DE2-115 Development and Education Board.

SAMPLE FILES

The software files related to the Altera DE2-115 Development and Education Board are available using OAK under "Labs – DE2-115 Board Information. In addition, your Roth & John textbook has a CD that contains all the VHDL code from the textbook.

COLLABORATION POLICY

Each team is responsible for completing the laboratory. Collaboration among teams is encouraged on the projects in this class, but only under the following conditions. Teams may discuss the laboratory assignment, the general approach taken to solve the problems, and compare results **without** comparing the entire solution. However, copying of code, results, or analyses of results is **NOT** allowed.

LABORATORY DESCRIPTION

You will need to read the following material from your textbook:

- CHAPTER 1 – Review of Logic Design Fundamentals

In addition, please refer to the documentation posted in the "DE2-115 Board Information" folder under the "Lab" section on OAK.

For each problem below, you should turn in the schematic or VHDL corresponding to the design as well as the simulation code and/or results that verify the design. In addition, you should answer any problem-specific questions (e.g., find the delay time). You will also need to demonstrate your solutions to your instructor. Demonstrations should be as efficient as possible. Simulation results can be as simple as loading a wave log file (WLF) from ModelSim-Altera that you have saved which corresponds to that exercise. DE2-115 demonstrations can be as simple as opening the Quartus II programmer and configuring the FPGA. **You will also need to upload all**

project-related files (including VHDL code) electronically to OAK for full credit. Place each problem/project in a separate folder. Make a ZIP file of all the folders and upload it into the "file exchange" of your Team Page.

- **Problem 1:** Complete the "Getting Started with Altera's DE2-115 Board" tutorial (tut_initialDE2-115.pdf), which is available in the "Laboratory Assignment #1" folder on OAK. This exercise will install the USB-Blaster driver that is necessary to program your DE2-115 board (if it is not installed already). The tutorial was not written for your version of the Quartus II software, but should still provide some guidance. The driver should be located in *C:\altera\13.0sp1\quartus\drivers\usb-blaster*. You may have to select the *\x32* or *\x64* folder depending upon your processor architecture type.

- **Problem 2:** Complete Sections 9.1 (JTAG programming) and 10 of the "Quartus II Introduction Using Schematic Design" tutorial (Quartus_II_Introduction.pdf), which are available in the "Laboratory Assignment #1" folder on OAK. **Do not** complete Section 9.2 (Active Serial Mode Programming). This exercise is your first opportunity to program the DE2-115 Board since you already completed the tutorial for Homework #1.

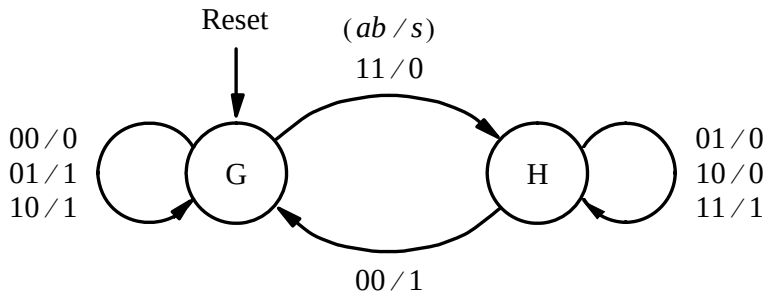
- **Problem 3:** Update your full adder design from the in-class tutorial to test on the DE2-115 Board. You will need to use switches for the various input signals and LEDs for the output signals (you are free to choose the switches/LEDs you prefer). Either change the names of your input and output pins to correspond to the names of the DE2-115 pin assignments, or clear the pin assignments and assign pins similar to the procedure in the tutorial from Problem 2. Download your design to the DE2-115 Board for testing.

- **Problem 4:** Simulate your full adder using ModelSim-Altera. Perform both a functional simulation and a timing simulation. Create a DO file for each test that will set up the simulation with the *vsim* command, add the signals to the waveform window, set up the input waveforms and run the entire simulation. Use the ModelSim-Altera tutorial as a reference.

- **Problem 5:** Draw a schematic that uses the LPM_ADD_SUB megafunction to add two 16-bit signed numbers. Use the MegaWizard Plug-In Manager tool to start the megawizard. Do not use any optional inputs or outputs, however, you should pipeline the function with a latency of 1 clock cycle. Verify the proper operation with two 16-bit numbers using ModelSim-Altera. You do not need to try every input combination, however, you should try several different cases (e.g., two positive numbers, two negative numbers, a positive and a negative number). You do not need to download this design to the DE2-115 Board. Show the WLF from your ModelSim-Altera verification. Then read the tutorial on "Using the TimeQuest Timing Analyzer" to learn how to set up a timing constraint for your design. Find and report the minimum pulse width for each of the three delay models for the FPGA.

- **Problem 6:** The state machine in Figure 1 is for a serial adder. All inputs and outputs should be synchronous. Use logic gates and D flip-flops to implement this state machine as a schematic. Verify correct operation with a simulation using ModelSim-Altera. Create

a DO file that will set up the simulation with the *vsim* command, add the signals to the waveform window, set up the input waveforms and run the entire simulation. The simulation should exercise all arcs in the state diagram. The two inputs are **a** and **b**, while **s** is the output. Use switches SW[0] and SW[1] for the two inputs and LEDG[8] for the output **s**. Use the switch SW[17] for the **Reset** signal. Use push button KEY[0] for the **Clock** signal. **G** and **H** are the two states. For state **G**, illuminate a green LED and for state **H**, illuminate a red LED. Use one-hot encoding on the state machine. For one-hot encoding, use two flip-flops with only one asserted high for each state. For state **G**, the flip-flop outputs would be "10" and for state **H**, the outputs would be "01". One-hot encoding is common for FPGAs. Use the TimeQuest Timing Analyzer to determine the maximum clock frequency (F_{max}) for each of the "Slow" models. Download your design to the DE2-115 Board for testing.



G: carry-in = 0
H: carry-in = 1

Figure 1: State diagram for a serial adder FSM

TEAM RESPONSIBILITY

This is a team assignment. Divide the assignment up such that each team member contributes equally to the problems described above. It is the team's responsibility to design and run adequate test cases. You may utilize the file exchange in OAK under "Groups." There should be only one (1) submission of the results/solutions for each team.

TEAM MEMBER EVALUATION

You will evaluate your teammate(s) on the quality and quantity of their contributions and cooperation. This team evaluation will comprise 10% of an individual's grade for the programming assignment. Each team member **MUST** complete the teammate evaluation form and submit it electronically before class. Use the link provided in **Session 11 - Friday, September 12, 2014** (under the "Lectures" menu item). **DO NOT USE THE FILE EXCHANGE FOR YOUR EVALUATION FORM!!!** Failure to submit your evaluation will result in a **10% penalty** for your individual grade.