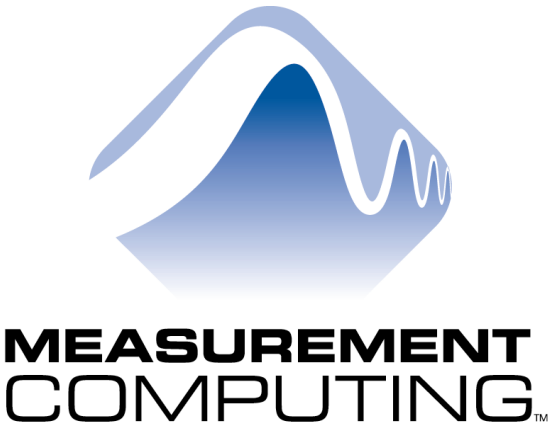
Register Map for the PCIe-DIO24



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Register Description

This document describes the register map for the PCIe-DIO24 board. Only experienced programmers should attempt register-level programming.

Overview

The system dynamically assigns base addresses of PCI boards. You can determine these addresses by examining the Bus Interface chip used by the board. The PCIe-DIO24 board uses the PLX PCI 9030 PCI Bus Interface chip.

- For more information on the PLX PCI 9030, refer to the *PCI 9030 Data Book* (May, 2002). This document is available from PLX Technology® at www.plxtech.com/products/9030/default.htm.

As an alternative to register level programming, the PCIe-DIO24 board is fully supported by the optional Universal Library™ software, as well as most high-level data acquisition and control application packages, such as SoftWIRE®, HP Vee™ or Labtech Notebook™.

Table 1 lists the I/O register map for the PCIe-DIO24 board.

Table 1. Board Registers

REGISTER	READ FUNCTION	WRITE FUNCTION
BADR1 + 4Ch	Interrupt Status	Interrupt Control
BADR2 + 0	Port A Data	Port A Output Data
BADR2 + 1	Port B Data	Port B Output Data
BADR2 + 2	Port C Data	Port C Output Data
BADR2 + 3	No readback	Configuration Register
EEPROM DIP Switch		
BADR3 + 0	I^2C Status	I^2C Timeout
BADR3 + 8	I^2C Data	I^2C Data
BADR3 + C	I^2C Control	I^2C Control

Interrupt status and control

Interrupt Status & Control

BADR1 + 4Ch

READ/WRITE

31:24	23:16
X	X

15	14	13	12	11	10	9	8
X	X	X	X	0	INTCLR	0	INTSEL

7	6	5	4	3	2	1	0
0	PCIINT	0	0	0	INT	INTPOL	INTE

This register is 32-bits long. Don't change the value of the bits set to 0 (bit 3, 4, 5, 7, 9 and 11). X indicates "don't care", meaning that it does not matter what data is written to these bits. The remaining register bits have specific control functions. If you write to the Interrupt Status & Control register, be sure to read the current status. Only change the bits you want, and then write the new status word.

INTE	Interrupt Enable:
	0 = disabled
	1 = enabled (default)
INTPOL	Interrupt Polarity:
	0 = active low (default)
	1 = active high
INT	Interrupt Status:
	0 = interrupt is not active
	1 = interrupt is active
PCIINT	PCI Interrupt Enable:
	0 = disabled
	1 = enabled (default)
INTSEL	Interrupt Edge/Level Select:
	0 = level-sensitive (default)
	1 = edge-sensitive
	Note that this bit only has an effect when in high-polarity mode (INTPOL=1). The interrupt is always level-sensitive when the INTPOL bit is set to low-polarity (INTPOL=0).
INTCLR	Clears the INT selected interrupt status:
	0 = no effect
	1 = clear the INT interrupt

Digital data I/O registers

Port A data

BADR2 + 0

READ/WRITE

7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0

Port B data

BADR2 + 1

READ/WRITE

7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0

You can program channels A and B to be input or output. Each channel is written to and read from in bytes, although for control and monitoring purposes, individual bits are used.

Port C data

BADR2 + 2

READ/WRITE

7	6	5	4	3	2	1	0
C7	C6	C5	C4	C3	C2	C1	C0
CH3	CH2	CH1	CH0	CL3	CL2	CL1	CL0

You can use port C as one eight-bit port for either input or output, or you can split it into two, four-bit ports which can be independently input or output. The notation for the upper four-bit port is CH3-CH0. The notation for the lower four-bit port is CL3-CL0.

Although you can split port C, every read and write to this port carries eight bits of data. To remove unwanted information, perform an AND on data reads, and perform an OR operation on data writes with the current status of the other nibble.

Input ports

In 82C55 mode 0 configuration, ports configured for input read the state of the input lines at the moment the read is executed; transitions are not latched.

Output ports

In 82C55 mode 0 configuration, ports configured for output hold the output data written to them. This output byte can be read back by reading the port.

Configuration register

Digital I/O configuration

BADR2 + 3

WRITE Only

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

You can program the 82C55 chip to operate in input/output mode (mode 0), Strobed Input/Output mode (mode 1), or bi-directional bus mode (mode 2). For more information on 82C55 modes 1 and 2, refer to the 82C55 data sheet on our web site at www.mccdaq.com/PDFmanuals/82C55A.pdf.

Mode 0 configuration codes for the PCI-DIO24, PCI-DIO24/S and PCI-DIO24/LP are listed in Table 2. Mode 0 configuration codes for the PCI-DIO24H are listed in Table 3.

Note: Since the 82C55 chip is emulated, the PCI-DIO24H only supports mode 0.

When the PC is powered-up or RESET, all 24 lines are reset to Input mode. No further programming is needed to use the 24 lines as TTL inputs. Each port A, B, CH and CL can be independently configured to be inputs or outputs.

Table 2. I/O Configuration Codes for PCI-DIO24, PCI-DIO24/S and PCI-DIO24/LP – Mode 0

A	CH	B	CL	D4	D3	D1	D0	HEX	DEC
OUT	OUT	OUT	OUT	0	0	0	0	80	128
OUT	OUT	OUT	IN	0	0	0	1	81	129
OUT	OUT	IN	OUT	0	0	1	0	82	130
OUT	OUT	IN	IN	0	0	1	1	83	131
OUT	IN	OUT	OUT	0	1	0	0	88	136
OUT	IN	OUT	IN	0	1	0	1	89	137
OUT	IN	IN	OUT	0	1	1	0	8A	138
OUT	IN	IN	IN	0	1	1	1	8B	139
IN	OUT	OUT	OUT	1	0	0	0	90	144
IN	OUT	OUT	IN	1	0	0	1	91	145
IN	OUT	IN	OUT	1	0	1	0	92	146
IN	OUT	IN	IN	1	0	1	1	93	147
IN	IN	OUT	OUT	1	1	0	0	98	152
IN	IN	OUT	IN	1	1	0	1	99	153
IN	IN	IN	OUT	1	1	1	0	9A	154
IN	IN	IN	IN	1	1	1	1	9B	155

Note: For mode 0, D7 is always 1; D6, D5 and D2 are always 0.

EEPROM DIP Switch – PCI Registers

Each Read/Write should wait >100 microseconds before each access to allow ample time for I^2C bus transactions.

I^2C Status

BADR3 + 0h

Read

7	6	5	4	3	2	1	0
STA7	STA6	STA5	STA4	STA3	STA2	STA1	STA0

Status of the I^2C Bus. Check after each Write to the Control Register; refer to the NXP PCA9564 datasheet for details on return codes.

I^2C Data

BADR3 + 08h

Read/Write

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Read/Write EEPROM DIP Switch address, Data and Value. Write to the Control Register to update the I^2C bus or for read values.

I^2C Control

BADR3 + 0Ch

Read/Write

7	6	5	4	3	2	1	0
AA	ENSIO	STA	STO	SI	CR2	CR1	CR0

Write I^2C Bus Control. Commands include Start, Repeated Start, End, etc. Refer to the NXP PCA9564 datasheet for details.

EEPROM DIP Switch – Addresses and Local Registers

The following registers are accessed via the parallel to I^2C device as local registers. Communicate via the PCI Registers mentioned above.

EEPROM DIP Switch Address

	Write Address	Read Address
Ports 1 and 2	98	99
Ports 3 and 4	9A	9B

EEPROM DIP Switch Data

1 = High; 0 = Low

7	6	5	4	3	2	1	0
x	x	Port2(4) C	Port2(4) B	Port2(4) A	Port1(3) C	Port1(3) B	Port1(3) A

EEPROM DIP Switch – Example Configuration Read and Write

Important! You must set up the EEPROM before performing read/write operations.

I/O map: **ib = inByte**; **ob = outByte**

SETUP EEPROM for read and write

I^2C Status	Status:	ib BADR3
	Return:	F8h (otherwise transmit STOP first)
I^2C Start Command (63h)	Control:	ob BADR3+C 63
I^2C Status	Status:	ib BADR3
	Return:	08h

I^2C Write Address - I^2C Data Register (for <write address> refer to "EEPROM DIP Switch Address" on page 5.)

	Data:	ob BADR3+8 <write address>
I^2C Transmit (43h)	Control:	ob BADR3+C 43
I^2C Status	Status:	ib BADR3
	Return:	18h

I^2C EEMPROM Address - I^2C Data Register (00h for defaults and power-up)

	Data:	ob BADR3+8 00
I^2C Transmit (43h)	Control:	ob BADR3+C 43
I^2C Status	Status:	ib BADR3
	Return:	28h

WRITE - EEPROM DIP output (perform after Setup)

I^2C EEPROM Config - I^2C Data Register (for <data> refer to "EEPROM DIP Switch Data" on page 5.)

	Data:	ob BADR3+8 <data>
I^2C Transmit (43h)	Control:	ob BADR3+C 43
I^2C Status	Status:	ib BADR3
	Return:	28h

I^2C Stop command (53h) [port pull will change after this command]

	Control:	ob BADR3+C 53
I^2C Status	Status:	ib BADR3
	Return:	F8h

READ - EEPROM DIP output (perform after Setup)

I^2C Start Command (63h) Control: ob BADR3+C 63

I^2C Status Status: ib BADR3

Return: 10h

I^2C Read Address - I^2C Data Register (for <read address> refer to "EEPROM DIP Switch Address" on page 5.)

Data: ob BADR3+8 <read address>

I^2C Transmit (43h) Control: ob BADR3+C 43

I^2C Status Status: ib BADR3

Return: 40h

I^2C Transmit (43h) Control: ob BADR3+C 43

I^2C Status Status: ib BADR3

Return: 58h

I^2C Data - I^2C Data Register (status of pull-up/down. For <data> see EEPROM DIP Switch Data" on page 5.)

Data: ib BADR3+8

Return: <data>

I^2C Status Status: ib BADR3

Return: F8h

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