PCI 9080-3

Design Notes Rev. 1.3
July 2001

A. Product Status

Product	Revision	Samples	Production
PCI 9080	Version 03	October 1997	January 1998

B. Documentation Status

Document	Revision	Description	Date
Data Book	Version 1.06	PCI 9080 Data Book	January 2000

C. Design Note Summary

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D. Design Notes

1. Recover from a Master Abort during a Non-Chain DMA operation:

Design Issue: When a Master or Target Abort condition occurs during a non-Chain DMA operation, the PCI 9080 DMA controller can be recovered by performing these steps in sequence:

Recommendation:

a. Clear the Enable bit in the DMA Channel Command/Status register (DMACSRx[0]).
b. Set the Abort bit to 1 in the DMA Channel Command/Status register (DMACSRx[2]).
c. Clear the Master or Target Abort bit in the PCI Status register (PCISR[13, 11]).
d. Configure the DMA registers to start a new DMA operation.

2. Recover from a Master Abort during a Chain DMA operation:

Design Issue: When a Master or Target Abort condition occurs during a Chain DMA operation, the PCI 9080 DMA controller can be recovered by performing these steps in sequence:

Recommendation:

a. Set the Software Reset bit (CNTRL[30]) to 1 – the Local Configuration Registers get reset and flush the data in the DMA FIFOs.
b. Clear the Software Reset bit by writing 0 to this bit.
c. Reload the Local Configuration Registers from the Serial EEPROM by writing a 1 to the Reload Configuration Registers bit (CNTRL[29]), or reload the registers via the Local bus master.
d. Configure the DMA registers to start a new Chain DMA operation.

3. DMA Done PCI Interrupt

Design Issue: The PCI 9080 can be programmed to generate either a Local or PCI interrupt when a DMA operation is done. To select PCI Interrupt:

Recommendation:

a. Set the Done Interrupt Enable bit (DMAMODEx[10]) for Channel 0 or 1.
b. Set the DMA Channel x Interrupt Select bit (DMAMODEx[17]) to 1.
c. Set the PCI Interrupt Enable bit (INTCSR[8]) to 1.
d. Set the Local DMA Channel x Interrupt Enable bit (INTCSR[18] or INTCSR[19] for DMA Channel 0 or Channel 1, respectively.

Note:

When the DMA operation is finished, the DMA Channel x Done bit (DMACSRx[4]) is set, and PCI 9080 generates a PCI interrupt. The status bit in INTCSR, bit 21 or bit 22, is also set to indicate that the DMA Channel 0 or Channel 1 interrupt is active.

If the Local DMA Channel 0 (or Channel 1) Interrupt Enable bit (INTCSR, bit 18 or bit 19) is mistakenly not enabled, the PCI 9080 still generates a PCI interrupt. However, the status bit in INTCSR, bit 21 or bit 22, will not get set. An ISR

(Interrupt Service Routine) might not be able to clear the interrupt since the source of the PCI interrupt cannot be identified.

4. Local Master Write to internal Configuration Registers with WAIT# being used to insert Wait States

Design Issue: During a configuration write, WAIT# must be asserted (by the local master) a minimum of two (2) clocks before READY# is asserted by the PCI 9080, for the PCI 9080 to sense the WAIT# input. The earliest READY# will be asserted is six (6) clocks after the assertion of ADS#. Therefore, in order to ensure that WAIT# is recognized by the PCI 9080, WAIT# should be asserted no later than four (4) clocks after the assertion of ADS#. Any assertion of WAIT# more than four (4) clocks after the assertion of ADS# may be ignored by the PCI 9080.

If the PCI 9080 does not sense WAIT# it will simply assert READY# for one clock (and think the cycle has ended) instead of waiting until WAIT# has been negated. This problem applies only when a local master is writing to the PCI 9080 internal configuration registers.

Recommendation: During a Local Master write to the PCI 9080 internal configuration registers, assert WAIT# no later than four (4) clocks after the assertion of ADS#, which will ensure that the PCI 9080 recognizes WAIT# at least two (2) clocks before it asserts READY#.

5. Delayed Read Retry/Disconnect

Design Issue: During Delayed Direct Slave Reads, if the Delayed Read mode bit (MARBR[24]) is set, the PCI 9080 will treat all PCI Delayed Read as Retries, which may allow a second chance for the initial Master to complete the requested Read cycle. Any subsequent Direct Slave cycles to a different address other than the address for which the disconnect occurred will be retried until the PCI address matches or a 32K clock timeout occurs.

Recommendations:

a. Software should recover from disconnect by retrying the initially requested Read cycle.
b. Software should wait for 32K clock timeout to occur before posting any other Reads to the PCI 9080.

6. Software Reset

All PCI 9080 Local Configuration Registers (not DMA) reset to default values when the Software Reset bit (CNTRL[30]) is set. The PCI Base Address 2 for Local Space 0 (PCIBAR2) and PCI Base Address 3 for Local Space 1 (PCIBAR3) also reset to 0 since the default value of the Decode Enable bit is disabled.

7. DMA may fail to start if the DMA Enable and Start bits are set simultaneously

Design Issue: DMA may fail to start if the DMA Enable and Start bits (DMACSRx[0, 1]) are set simultaneously, due to a race condition with these bits. If the DMA fails to start, the DMA Done bit (DMACSRx[4]) will not be set, nor will an interrupt occur to signal DMA completion for that channel.

Recommendation: Set the DMA Enable and Start bits sequentially by first writing the value 1h and then 3h to the DMA Channel x Command/Status register (DMACSRx).

8. DMPAF# (Direct Master Programmable Almost Full) output pin negation timing

Specification Clarification: DMPAF# pin output assertion relies on the programmable value in DMPBAM[10, 8:5] to determine when to signal that the Direct Master Write FIFO is almost full. After DMPAF# assertion, the PCI 9080 negates the DMPAF# pin upon the last word of the transfer entering into the Data Out Holding Register. The DMPAF# signal indicates the Direct Master Write FIFO status, not the completion of the transfer status.

9. Messaging Unit data corruption if Queue Prefetch (Inbound Free List FIFO Prefetch and/or Outbound Post List FIFO Prefetch) is enabled

Design Issue: When the Messaging Unit is enabled (QSR[0] = 1), the Inbound Free List FIFO holds the message frame addresses (MFA) of available message Frames (available to an external PCI agent) in shared Local memory. The Outbound Post List FIFO holds the MFA of all currently posted messages (destined to an external PCI agent) that are in shared Local memory.

To reduce read latency, queue prefetching can be enabled in QSR[2] and QSR[3]. However, if queue prefetching is enabled, the Messaging Unit data can return incorrect data due to internal updating of the pointers.

Recommendation: Disable queue prefetching for the Messaging Unit by clearing the QSR[2] and QSR[3] register bits (default value).

10. PCI Target Abort during DMA Transfer

Design Issue: During a PCI-to-Local DMA transfer, if a Target Abort occurs on the last DMA data transfer cycle, the PCI 9080 will generate an unknown data cycle for the last data to the Local bus. A PCI Target Abort at any other time during the DMA transaction will be successfully completed. This is a rare case condition. If a Target Abort during a DMA transaction occurs, it will be required for the system to repeat the operation.

Recommendation: A Target Abort is by definition an error condition, and if a Target Abort occurs the last data should be assumed to be invalid. After a DMA transaction is complete, software should check the status bits in INTCSR[25:26]. If the bits indicate that a PCI Target abort occurred, software should repeat the DMA transaction.

11. Interrupt Control/Status register (INTCSR) indication of a Master Abort or Target Abort condition

Design Issue: When a Master Abort or Target Abort condition is detected, status bits INTCSR[27:24] could reflect an error condition depending on the abort received. Clearing the abort condition will not reset these status bits to their default values of 1.

Recommendation: The state machine for status bits INTCSR[27:24] is updated when either another abort condition occurs, or a PCI reset is applied to the PCI 9080 (a software reset via CNTRL[30] will not change INTCSR register contents). Otherwise, these bits reflect the status of the last abort condition received. If monitoring of these bits is necessary for error recovery, monitor the equivalent PCI configuration register error bits in the PCI Status register (PCISR[13:11]). PCI 9080 issuance of a Master Abort is signaled in PCISR[13], PCI 9080 issuance of a Target Abort is signaled in PCISR[11], and receipt of a Target Abort from another device while PCI 9080 is master is signaled in PCISR[12].

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