Register map for the PCI-QUAD04

MEASUREMENT COMPUTING™

Document Revision 1.0, June, 2005

Register Description

Overview

The following section outlines the register map of the PCI-QUAD04 as well as briefly describing the commands necessary to program the PCI-QUAD04 at the register level (refer to Table 1 below). The heart of the PCI-QUAD04 is the LSI/CSI LS7266R1, a powerful device which is highly integrated to allow few external components to be needed. As seen in the LS7266R1 block diagram, many functions are controlled through register programming.

Table 1. I/O Region Register Operations

I/O Region	Function	Operations
BADR0	PCI memory-mapped configuration registers	32-bit double word
BADR1	PCI I/O-mapped configuration registers	32-bit double word
BADR2	Configuration and control registers	8-bit byte

BADR0

BADR0 is reserved for the PLX PCI 9052 configuration registers. This address space is used for memory mapped I/O access of the configuration registers.

For more information on the PLX PCI 9052 PCI Bus Interface chip, refer to the *PCI 9052 Data Book* (September, 2001). This document is available from PLX Technology® at www.plxtech.com/products/io_accelerators/PCI9052/default.htm.

BADR1+4Ch

INTCSR Configure

32:15	14	13	12	11	10	9	8
X	X	X	X	X	INTCLR	X	LEVEL/EDGE

7	6	5	4	3	2	1	0
X	PCINT	X	X	X	INT	INTPOL	INTE

READ/WRITE

The INTCSR (Interrupt Control/Status Register) controls the interrupt features of the PLX-9052 controller. The INTCSR register is 32-bits in length (as with all PLX-9052 registers). Since the rest of the register has specific control functions, those bits must be masked off in order to access the specific interrupt control functions listed below.

INTE — Interrupt enable (local):

0 = disabled

1 = enabled (default)

INTPOL — Interrupt polarity:

0 = active low (default)

1 = active high

INT — Interrupt status:

0 = interrupt not active

1 = interrupt active

PCINT — PCI interrupt enable:

0 = disabled (default)

1 = enabled

LEVEL/EDGE Interrupt trigger control:

0 = level triggered mode (default)

1 = edge triggered mode

INTCLR Interrupt clear (edge triggered mode only):

0 = N/A

1 = clear interrupt

Note:
For applications requiring edge triggered interrupts (LEVEL/EDGE bit 8 = 1), the user must configure the INTPOL bit for active high polarity (bit 1=1).

Channel Control Registers (BADR2 +0 THROUGH BADR2 +7)

Table 2. PCI-QUAD04 register map

Register		Data Bits								Function
		D7	D6	D5	D4	D3	D2	D1	D0	
BADR2 + 0	RD	D7	D6	D5	D4	D3	D2	D1	D0	Read channel 1 OL byte segment addressed by BP
	WR	D7	D6	D5	D4	D3	D2	D1	D0	Write channel 1 PR byte segment addressed by BP
BADR2 + 1	RD	0	IDX	U/D	E	S	CPT	CT	BT	Read channel 1 FLAG register
	WR	0	0	0	* Refer to the LS7266R1 data sheet					Write to channel 1 RLD register
	WR	0	0	1	* Refer to the LS7266R1 data sheet					Write to channel 1 CMR register
	WR	0	1	0	* Refer to the LS7266R1 data sheet					Write to channel 1 IOR register
	WR	0	1	1	* Refer to the LS7266R1 data sheet					Write to channel 1 IDR register
	WR	1	0	0	* Refer to the LS7266R1 data sheet					Write to channel 1 and channel 2 RLD register
	WR	1	0	1	* Refer to the LS7266R1 data sheet					Write to channel 1 and channel 2 CMR register
	WR	1	1	0	* Refer to the LS7266R1 data sheet					Write to channel 1 and channel 2 IOR register
	WR	1	1	1	* Refer to the LS7266R1 data sheet					Write to channel 1 and channel 2 IDR register
BADR2 + 2	RD	D7	D6	D5	D4	D3	D2	D1	D0	Read channel 2 OL byte segment addressed by BP
	WR	D7	D6	D5	D4	D3	D2	D1	D0	Write channel 2 PR byte segment addressed by BP
BADR2 + 3	RD	0	IDX	U/D	E	S	CPT	CT	BT	Read channel 2 FLAG register
	WR	0	0	0	* Refer to the LS7266R1 data sheet					Write to channel 2 RLD register
	WR	0	0	1	* Refer to the LS7266R1 data sheet					Write to channel 2 CMR register
	WR	0	1	0	* Refer to the LS7266R1 data sheet					Write to channel 2 IOR register
	WR	0	1	1	* Refer to the LS7266R1 data sheet					Write to channel 2 IDR register
	WR	1	0	0	* Refer to the LS7266R1 data sheet					Write to channel 1 and channel 2 RLD register
	WR	1	0	1	* Refer to the LS7266R1 data sheet					Write to channel 1 and channel 2 CMR register
	WR	1	1	0	* Refer to the LS7266R1 data sheet					Write to channel 1 and channel 2 IOR register
	WR	1	1	1	* Refer to the LS7266R1 data sheet					Write to channel 1 and channel 2 IDR register
BADR2 + 4	RD	D7	D6	D5	D4	D3	D2	D1	D0	Read channel 3 OL byte segment addressed by BP
	WR	D7	D6	D5	D4	D3	D2	D1	D0	Write channel 3 PR byte segment addressed by BP

Register		Data Bits								Function
		D7	D6	D5	D4	D3	D2	D1	D0	
BADR2 + 5	RD	0	IDX	U/D	E	S	CPT	CT	BT	Read channel 3 FLAG register
	WR	0	0	0	* Refer to the LS7266R1 data sheet					Write to channel 3 RLD register
	WR	0	0	1	* Refer to the LS7266R1 data sheet					Write to channel 3 CMR register
	WR	0	1	0	* Refer to the LS7266R1 data sheet					Write to channel 3 IOR register
	WR	0	1	1	* Refer to the LS7266R1 data sheet					Write to channel 3 IDR register
	WR	1	0	0	* Refer to the LS7266R1 data sheet					Write to channel 3 and channel 4 RLD register
	WR	1	0	1	* Refer to the LS7266R1 data sheet					Write to channel 3 and channel 4 CMR register
	WR	1	1	0	* Refer to the LS7266R1 data sheet					Write to channel 3 and channel 4 IOR register
	WR	1	1	1	* Refer to the LS7266R1 data sheet					Write to channel 3 and channel 4 IDR register
BADR2 + 6	RD	D7	D6	D5	D4	D3	D2	D1	D0	Read channel 4 OL byte segment addressed by BP
	WR	D7	D6	D5	D4	D3	D2	D1	D0	Write channel 4 PR byte segment addressed by BP
BADR2 + 7	RD	0	IDX	U/D	E	S	CPT	CT	BT	Read channel 4 FLAG register
	WR	0	0	0	* Refer to the LS7266R1 data sheet					Write to channel 4 RLD register
	WR	0	0	1	* Refer to the LS7266R1 data sheet					Write to channel 4 CMR register
	WR	0	1	0	* Refer to the LS7266R1 data sheet					Write to channel 4 IOR register
	WR	0	1	1	* Refer to the LS7266R1 data sheet					Write to channel 4 IDR register
	WR	1	0	0	* Refer to the LS7266R1 data sheet					Write to channel 3 and channel 4 RLD register
	WR	1	0	1	* Refer to the LS7266R1 data sheet					Write to channel 3 and channel 4 CMR register
	WR	1	1	0	* Refer to the LS7266R1 data sheet					Write to channel 3 and channel 4 IOR register
	WR	1	1	1	* Refer to the LS7266R1 data sheet					Write to channel 3 and channel 4 IDR register
BADR2 + 8	RD	CBINT4	CBINT3	CBINT2	CBINT1	IND4SEL	IND3SEL	IND2SEL	IND1SEL	Interrupt routing control register
	WR	CBINT4	CBINT3	CBINT2	CBINT1	IND4SEL	IND3SEL	IND2SEL	IND1SEL	
BADR2 + 9	RD	N/A	PH4B1	PH4B0	PH4A	PH3B	PH3A	PH2B	PH2A	Interrupt signal control register (for cascading counters)
	WR	N/A	PH4B1	PH4B0	PH4A	PH3B	PH3A	PH2B	PH2A	
BADR2 + 10	RD	8259 Programmable Interrupt Controller Part A								8259 Programmable Interrupt Controller Part A
	WR									
BADR2 + 11	RD	8259 Programmable Interrupt Controller Part B								8259 Programmable Interrupt Controller Part B
	WR									

The LS7266R1 contains two control registers per axis, and the configuration of each axis requires a sequence of writes to set the operating mode of the chip. The following description outlines the configuration steps for a single axis. The first axis control registers are contained at the BADR2 +0 address and at BADR2+1. The other axis perform identically.

When read, the BADR2 +0 address returns the Output Latch (OL) data. Writes to the BADR2 +0 address set the Preset Register (PR). All register access to the LS7266R1 is done through byte wide operations. However, the PR and OL registers are 24-bits wide. The LS7266R1 contains a byte pointer that is auto-incremented after each write. Setting the preset register requires three byte-wide writes (outport b), starting with the least significant byte. Be sure to reset the byte pointer prior to any register writes. The BADR2+1 address accesses the status and control registers for the given axis. There are four unique registers which can be configured by writing to the BADR2+1 register. For further details, refer to the LS7266R1 data sheet at www.mccdaq.com/PDFmanuals/LS7266R1.pdf.

At the BADR2 +1 location, the four registers are uniquely selected for write access by the value in bits 5 and 6. The following table indicates the bit values for each register.

Register Name	Selected for Write Access by bits 5 & 6
Reset and Load (RLD)	x00x xxxx
Count Mode (CMR)	x01x xxxx
Input/Output Control (IOR)	x10x xxxx
Index Control (IDR)	x11x xxxx

If bit 7 is one (1), the selected operation will affect both the X and Y channels. If bit 7 is zero, the X*/Y input is used to select the target channel. The remaining bits in each register are used to configure the LS7266R1 for various operating modes.

The following sections describe how each register can be configured. In several instances there are bit fields that support multiple options. Obviously, only one option can be selected for each write operation. It may be necessary to perform several writes to the same register to achieve the desired results. For example, to initialize the RLD register, that is, to clear all of the status flags and reset the counter, requires three separate writes to the register. Refer to the tables below for details.

Counter Mode Register (CMR)

The CMR contains three user-configurable fields — count representation, count mode, and quadrature scaling. Each field consists of one or more bits in the CMR register. After you select the desired mode, the bit fields need to be assembled into a byte that can be written to the CMR register. Bits 5 and 6 are always 1 and 0, respectively, for CMR register accesses.

Data Encoding

The quadrature count can be represented in either BCD or binary. Bit 0 of the CMR register selects the desired option.

CMR Count Representation	Bit 0 Value for Count Configuration
BINARY	x01x xxx0
BCD	x01x xxx1

Count Mode

There are four different count modes that are selected by bits 1 and 2. The count modes are Normal, Range-Limit, Non-recycle, and Modulo-N.

CMR Count Mode	Bit 1 & 2 Value for Mode Selection
Normal	x01x x00x
Range Limit	x01x x10x
Non-recycle	x01x x01x
Modulo-N	x01x x11x

Count Mode definitions:

Range Limit: An upper limit, set by PR, and a lower limit, set to 0, are set. The CNTR stops at CNTR = PR when counting UP and when CNTR = 0 when counting DOWN. Counting is resumed only when the count direction is reversed.

Non-Recycle: CNTR is disabled whenever overflow or underflow happens. End-of-cycle marked by Carry (UP) or Borrow (DOWN). Re-enabled by reset or load on CNTR.

Modulo-N: Count boundary set between 0 and content of PR. When counting up, at CNTR = PR, the CNTR is reset to 0 and the up count is continued from that point. When counting down, at CNTR = 0, the CNTR is loaded with content of PR and down count is continued from that point.

Quadrature Scaling

There are four different scaling values that can be applied to quadrature signals — Non-quad, X1, X2, and X4. The scaling to be applied is set in bits 3 and 4 of the CMR register. Assuming the attached encoder generates 2500 pulses per revolution in X1 mode, you would receive 5000 pulses in X2 mode and 10,000 pulses in X4 mode. If the board will be used to detect simple clock pulses then select Non-Quadrature mode.

CMR Quadrature Scaling	Bit 3 & 4 value for quad scaling
Non-Quadrature	x010 0xxx
X1	x010 1xxx
X2	x011 0xxx
X4	x011 1xxx

Reset and Load Signal Decoders (RLD)

The RLD contains three user configurable fields. This register controls all of the reset options as well as the data transfer options. The following sections describe each field in the RLD register and the various modes that can be set for operation. The RLD register is used to reset the counter and the status flags and also to provide access to the error bit E, which is the only means for resetting this flag once it is set.

RLD Reset Byte Pointer Field

This field is used to reset the byte pointer. The byte pointer is auto-incremented each time the Output Latch (OL) register is read or the Preset Register (PR) is written to. The byte pointer must be reset prior to any access to the 24-bit counter register.

RLD Byte Pointer Reset	Bit 0 value for Byte Pointer Reset
NOP	x00x xxx0
BP Reset	x00x xxx1

RLD Reset Fields

In addition to the byte pointer, there are several other fields that can be reset. This field provides the mechanism for resetting the counter and all of the status flags. The Borrow Toggle (BT), Carry Toggle (CT), Compare Toggle (CPT), and the Sign Flag (S) can all be reset through bits 1 and 2 of the RLD register. Finally, the only way to clear the Error (E) flag once it has been set is through the RLD register.

RLD Reset	Bit 1 & 2 value for Reset Fields
NOP	x00x x00x
CNTR	x00x x01x
BT, CT, CPT, and S	x00x x10x
E	x00x x11x

RLD Transfer Fields

The final bit field in the RLD register consists of bits 3 and 4. This field controls the data transfer operation of the LS7266 chip. There are three options that are available as listed in the table below. The contents of the Preset Register can be transferred to the Counter, the contents of the Counter can be copied to the Output Latch for reading, and the Preset Register contents can be copied to the Filter Clock Prescalar. This register provides the software mechanism for reading the current count from the encoder. First write to the RLD register to transfer the contents of the counter to the output latch, then reset the byte pointer and perform three reads of the output latch.

RLD Transfer	Bit 3 & 4 value for Transfer Fields
NOP	x000 0xxx
Preset to Counter	x000 1xxx
Counter to Output Latch	x001 0xxx
Preset to Filter Clock Prescalar	x001 1xxx

Input/Output Control Register (IOR)

The IOR register contains four user configurable fields and should be initialized prior to writing the IDR register which follows. The IOR register, in conjunction with the IDR register, configures how the A and B input signals are interpreted.

A/B configuration bit

This configuration bit controls whether or not the A and B inputs are enabled or disabled. This bit must be enabled for the counter to respond to input clock pulses.

IOR A/B enable/disable	Bit 0 value for Enable/Disable
Disable A and B	x10x xxx0
Enable A and B	x10x xxx1

LCNTR/LOL pin configuration

This register bit field is only applicable if the IDR register bit 2 is set to 0. In this case, the Index input from the external encoder is directed to the LCNTR/LOL pin. This bit then configures the operation of the LCNTR/LOL pin. The operation can be set to either load the counter with the preset value or load the output latch input. Thus, if the IDR register specifies the Load CNTR operation, each time the Index input is asserted the counter will be reloaded with the value stored in the preset. If the Load OL input option is selected, then each Index input will cause the current counter value to be updated to the Output Latch. In this mode you are not required to use the RLD register to force the contents of the counter to be copied to the output latch. The contents of the counter will automatically be available at the Output Latch every time the Index signal is asserted.

Note

The Index input is asserted once per revolution.

IOR LCNTR/LOL pin configuration	Bit 1 value for CNTR/LOL Select
Load CNTR	x10x xx0x
Load OL input	x10x xx1x

RCNTR/ABG pin configuration

This bit configures the operation of the RCNTR/ABG pin. This register bit field is only applicable if the IDR register bit 2 is set to 1. In this mode, the Index input from the encoder is directed to the RCNTR/ABG input. The operation can be configured to either reset the CNTR input or as an A/B enable gate.

Note

In non-quadrature mode, this register should be set for A/B enable gate operation.

IOR RCNTR/ABG pin configuration	Bit 2 value for RCNTR/ABG Select
Reset CNTR	x10x x0xx
A/B enable gate	x10x x1xx

FLAG 1 & 2 configuration

This bit field controls the operation of the FLG1 and FLG2 real-time counter outputs. The selected configuration will determine what signal is output on the FLG1 and FLG2 output pins. For cascading the counters this register should be set for Carry/Borrow, Up/Down operation. The FLGx output pins are also redirected to the onboard 8259 Programmable Interrupt Controller (PIC). Depending on how the FLGx register is configured an interrupt can be generated based on the options in the following table.

IOR FLG1/FLG2 configuration	Bit 3 & 4 value for FLG1/FLG2 Select
FLG1 Carry, FLG2 Borrow	x100 0xxx
FLG1 Compare, FLG2 Borrow	x100 1xxx
FLG1 Carry/Borrow, FLG2 U/D	x101 0xxx
FLG1 IDX, FLG2 is E	x101 1xxx

Index Control Register (IDR)

The IDR register controls how the Index input from the encoder should be treated; it contains three user-configurable fields. The polarity and Index routing selections are also made through this register.

Note

Disable indexing for non-quadrature inputs.

Enable/Disable Index

This bit is used to select whether or not indexing is enabled for the LS7266.

IDR Index enable/disable	Bit 0 value for Enable/Disable Select
Disable Index	x11x xxx0
Enable Index	x11x xxx1

Index Polarity Select

If you are connecting a quadrature encoder, then this bit selects the polarity for the index: 0 for negative polarity and 1 for positive polarity.

IDR Index Polarity	Bit 1 value for Index Polarity Select
Negative Index Polarity	x11x xx0x
Positive Index Polarity	x11x xx1x

Index Pin Select

The final bit field in the IDR register determines where the index input will be connected. A 0 in this field will select the LCNTR/LOL pin as the connection for the encoder index output. If the field is set to 1, the RCNTR/ABG pin is selected as the index input. Prior to configuring this field, the IOR register bit 1 or 2 must be configured. Refer to the Input/Output Control Register (IOR) on page 5 for more details on these bit fields.

IDR Index Pin Select	Bit 2 value for Index Pin Select
LCNTR/LOL pin is indexed	x11x x0xx
RCNTR/ABG pin is indexed	x11x x1xx

Global Control Registers

Four global control registers are located at offsets 8-11 from the BADR2 address. The following sections outline these four registers and the various control functionality which they provide. Unlike the channel configuration registers, the current state of the global control registers can be obtained through reading the desired register. To help understand the registers and their functions, refer to Figure 1 as you read the register descriptions.

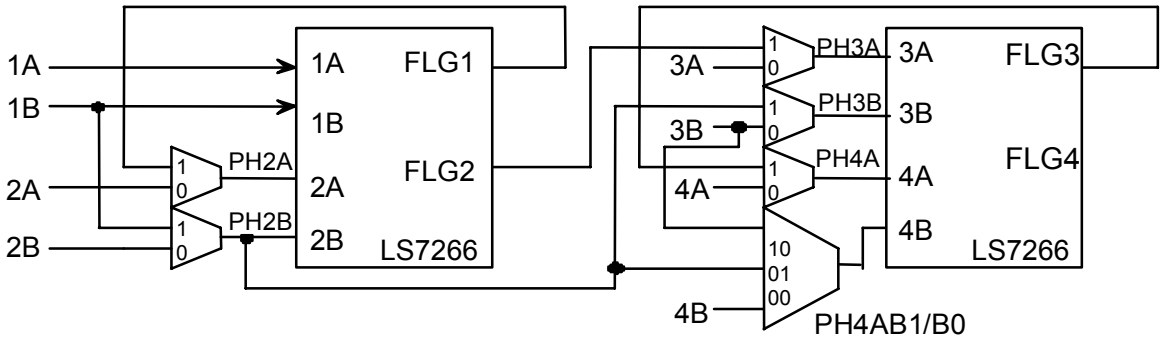

Figure 1. Cascade counting functional diagram

Index and Interrupt Routing Control (BADR2 + 8)

The first four bits of this register route the index pin from the quadrature encoder to either the LCNTR/LOL input or the RCNTR/ABG input for each of the four encoder inputs. The value set in this register should be consistent with the value written in the IDR register. The most significant four bits select the interrupt source as either Compare select or Carry/Borrow select.

Interrupt routing (Register BADR2 + 8 D4-D7)

	Channel 1	Channel 2	Channel 3	Channel 4
Input	**CBINT1**	**Input CBINT2**	**Input CBINT3**	**Input CBINT4**
FLG1 – Carry/Compare/Index	0	0	0	0
FLG2 – Borrow/Up/Down	1	1	1	1

Index routing (Register BADR2 + 8 D0-D3)

Connects the index input to the counter control input pin listed below.

	Channel 1	Channel 2	Channel 3	Channel 4
Input	**IND1SEL**	**IND2SEL**	**IND3SEL**	**IND4SEL**
RCNTR/ABG	0	0	0	0
LCNTR/LOL	1	1	1	1

*The FLG1 and FLG2 output pins are register programmable for Carry, Borrow, Compare and flag status functions. Refer to the 7266 IOR register for proper functionality.

Input Signal Control (BADR2 + 9)

Controls Counter Cascading: (Non-quadrature mode)

Set the FLGx pin for the CARRY/BORROW function through the IOR Register bits 3 and 4 so that the cascaded direction output will be CARRY for UP counting and BORROW for DOWN counting.

Register BADR2 + 9 D0-D6

	PH2A	PH2B	PH3A	PH3B	PH4A	PH4B1/PH4B0
(4) 24-bit counters (1/2/3/4)	0	0	0	0	0	0,0
(2) 48-bit counters (1-2/3-4)	1	1	0	0	1	1.0
(1) 24-bit/1 - 72bit (1/2-3-4)	0	0	1	1	1	0,1
(1) 96-bit counter (1-2-3-4)	1	1	1	1	1	0,1

Defaults to 0x00 (no inter-counter connections).

Programmable Interrupt Control Port A and B (BADR2 + 10 and 11)

The PCI-QUAD04 uses an 8259A Programmable Interrupt Controller. This controller routes up to eight interrupts from the Index inputs or Carry/Borrow outputs (due to overflow, underflow, or compare match, depending on strap setting and register programming) from the LS7266. The interrupt output from the 8259 is routed through the FPGA and register enabled and set to IRQ 2, 3, 5, 7, 10, 11, 12, or 15 on the PC bus. Each interrupt can be masked to prevent unwanted interrupt generation through 8259 programming.

The 8259A can only be used in non-vectored x86/x88 mode, or polled mode. That is, when an interrupt is generated, you must poll the 8259A to determine which interrupt was set. This mode is set external to the 8259A on the board by wiring:

- INTA* (pin 26) connected to +5VDC
- SP\EN (pin 16) connected to 10kohm pull-up to +5VDC
- CAS0:2 (pins 12,13,15) connected to 10kohm pull-up to +5VDC

For programming and further information on the 8259A interrupt controller, refer to the *Intel Peripheral Components* 1992 data book or the *Harris 8259A* data sheet (available at www.ele.uva.es/~jesman/BigSeti/ftp/Perifericos/INTERRUPCIONES/8259.pdf).

Measurement Computing Corporation
16 Commerce Boulevard,
Middleboro, Massachusetts 02346
(508) 946-5100
Fax: (508) 946-9500
E-mail: info@mccdaq.com
www.mccdaq.com