Register Map for the PCI-DAS1000 Series

PCI-DAS1000
PCI-DAS1001
PCI-DAS1002

Document Revision 1, July, 2002

PCI-DAS1000 Series Register Description

Register Overview

The PCI-DAS1000, PCI-DAS1001, and PCI-DAS1002 operation registers are mapped into I/O address space. Unlike ISA bus designs, these boards have *several* base addresses, each corresponding to a reserved block of addresses in I/O space. As mentioned in Chapter 3, "Programming & Applications," of the *PCI-DAS1000, PCI-DAS1001, &PCI-DAS1002 Multifunction Analog & Digital I/O User's Manual*, we recommend using the Universal Library™ package. Only experienced programmers should do direct, register-level programming.

Of the six base address regions (BADR) available in the PCI 2.1 specification, four are implemented in this design and are summarized in Table 1.

Table 1. Base Address Regions Implemented in the PCI-DAS1000 Series

I/O Region	Function	Operations
BADR0	PCI Controller Operation Registers	32-bit double word
BADR1	General Control/Status Registers	16-bit word
BADR2	ADC Data, FIFO Clear Registers	16-bit word
BADR3	Pacer, Counter/Timer and DIO Registers	eight-bit byte
BADR4	DAC Data Registers (1001 & 1002 Only)	16-bit word

BADR*n* is likely different on different machines. Assigned by the PCI BIOS, these base address values may not be the same even on subsequent power-on cycles of the same machine. All software must examine BADR0 at run-time with a READ_CONFIGURATION_WORD instruction to determine the BADR*n* values.

BADR0

BADR0 is reserved for the AMCC S5933 PCI Controller operations. There is no reason to access this region of I/O space for most PCI-DAS1000, PCI-DAS1001, and PCI-DAS1002 users. The installation procedures and Universal Library access all required information in this area. Unless you are writing direct register level software for a PCI-DAS1000 series board, don't be concerned with the BADR0 address.

For more information, refer to Applied Micro Circuits Corporation's (AMCC®) *PCI Products Data Book* (April, 1998) available at http://www.amcc.com/pdfs/pciprod.pdf.

BADR1

The I/O region defined by BADR1 contains five control and status registers for ADC, interrupt and Autocal operations. This region supports 16-bit word operations.

Interrupt / ADC FIFO Register

BADR1+ 0:

This register sets the Interrupt Control and ADC status. This is a read/write register.

WRITE

15	14	13	12	11	10	9	8
-	-	ADFLCL	-	-	-	-	-

7	6	5	4	3	2	1	0
INTCL	EOACL	-	EOAIE	-	INTE	INT1	INT0

Write operations to this register allow the user to select interrupt sources, enable interrupts, and clear interrupts, as well as set ADC FIFO flags. Table 2 describes Interrupt/ADC FIFO Register:

INT[1:0] General Interrupt Source selection bits (Table 2).

Table 2 Interrupt Source Selection Bits

INT1	INT0	Source
0	0	Not Defined
0	1	End of Channel Scan
1	0	AD FIFO Half Full
1	1	AD FIFO Not Empty

INTE Enables interrupt source selected via the INT[1:0] bits.
1 = Selected interrupt Enabled
0 = Selected interrupt Disabled

EOAIE Enables End-of-Acquisition interrupt (from residual counter). Used during FIFO-ADC operations to indicate that the desired sample size has been gathered.
1= Enable EOA interrupt
0 = Disable EOA interrupt

EOACL A write-clear to reset EOA interrupt status.
1 = Clear EOA interrupt
0 = No effect

INTCL A write-clear to reset **INT[1:0]** selected interrupt status.
1 = Clear **INT[1:0]** interrupt
0 = No effect

ADFLCL A write-clear to reset latched ADC FIFO Full status.
1 = Clear ADC FIFO Full latch
0 = No effect

Note: It is not necessary to reset any write-clear bits after they are set.

READ

15	14	13	12	11	10	9	8
-	-	LADFUL	ADNE	ADNEI	ADHFI	EOBI	-

7	6	5	4	3	2	1	0
INT	EOAI	-	-	-	-	-	-

Read operations to this register allow the user to check status of the selected interrupts and ADC FIFO flags. The following is a description of Interrupt / ADC FIFO Register Read bits:

EOAI Status bit of ADC FIFO End-of-Acquisition interrupt (from residual counter).
1 = Indicates an EOA interrupt has been latched
0 = Indicates an EOA interrupt has not occurred

INT Status bit of General interrupt selected via **INT[1:0]** bits. This bit indicates that *any* one of these interrupts has occurred.
1 = Indicates a General interrupt has been latched
0 = Indicates a General interrupt has not occurred

EOBI Status bit ADC End-of-Burst interrupt (End of Channel Scan). Only valid for ADC Burst Mode enabled.
1 = Indicates an EOB interrupt has been latched
0 = Indicates an EOB interrupt has not occurred

ADHFI Status bit of ADC FIFO Half-Full interrupt. Used during REP INSW operations.
1 = Indicates an ADC Half-Full interrupt has been latched. FIFO has been filled with more than 511 samples.
0 = Indicates an ADC Half-Full interrupt has not occurred. FIFO has not yet exceeded 1/2 of its total capacity.

ADNEI Status bit of ADC FIFO Not-Empty interrupt. Used to indicate ADC conversion complete in single conversion applications.
1 = Indicates an ADC FIFO Not-Empty interrupt has been latched and that one data word may be read from the FIFO.
0 = Indicates an ADC FIFO Not-Empty interrupt has not occurred. FIFO has been cleared, read until empty or ADC conversion still in progress.

ADNE Real-time status bit of ADC FIFO Not-Empty status signal.
1 = Indicates ADC FIFO has at least one word to be read.
0 = Indicates ADC FIFO is empty.

LADFUL Status bit of ADC FIFO FULL status. This bit is latched.
1 = Indicates the ADC FIFO has *exceeded* full state. Data may have been lost.
0 = Indicates non-overflow condition of ADC FIFO.

ADC Channel MUX and Control Register

BADR1 + 2

This register sets channel MUX HI/LO limits, ADC gain, offset and pacer source.

This register is read/write.

WRITE

15	14	13	12	11	10	9	8
-	-	ADPS1	ADPS0	UNIBIP	SEDIFF	GS1	GS0

7	6	5	4	3	2	1	0
CHH8	CHH4	CHH2	CHH1	CHL8	CHL4	CHL2	CHL1

CHL8-CHL1, CHH8-CHH1

When these bits are written, the analog input multiplexers are set to the channel specified by CHL8-CHL1. After each conversion, the input multiplexers increment to the next channel, reloading to the "CHL" start channel after the "CHH" stop channel is reached. LO and HI channels are decodes of the four-bit binary patterns. The binary coding for the CHH/CHL channels is listed in Table 3.

Table 3. HI/LO Channel 4-bit Binary Decode

Channel	CHx8	CHx4	CHx2	CHx1
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

GS[1:0] These bits determine the ADC range as indicated in Table 4.

Table 4. ADC Selection Bits Coding

GS1	GS0	Range PCI-DAS1002	Range PCI-DAS1001	Range PCI-DAS1000
0	0	10V	10V	10V
0	1	5V	1V	5V
1	0	2.5V	0.1V	2.5V
1	1	1.25V	0.01V	1.25V

SEDIFF Selects measurement configuration for the Analog Front-End.
1 = Analog Front-End in Single-Ended Mode. This mode supports up to 16 channels.
0 = Analog Front-End in Differential Mode. This mode supports up to eight channels.

UNIBIP Selects offset configuration for the Analog Front-End.
1 = Analog Front-End Unipolar for selected range
0 = Analog Front-End Bipolar for selected range.

Tables 5 and 6 summarize all possible Offset/Range configurations.

Table 5. PCI-DAS1000/1002 Offset/Range Configurations

UNIBIP	GS1	GS0	Input Range	Input Gain	Measurement Resolution
0	0	0	±10V	1	4.88 mV
0	0	1	±5V	2	2.44 mV
0	1	0	±2.5V	4	1.22 mV
0	1	1	±1.25V	8	610 µV
1	0	0	0 to 10V	1	2.44 mV
1	0	1	0 to 5V	2	1.22 mV
1	1	0	0 to 2.5V	4	610 µV
1	1	1	0 to 1.25V	8	305 µV

Table 6. PCI-DAS1001 Offset/Range Configurations

UNIBIP	GS1	GS0	Input Range	Input Gain	Measurement Resolution
0	0	0	±10V	1	4.88 mV
0	0	1	±1V	10	488 µV
0	1	0	±0.1V	100	48.8 µV
0	1	1	±0.01V	1,000	4.88 µV
1	0	0	0 to 10V	1	2.44 mV
1	0	1	0 to 1V	10	244 µV
1	1	0	0 to 0.1V	100	24.4 µV
1	1	1	0 to 0.01V	1,000	2.44 µV

ADPS[1:0] These bits select the ADC Pacer Source (Table 7).

Table 7. ADC Pacer Source Select Bits

ADPS1	ADPS0	Pacer Source
0	0	SW Convert
0	1	82C54 Counter/Timer
1	0	External Falling
1	1	External Rising

Note: For ADPS[1:0] = 00 case, SW conversions are initiated via a word write to BADR2 + 0. Data is don't care.

READ

15	14	13	12	11	10	9	8
	EOC						

7	6	5	4	3	2	1	0

EOC Real-time, non-latched status of ADC End-of-Conversion signal.
1 = ADC DONE
0 = ADC BUSY

Trigger Control / Status Register

BADR1 + 4

This register provides control bits for all ADC trigger modes. It is a read/write register.

WRITE

15	14	13	12	11	10	9	8
-	-	C0SRC	FFM0	ARM	-	-	-

7	6	5	4	3	2	1	0
XTRCL	PRTRG	BURSTE	TGEN	-	-	TS1	TS0

TS[1:0] These bits select one of two possible ADC Trigger Sources; refer to Table 8 below.

Table 8. ADC Trigger Source Select Bits

TS1	**TS0**	**Source**
0	0	Disabled
0	1	SW Trigger
1	0	External (Digital)
1	1	Not Defined

Note: TS[1:0] should be set to 0 while setting up Pacer source and count values.

TGEN This bit is used to enable the External Trigger function.
1 = External rising-edge Digital Trigger enabled.
0 = External Digital Trigger has no effect.

Note: The external trigger requires proper setting of the TS[1:0] and TGEN bits. After these bits are set, the next rising edge will start a Paced ADC conversion. Subsequent triggers will have no effect until external trigger flop is cleared (XTRCL).

BURSTE This bit enables ADC Burst mode. Start/Stop channels are selected via the CHL*x*, CHH*x* bits in ADC CTRL/STAT register at BADR1 + 2.
1 = Burst Mode enabled
0 = Burst Mode disabled

PRTRG This bit enables ADC Pre-trigger Mode. This bit works with the ARM and FFM0 bits when using Pre-trigger mode.
1 = Enable Pre-trigger Mode
0 = Disable Pre-trigger Mode

XTRCL A write-clear to reset the **XTRIG** flip-flop.
1 = Clear **XTRIG** status
0 = No Effect

ARM *and*

FFM0 These bits work in conjunction with **PRTRG** during FIFO-ADC operations. Table 9 presents a summary of bit settings and operation.

Table 9. Summary of PRTRG and FFM0 Bit Functions

PRTRG	FFM0	FIFO Mode	ARM is set..	Sample CTR Starts on…
0	0	# Samples >1 FIFO Normal Mode	via SW when remaining count <1024	ADHF
		1/2 FIFO < # Samples < 1 FIFO Normal Mode	via SW immediately	
0	1	# Samples <1/2 FIFO Normal Mode	via SW immediately	ADC Pacer
1	0	# Samples >1 FIFO Pre-Trigger Mode	via SW when remaining count <1024	ADHF
		1/2 FIFO < # Samples < 1 FIFO Pre-Trigger Mode	via SW immediately	
1	1	# Samples <1/2 FIFO, Pre-Trigger Mode	via SW immediately	XTRIG

C0SRC This bit allows the user to select the clock source for 82C54B Counter 0 (user counter 4).
1 = Internal 10 MHz oscillator
0 = External clock source input via *CLK4* pin on 100-pin connector.

READ

15	14	13	12	11	10	9	8
-	-	-	INDX_GT	-	-	-	-

7	6	5	4	3	2	1	0
XTRIG	-	-	-	-	-	-	-

XTRIG State of External Trigger flip-flop.
1 = External Trigger flip-flop has been set. This bit is write-cleared (see XTRCL above).
0 = External Trigger flip-flop reset. No trigger has been received.

INDX_GT State of Pre-trigger index counter.
1 = Pre-trigger index counter has completed its count.
0 = Pre-trigger index counter has not been gated on or has not yet completed its count.

Calibration Register

Refer to Chapter 4, "Calibration," in the *PCI-DAS1000, PCI-DAS1001, &PCI-DAS1002 Multifunction Analog & Digital I/O User's Manual* for additional programming details.

BADR1 + 6

This register controls all autocal operations. This is a write-only register.

WRITE

15	14	13	12	11	10	9	8
SDI	CALEN	CSRC2	CSRC1	CSRC0	-	SEL7376	SEL8800

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-

SEL8800 This bit enables the eight-bit trim DACs for the following circuits (Table 10):

Table 10. DAC Channel Functions

DAC Channel	Cal Function	
	PCI-DAS1001 & PCI-DAS1002	**PCI-DAS1000**
0	**DAC0** Fine gain	**N/A**
1	**DAC0** Course gain	**N/A**
2	**DAC0** Offset	**N/A**
3	**DAC1** Offset	**N/A**
4	**DAC1** Fine gain	**N/A**
5	**DAC1** Course gain	**N/A**
6	**ADC** Coarse Offset	**ADC** Coarse Offset
7	**ADC** Fine Offset	**ADC** Fine Offset

SEL7376 This bit latches the seven-bit serial data stream into the AD7376 digital potentiometer (10KOhm). The AD7376 is used for analog input front-end gain calibration.

CSRC[2:0] These bits select the different calibration sources available to the ADC front end. See Table 11 below.

Table 11. Calibration Sources Select Bits

CSRC2	CSRC1	CSRC0	Cal Source	
			PCI-DAS1001 & PCI-DAS1002	**PCI-DAS1000**
0	0	0	AGND	AGND
0	0	1	7.0V	7.0V
0	1	0	3.5V	3.5V
0	1	1	1.75V	1.75V
1	0	0	0.875V	0.875V
1	0	1	8.6 mV	8.6 mV
1	1	0	VDAC0	**N/A**
1	1	1	VDAC1	**N/A**

CALEN This bit is used to enable Cal Mode.
1 = Selected Cal Source, **CSRC[2:0]**, is fed into Analog Channel 0.
0 = Analog Channel 0 functions as normal input.

SDI Serial Data In. This bit is used to set serial address/data stream for the DAC8800 TrimDac and 7376 digital potentiometer. The SDI bit is used in conjunction with **SEL8800** and **SEL7376** bits.

DAC Control / Status Register (PCI-DAS1001 & PCI-DAS1002 Only)

BADR1 + 8

This register selects the DAC gain/range and update modes. This is a write-only register.

WRITE

15	14	13	12	11	10	9	8
-	-	-	-	DAC1R1	DAC1R0	DAC0R1	DAC0R0

7	6	5	4	3	2	1	0
MODE	-	-	-	-	-	DACEN	-

DACEN This bit enables the analog out functions of the PCI-DAS1001 and PCI-DAS1002 boards. The Power-ON state of this bit is 0.
1 = DAC0/1 enabled
0 = DAC0/1 disabled

MODE This bit sets the analog output mode of operation.

1 = Both DAC0 and DAC1 updated with data written to the DAC0 register.
0 = DAC*n* updated with data written to the DAC*n* register.

DAC*n*R[1:0] These bits select the independent gains/ranges for either DAC0 or DAC1
n = 0 for DAC0 and *n* = 1 for DAC1. Refer to Table 12 for ranges/LSB values.

Table 12. DAC0/1 Ranges Select Bits

DAC*n*R1	DAC*n*R2	Range	LSB Size
0	0	Bipolar 5V	2.44mV
0	1	Bipolar 10V	4.88mV
1	0	Unipolar 5V	610mV
1	1	Unipolar 10V	1.22mV

BADR2

The I/O Region defined by BADR2 contains the ADC Data register and the ADC FIFO clear register.

ADC Data Register

BADR2 + 0

ADC Data register.

WRITE

Writing to this register is only valid for software-initiated conversions. The ADC Pacer source must be set to 00 via the ADPS[1:0] bits. A null write to BADR2 + 0 will begin a single conversion. Conversion status may be determined in two ways. The EOC bit in BADR1 + 2 can be polled until true or ADNEI (the AD FIFO not-empty interrupt) may be used to signal that the ADC conversion is complete and the data word is present in the FIFO.

READ

15	14	13	12	11	10	9	8
0	0	0	0	AD11	AD10	AD9	AD8
				MSB			
7	6	5	4	3	2	1	0
AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
							LSB

AD[11:0] This register contains the current ADC data word. Data format is dependent upon offset mode:

Bipolar Mode: Offset Binary Coding
000 h = –FS
800h = Mid-scale (0V)
FFFh = +FS – 1LSB

Unipolar Mode: Straight Binary Coding
000 h = –FS (0V)
800h = Mid-scale (+FS/2)
FFFh = +FS – 1LSB

ADC FIFO Clear Register

BADR2 + 2

ADC FIFO Clear register (a write-only register). A write to this address location clears the ADC FIFO. Data is Don't Care. Clear the ADC FIFO before all new ADC operations.

BADR3

The I/O Region defined by BADR3 contains data and control registers for the ADC Pacer, Pre/Post-Trigger Counters, User counters and digital I/O bytes. All reads/writes to BADR3 are *byte* operations. The PCI-DAS1000 series boards have two 82C54 counter/timers. These are referred to as 8254A and 8254B and are assigned as shown in Table 13:

Table 13. Counter/Timer Assignments

Counter/Timer	Counter #	Function
8254A	0	ADC Post-Trigger Sample Counter
8254A	1	ADC Pacer Lower Divider
8254A	2	ADC Pacer Upper Divider
8254B	0	User Counter #4 & ADC Pre-Trigger Index Counter
8254B	1	User Counter #5
8254B	2	User Counter #6

ADC Pacer Clock Data and Control Registers

8254A COUNTER 0 DATA - ADC POST TRIGGER CONVERSION COUNTER

BADR3 + 0

READ/WRITE

7	6	5	4	2	3	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Counter 0 is used to stop the acquisition when the desired number of samples have been gathered. It essentially is gated on when a 'residual' number of conversions remain. The main counting of samples is done by the Interrupt Service Routine, which will increment each time by 'packets' equal to 1/2 FIFO. Generally the value loaded into Counter 0 is N mod 1024, where N is the total count, or the post trigger count, since Total count is not known when pre-trigger is active. Counter 0 will be enabled by use of the ARM bit (BADR1 + 4) when the next-to-last 1/2-full interrupt is processed. Counter 0 is to operated in Mode 0.

8254A COUNTER 1 DATA - ADC PACER DIVIDER LOWER

BADR3 + 1

READ/WRITE

7	6	5	4	2	3	1	0
D7	D6	D5	D4	D3	D2	D1	D0

8254A COUNTER 2 DATA - ADC PACER DIVIDER UPPER

BADR3 + 2

READ/WRITE

7	6	5	4	2	3	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Counter 1 provides the lower 16 bits of the 32-bit pacer clock divider. Its output is fed to the clock input of Counter 2 which provides the upper 16-bits of the pacer clock divider. The clock input to Counter 1 is a precision 10 MHz oscillator source.

Counter 2 output is called the 'Internal Pacer' and can be selected by software to the be the ADC Pacer source. Counters 1 & 2 should be configured to operate in 8254 Mode 2.

ADC 8254 CONTROL REGISTER

BADR3 + 3

WRITE ONLY

7	6	5	4	2	3	1	0
D7	D6	D5	D4	D3	D2	D1	D0

The control register is used to set the operating Modes of 8254 Counters 0, 1 & 2. A counter is configured by writing the correct Mode information to the Control Register followed by count written to the specific Counter Register.

The Counters on the 8254 are 16-bit devices. Since the interface to the 8254 is only eight bits wide, count data is written to the Counter Register as two successive bytes. The low byte is written first, then the high byte. The Control Register is eight bits wide. For more information, refer the 8254 data sheet available at http://www.measurementcomputing.com/PDFmanuals/82C54.pdf.

Digital I/O Data and Control Registers

The 24 DI/O lines are grouped as three, byte-wide I/O ports. Port assignment and functionality is according to the industry-standard 8255 Peripheral Interface. For more information on using the 82C55 in modes 1 or 2, refer the 8255 data sheet available at http://www.measurementcomputing.com/PDFmanuals/82C55A.pdf.

DIO PORT A DATA

BADR3 + 4

PORT A can be configured as an eight-bit I/O channel.

READ/WRITE

7	6	5	4	2	3	1	0
D7	D6	D5	D4	D3	D2	D1	D0

DIO PORT B DATA

BADR3 + 5

PORT B can be configured as an eight-bit I/O channel. Its functionality is identical to PORT A.

READ/WRITE

7	6	5	4	2	3	1	0
D7	D6	D5	D4	D3	D2	D1	D0

DIO PORT C DATA

BADR3 + 6

PORT C can be configured as an eight-bit port of either input or output, or it can be split into two independent four-bit ports of input or output. When split into two, four-bit I/O ports, D[3:0] make up the lower nibble, D[7:4] comprise the upper nibble. Although it can be split, every write to Port C is a byte operation. Unwanted information must be ANDed out during reads and writes must be ORed with current value of the other four-bit port.

READ/WRITE

7	6	5	4	2	3	1	0
D7	D6	D5	D4	D3	D2	D1	D0

DIO CONTROL REGISTER

BADR3 + 7

The DIO Control register is used configure Ports A, B, and C as inputs or outputs. Operation is identical to that of the 8255 parallel I/O device.

WRITE

7	6	5	4	2	3	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Table 14 lists the possible I/O Port configurations for operation in MODE 0 (for mode 0, D7 is always "1", D2, D5 and D6 are always "0"):

Table 14. Possible I/O Port Configurations in DIO - Mode 0

D4	D3	D1	D0	PORT A	PORT C UPPER	PORT B	PORT C LOWER	HEX	DECIMAL
0	0	0	0	OUT	OUT	OUT	OUT	80	128
0	0	0	1	OUT	OUT	OUT	IN	81	129
0	0	1	0	OUT	OUT	IN	OUT	82	130
0	0	1	1	OUT	OUT	IN	IN	83	131
0	1	0	0	OUT	IN	OUT	OUT	88	136
0	1	0	1	OUT	IN	OUT	IN	89	137
0	1	1	0	OUT	IN	IN	OUT	8A	138
0	1	1	1	OUT	IN	IN	IN	8B	139
1	0	0	0	IN	OUT	OUT	OUT	90	144
1	0	0	1	IN	OUT	OUT	IN	91	145
1	0	1	0	IN	OUT	IN	OUT	92	146
1	0	1	1	IN	OUT	IN	IN	93	147
1	1	0	0	IN	IN	OUT	OUT	98	152
1	1	0	1	IN	IN	OUT	IN	99	153
1	1	1	0	IN	IN	IN	OUT	9A	154
1	1	1	1	IN	IN	IN	IN	9B	155

Index and User Counter 4 Data and Control Registers

8254B COUNTER 0 DATA - ADC PRE-TRIGGER INDEX COUNTER (user-counter #4)

BADR3 + 8

READ/WRITE

7	6	5	4	2	3	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Counter 0 of the 8254B device is a shared resource. When not in ADC pre-trigger mode, the clock, gate and output lines of Counter 0 are available to the user at the 100 pin connector as user counter 4. The 8254's Counter 0 clock source is software-selectable via the C0SRC bit in BADR1+4.

When in ADC Pre-trigger mode, this counter is used as the ADC Pre-Trigger index counter. When the ADC is operating in Pre-Trigger Mode, this counter serves to mark the boundary between pre- and post-trigger samples. The External ADC Trigger flip flop gates Counter 0 on; the ADC FIFO Half-Full signal gates it off. Knowing the desired number of post-trigger samples, software can then calculate how may 1/2 FIFO data packets need to be collected and what corresponding residual sample count needs to be written to BADR3 + 0.

82C54B COUNTER 1 DATA - USER COUNTER 5

BADR3 + 9

READ/WRITE

7	6	5	4	2	3	1	0
D7	D6	D5	D4	D3	D2	D1	D0

The clock, gate and output lines of Counter 1 are available at the 100-pin connector as user counter 5. The 8254's Counter 1 clock source is always external and must be provided by the user.

8254B COUNTER 2 DATA - USER COUNTER 6

BADR3 + Ah

READ/WRITE

7	6	5	4	2	3	1	0
D7	D6	D5	D4	D3	D2	D1	D0

The clock, gate and output lines of Counter 2 are available at the 100-pin connector as user-counter 6. The 8254's Counter 2 clock source is always external and must be provided by the user.

82C54B CONTROL REGISTER

BADR3 + Bh

WRITE ONLY

7	6	5	4	2	3	1	0
D7	D6	D5	D4	D3	D2	D1	D0

The control register is used to set the operating modes of 8254B Counters 0, 1, and 2. These counters correspond to user counters 4, 5 and 6. A counter is configured by writing the correct mode information to the Control Register, then the proper count data must be written to the specific Counter Register.

The Counters on the 8254 are 16-bit devices. Since the interface to the 8254 is only eight bits wide, count data is written to the Counter Register as two successive bytes. First the low byte is written, then the high byte. The Control Register is eight bits wide. For more information, refer the 8254 data sheet available at http://www.measurementcomputing.com/PDFmanuals/82C54.pdf.

BADR4 (PCI-DAS1001 & PCI-DAS1002 only)

The I/O region defined by BADR4 contains the DAC0 and DAC1 analog output data registers.

DAC0 DATA REGISTER

BADR4 + 0

WRITE

15	14	13	12	11	10	9	8
-	-	-	-	DAC0	DAC0	DAC0	DAC0
				MSB			
7	6	5	4	3	2	1	0
DAC0	DAC0	DAC0	DAC0	DAC0	DAC0	DAC0	DAC0
							LSB

Writing to this register initiates a conversion on DAC0. If the MODE bit in BARD1 + 8 is set, writes to this register simultaneously updates both DAC0 and DAC1 with the data written to this register. The data format is dependent on the offset mode described below.

Bipolar Mode: Offset Binary Coding

000h = –FS
800h = Mid-scale (0V)
FFFh = +FS – 1LSB

Unipolar Mode: Straight Binary Coding

000h = –FS (0V)
800h = Mid-scale (+FS/2)
FFFh = +FS – 1LSB

DAC1 DATA REGISTER

BADR4 + 2

WRITE

15	14	13	12	11	10	9	8
-	-	-	-	DAC1	DAC1	DAC1	DAC1
				MSB			
7	6	5	4	3	2	1	0
DAC1	DAC1	DAC1	DAC1	DAC1	DAC1	DAC1	DAC1
							LSB

Writing to this register initiates a conversion on DAC1. If the MODE bit in BADR1 + 8 is set, writes to this register will have no effect.

Measurement Computing Corporation
16 Commerce Boulevard,
Middleboro, Massachusetts 02346
(508) 946-5100
Fax: (508) 946-9500
E-mail: info@measurementcomputing.com
www.measurementcomputing.com