Register Map for the PCI-CTR10

Revision 1, June, 2002

Register description

The registers that are used in the PCI-CTR10 board are listed below.

Register	Read Function	Write Function	Operation
BADR1+4Ch	Interrupt Status	Interrupt Control	32-bit Dbl Word
BARD1+50h	User I/O Status	User I/O Control	32-bit Dbl Word
BADR2+0	9513_A Input Data Port_A	9513_A Output Data Port	8-bit byte
BADR2+1	9513_A Control Port_A Readback	9513_A Control Port	8-bit byte
BADR2+2	Digital Input Port_A	No function	8-bit byte
BADR2+3	Digital Output Port_A Readback	Digital Output Port_A	8-bit byte
BADR2+4	9513_B Input Data Port_B	9513_B Output Data Port_B	8-bit byte
BADR2+5	9513_B Control Port_B Readback	9513_B Control Port_B	8-bit byte
BADR2+6	Digital Input Port_B	No function	8-bit byte
BADR2+7	Digital Output Port_B Readback	Digital Output Port_B	8-bit byte

The PCI-CTR10 uses two 9513 counter timer chips. The 9513 contains five counters of 16 bits each. An input source, a count register, load register, hold register, alarm register, an output, and a gate are associated with each counter.

The 9513 is extremely flexible. However, this flexibility can make it a challenge to program the chip directly. Unlike an Intel 8254, which has a single source, single gate, and unique I/ O address for each counter, the 9513 is fully programmable, and any counter may be internally connected to any gate and receive its counts from a number of sources.

Detailed 9513 register information is not included in this manual. Those wishing to know more about the 9513 and its programming should contact our technical support group and request the *9513 System Timing Controller Technical Manual*. As of this writing there is no charge for the manual.

- Phone: 508-946-5100
- Fax: 508-946-9500 to the attention of Tech Support
- Email: techsupport@measurementcomputing.com.

In addition to the manual, a 9513 data sheet is available at http://www.measurementcomputing.com/PDFmanuals/9513A.pdf.

We suggest that you use the Universal Library™ rather than resort to programming the 9513 directly. It is difficult to program, and since programming support is available through the Universal Library, we cannot help with other 9513 programming.

Interrupt Status and Control

BADR1 + 4Ch

This register is 32-bits long. Since the rest of the register has specific control functions, they need to be masked off in order to access the interrupt control functions.

Note that Interrupt_A refers to the interrupt associated with IRQENA and IRQINA signals on the P1 connector. Interrupt_B refers to the interrupt associated with IRQENB and IRQINB signals on the P2 connector.

READ/ WRITE

31:12	11	10	9	8
Unused	INTCLR_B	INTCLR_A	INTSEL_B	INTSEL_A

7	6	5	4	3	2	1	0
SW_INT	PCIINT	INT_B	INTPOL_B	INTE_B	INT_A	INTPOL_A	INTE_A

INTE_A is the Interrupt_A Enable: 0 = disabled (default), 1 = enabled.

INTPOL_A is the Interrupt_A Polarity: 0 = active low (default), 1 = active high.

INT_A is the Interrupt_A Status: 0 = interrupt is not active, 1 = interrupt is active.

INTE_B is the Interrupt_B Enable: 0 = disabled (default), 1 = enabled.

INTPOL_B is the Interrupt_B Polarity: 0 = active low (default), 1 = active high.

INT_B is the Interrupt_B Status: 0 = interrupt is not active, 1 = interrupt is active.

PCIINT is the PCI Interrupt Enable: 0 = disabled (default), 1 = Enabled

SW_INT A value of 1 generates a software interrupt.

INTSEL_A is the Interrupt_A select bit: 0 = level-sensitive (default), 1 = edge-sensitive. Note that this bit only has an effect when in high polarity mode. The interrupt is always level-sensitive when low polarity is selected.

INTSEL_B is the Interrupt_B select bit: 0 = level-sensitive (default), 1 = edge-sensitive. Note that this bit only has an effect when in high polarity mode. The interrupt is always level-sensitive when low polarity is selected.

INTCLR_A is used to clear Interrupt_A when in edge-triggered triggered configuration.

INTCLR_B is used to clear Interrupt_B when in edge-triggered triggered configuration.

User I/O Status and Control

BADR1 + 50h

OUT0 and OUT1 signals select the clock input to the 9513 Counter/ Timers. Since the rest of the register has specific control functions, mask them off to access the OUT0/OUT1 general purpose I/ O bits.

READ/ WRITE

31:8	7	6	5	4	3	2	1	0
X	X	X	OUT1	1	0	OUT0	1	0

OUT1	OUT0	Clock	Source
0	0	5 MHz (default)	10 MHz Xtal/2
0	1	1 MHz	10 MHz Xtal/10
1	0	3.33 MHz	PCI 33 MHz/10
1	1	1.67 MHz	PCI 33 MHz/20

Bits 0, 1, 3 and 4 should not be modified. Bits 0 and 3 enable OUT0/OUT1 functions. Bits 1 and 4 set OUT0/OUT1 for output.

9513_A Data Port

BADR2 + 00h

The 9513_A Data Port communicates with the internal registers such as the Master Mode register and the five Counter Mode registers, one for each counter. The internal Data Pointer controls the Data Port addressing.

READ/ WRITE

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

9513_A Control Port

BADR2 + 01h

The 9513 Control Port allows direct access to the internal Status and Command registers as well as updating the Data Pointer register.

READ/ WRITE

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Digital Input Port_A

BADR2 + 02h

READ ONLY

7	6	5	4	3	2	1	0
Din7	Din6	Din5	Din4	Din3	Din2	Din1	Din0

This register reads the Digital Input Port_A.

The external signal DIN STROBE_A is also used with the Digital Input Port. DIN STROBE_A is internally pulled high through a 10 kohm resistor to allow software to read the Digital Input Port_A by simply reading BADR2 + 02h (as described above). The user can also latch the Digital Input Port_A data into the register by strobing DIN STROBE_A low. This allows the user to read the Digital Input Port_A at a later time.

Digital Output Port_A

BADR2 + 03h

READ/ WRITE

7	6	5	4	3	2	1	0
Dout7	Dout6	Dout5	Dout4	Dout3	Dout2	Dout1	Dout0

This register sets the Digital Output Port_A. Reading this register reads the current status of the output port.

9513_B Data Port

BADR2 + 04h

The 9513_B Data Port communicates with the internal registers such as the Master Mode register and the five Counter Mode registers, one for each counter. The internal Data Pointer controls the Data Port addressing.

READ/ WRITE

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

9513_B Control Port

BADR2 + 05h

The 9513 Control Port allows direct access to the internal Status and Command registers as well as updating the Data Pointer register.

READ/ WRITE

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Digital Input Port_B

BADR2 + 06h

READ ONLY

7	6	5	4	3	2	1	0

Din7	Din6	Din5	Din4	Din3	Din2	Din1	Din0

This register reads the Digital Input Port_B.

The external signal DIN STROBE_B is also used with the Digital Input Port. DIN STROBE_B is internally pulled high through a 10 kohm resistor to allow software to read the Digital Input Port_B by simply reading BADR2 + 02h (as described above). The user can also latch the Digital Input Port_B data into the register by strobing DIN STROBE_B low. This allows the user to read the Digital Input Port_B at a later time.

Digital Output Port_B

BADR2 + 07h

READ/ WRITE

7	6	5	4	3	2	1	0
Dout7	Dout6	Dout5	Dout4	Dout3	Dout2	Dout1	Dout0

This register sets the Digital Output Port_B. Reading this register reads the current status of the output port.

Measurement Computing Corporation
16 Commerce Blvd.
Middleboro, Massachusetts 02346
(508) 946-5100
Fax: (508) 946-9500
E-mail: info@measurementcomputing.com
www.measurementcomputing.com