Register Map for the PCI-DDA0x/12 Series

PCI-DDA02/12

PCI-DDA04/12

PCI-DDA08/12

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Register Description

This document describes the register map for the PCI-DDA0x/12 Series boards. PCI-DDA0x/12 Series boards include the PCI-DDA02/12, PCI-DDA04/12, and PCI-DDA08/12 analog output and digital I/O boards. Only experienced programmers should attempt register-level programming.

Register Overview

NOTE: Ignore references to D/A channels 4 through 7 on the PCI-DDA04/12, and references to channels 2 through 7 on the PCI-DDA02/12. Otherwise, the three boards are identical.

PCI-DDA0x/12 Series board operation registers are mapped into I/O space. Unlike ISA bus designs, this board has several base addresses, each corresponding to a reserved block of addresses in I/O space.

Of the six Base Address Regions (BADR) available per the PCI 2.1 specification, four are implemented in this design and are summarized in Table 1.

Table 1. Board I/O Address Regions

I/O Region	Function	Operations
BADR0	PCI memory mapped configuration registers	32-bit Double word
BADR1	PCI I/O mapped configuration registers	32-bit Double word
BADR2	Digital I/O registers	8-bit Byte
BADR3	DAC registers	16-bit Word

The PCI-DDA0x/12 series boards use the PLX PCI 9052 PCI Bus Interface chip. For detailed information about this chip, refer to the *PCI 9052 Data Book* (September, 2001). This document is available from PLX Technology® at www.plxtech.com/products/9052/default.htm.

- BADR0 and BADR1 registers are used for PCI configuration and have no user functions.
- BADR2 is an 8-bit data/address bus for compatibility with our other digital I/O PCI cards.
- BADR3 is a 16-bit data/address bus for software ease when writing to 12-bit DACs.

BADR2

Table 2. BADR2 Read/Write Functions

Register	READ Function	WRITE Function
BADR2 + 0	Input Port 0A data	Output Port 0A data
BADR2 + 1	Input Port 0B data	Output Port 0B data
BADR2 + 2	Input Port 0C data	Output Port 0C data
BADR2 + 3	Readback - Control Register 0	Control Register 0
BADR2 + 4	Input Port 1A data	Output Port 1A data
BADR2 + 5	Input Port 1B data	Output Port 1B data
BADR2 + 6	Input Port 1C data	Output Port 1C data
BADR2 + 7	Readback - Control Register 1	Control Register 1

The digital I/O ports emulate 82C55 Mode 0 operation.

Port 0A data

BADR2 + 0

Read/Write

7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0

Port 0B data

BADR2 + 1

Read/Write

7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0

Port 0C data

BADR2 + 02h

Read/Write

7	6	5	4	3	2	1	0
CH3	CH2	CH1	CH0	CL3	CL2	CL1	CL0

Control Register 0

BADR2 + 03h

Read/Write

7	6	5	4	3	2	1	0
-	-	-	D4	D3	-	D1	D0

The operating mode of the digital I/O port is set to Mode 0. The control register is used to configure the ports for either input or output. For example, to set all ports to output, write the value **0h to Base + 3**. To set all ports to input, write the value **13h to Base + 3**. You can read the current state of an output port by simply reading that port.

In Table 3, D7, D6, D5, and D2 are 'don't care', and are listed in the table as 0. It does not matter what data is written to these bits. 'CU' is port C upper nibble, 'CL' is port C lower nibble.

Table 3. Digital I/O Configuration Codes

Control Register codes				Values		DIO port mode			
D4	D3	D1	D0	Hex	Dec	A	B	CU	CL
0	0	0	0	0	0	OUT	OUT	OUT	OUT
0	0	0	1	1	1	OUT	OUT	OUT	IN
0	0	1	0	2	2	OUT	OUT	IN	OUT
0	0	1	1	3	3	OUT	OUT	IN	IN
0	1	0	0	8	8	OUT	IN	OUT	OUT
0	1	0	1	9	9	OUT	IN	OUT	IN
0	1	1	0	A	10	OUT	IN	IN	OUT
0	1	1	1	B	11	OUT	IN	IN	IN
1	0	0	0	10	16	IN	OUT	OUT	OUT
1	0	0	1	11	17	IN	OUT	OUT	IN
1	0	1	0	12	18	IN	OUT	IN	OUT
1	0	1	1	13	19	IN	OUT	IN	IN
1	1	0	0	18	24	IN	IN	OUT	OUT

Control Register codes				Values		DIO port mode			
D4	**D3**	**D1**	**D0**	**Hex**	**Dec**	**A**	**B**	**CU**	**CL**
1	1	0	1	19	25	IN	IN	OUT	IN
1	1	1	0	1A	26	IN	IN	IN	OUT
1	1	1	1	1B	27	IN	IN	IN	IN

Port 1A data

BADR2 + 04h

Read/Write

7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0

Port 1B data

BADR2 + 05h

Read/Write

7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0

Port 1C data

BADR2 + 06h

Read/Write

7	6	5	4	3	2	1	0
CH3	CH2	CH1	CH0	CL3	CL2	CL1	CL0

Control Register 1

BADR2 + 07h

Read/Write

7	6	5	4	3	2	1	0
-	-	-	D4	D3	-	D1	D0

See BADR2 + 03h and Table 3 for full description of the Control Register.

BADR3

Table 4. BADR3 Registers

Register	READ Function	WRITE Function
BADR3 + 0	Initiate a simultaneous update	D/A Control Register
BADR3 + 2h		Reserved
BADR3 + 4h	D/A Calibration Register 1 Data	D/A Calibration Register 1
BADR3 + 6h	D/A Calibration Register 2 Data	D/A Calibration Register 2
BADR3 + 8h		D/A 0 DATA
BADR3 + Ah		D/A 1 DATA
BADR3 + Ch		D/A 2 DATA
BADR3 + Eh		D/A 3 DATA
BADR3 + 10h		D/A 4 DATA
BADR3 + 12h		D/A 5 DATA
BADR3 + 14h		D/A 6 DATA
BADR3 + 16h		D/A 7 DATA

D/A Control Register

BADR3 + 0h

Write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	R2	R1	R0	X	D2	D1	D0	EN	SU

Read

Reading this register initiates a simultaneous update for all DACs.

SU — This bit enables simultaneous update for the DAC pair specified by D2 and D1 (see table below). Setting the simultaneous update bit inhibits updating the DAC output until a simultaneous update is initiated (see Read below). The DACs are paired as follows; DACs 0 and 1, DACs 2 and 3, DACs 4 and 5, and DACs 6 and 7. Setting simultaneous update for either DAC in the pair will set it for both.

0 = Simultaneous update disabled

1 = Simultaneous update enabled

The power-on status of this bit is 0.

EN — This bit enables the DAC specified by D2, D1, D0.

0 = DAC disabled

1 = DAC enabled

The power-on status of this bit is 0. A disabled DAC is held at 0v.

D[2:0] — These bits specify the DAC that is being configured (Table 5).

Table 5. DAC Channel Codes

D2	D1	D0	DAC Channel
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

R[2:0] — These bits select the gain/range for the DAC specified by D2, D1, and D0. The power on setting is Bipolar 2.5V (Table 6).

Table 6. DAC Range Codes

R2	R1	R0	RANGE	LSB Size
0	0	X	Bipolar 2.5V	1.22mV
0	1	0	Bipolar 5V	2.44mV
0	1	1	Bipolar 10V	4.88mV
1	0	X	Unipolar 2.5V	611uV
1	1	0	Unipolar 5V	1.22mV
1	1	1	Unipolar 10V	2.44mV

D/A Calibration Register 1

BADR3 + 4h

Use *Insta*Cal for all board calibration functions.

Direct reads and writes to the calibration registers require a complex sequence, the scope of which is beyond the scope of this document. If you need to program the calibration registers, please contact the factory for further information.

D/A Calibration Register 2

BADR3 + 6h

Use *Insta*Cal for all board calibration functions.

Direct reads and writes to the calibration registers require a complex sequence, the scope of which is beyond the scope of this document. If you need to program the calibration registers, please contact the factory for further information.

D/A 0 - D/A 7 Data

The following eight registers are the data registers for the eight, 12-bit output DACs. Writing to the register will automatically update the DAC output unless the simultaneous update bit is set for that DAC. (Refer to the *D/A Control Register* on page 4 for more information simultaneous update.) The data format is mode-dependent as shown below.

Bipolar Mode:

Offset Binary Coding

000h = –FS 800h = Mid Scale (0V) FFFh = +FS – 1 LSB

Unipolar Mode:

Straight Binary Coding

000h = – FS (0V) 800h = Mid Scale (+FS/2) FFFh = +FS – 1 LSB

D/A 0 Data

BADR3 + 8h

Write only

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

D/A 1 Data

BADR3 + 0Ah

Write only

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

D/A 2 Data

BADR3 + 0Ch

Write only

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

D/A 3 Data

BADR3 + 0Eh

Write only

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

D/A 4 Data

BADR3 + 10h

Write only

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

D/A 5 Data

BADR3 + 12h

Write only

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

D/A 6 Data

BADR3 + 14h

Write only

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

D/A 7 Data

BADR3 + 16h

Write only

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

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