Register Map for the PCI-CTR20HD

Revision 1, May, 2003

Register Description

The registers that are used in the PCI-CTR20HD board are listed below.

Register	Read Function	Write Function	Operation
BADR1+4Ch	Interrupt Status	Interrupt Control	32-bit Dbl Word
BADR2+0	9513_A Input Data Port	9513_A Output Data Port	8-bit byte
BADR2+1	9513_A Control Port Readback	9513_A Control Port	8-bit byte
BADR2+2	9513_B Input Data Port	9513_B Output Data Port	8-bit byte
BADR2+3	9513_B Control Port Readback	9513_B Control Port	8-bit byte
BADR2+4	9513_C Input Data Port	9513_C Output Data Port	8-bit byte
BADR2+5	9513_C Control Port Readback	9513_C Control Port	8-bit byte
BADR2+6	9513_D Input Data Port	9513_D Output Data Port	8-bit byte
BADR2+7	9513_D Control Port Readback	9513_D Control Port	8-bit byte
BADR2+8	N/A	Counter A&B Source Select, INTAB Pol	8-bit byte
BADR2+9	N/A	Counter C&D Source Select, INTCB Pol	8-bit byte

The PCI-CTR20HD uses four 9513 counter timer chips. The 9513 contains five counters of 16-bits each. An input source, a count register, load register, hold register, alarm register, an output, and a gate are associated with each counter.

The 9513 counter/timer device is extremely flexible. However, this flexibility can make it a challenge to program the chip directly. Unlike an Intel 8254 counter/timer device, which has a single source, single gate, and unique I/ O address for each counter, the 9513 is fully programmable. Any counter may be internally connected to any gate and receive its counts from a number of sources.

Detailed 9513 register information is not included in this document. For detailed information about the 9513 and its programming, request the *9513 System Timing Controller Technical Manual* from our technical support group. As of this writing there is no charge for the manual.

- Phone: 508-946-5100
- Fax: 508-946-9500 to the attention of Tech Support
- Email: techsupport@measurementcomputing.com

In addition to the manual, a 9513 data sheet is available from our web site at www.mccdaq.com/PDFmanuals/9513A.pdf. However, we suggest that you use the Universal Library rather than attempt to program the 9513 directly. It is difficult to program, and since programming support is available through the Universal Library, we cannot provide support with 9513 programming.

Interrupt Status and Control

BADR1 + 4Ch

This register is 32-bits long. Since the rest of the register has specific control functions, they need to be masked off in order to access the interrupt control functions. Note that Interrupt_AB refers to the interrupt associated with IRQAB_IN signal on pin 26 of the J1 connector. Interrupt_CD refers to the interrupt associated with IRQCD_IN signal on pin 76 of the J1 connector.

Read/Write

31:12	11	10	9	8
Unused	INTCLR_CD	INTCLR_AB	INTSEL_CD	INTSEL_AB

7	6	5	4	3	2	1	0
SW_INT	PCIINT	INT_CD	INTPOL_CD	INTE_CD	INT_AB	INTPOL_AB	INTE_AB

INTE_AB	The Interrupt_AB Enable: 0 = disabled (default), 1 = enabled.
INTPOL_AB	The Interrupt_AB Polarity: 0 = active low (default), 1 = active high. This bit should always be set to 1 for this product. Actual interrupt polarity is determined via the INTAB_POL bit at BADR2+8.
INT_AB	The Interrupt_AB Status: 0 = interrupt is not active, 1 = interrupt is active
INTE_CD	The Interrupt_CD Enable: 0 = disabled (default), 1 = enabled. Always set to one for this product
INTPOL_CD	The Interrupt_CD Polarity: 0 = active low (default), 1 = active high. This bit should always be set to 1 for this product. Actual interrupt polarity is determined via the INTCD_POL bit at BADR2+9.
INT_CD	The Interrupt_CD Status: 0 = interrupt is not active, 1 = interrupt is active
PCIINT	The PCI Interrupt Enable: 0 = disabled (default), 1 = Enabled
SW_INT	A value of 1 generates a software interrupt
INTSEL_AB	The Interrupt_AB select bit: 0 = level-sensitive (default), 1 = edge-sensitive. Note that this bit only has an effect when in high polarity mode. The interrupt is always level-sensitive when low polarity is selected.
INTSEL_CD	The Interrupt_CD select bit: 0 = level-sensitive (default), 1 = edge-sensitive. Note that this bit only has an effect when in high polarity mode. The interrupt is always level-sensitive when low polarity is selected
INTCLR_AB	Used to clear Interrupt_AB when in edge-triggered triggered configuration.
INTCLR_CD	Used to clear Interrupt_CD when in edge-triggered triggered configuration.

9513_A Data Port

BADR2 + 0

The 9513_A Data Port communicates with the internal registers such as the Master Mode register and the five Counter Mode registers, one for each counter. The internal Data Pointer controls the Data Port addressing.

Read/Write

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

9513_A Control Port

BADR2 + 1

The 9513 Control Port allows direct access to the internal Status and Command registers, as well as updating the Data Pointer register.

Read/Write

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

9513_B Data Port

BADR2 + 2

The 9513_B Data Port communicates with the internal registers, such as the Master Mode register and the five Counter Mode registers, one for each counter. The internal Data Pointer controls the Data Port addressing.

Read/Write

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

9513_B Control Port

BADR2 + 3

The 9513 Control Port allows direct access to the internal Status and Command registers, as well as updating the Data Pointer register.

Read/Write

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

9513_C Data Port

BADR2 + 4

The 9513_C Data Port communicates with the internal registers such as the Master Mode register and the five Counter Mode registers, one for each counter. The internal Data Pointer controls the Data Port addressing.

Read/Write

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

9513_C Control Port

BADR2 + 5

The 9513 Control Port allows direct access to the internal Status and Command registers, as well as updating the Data Pointer register.

Read/Write

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

9513_D Data Port

BADR2 + 6

The 9513_D Data Port communicates with the internal registers such as the Master Mode register and the five Counter Mode registers, one for each counter. The internal Data Pointer controls the Data Port addressing.

Read/Write

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

9513_D Control Port

BADR2 + 7

The 9513 Control Port allows direct access to the internal Status and Command registers, as well as updating the Data Pointer register.

Read/Write

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Counters A & B Clock Source Select Register

BADR2+ 8

Write Only

7	6	5	4	3	2	1	0
INTAB_POL	X	CLKB_2	CLKB_1	CLKB_0	CLKA_2	CLKA_1	CLKA_0

CLK#_n

CLK#_2	CLK#_1	CLK#_0	9513_# CLOCK	Source
0	0	0	5.0 MHz	10 MHz Xtal/2
0	0	1	1.0 MHz	10 MHz Xtal/10
0	1	0	10.0 MHz*	10 MHz Xtal
0	1	1	External	External
1	0	0	16.67 MHz*	33 MHz PCI clock/2
1	0	1	8.33 MHz*	33 MHz PCI clock/4
1	1	0	3.33 MHz	33 MHz PCI clock/10
1	1	1	1.67 MHz	33 MHz PCI clock/20

* Note: These higher frequencies are not supported for all manufacturers' versions of the 9513 counter. Please consult with MCC technical support to determine compatibility with these frequencies.

INTAB_POL	Sets the polarity of the external interrupt signal associated with Counters A and B. 0 = Active high or rising edge. 1 = Active low or falling edge.

Counters C & D Clock Source Select Register

BADR2+ 9

Write Only

7	6	5	4	3	2	1	0
INTCD_POL	X	CLKD_2	CLKD_1	CLKD_0	CLKC_2	CLKC_1	CLKC_0

CLK#_n

CLK#_2	CLK#_1	CLK#_0	9513_# CLOCK	Source
0	0	0	5.0 MHz	10 MHz Xtal/2
0	0	1	1.0 MHz	10 MHz Xtal/10
0	1	0	10.0 MHz*	10 MHz Xtal
0	1	1	External	External
1	0	0	16.67 MHz*	33 MHz PCI clock/2
1	0	1	8.33 MHz*	33 MHz PCI clock/4
1	1	0	3.33 MHz	33 MHz PCI clock/10
1	1	1	1.67 MHz	33 MHz PCI clock/20

* Note: These higher frequencies are not supported for all manufacturers' versions of the 9513 counter. Please consult with MCC technical support to determine compatibility with these frequencies.

INTCD_POL	POL sets the polarity of the external interrupt signal associated with the Counters C and D. 0 = Active high or rising edge 1 = Active low or falling edge

Measurement Computing Corporation
16 Commerce Boulevard,
Middleboro, Massachusetts 02346
(508) 946-5100
Fax: (508) 946-9500
E-mail: info@measurementcomputing.com
www.measurementcomputing.com