Register Map for the PCI-DDA0x/16 Series

PCI-DDA02/16

PCI-DDA04/16

PCI-DDA08/16

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Register Description

This document describes the register map for the PCI-DDA0x/16 Series boards. PCI-DDA0x/16 Series boards include the PCI-DDA02/16, PCI-DDA04/16, and PCI-DDA08/16. Only experienced programmers should attempt register-level programming.

Register Overview

NOTE: Ignore references to D/A channels 4 through 7 on the PCI-DDA04/16, and references to channels 2 through 7 on the PCI-DDA02/16. Otherwise, the three boards are identical.

PCI-DDA0#/16 operation registers are mapped into I/O space. Unlike ISA bus designs, this board has several base addresses, each corresponding to a reserved block of addresses in I/O space.

Of the six Base Address Regions (BADR) available per the PCI 2.1 specification, four are implemented in this design and are summarized as follows.

Table 1. BADR Register Summary

I/O Region	Function	Operations
BADR0	PCI memory mapped configuration registers	32-bit DOUBLE WORD
BADR1	PCI I/O mapped configuration registers	32-bit DOUBLE WORD
BADR2	Digital I/O registers	8-bit BYTE
BADR3	DAC registers	16-bit WORD

- BADR0 and BADR1 are used for PCI configuration and have no user functions.
- BADR2 is an 8-bit data/address bus for compatibility with our other digital I/O PCI cards.
- BADR3 is a 16-bit data/address bus.

BADR2

Table 2. BADR2 Read/Write Functions

Register	Read Function	Write Function
BADR2 + 0	Input Port 1A Data	Output Port 1A Data
BADR2 + 1	Input Port 1B Data	Output Port 1B Data
BADR2 + 2	Input Port 1C Data	Output Port 1C Data
BADR2 + 3	Control Register Readback 1	Control Register 1
BADR2 + 4	Input Port 2A Data	Output Port 2A Data
BADR2 + 5	Input Port 2B Data	Output Port 2B Data
BADR2 + 6	Input Port 2C Data	Output Port 2C Data
BADR2 + 7	Control Register Readback 2	Control Register 2

The Digital I/O ports simulate the 8255 Mode 0 function.

Port 1A Data

BADR2 + 0h

Read/Write

7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0

Port 1B Data

BADR2 + 1h

Read/Write

7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0

Port 1C Data

BADR2 + 02h

Read/Write

7	6	5	4	3	2	1	0
CH3	CH2	CH1	CH0	CL3	CL2	CL1	CL0

Control Register 1

BADR2 + 03h

Read/Write

7	6	5	4	3	2	1	0
-	-	-	D4	D3	-	D1	D0

The operating mode of the Digital I/O ports is set to Mode 0. The control register is used to enable the ports for input/output to the connector. For example, to set all ports to output, write the value 0h to BADR2 + 3. To set all ports to input, write the value 1Bh to BADR2 + 3. You can read the current state of an output port by reading that port when configured for output. Codes D7, D6, D5, and D2 are 'don't care'. 'CU' is PORT C upper nibble, 'CL' is PORT C lower nibble.

Table 3. BADR2 Code Functions

Programming Codes				Values		DIO Port			
D4	**D3**	**D1**	**D0**	**H**	**Dec**	**A**	**B**	**CU**	**CL**
0	0	0	0	0	0	OUT	OUT	OUT	OUT
0	0	0	1	1	1	OUT	OUT	OUT	IN
0	0	1	0	2	2	OUT	IN	OUT	OUT
0	0	1	1	3	3	OUT	IN	OUT	IN
0	1	0	0	8	8	OUT	OUT	IN	OUT
0	1	0	1	9	9	OUT	OUT	IN	IN
0	1	1	0	A	10	OUT	IN	IN	OUT
0	1	1	1	B	11	OUT	IN	IN	IN
1	0	0	0	10	16	IN	OUT	OUT	OUT
1	0	0	1	11	17	IN	OUT	OUT	IN
1	0	1	0	12	18	IN	IN	OUT	OUT
1	0	1	1	13	19	IN	IN	OUT	IN
1	1	0	0	18	24	IN	OUT	IN	OUT
1	1	0	1	19	25	IN	OUT	IN	IN
1	1	1	0	1A	26	IN	IN	IN	OUT
1	1	1	1	1B	27	IN	IN	IN	IN

Port 2A Data

BADR2 + 04h

Read/Write

7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0

Port 2B Data

BADR2 + 05h

Read/Write

7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0

Port 2C Data

BADR2 + 06h

Read/Write

7	6	5	4	3	2	1	0
CH3	CH2	CH1	CH0	CL3	CL2	CL1	CL0

Control Register 2

BADR2 + 07h

Read/Write

7	6	5	4	3	2	1	0
-	-	-	D4	D3	-	D1	D0

See BADR2 + 03h and Table 3 for a full description of the Control Register.

BADR3

Table 4. BADR3 Read/Write Functions

Register	Read Function	Write Function
BADR3 + 0	Initiate a simultaneous update	D/A Control Register
BADR3 + 2h		reserved
BADR3 + 4h	D/A Calibration Register 1 Data	D/A Calibration Register 1
BADR3 + 6h		D/A Calibration Register 2
BADR3 + 8h		D/A 0 DATA
BADR3 + Ah		D/A 1 DATA
BADR3 + Ch		D/A 2 DATA
BADR3 + Eh		D/A 3 DATA
BADR3 + 10h		D/A 4 DATA
BADR3 + 12h		D/A 5 DATA
BADR3 + 14h		D/A 6 DATA
BADR3 + 16h		D/A 7 DATA

D/A Control Register

BADR3 + 0h

Read/Write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	R2	R1	R0	X	D2	D1	D0	EN	SU

Write

SU This bit enables simultaneous update for the DAC specified by D2, D1, and D0 (see table below). Setting the simultaneous update bit inhibits updating the DAC output until a simultaneous update is initiated (see READ below).

0 = Simultaneous update disabled

1 = Simultaneous update enabled

The power-on status of this bit is 0

NOTE

Writing to any DAC that does not have its SU bit set will also initiate an update. Therefore, load all the DACs with the SU bit set and then initiate the update before writing to any other DAC.

EN This bit enables the DAC specified by D2, D1, D0.

0 = DAC disabled

1 = DAC enabled

The power-on status of this bit is 0. A disabled DAC is pulled to 0v.

D[2:0] These bits specify the DAC that is being configured.

Table 5. DAC Channel Coding

D2	D1	D0	DAC Channel
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

R[2:0] These bits select the gain/range for the DAC specified by D2, D1, and D0.

The DACs power up at 0V (–FS) in the unipolar 10V range.

Table 6. BADR3 Unipolar/Bipolar Gain/Range Coding

R2	R1	R0	RANGE	LSB Size
0	0	X	Bipolar 2.5V	76.3µV
0	1	0	Bipolar 5V	152.6µV
0	1	1	Bipolar 10V	305.2µV
1	0	X	Unipolar 2.5V	38.1µV
1	1	0	Unipolar 5V	76.3µV
1	1	1	Unipolar 10V	152.6µV

Read

Reading this register initiates a simultaneous update for all DACs.

D/A Calibration Register 1

BADR3 + 4h

Use *Insta*Cal for all board calibration functions.

Direct reads and writes to the calibration registers require a complex sequence, the scope of which is beyond the scope of this document. If you need to program the calibration registers, please contact the factory for further information.

D/A Calibration Register 2

BADR3 + 6h

Use *Insta*Cal for all board calibration functions.

Direct reads and writes to the calibration registers require a complex sequence, the scope of which is beyond the scope of this document. If you need to program the calibration registers, please contact the factory for further information.

D/A 0 - D/A 7 Data

The following eight registers are the data registers for the eight 16-bit output DACs. D0 is the LSB. Writing to the register will automatically update the DAC output unless the simultaneous update bit is set for that DAC (See the D/A Control Register description for more information on simultaneous update.) The data format is mode-dependent as shown below.

Bipolar Mode:

Offset Binary Coding

0000h = –FS 8000h = Mid Scale (0V) FFFFh = +FS – 1LSB

Unipolar Mode:

Straight Binary Coding

0000h = – FS (0V) 8000h = Mid Scale (+FS/2) FFFFh = +FS – 1LSB

D/A 0 Data

BADR3 + 8h

Write only

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

D/A 1 Data

BADR3 + 0Ah

Write only

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

D/A 2 Data

BADR3 + 0Ch

Write only

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

D/A 3 Data

BADR3 + 0Eh

Write only

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

D/A 4 Data

BADR3 + 10h

Write only

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

D/A 5 Data

BADR3 + 12h

Write only

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

D/A 6 Data

BADR3 + 14h

Write only

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

D/A 7 Data

BADR3 + 16h

Write only

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Measurement Computing Corporation
16 Commerce Boulevard,
Middleboro, Massachusetts 02346
(508) 946-5100
Fax: (508) 946-9500
E-mail: info@mccdaq.com
www.mccdaq.com