Register Map for the PCI-CTR05

Revision 1, June, 2002

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Register description

The registers that are used in the PCI-CTR05 board are listed below.

Register	Read Function	Write Function	Operation
BADR1+4Ch	Interrupt Status	Interrupt Control	32-bit Dbl Word
BARD1+50h	User I/O Status	User I/O Control	32-bit Dbl Word
BADR2+0	9513 Input Data Port	9513 Output Data Port	8-bit byte
BADR2+1	9513 Control Port Readback	9513 Control Port	8-bit byte
BADR2+2	Digital Input Port	No function	8-bit byte
BADR2+3	Digital Output Port Readback	Digital Output Port	8-bit byte

The PCI-CTR05 uses one 9513 counter timer chip. The 9513 contains five counters of 16 bits each. An input source, a count register, load register, hold register, alarm register, an output, and a gate are associated with each counter.

The 9513 is extremely flexible. However, this flexibility can make it a challenge to program the chip directly. Unlike an Intel 8254, which has a single source, single gate, and unique I/ O address for each counter, the 9513 is fully programmable, and any counter may be internally connected to any gate and receive its counts from a number of sources.

Detailed 9513 register information is not included in this manual. Those wishing to know more about the 9513 and its programming should contact our technical support group and request the *9513 System Timing Controller Technical Manual*. As of this writing there is no charge for the manual.

- Phone: 508-946-5100
- Fax: 508-946-9500 to the attention of Tech Support
- Email: techsupport@measurementcomputing.com.

In addition to the manual, a 9513 data sheet is available at http://www.measurementcomputing.com/PDFmanuals/9513A.pdf.

We suggest that you use the Universal Library™ rather than resort to programming the 9513 directly. It is difficult to program, and since programming support is available through the Universal Library, we cannot help with other 9513 programming.

Interrupt Status and Control

BADR1 + 4Ch

This register is 32-bits long. Since the rest of the register has specific control functions, they need to be masked off in order to access the interrupt control functions.

READ/ WRITE

31:12	11	10	9	8
Unused	X	INTCLR	X	INTSEL

7	6	5	4	3	2	1	0
SW_INT	PCIINT	X	0	0	INT	INTPOL	INTE

INTE is the Interrupt Enable: 0 = disabled (default), 1 = enabled.

INTPOL is the Interrupt Polarity: 0 = active low (default), 1 = active high.

INT is the Interrupt Status: 0 = interrupt is not active, 1 = interrupt is active.

PCIINT is the PCI Interrupt Enable: 0 = disabled (default), 1 = Enabled

SW_INT A value of 1 generates a software interrupt.

Bits 3 and 4 should be set to 0 for proper operation of this board.

INTSEL is the Interrupt select bit: 0 = level-sensitive (default), 1 = edge-sensitive. Note that this bit only has an effect when in high polarity mode. The interrupt is always level-sensitive when low polarity is selected.

INTCLR is used to clear the Interrupt when in edge-triggered triggered configuration.

User I/O Status and Control

BADR1 + 50h

OUT0 selects the clock input to the 9513 Counter/ Timer. Since the rest of the register has specific control functions, mask them off to access the OUT0 general purpose I/ O bit.

READ/ WRITE

31:8	7	6	5	4	3	2	1	0
X	X	X	X	X	X	OUT0	1	0

If OUT0 = 0, input = 5 MHz (default)

If OUT0 = 1, input = 1 MHz.

Bit 0 enables the bit for OUT0 functions, and bit 1 sets the OUT0 for output so these settings should not be modified.

9513 Data Port

BADR2 + 00h

The 9513 Data Port communicates with the internal registers such as the Master Mode register and the five Counter Mode registers, one for each counter. The internal Data Pointer controls the Data Port addressing.

READ/ WRITE

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

9513 Control Port

BADR2 + 01h

The 9513 Control Port allows direct access to the internal Status and Command registers as well as updating the Data Pointer register.

READ/ WRITE

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Digital Input Port

BADR2 + 02h

READ ONLY

7	6	5	4	3	2	1	0
Din7	Din6	Din5	Din4	Din3	Din2	Din1	Din0

This register reads the digital input Port.

The external signal DIN STROBE is also used with the Digital Input Port. DIN STROBE is internally pulled high through a 10 kohm resistor to allow software to read the Digital Input Port by simply reading BADR2 + 02h (as described above). The user can also latch the Digital Input Port data into the register by strobing DIN STROBE low. This allows the user to read the Digital Input Port at a later time.

Digital Output Port

BADR2 + 03h

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READ/ WRITE

7	6	5	4	3	2	1	0
Dout7	Dout6	Dout5	Dout4	Dout3	Dout2	Dout1	Dout0

This register sets the Digital Output Port. Reading this register reads the current status of the output port.

Measurement Computing Corporation
16 Commerce Blvd.
Middleboro, Massachusetts 02346
(508) 946-5100
Fax: (508) 946-9500
E-mail: info@measurementcomputing.com
www.measurementcomputing.com