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CTS82C54-50

3 Channel 16 Bit Counter / Timer

Compatible with Industry Standard 8254 Counter / Timer

FUNCTIONS

- Programmable Rate Generator
- Programmable Delay Generator
- Interrupt Generation
- Event Counter
- Elapsed Time Counter
- Frequency Generator

APPLICATIONS

- Computer System Timing
  - Programmable System Clock
  - Watchdog Timer
  - Wait State Generator
  - Refresh Generator
- Data Aquisition
  - Event Counter
  - Frequency Counter
  - Programmable Converter Clock / Trigger
- ATE
  - Programmable Stimulus Generator
  - Timing Extremes Generator
- Industrial / Process Controls
  - External Timing Synchronization
  - Programmable Pulse Generator

STANDARD 82C54 FEATURES

- Three programmable 16 bit counters
- Six operating modes
- BCD / Binary Counting
- Independent counter clocks
- TTL compatible
- Low Power
- DIP-24, PLCC and LCC packaging
- Software / Hardware Gating
- Count value accessable while counting

EXTENDED FEATURES

- 50 MHz maximum operating speed
- Alternate packaging available
  - SOIC-24
  - PLCC-28

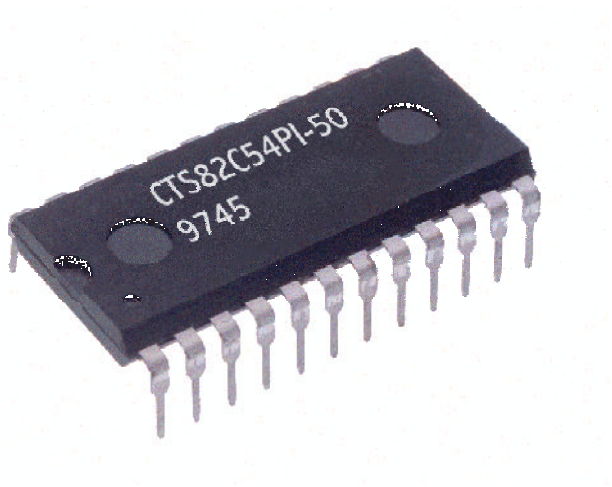


Figure 1 - CTS82C54 DIP-24 Package

CTS82C54 OVERVIEW

The CTS82C54 is a high speed, high performance replacement for the industry standard 82C54 programmable timer peripheral manufactured by Intel©, Harris© and others. Originally design for modest system speeds, this device is now being discontinued by the major manufacturers in favor of more highly integrated peripherals. Implemented in a high speed CMOS ASIC, this device gives a new lease on life to this venerable part by boosting the maximum clock speed from a plodding 10 MHz to a more respectable 50 MHz to keep up with newer systems.

The 8254 has long been the industry standard counter/ timer peripheral for Intel© based microprocessor systems as well as a host of other processors and microcontrollers. Its simple design, instruction set and interface make it a favorite for system timing in a wide variety of processor based systems. Widely used to provide system timing functions indenpendent of software timing loops and varying processor speeds, it has also found wide use as a programmable system clock in a wide variety of data aquisition and embedded controller applications. Its design is still used as a core element of many large multi-function chip sets.

Since this device is based on flexible, widely available ASIC technology, it cannot be obsoleted. It is cost competitive with the original device and is available in a wide variety of packaging options in production quantities. Free yourself from the uncertain availability and history of aftermarket devices with a new, improved, economical alternative.

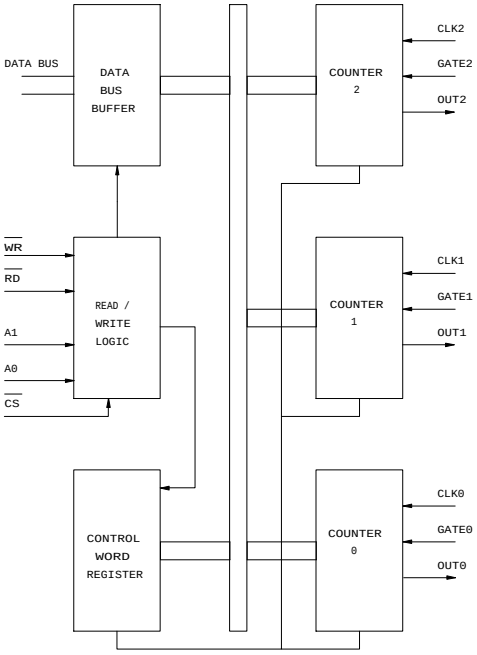


Figure 2 - 82C54 Block Diagram

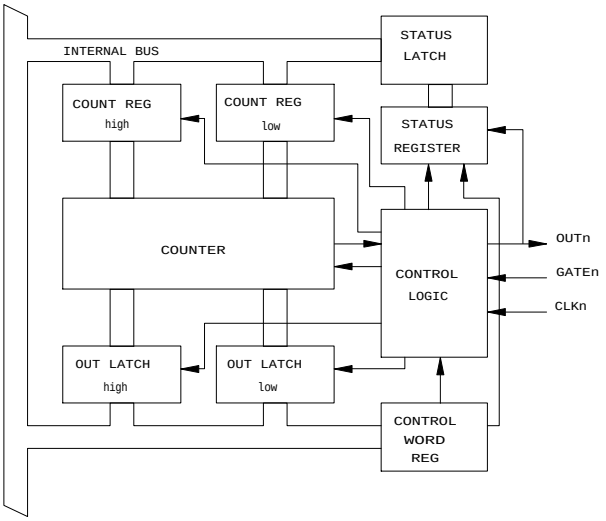


Figure 3 - 82C54 Counter Internal Block Diagram

OVERVIEW

As shown in Figure 2, the 82C54 is composed of three identical, independent counter blocks, a control register and bus interface logic .

The bus interface logic, consisting of the data bus buffer and Read/Write control logic is responsible for communications with the host system. This interface is compatible with most microprocessor and microcontroller architectures, particularly those from Intel.

The Control register is used to set the mode of each of the counters as well as some device level bus interface options.

The counters each consist of a block as illustrated in Figure 2. The counter blocks contain the counter as well as a number of data registers. These include the Count Value Register, Output Latch Register and Status Register.

The Count Value Register holds the count programmed by the user which is loaded into the counter when enabled. The Output Latch is used to latch the instantaneous count value in order to read the current count value without disturbing the counter operation. The status register is used to read back the current operating mode and status of the counter.

The device appears to the host system as four memory or I/O port addresses, controlled by address lines A0 and A1. The four ports consist of the Control Register, Counter 0, Counter 1 and Counter 2 Ports.

The control register port serves two functions. When written to, it controls the mode of the device and counters. When read from, it contains status information on the counter selected.

The Counter ports are used to write data into the count value register and read data latched into the Output Latch registers.

While the counters are 16 bits in length, the 8254 data bus is only 8 bits wide, requiring all counter data transfers to take place in two sequential read or write operations. The lower or least significant byte (LSB) is always transferred first.

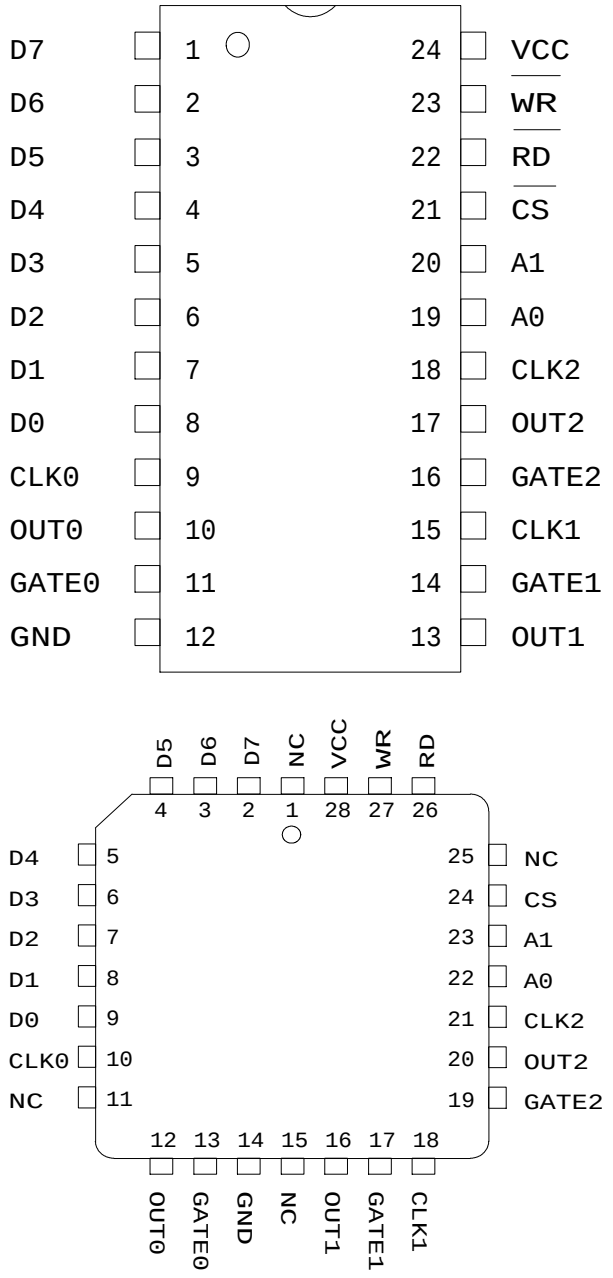


Figure 4 Pinouts of DIP24/SOIC24 and PLCC28 Packages

A0	A1	Register
0	0	Counter 0
1	0	Counter 1
0	1	Counter 2
1	1	Control Register

Table 1. - Internal Register Addressing

PIN SIGNAL DESCRIPTIONS

Figure 4 shows the pinouts for the DIP-24 and PLCC package devices. Pinouts for the SOIC package are the same as the DIP-24.

The signals consist of:

VCC +5 Volt Power Supply

VSS 5 Volt return or ground

D0-7 Bi-directional tri-state 8 bit data bus.

A0-1 Register Address, Input
These lines select the internal register being written to or read from. Table 1 summarizes the internal registers and their respective addresses.

!RD Read Strobe - Input, Active low
When asserted by the system, the contents of the register addressed by A0,1 are placed on the data bus D0-7.

!WR Write Strobe - Input, Active Low
When asserted by the system, the data currently on the data bus is latched into the register being addressed by A0,1.

!CS Chip Select - Input, Active low
When asserted, the Chip select line allows reading and writing of data to the device. When de-asserted, the device ignores !RD and !WR signals.

CLK 0, 1, 2 Counter Clock Inputs
These line are clock inputs to the three internal counters.

GATE 0, 1,2 Counter Gate Inputs
These lines, depending on the individual counter mode selected may be used to enable and disable the counter depending on the state of the gate line.

OUT 0, 1,2 Counter Output Lines
These lines are the outputs of the three independent counters.

DETAILED DEVICE DESCRIPTION

BUS INTERFACE

The data bus buffer is an 8 bit, tri-state, bidirectional buffer used to transfer information between the host system and the device. These transfers are controlled by the Read/Write Logic Block.

Data may be written to or read from any of the four addressable ports of the device. The port to be written to or read from is controlled by the signals on A0 and A1 according to Table 1.

In order to read or write from the device, the Chip Select line (!CS) must be asserted (driven low). Read or write signals will be ignored as long as the Chip Select Line (!CS) is de-asserted (high).

As illustrated in Figure 5, when data is to be written to one of the four device ports, the Write line (!WR) and Chip Select, (!CS) must be brought low to transfer the data into the device. When data is read from one of the four ports, the Read line (!RD) and the Chip Select line (!CS) must both be brought low to place data on the bus.

CONTROL REGISTER

The Control Register programs a variety of functions including:

Counter Mode for each counter,
BCD or Binary Counting,
Latching the count value for each counter,
Counter data programming sequence and
What data is to be Read Back

The control register is write only via the control port address. Control data may not be read back. Status information is read from the Control port address. The selected counter and its status may be selected by use of the appropriate readback command.

COUNTER BLOCKS

Since all three counters are identical in operation, only one will be described. Each counter is fully independent, having its own clock source input, hardware gate input and output. Each counter may be operating in different modes simultaneously.

The core of each counter block is a 16 bit presettable synchronus down counter. In all modes, the counter is loaded with a count value loaded by the user and will count to zero on application of a hardware or software gate then reload the counter. The various modes are variations of the gating source and action of the output when the counter reaches zero or its Terminal Count (TC).

The counter value programmed by the user is stored in the Count Value Register. This register is accessed by writing to the counter address port and is loaded 8 bits at a time. This value continues to be reloaded into the counter every time the counter reaches TC until changed by writing a new value to the counter port address.

The Output Latch Register normally follows the counter when it is active. If a counter latch command is received for that counter, the Output Latch Register latches or freezes the current counter value which may then be read by the host system at the counter port address. The counter continues counting undisturbed when a latch command is received. The Output Latch will continue to hold the last value latched until read by the host system, and will only then resume following the counter value.

The status register is a latch that takes a snapshot of the current counter mode and status when a status readback command is received. The status register may then be read back at the control port address.

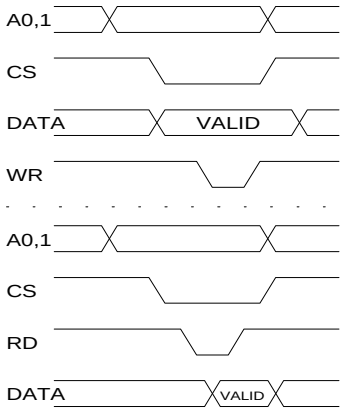


Figure 5 - Bus Read / Write Control Signal Timing

DEVICE MODES

The CTS8254 provides six different counter modes of operation. These modes are differentiated by the action of the counter when it reaches zero, or its Terminal Count (TC) and the action of the Gate line of the counter.

As mentioned before, all counters are down counters only, starting with the value programmed into the Count Value Register and counting down until the counter reaches zero.

The following definitions apply to the operation of all counter modes.

Clock Pulse
All three counters consider one count or clock pulse of the clock input to be a rising edge, followed by a falling edge.

Trigger
A trigger on the gate input of the counter is defined as a rising edge on the Gate Input

Counter Load
The counter is loaded when data is transferred from the Count Value Register into the counter.

COUNTER MODE 0 - INTERRUPT ON TERMINAL COUNT

Mode 0 is normally used for event counting. The output is initially low after the control word is written to the counter and remains low until the counter reaches terminal count (TC).

The counter will count as long as the Gate Input is asserted (High) and is stopped for as long as the Gate input is de-asserted.

After a control word and counter data (N) are written to the Count Value Register , the counter will be loaded on the next Clock Pulse and the counter will begin counting down from the count value on the next clock pulse. The output will go high on N+1 clock pulses after the count is written as illustrated in Figure 6.

The counter may be reloaded with a new count value anytime prior to reaching TC in order to extend the count. During a two-byte counter value load, the counter is disabled when the first byte is written and loads the counter with the new count value on the first clock pulse following the second data byte.

If the Gate is deasserted during the programming of the counter mode and count value, the counter is still loaded on the first clock pulse following the data write. The output will remain low until the Gate line is asserted and go high N clock pulses later. In this case, no clock pulse may be necessary to load the counter as this may have been done much earlier at the time of the count value write. The Gate line has no direct control of the Output of the counter in this mode. It strictly enables and disable the counter.

MODE 1 - HARDWARE RETRIGGERABLE ONE-SHOT

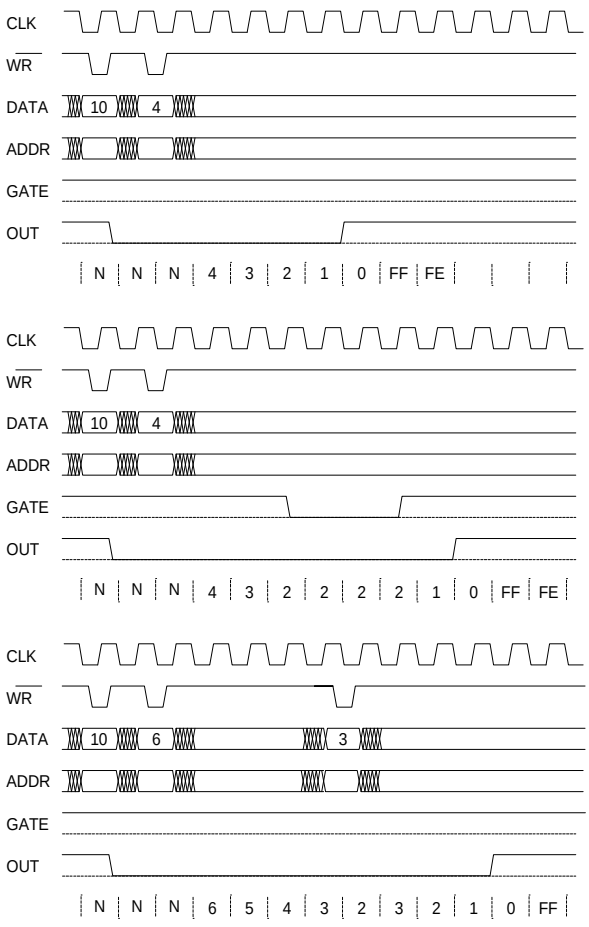


FIGURE 6 - COUNTER MODE 0 REPRESENTATIVE

In this mode the Output is initially high. When triggered by assertion of the counter Gate line, the Output goes low on the clock pulse following the trigger. The counter will begin counting until TC is reached and the Output will go high and remain high until the application of a new trigger edge. The counter is not sensitive to the level of the gate line and will only be triggered by a rising edge on the Gate line as shown in Figure 7.

After the counter mode and Count Values are written, the counter is automatically armed on the clock pulse following the last count data write. The output duration will therefore be N clock pulses in duration.
The counter may be retriggered by application of a additional trigger edge(s) prior to TC. The counter will be reloaded with the last count value and continue counting for each trigger pulse received prior to reaching TC.

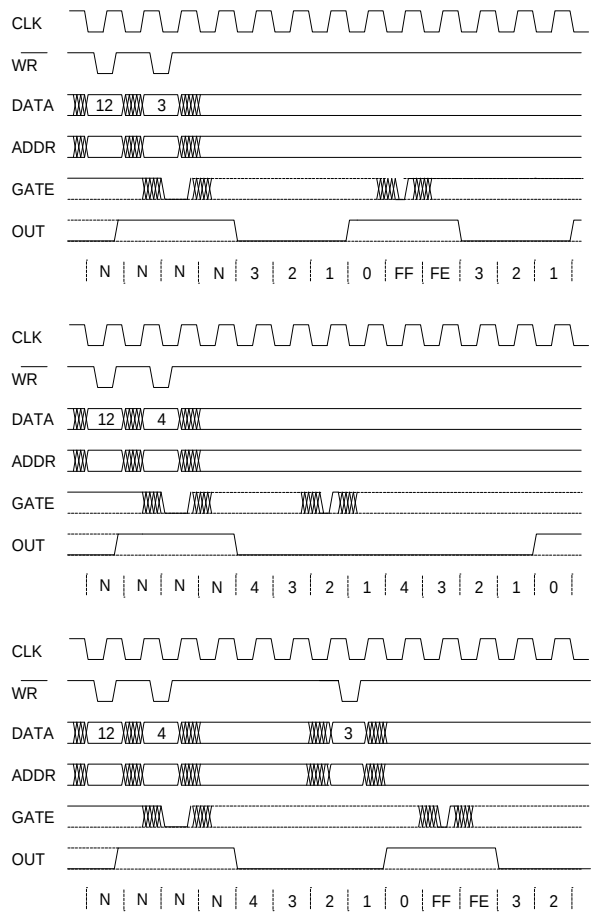


FIGURE 7 - COUNTER MODE 1 REPRESENTATIVE

If a new count is written to the Count Value Register prior to reaching TC, the current one shot is only affected if the counter is retriggered during the count, otherwise the counter will reach TC with the last count value and reload the new count on the next trigger.

MODE 2 - RATE GENERATOR

This mode is most often used as a frequency divider. The Output of the counter is initially high. As long as the Gate line is asserted the output will remain high until TC+1 is reached upon which the output will go low for one clock pulse. The Output then goes high once again, the counter is reloaded with the Count Value and counting begins again automatically. The resulting output is a pulse train of N-1 counts high and 1 count low on the output as shown in Figure 8.

As long as the Gate Line is asserted, the counter will be loaded with the value in the Count Value Register on the first clock pulse following the last count data write, allowing software synchronization.

During counting, the count may be suspended or inhibited by de-asserting the Gate line. If the gate line goes low while the output is low, the output will immediately be set high. This allows for external or hardware synchronization.

When the Gate line is re-asserted the counter will be reloaded from the Count Value register and resume counting, with the first low output occuring N clock pulses later.

If a new value is written to the Count Value Register during a count, it does not affect the current counting sequence unless a new trigger signal is received prior to TC. On reaching TC or receipt of a new trigger prior to TC the counter will be reloaded with the new Count Value.

MODE 3 - SQUARE WAVE MODE

Mode 3 is similar to Mode 2 in that the output produced is a periodic waveform as long as the Gate line is asserted. The difference is in the duty cycle

produced. Instead of an output which goes low every N counts, the output will approximate a square wave by counting down half the count before changing state as shown in Figure 9.

Initially the Output is high. While the Gate line is asserted, the counter is loaded with the value in the Count Value Register on the first clock pulse following the last counter data write and the counter begins counting. When the counter reaches half the count value ((N+1)/2 for ODD counts, N/2 for Even Counts) the counter Output goes low until the counter reaches TC. The counter will then be reloaded from the Count Value Register and will begin counting again. This produces an output that approximates a square wave of N clock pulses duration with a duty cycle off 1 clock pulse for odd counts.

If the Gate line is de-asserted prior to the counter reaching TC, counting is suspended. If the Gate line is de-asserted while the output is low, the output will immediately go high. When the Gate line is re-asserted, the counter reloads form the count value register and begins counting from N again.

If a new count is written to the count value register during a count it will only be loaded into the counter after it reaches TC or if a new trigger is received prior to reaching TC.

MODE 4 - SOFTWARE TRIGGERED STROBE

This mode produces a one clock pulse wide strobe N+1 clock pulses after the last count value data write, allowing the counter to produce a software synchronized delay. As shown in Figure 10, the

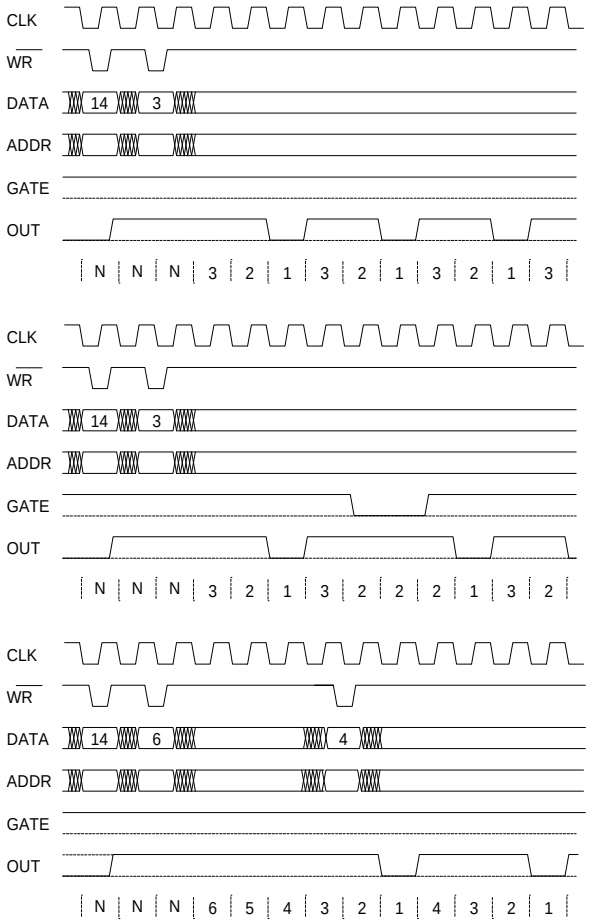


FIGURE 8 - COUNTER MODE 2 REPRESENTATIVE

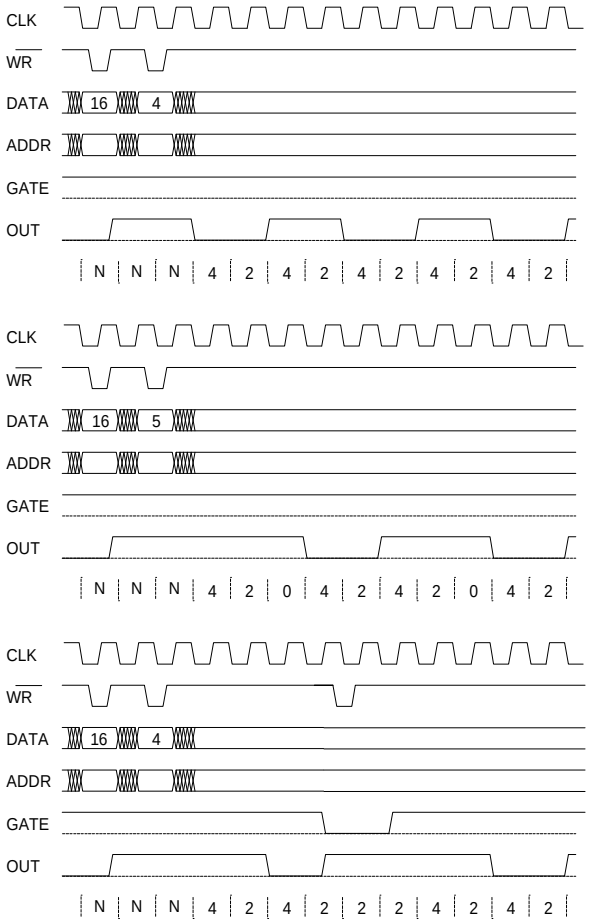


FIGURE 9 - MODE 3 REPRESENTATIVE WAVEFORMS

output is initially high. If the Gate line is asserted, the counter is loaded on the clock pulse following the last count value data write and begins counting down. When TC is reached the Output goes low for one clock pulse.

At TC the counter will go high again and await the next count value write. If a new value is written to the Count Value Register prior to TC it will be loaded on the next clock pulse into the counter and the count will continue from the new value. This allows "retriggering" of the counter by software.

If the Gate line is de-asserted during counting, the counter will be inhibited until the Gate line is re-asserted.

MODE 5 - HARDWARE TRIGGERED STROBE

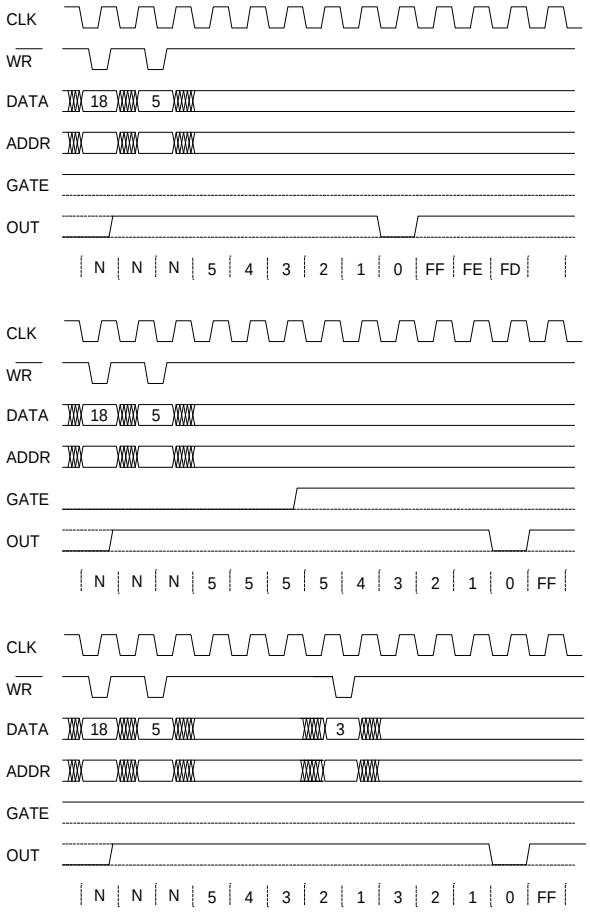


FIGURE 10 - MODE 4 REPRESENTATIVE WAVEFORMS

Mode 5 is similar to Mode 4 except the count is hardware rather than software triggered. The output is initially high. The counter is not loaded with the count value until the first clock pulse following a trigger on the counter gate line. The counter then counts down to TC and the output goes low for one count N+1 clock pulses following the trigger.

Application of a new trigger prior to reaching TC results in the counter being reloaded from the count value register and counting begins at N again. This makes the delay hardware retriggerable.

If a new count is loaded into the count value register while the counter is counting, the new value will not be loaded until the TC is reached or if a new trigger is received prior to reaching TC.

BEHAVIOR COMMON TO ALL MODES

Programming

When a control word is written to a counter, the Output is set and all control logic is reset. No active clock is required for this initialization.

Gate Signal

In modes 0 and 4, the gate is level sensitive and is sampled on the rising edge of the Clock signal.

In modes 1 and 5, the gate is rising edge sensitive. An internal flip-flop is set on the rising edge of the gate which is sampled and cleared on the rising edge of the next clock pulse. The gate need not stay asserted until the next clock pulse.

In modes 2 and 3 the gate is both level and edge sensitive.

Counter Behavior

New counts are loaded from the Count Value Register and count values are decremented on the falling edge of the Clock pulse.

The largest initial count is zero, representing 2^{16} for binary counting and 10^4 for BCD counting.

The counter does not stop counting in Modes 0,1,4 and

5 when it reaches zero. It wraps around to FFFF or 9999 and continues to count. In Modes 2 and 3 the counts are periodic and the counters are automatically reloaded with the count value.

ERRATA

A Gate Transition should not occur less than 1 clock cycle prior to TC

In modes 2 and 3, the 8254 (and 82C54) uses "look ahead" logic to precondition OUT to go low on the falling edge of the CLK input upon terminal count. Without this look ahead feature, the 8254 would not have time to resolve its internal logic at the same time OUT is to go low upon reaching terminal count. Monitoring the count value in software, before disabling counting via the GATE, is usually sufficient to prevent this combination of events.

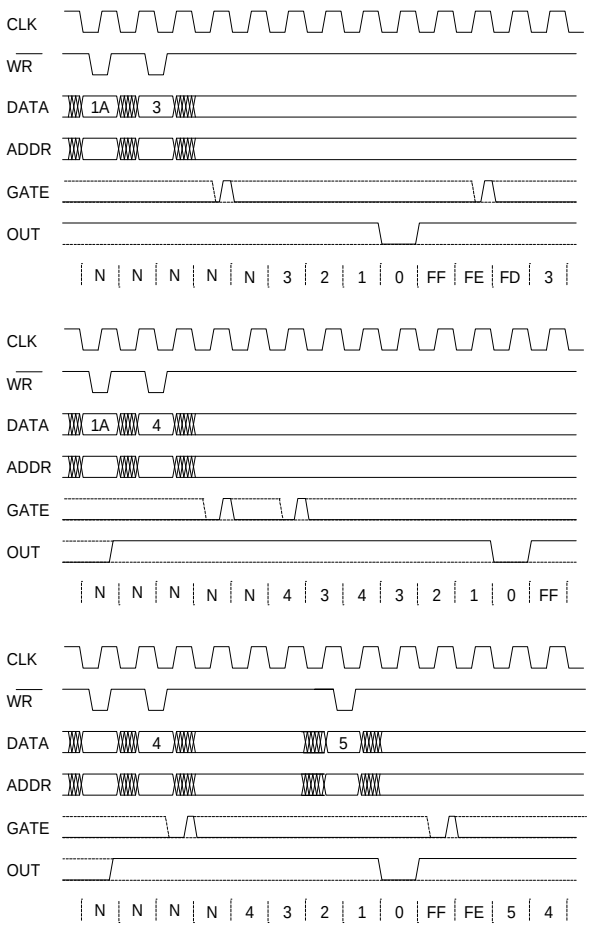


FIGURE 11 - MODE 5 REPRESENTATIVE WAVEFORMS

Power-Up State

At power up, the default condition of the 8254 is undefined. The mode, count value, and state of the OUT pins are undefined or random. Each counter must be initialized via software before it can be used.

In Modes 2 and 3, if a CLK source other than the system clock is used, GATE should be pulsed immediately following !WR

The GATE input, when low in MODE 2, will force the output high. When the GATE input goes high, the counter will start from the initial count. The GATE can be used to synchronize the counter. In MODE 3, the output will remain high until 1/2 the count has been completed and go low for the other half. In both cases the CLK input is used as the pulse period. If the system clock is not the 8254 CLK input, you must pulse GATE following WR# of a new count value to synchronize the loading of the new count.

The CLK cannot be used to start and stop counting.

This can cause the counter to lock up and require reprogramming the 8254 before further operation is possible. Turning the CLK on or off usually results in noise spikes. These spikes appear to the 8254 as CLK input pulses which violate TPWH and TPWL timing. The internal counter logic is unable to resolve the high or low state of the CLK input and locks up.

In Mode 2, when the counter is programmed with a count of 1 OUT never goes low.

This is due to the internal look ahead logic and the reloading of the count in Mode 2. As described in the data sheet, the count is loaded on the falling edge of the CLK input. One CLK input pulse prior to terminal count, the 8254 internal look ahead logic conditions OUT to go low on the falling edge of the next CLK input pulse. The terminal count CLK input pulse falling edge should cause the OUT to go low immediately but is overridden by the count reload

occurring on the same CLK input falling edge. This conflict results in OUT remaining high continuously. Also, a count of 1 in Mode 2 is not appropriate (or useful). A count of 1 in Mode 2, Rate Generator Mode, would result in a rate of 1. In theory, this would be a square wave with a period the same as the CLK input. Should the user require such an output, Mode 3, Square Wave Mode, is the appropriate choice. Table 2 gives the minimum and maximum counts for each Mode:

The original value programmed into the counter cannot be read

The Count register (low and high) cannot be read. The Output Latch (low and high) are the only things which can be read. In other words, only the value of a counter can be read, not the initial count programmed into the device.

DEVICE PROGRAMMING

POWER-UP STATE

The power-up state of the CTS82C54 counter and mode registers is undefined. The device must be programmed prior to use. Unused counters may be left unprogrammed.

PROGRAMMING OVERVIEW

In general, all programming operations are performed by writing a control word to the control register followed by either writing data to one of the counter count value registers or by reading back status or count data.

WRITE OPERATIONS

Programming the CTS82C54 is very straightforward and flexible. Since the control register and counter data registers are addressed separately, once the counter modes are written, the counter data may be updated without affecting the mode programming. Only two programming conventions need to be remembered.

1 A control word must be written for a counter prior to writing data to a counter's count value register.

2 The count value must conform to the data sequence format specified in the control word. These formats include: LSB (least significant byte) followed by MSB (most significant byte), MSB only or LSB only.

Mode	Min Count	Max Count
0	1	0
1	1	0
2	2	0
3	3	0
4	1	0
5	1	0

TABLE 2 - MINIMUN AND MAXIMUM COUNTS

The control word format is shown in Table 3.

Several of the possible programming sequences are illustrated in Table 4.

READ OPERATIONS

The CTS82C54 allows reading the current contents of the counter without disturbing the count as well as reading the current status of each counter including current operating mode and state of the output. All counter read-back is performed through the counter data ports. Reads form the counter mode register are not defined.

Counter Readback

The CTS82C54 provide three different methods of reading back the value of a selected counter. The data read back conforms to the same programmed sequence as writing data in that the data may be read back LSB then MSB, LSB only or MSB only.

The counter readback methods include:

1 A simple read from the counter addressed by A1,0. This requires that the counter be inhibited by deassertion of the gate line during the read so a read is not performed during a counter transistion. It is not acceptable to inhibit the

b7	b6	b5	b4	b3	b2	b1	b0
SC1	SC0	RW1	RW0	M2	M1	M0	BCD

SC1, 0 - Counter Select Bits

SC1	SC0	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Read-Back Commmand - See Table 6

RW1, 0 - Read / Write Data Format

RW1	RW0	
0	0	Counter Latch Command - See Table 5
0	1	Read/Write LSB only
1	0	Read/Write MSB only
1	1	Read/Write LSB then MSB

M2-0 - Counter Mode

M2	M1	M0	
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

BCD:

0	Binary Counting
1	BCD Counting

TABLE 3 CONTROL WORD FORMAT

RW1,0 = 11 - Two Byte LSB then MSB Sequence		
	A1	**A0**
Control Word - Counter 0	1	1
Counter 0 LSB	0	0
Counter 0 MSB	0	0
Control Word - Counter 1	1	1
Counter 1 LSB	0	1
Counter 1 MSB	0	1
Control Word - Counter 2	1	1
Counter 2 LSB	1	0
Counter 2 MSB	1	0
Control Word - Counter 0	1	1
Control Word - Counter 1	1	1
Control Word - Counter 2	1	1
Counter 2 LSB	1	0
Counter 1 LSB	0	1
Counter 0 LSB	0	0
Counter 0 MSB	0	0
Counter 1 MSB	0	1
Counter 2 MSB	1	0
Control Word - Counter	1	1
Control Word - Counter	1	1
Control Word - Counter	1	1
Counter 0 LSB	0	0
Counter 0 MSB	0	0
Counter 1 LSB	0	1
Counter 1 MSB	0	1
Counter 2 LSB	1	0
Counter 2 MSB	1	0

TABLE 4 EXAMPLE PROGRAMMING SEQUENCES

counter by stopping the clock input.

2 Latching the counter data on-the-fly using a counter latch command written to the control register. This latches the current count into the counter output latches without disturbing the counter and may be done without inhibiting the counter. The output latches retain this count value until read. Once read the output latches resume following the counter value.

Once a counter has been latched, it will ignore subsequent latch commands until read. The counter latch command format is shown in Table 5.

Since the write and read commands are governed by the data format specified in the counter mode,

counter data reads and writes may be interleaved as long as the data format is observed. The following sequences are all valid:

1 Counter Data format is LSB then MSB
- Read counter n LSB
- Write counter n LSB
- Read counter n MSB
- Write counter n MSB

2 Counter Data format is LSB Only
- Read counter n LSB
- Write counter n LSB
- Read counter x LSB
- Write counter x LSB

The third counter read method allows data to be read back from both the counter output latches, and counter status information. This is through writing a Read-Back command to the counter mode register.

Read-Back Command

The Read-Back command may latch any or all of the timers simultaneously depending on the setting of the counter bits in the readback command as shown in Table 6.

The Read-Back command may also be used to latch counter status information for any one or all counters. It may also be used to latch the counter and status information simultaneously.

The Read-Back command format is shown in Table 6. If bits 4 and 5 of the Read-Back control word are set to 0 both status and counter values will be latched. Several representative Read-Back commands are shown in Table 4.

b7	b6	b5	b4	b3	b2	b1	b0
SC1	SC2	0	0	X	X	X	X
0	0	Latch Counter 0					
0	1	Latch Counter 1					
1	0	Latch Counter 2					
1	1	Read-Back Command - See Table 6					

TABLE 5 COUNTER LATCH COMMAND

b7	b6	b5	b4	b3	b2	b1	b0
1	1	CNT	STAT	C2	C1	C0	0
CNT	**STAT**	**Cn**					
0	1		Latch Selected Counters				
1	0		Latch Status of Selected Counters				
1	1		Latch Status and Count of selected counters				
		1	Select Counter Cn				
		0	Deselect Counter Cn				

TABLE 6 READ-BACK COMMAND FORMAT

As shown in Table 7 the status byte contains information on the selected counter mode and the output state at the time the counter status was latched.

Counter data and status data remains latched until read, when it resumes following the counter value and status. Subsequent Read-Back commands without an interveining reads are ignored.

When both the counter status and counter value bits are selected, the first byte read back from the couter will be the counter status byte. The next one or two byte sequence comforms to the programmed data format of LSB only, MSB only or LSB the MSB.

b7	b6	b5	b4	b3	b2	b1	b0
OUT	NULL	RW1	RW0	M2	M1	M0	BCD
OUT							
0	Counter output = 0						
1	Counter Output = 1						
NULL							
0	Valid Count Available for Read-Back						
1	Count Value Invalid						
b5-0	per mode program specifications - see Table 3						

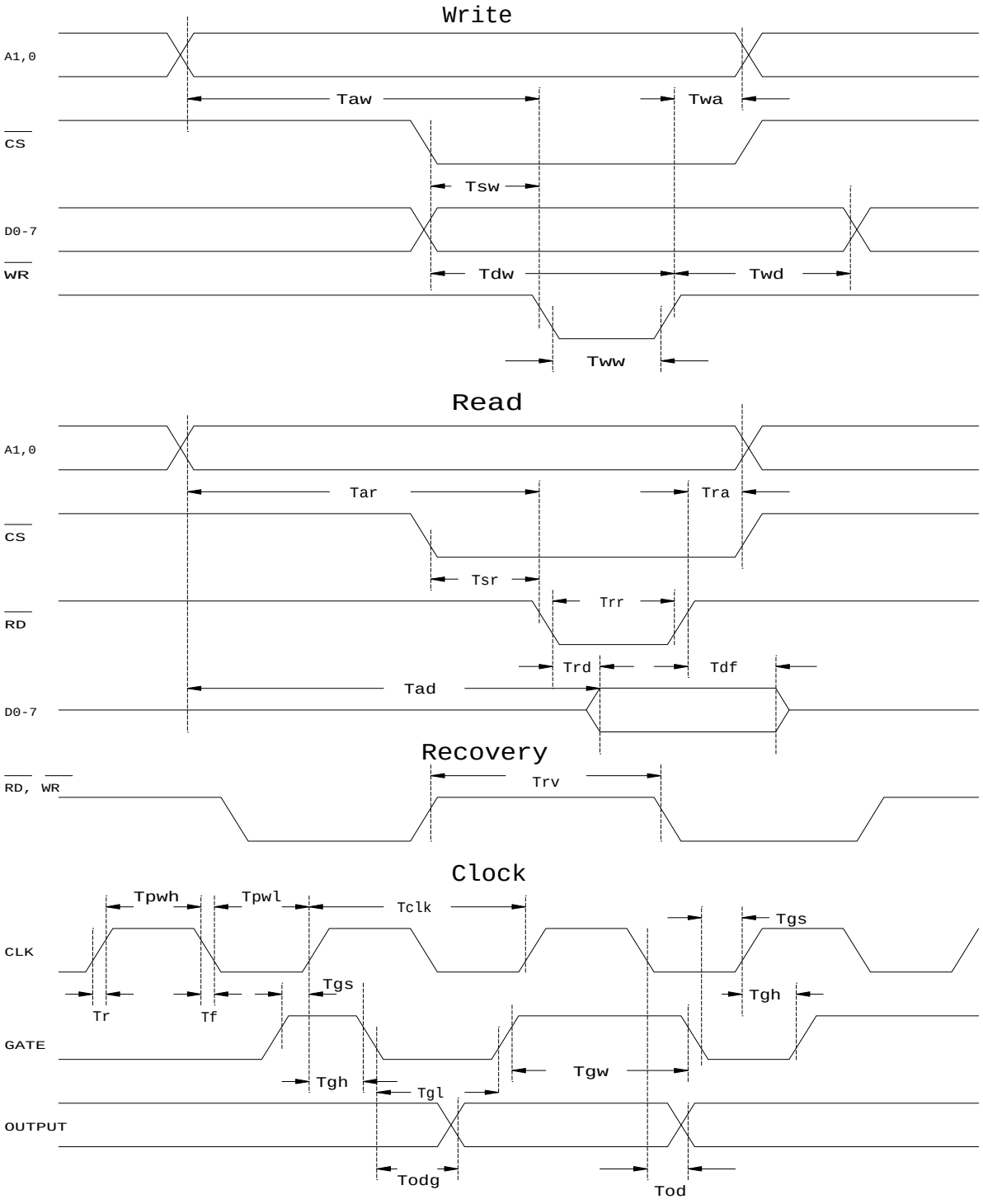
TABLE 7 STATUS BYTE FORMAT

Supply Voltage	+8.0 Volts
Operating Voltage Range	+4 - +7 Volts
Input Voltage	GND-0.2V to +8.5V
Output Voltage	GND-0.5V to VCC+0.5V
Storage Temperature Range	-65C to +150C
Operating Temperature	-40C to 85C
Maximum Power Dissipation	TBD

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITION
VIH	Logical 1 Input Voltage	2.0		V	
VIL	Logical 0 Input Voltage		0.8	V	
VOH	Logical 1 Output Voltage	3.0		V	
VOL	Logical 0 Output Voltage		0.4	V	
IIL	Input Leakage Current		TBD	uA	
IO	Output Leakage Current		TBD	uA	
ICCSB	Standby Device Current		TBD	uA	
ICCOP	Operating Device Current		TBD	mA	

DC ELECTRICAL CHARACTERISTICS



AC TIMING WAVEFORMS

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
Tar	Address Stable before RD	TBD			
Tsr	CS stable before RD	TBD			
Tra	Address Hold Time After RD	TBD			
Trr	RD Pulse Width	TBD			
Trd	Data Delay from RD	TBD			
Tad	Data Delay from Address	TBD			
Tdf	RD to Data Floating	TBD			
Trv	Command Recovery Time	TBD			
Taw	Address Stable before WR	TBD			
Tsw	CS Stable before WR	TBD			
Twa	Address Hold Time	TBD			
Tww	WR Pulse Width	TBD			
Tdw	Data Setup Time before WR	TBD			
Twd	Data Hold Time after WR	TBD			
Trv	Command Recovery Time	TBD			
Tclk	Clock Period	TBD			
Tpwh	High Clock Pulse Width	TBD			
Tpwl	Low CLock Pulse Width	TBD			
Tr	Clock Rise Time	TBD			
Tf	Clock Fall Time	TBD			
Tgw	Gate Width High	TBD			
Tgl	Gate Width Low	TBD			
Tgs	Gate Setup Time to Clock	TBD			
Tgh	Gate Hold Time after Clock	TBD			
Tod	Output Delay from Clock	TBD			
Todg	Output Delay from Gate	TBD			

AC TIMING CHARACTERISTICS

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