Register Map for the PCI-DIO48H and PCI-DIO96H

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Register Description

Control & Data Registers

BADR2 is an eight-bit data bus for reading, writing and control of the emulated 8255 chips operating in mode 0. Refer to Table 1 for register offsets.

Table 1. I/O Registers - PCI-DIO48H and PCI-DIO96H

Register	Read Function	Write Function
BADR2 + 0	FIRSTPORTA Data	FIRSTPORTA Data
BADR2 + 1	FIRSTPORTB Data	FIRSTPORTB Data
BADR2 + 2	FIRSTPORTC Data	FIRSTPORTC Data
BADR2 + 3	No Register Readback	FIRSTPORT Configuration Register
BADR2 + 4	SECONDPORTA Data	SECONDPORTA Data
BADR2 + 5	SECONDPORTB Data	SECONDPORTB Data
BADR2 + 6	SECONDPORTC Data	SECONDPORTC Data
BADR2 + 7	No Register Readback	SECONDPORT Configuration Register
The following addresses are for the PCI-DIO96H only:		
BADR2 + 8	THIRDPORTA Data	THIRDPORTA Data
BADR2 + 9	THIRDPORTB Data	THIRDPORTB Data
BADR2 + A	THIRDPORTC Data	THIRDPORTC Data
BADR2 + B	No Register Readback	THIRDPORT Configuration Register
BADR2 + C	FOURTHPORTA Data	FOURTHPORTA Data
BADR2 + D	FOURTHPORTB Data	FOURTHPORTB Data
BADR2 + E	FOURTHPORTC Data	FOURTHPORTC Data
BADR2 + F	No Register Readback	FOURTHPORT Configuration Register

The boards are designed to operate in input/output mode only (8255 mode 0). Strobed input/output (mode 1) or bi-directional bus (mode 2) are not supported.

The following information explains mode 0 operation. Upon power-up, the board is reset and defaults to the input mode. No further programming is needed to use the 24 lines as inputs.

FIRSTPORT Configuration and Data

FIRSTPORTA Data

BADR2 + 0h

Read/Write

7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0

FIRSTPORTB Data

BADR2 + 1h

Read/Write

7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0

FIRSTPORTC Data

BADR2 + 2h

Read/Write

7	6	5	4	3	2	1	0
C7	C6	C5	C4	C3	C2	C1	C0
CH3	CH2	CH1	CH0	CL3	CL2	CL1`	CL0

FIRSTPORT Configuration Register

BADR2 + 3h

Write

7	6	5	4	3	2	1	0
-	-	-	D4	D3	-	D1	D0

This register is used to configure FIRSTPORT as either input or output. Refer to the following section and Table 2 for information about mode 0 configuration.

8255 Emulation - mode 0 configuration

Output ports

In mode 0 configuration, each port can be configured for output, holding the data written to them. For example, to set all three of the FIRSTPORT ports (A, B, and C) to output mode, write the value 0h to BADR2 + 3 (refer to Table 2). To read the current state of an output port's bits, simply read the address of that port.

Input ports

In mode 0 configuration, ports can be configured as inputs, reading the state of the inputs lines. For example, to set all FIRSTPORT ports to the input mode, write the value 1Bh to BADR2 + 3.

In Table 2, **CU** refers to port C upper nibble, and **CL** refers to port C lower nibble.

Table 2. DIO Port Configurations/Per Group

Programming Codes				Values		DIO Port			
D4	**D3**	**D1**	**D0**	**Hex**	**Dec**	**A**	**B**	**CU**	**CL**
0	0	0	0	0	0	OUT	OUT	OUT	OUT
0	0	0	1	1	1	OUT	OUT	OUT	IN
0	0	1	0	2	2	OUT	IN	OUT	OUT
0	0	1	1	3	3	OUT	IN	OUT	IN
0	1	0	0	8	8	OUT	OUT	IN	OUT
0	1	0	1	9	9	OUT	OUT	IN	IN
0	1	1	0	A	10	OUT	IN	IN	OUT
0	1	1	1	B	11	OUT	IN	IN	IN
1	0	0	0	10	16	IN	OUT	OUT	OUT
1	0	0	1	11	17	IN	OUT	OUT	IN
1	0	1	0	12	18	IN	IN	OUT	OUT
1	0	1	1	13	19	IN	IN	OUT	IN
1	1	0	0	18	24	IN	OUT	IN	OUT
1	1	0	1	19	25	IN	OUT	IN	IN
1	1	1	0	1A	26	IN	IN	IN	OUT
1	1	1	1	1B	27	IN	IN	IN	IN

SECONDPORT Configuration and Data

SECONDPORTA Data

BADR2 + 4h

Read/ Write

7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0

SECONDPORTB Data

BADR2 + 5h

Read/ Write

7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0

SECONDPORTB Data

BADR2 + 6h

Read/ Write

7	6	5	4	3	2	1	0
C7	C6	C5	C4	C3	C2	C1	C0
CH3	CH2	CH1	CH0	CL3	CL2	CL1	CL0

SECONDPORT Configuration Register

BADR2 + 7h

Write

7	6	5	4	3	2	1	0
-	-	-	D4	D3	-	D1	D0

Refer to "8255 Emulation - mode 0 configuration" and to Table 2 for information on this register.

THIRDPORT Configuration and Data - PCI-DIO96H Only

THIRDPORTA Data

BADR2 + 8h

Read/Write

7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0

THIRDPORTB Data

BADR2 + 9h

Read/Write

7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0

THIRDPORTC Data

BADR2 + Ah

Read/Write

7	6	5	4	3	2	1	0
C7	C6	C5	C4	C3	C2	C1	C0
CH3	CH2	CH1	CH0	CL3	CL2	CL1	CL0

THIRDPORT Configuration Register

BADR2 + Bh

Write

7	6	5	4	3	2	1	0
-	-	-	D4	D3	-	D1	D0

Refer to the "8255 Emulation - mode 0 configuration" section and Table 2 for information on this register.

FOURTHPORT Configuration and Data - PCI-DIO96H Only

FOURTHPORTA Data

BADR2 + Ch

Read/ Write

7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0

FOURTHPORTB Data

BADR2 + Dh

Read/ Write

7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0

FOURTHPORTC Data

BADR2 + Eh

Read/ Write

7	6	5	4	3	2	1	0
C7	C6	C5	C4	C3	C2	C1	C0
CH3	CH2	CH1	CH0	CL3	CL2	CL1	CL0

FOURTHPORT Configuration Register

BADR2 + Fh

Write

7	6	5	4	3	2	1	0
-	-	-	D4	D3	-	D1	D0

Refer to the "8255 Emulation - mode 0 configuration" section and Table 2 on page 2 for information on this register.

Measurement Computing Corporation
16 Commerce Boulevard,
Middleboro, Massachusetts 02346
(508) 946-5100
Fax: (508) 946-9500
E-mail: info@measurementcomputing.com
www.measurementcomputing.com