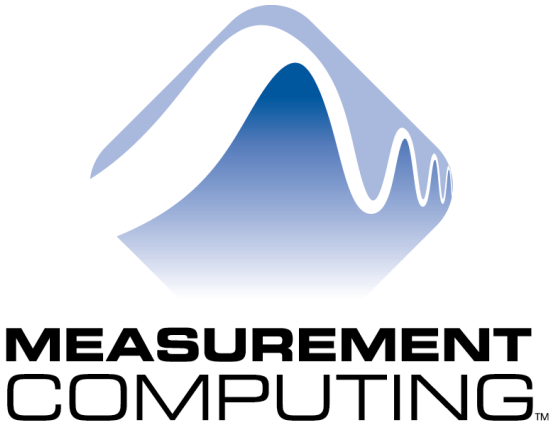
Register Map for the PCIe-DIO96H



Document Revision 1.0, June, 2008

Register Description

Control & Data Registers

BADR2 is an eight-bit data bus for reading, writing and control of the emulated 8255 chips operating in mode 0. Refer to Table 1 for register offsets.

Table 1. I/O Registers – PCIe-DIO96H

Register	Read Function	Write Function
BADR2 + 0	FIRSTPORTA Data	FIRSTPORTA Data
BADR2 + 1	FIRSTPORTB Data	FIRSTPORTB Data
BADR2 + 2	FIRSTPORTC Data	FIRSTPORTC Data
BADR2 + 3	No Register Readback	FIRSTPORT Configuration Register
BADR2 + 4	SECONDPORTA Data	SECONDPORTA Data
BADR2 + 5	SECONDPORTB Data	SECONDPORTB Data
BADR2 + 6	SECONDPORTC Data	SECONDPORTC Data
BADR2 + 7	No Register Readback	SECONDPORT Configuration Register
BADR2 + 8	THIRDPORTA Data	THIRDPORTA Data
BADR2 + 9	THIRDPORTB Data	THIRDPORTB Data
BADR2 + A	THIRDPORTC Data	THIRDPORTC Data
BADR2 + B	No Register Readback	THIRDPORT Configuration Register
BADR2 + C	FOURTHPORTA Data	FOURTHPORTA Data
BADR2 + D	FOURTHPORTB Data	FOURTHPORTB Data
BADR2 + E	FOURTHPORTC Data	FOURTHPORTC Data
BADR2 + F	No Register Readback	FOURTHPORT Configuration Register
EEPROM DIP Switch		
BADR3 + 0	I2C Status	I2C Timeout
BADR3 + 8	I2C Data	I2C Data
BADR3 + C	I2C Control	I2C Control

Table 2. Memory Registers – PCIe-DIO96H

Register	Read Function	Write Function
BADR0 + 54	GPIO Data and Control	GPIO Data and Control

The board is designed to operate in input/output mode only (8255 mode 0). Strobed input/output (mode 1) or bi-directional bus (mode 2) are not supported.

The following information explains mode 0 operation. Upon power-up, the board is reset and defaults to the input mode. No further programming is needed to use the 96 lines as inputs.

FIRSTPORT Configuration and Data

FIRSTPORTA Data

BADR2 + 0h

Read/Write

7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0

FIRSTPORTB Data

BADR2 + 1h

Read/Write

7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0

FIRSTPORTC Data

BADR2 + 2h

Read/Write

7	6	5	4	3	2	1	0
C7	C6	C5	C4	C3	C2	C1	C0
CH3	CH2	CH1	CH0	CL3	CL2	CL1`	CL0

FIRSTPORT Configuration Register

BADR2 + 3h

Write

7	6	5	4	3	2	1	0
-	-	-	D4	D3	-	D1	D0

This register is used to configure FIRSTPORT as either input or output. Refer to the following section and Table 2 for information about mode 0 configuration.

8255 Emulation - mode 0 configuration

Output ports

In mode 0 configuration, each port can be configured for output, holding the data written to them. For example, to set all three of the FIRSTPORT ports (A, B, and C) to output mode, write the value 0h to BADR2 + 3 (refer to Table 3). To read the current state of an output port's bits, simply read the address of that port.

Input ports

In mode 0 configuration, ports can be configured as inputs, reading the state of the inputs lines. For example, to set all FIRSTPORT ports to the input mode, write the value 1Bh to BADR2 + 3.

In Table 3, **CU** refers to port C upper nibble, and **CL** refers to port C lower nibble.

Table 3. DIO Port Configurations/Per Group

Programming Codes				Values		DIO Port			
D4	**D3**	**D1**	**D0**	**Hex**	**Dec**	**A**	**B**	**CU**	**CL**
0	0	0	0	0	0	OUT	OUT	OUT	OUT
0	0	0	1	1	1	OUT	OUT	OUT	IN
0	0	1	0	2	2	OUT	IN	OUT	OUT
0	0	1	1	3	3	OUT	IN	OUT	IN
0	1	0	0	8	8	OUT	OUT	IN	OUT
0	1	0	1	9	9	OUT	OUT	IN	IN
0	1	1	0	A	10	OUT	IN	IN	OUT
0	1	1	1	B	11	OUT	IN	IN	IN
1	0	0	0	10	16	IN	OUT	OUT	OUT
1	0	0	1	11	17	IN	OUT	OUT	IN
1	0	1	0	12	18	IN	IN	OUT	OUT
1	0	1	1	13	19	IN	IN	OUT	IN
1	1	0	0	18	24	IN	OUT	IN	OUT
1	1	0	1	19	25	IN	OUT	IN	IN
1	1	1	0	1A	26	IN	IN	IN	OUT
1	1	1	1	1B	27	IN	IN	IN	IN

SECONDPORT Configuration and Data

SECONDPORTA Data

BADR2 + 4h

Read/ Write

7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0

SECONDPORTB Data

BADR2 + 5h

Read/ Write

7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0

SECONDPORTC Data

BADR2 + 6h

Read/ Write

7	6	5	4	3	2	1	0
C7	C6	C5	C4	C3	C2	C1	C0
CH3	CH2	CH1	CH0	CL3	CL2	CL1	CL0

SECONDPORT Configuration Register

BADR2 + 7h

Write

7	6	5	4	3	2	1	0
-	-	-	D4	D3	-	D1	D0

Refer to "8255 Emulation - mode 0 configuration" and to Table 3 for information on this register.

THIRDPORT Configuration and Data

THIRDPORTA Data

BADR2 + 8h

Read/Write

7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0

THIRDPORTB Data

BADR2 + 9h

Read/Write

7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0

THIRDPORTC Data

BADR2 + Ah

Read/Write

7	6	5	4	3	2	1	0
C7	C6	C5	C4	C3	C2	C1	C0
CH3	CH2	CH1	CH0	CL3	CL2	CL1	CL0

THIRDPORT Configuration Register

BADR2 + Bh

Write

7	6	5	4	3	2	1	0
-	-	-	D4	D3	-	D1	D0

Refer to the "8255 Emulation - mode 0 configuration" section and Table 3 for information on this register.

FOURTHPORT Configuration and Data

FOURTHPORTA Data

BADR2 + Ch

Read/ Write

7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0

FOURTHPORTB Data

BADR2 + Dh

Read/ Write

7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0

FOURTHPORTC Data

BADR2 + Eh

Read/ Write

7	6	5	4	3	2	1	0
C7	C6	C5	C4	C3	C2	C1	C0
CH3	CH2	CH1	CH0	CL3	CL2	CL1	CL0

FOURTHPORT Configuration Register

BADR2 + Fh

Write

7	6	5	4	3	2	1	0
-	-	-	D4	D3	-	D1	D0

Refer to the "8255 Emulation - mode 0 configuration" section and Table 3 on page 2 for information on this register.

GPIO Data and Control – 5 V Present

BADR0 + 54h (Memory Mapped)

Read

31	30	29	28	27	26	25	24
-	-	-	-	-	5V PRSNT	I/O	-

5V PRSNT = 1, external power is connected; = 0, external power is not connected. I/O Bit 25 should always read 0 for input.

EEPROM DIP Switch PCI Registers

Each Read/Write should wait >100 microseconds before each access to allow ample time for I^2C bus transactions.

I2C Status

BADR3 + 0h

Read

7	6	5	4	3	2	1	0
STA7	STA6	STA5	STA4	STA3	STA2	STA1	STA0

Status of the I^2C Bus. Check after each Write to the Control Register; refer to PCA9564 datasheet for details on return codes.

I2C Data

BADR3 + 08h

Read/Write

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Read/Write EEPROM DIP Switch address, Data and Value. Write to the Control Register to update the I^2C bus or for read values.

I2C Control

BADR3 + 0Ch

Read/Write

7	6	5	4	3	2	1	0
AA	ENSIO	STA	STO	SI	CR2	CR1	CR0

Write I2C Bus Control. Commands include Start, Repeated Start, End, etc. Refer to PCA9564 datasheet.

EEPROM DIP Switch – Addresses and Local Registers

The following registers are accessed via the parallel to I^2C device as local registers. Communicate via the PCI Registers previously mentioned.

EEPROM DIP Switch Address

	Address	
	Write	Read
Ports 1 & 2	98	99
Ports 3 & 4	9A	9B

EEPROM DIP Switch Data (1 = High; 0 = Low)

7	6	5	4	3	2	1	0
x	x	Port2(4)C	Port2(4)B	Port2(4)A	Port1(3)C	Port1(3)B	Port1(3)A

EEPROM DIP Switch – Example Configuration Write and Read

I/O Map (ib = inByte; ob = outByte)

SETUP - EEPROM for Read & Write	
I2C Status	
Status: ib BADR3	Return: F8h (otherwise transmit STOP first)
I2C Start Command (63h)	
Control: ob BADR3+C 63	
I2C Status	
Status: ib BADR3	Return: 08h
I2C Write Address - I2C Data Register (For <write address> see EEPROM DIP Switch info at top)	
Data: ob BADR3+8 <write address>	
I2C Transmit (43h)	
Control: ob BADR3+C 43	
I2C Status	
Status: ib BADR3	Return: 18h
I2C EEMPROM Address - I2C Data Register (00h for defaults and power-up)	
Data: ob BADR3+8 00	
I2C Transmit (43h)	
Control: ob BADR3+C 43	
I2C Status	
Status: ib BADR3	Return: 28h

<Continue to Write/Read EEPROM DIP output>

WRITE - EEPROM DIP output (After **SETUP**)

I2C EEPROM Config - I2C Data Register (For <data> see EEPROM DIP Switch info at top)

Data: ob BADR3+8 <data>

I2C Transmit (43h)

Control: ob BADR3+C 43

I2C Status

Status: ib BADR3 Return: 28h

I2C Stop command (53h) [Port pull will change after this command]

Control: ob BADR3+C 53

I2C Status

Status: ib BADR3 Return: F8h

READ - EEPROM DIP output (After **SETUP**)

I2C Start Command (63h)

Control: ob BADR3+C 63

I2C Status

Status: ib BADR3 Return: 10h

I2C Read Address - I2C Data Register (For <read address> see EEPROM DIP Switch info at top)

Data: ob BADR3+8 <read address>

I2C Transmit (43h)

Control: ob BADR3+C 43

I2C Status

Status: ib BADR3 Return: 40h

I2C Transmit (43h)

Control: ob BADR3+C 43

I2C Status

Status: ib BADR3 Return: 58h

I2C Data - I2C Data Register (Status of Pull-up/down, for <data> see EEPROM DIP Switch info at top)

Data: ib BADR3+8 Return: <data>

I2C Status

Status: ib BADR3 Return: F8h

Measurement Computing Corporation
10 Commerce Way
Suite 1008
Norton, Massachusetts 02766
(508) 946-5100
Fax: (508) 946-9500
E-mail: info@mccdaq.com
www.mccdaq.com