PCI-DIO96H

DIGITAL INPUT/OUTPUT

User's Manual

MEASUREMENT COMPUTING

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1 INTRODUCTION

The PCI-DIO96H is a high-drive 96-line digital I/O board. The 96 bits are organized in four 24-bit groups. Each group is further divided into an 8-bit port A, an 8-bit port B, and an 8-bit port C that can be split into separate 4-bit nibbles, port C-HI and port C-LO. See Figure 1-1 below.

The digital output drivers are 74S244 chips that can sink 64 mA and source 15 mA. The input buffers are 74LS373 chips and have standard high input impedance of the 74LS series devices.

On power up and reset, all I/O bits are set to input mode. If you are using the board to control items that must be OFF on reset, install pull-down resistors. Provisions on the board allow users to install SIP resistor networks for either pull-up or pull-down.

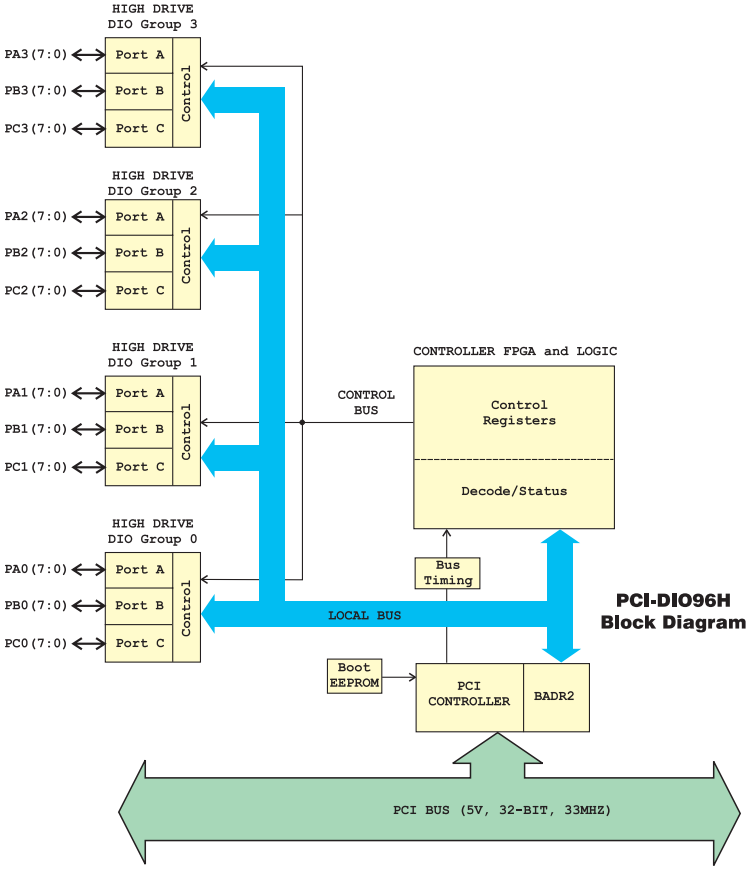

Figure 1-1. PCI-DIO96H Block Diagram

2 INSTALLATION

The PCI-DIO96H boards are completely plug-and-play. There are no switches or jumpers on the board. All board addresses are set by your computer's plug-and-play software.

*Insta*Cal is the installation, calibration and test software supplied with your data acquisition / IO hardware. Refer to the *Extended Software Installation Manual* to install *Insta*Cal.

If you need it, there is some on-line help in the InstaCal program.
Owners of the Universal Library should read the manual and examine the example programs prior to attempting any programming tasks.

3 I/O CONNECTIONS

3.1 CABLES AND SCREW TERMINAL BOARDS

The board has a 100-pin, high-density Robinson-Nugent male connector (Figure 3-1). A C100FF-# cable is used to split the 100 I/O lines into two, 50-wire cables. One connector has pins 1 to 50, the other has 51 to 100. The two I/O connectors can be connected directly to two screw-terminal boards such as the CIO-MINI50, CIO-TERM100, CIO-SPADE50 or SCB-50. See Figures 3-2 and 3-3 for configuration and pin out.

3.2 CONNECTOR DIAGRAM

The I/O connector is a 100-pin type connector accessible from the rear of the PC at the expansion backplate See Figure 3-1 below for the board pin out.

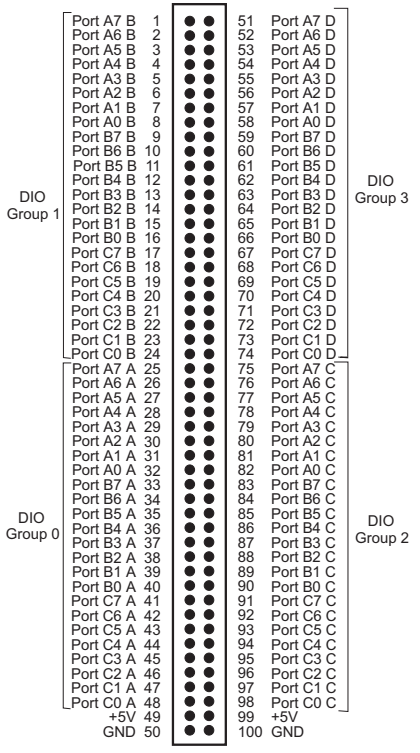

Figure 3-1. 100-Pin Connector Pin Out

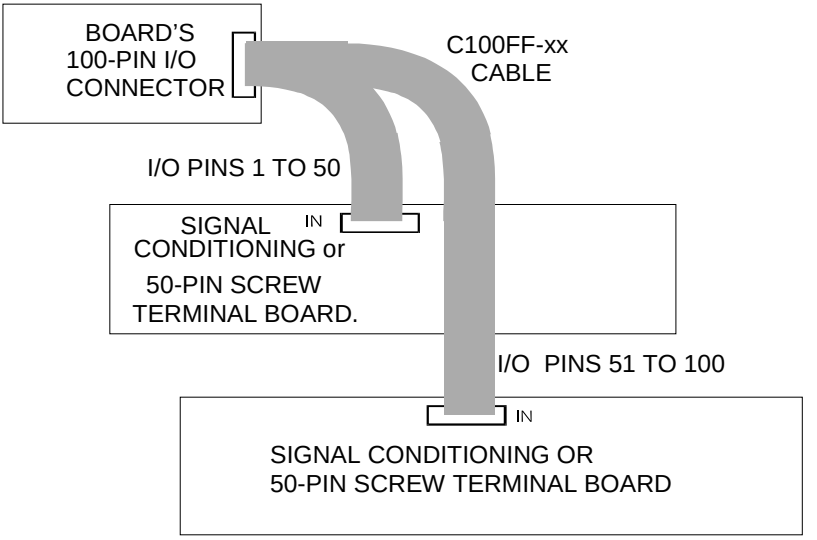

Figure 3-2. Cable C100FF-xx Configuration

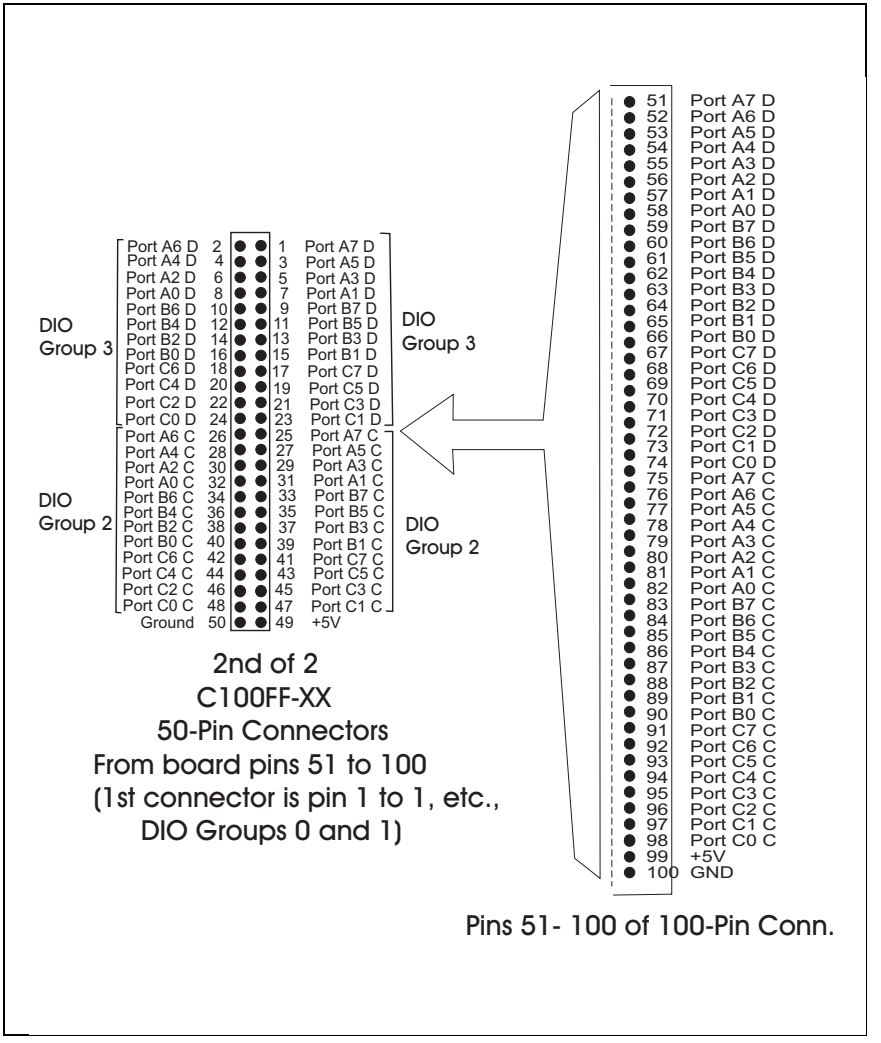

Figure 3-3. Pin Translation - Pins 51 to 100 DI/O Signals

3.3 SIGNAL CONNECTION CONSIDERATIONS

All the digital inputs on the PCI-DIO96H are LSTTL. The output signals are buffered high output drive TTL.

Measurement Computing Corp. offers a wide variety of digital signal conditioning products that provide an ideal interface between high voltage and/or high current signals and the PCI-DIO96H. If you need control or monitor non-TTL level signals with your board, please refer to our catalog or our web site for the following products:

CIO-ERB series, electromechanical relay output boards
CIO-SERB series, 10A electromechanical relay output boards
SSR-RACK series solid state relay I/O module racks

A description of digital interfacing is found in the Interface Electronics section.

IMPORTANT NOTE
This board emulates the 82C55 chip.

The 82C55 digital I/O chip initializes all ports as inputs on power-up and reset. A TTL input is a high impedance input. If you connect another TTL input device to the 82C55 it could be turned ON or OFF every time the 82C55 is reset.
Remember, the 82C55 is reset to the INPUT mode.

There are positions for pull-up and pull-down resistor packs on the board. To implement these, please refer to the application section.

3.4 CIO-ERB24 & SSR-RACK24 CONNECTIONS

PCI-DIO96H boards provide digital I/O in two major groups of 48 bits each (Each side of the C100FF-xx cable provides 48 bits). However, many popular relay and SSR boards provide only 24-bits of I/O. The CIO-ERB24 and SSR-RACK24 each implements a connector scheme where all 96 bits of the PCI-DIO96H board can be used to control relays and/or SSRs. This configuration is shown in Figure 3-4 below. The 24-bits of digital I/O on PCI-DIO96H connector pins 1-24 (base address +0 through +3) control the first relay board. The 24-bits on pins 25-50 will control the second relay/SSR board on the daisy chain and so on up to 100 pins.

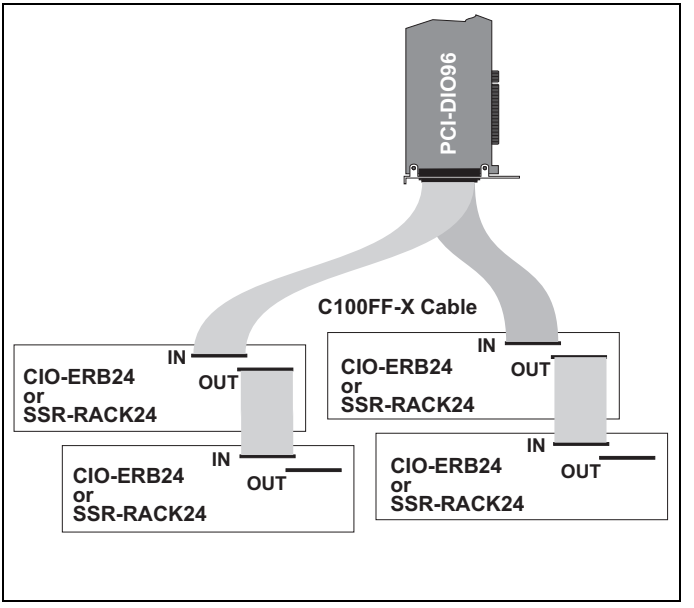

Figure 3-4. Relay Rack Cabling

4 SOFTWARE

We highly recommend that users take advantage of our Universal Library package's easy-to-use programming interfaces. However, if you are an experienced programmer, and wish to read and write directly to the board, we have provided a detailed register map in the next chapter.

4.1 UNIVERSAL LIBRARY

The Universal Library provides complete access to the PCI-DIO96H functions from a range of programming languages. If you are planning to write programs, or would like to run the example programs for Visual Basic or any other language, please turn now to the Universal Library manual.

4.2 PACKAGED APPLICATION PROGRAMS

Most packaged application programs, such as SoftWIRE, DAS Wizard and HP-VEE have drivers for the PCI-DIO96H. If the package you own does not appear to have drivers for the board, please fax or e-mail the package name and the revision number from the install disks. We will research the package for you and advise you on how to utilize the PCI-DIO96H boards with the available driver.

Some application drivers are included with the Universal Library package, but not with the application package. If you have purchased an application package directly from the software vendor, you may need to purchase our Universal Library and drivers. Please contact us for more information.

5 REGISTER MAPS

5.1 CONTROL & DATA REGISTERS

BADR2 is an 8-bit data bus for reading, writing and control of the emulated 82C55 chips operating in mode 0. Refer to Table 5-1 for register offsets.

Table 5-1. I/O Registers

REGISTER	READ FUNCTION	WRITE FUNCTION
BADR2 + 0	Group 0 Port A Data	Group 0 Port A Data
BADR2 + 1	Group 0 Port B Data	Group 0 Port B Data
BADR2 + 2	Group 0 Port C Data	Group 0 Port C Data
BADR2 + 3	Control Register Readback	Control Register 1
BADR2 + 4	Group 1 Port A Data	Group 1 Port A Data
BADR2 + 5	Group 1 Port B Data	Group 1 Port B Data
BADR2 + 6	Group 1 Port C Data	Group 1 Port C Data
BADR2 + 7	Control Register Readback	Control Register 2
BADR2 + 8	Group 2 Port A Data	Group 2 Port A Data
BADR2 + 9	Group 2 Port B Data	Group 2 Port B Data
BADR2 + A	Group 2 Port C Data	Group 2 Port C Data
BADR2 + B	Control Register Readback	Control Register 3
BADR2 + C	Group 3 Port A Data	Group 3 Port A Data
BADR2 + D	Group 3 Port B Data	Group 3 Port B Data
BADR2 + E	Group 3 Port C Data	Group 3 Port C Data
BADR2 + F	Control Register Readback	Control Register 4

The board is programmed to operate in Input/Ouput (mode 0).

NOTE: Strobed Input/Ouput (mode 1) or Bi-Directional Bus (mode 2) are not supported.

The following information describes mode 0 operation.
Upon power-up, an board is reset and defaults to the input mode. No further programming is needed to use the 24 lines as inputs.

5.2 GROUP 0 CONFIGURATION & DATA

GROUP 0 - PORT 1A DATA
BADR2 + 0h
READ/WRITE

7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0

GROUP 0 - PORT 1B DATA
BADR2 + 1h
READ/WRITE

7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0

GROUP 0 - PORT 1C DATA
BADR2 + 2h
READ/WRITE

7	6	5	4	3	2	1	0
C7	C6	C5	C4	C3	C2	C1	C0
CH3	CH2	CH1	CH0	CL3	CL2	CL1`	CL0

GROUP 0 CONFIGURATION
BADR2 + 3h
READ/WRITE

7	6	5	4	3	2	1	0
-	-	-	D4	D3	-	D1	D0

This register is used to configure the Group 0 ports as either input or output.
The following paragraphs and Table 5-2 describe configurations for mode 0.

5.3 8255 EMULATION - MODE 0 CONFIGURATION

1. Output Ports
In mode 0 configuration, each port can be configured for output, holding the data written to them. For example, to set all three ports (A, B, and C) of Group 0 to output mode, write the value 0h to BADR2 + 3 (refer to Table 5-2 below). To read the current state of an output port's bits, simply read the address of that port.

2. Input Ports
In mode 0 configuration, ports can be configured as inputs, reading the state of the inputs lines. For example, to set all of the ports of Group 0 to the input mode, write the value 1Bh to BADR2 + 3.

Table 5-2. DIO Port Configurations/Per Group

Programming Codes				**Values**		**DIO Port**			
D4	**D3**	**D1**	**D0**	**Hex**	**Dec**	**A**	**B**	**CU**	**CL**
0	0	0	0	0	0	OUT	OUT	OUT	OUT
0	0	0	1	1	1	OUT	OUT	OUT	IN
0	0	1	0	2	2	OUT	IN	OUT	OUT
0	0	1	1	3	3	OUT	IN	OUT	IN
0	1	0	0	8	8	OUT	OUT	IN	OUT
0	1	0	1	9	9	OUT	OUT	IN	IN
0	1	1	0	A	10	OUT	IN	IN	OUT
0	1	1	1	B	11	OUT	IN	IN	IN
1	0	0	0	10	16	IN	OUT	OUT	OUT
1	0	0	1	11	17	IN	OUT	OUT	IN
1	0	1	0	12	18	IN	IN	OUT	OUT
1	0	1	1	13	19	IN	IN	OUT	IN
1	1	0	0	18	24	IN	OUT	IN	OUT
1	1	0	1	19	25	IN	OUT	IN	IN
1	1	1	0	1A	26	IN	IN	IN	OUT
1	1	1	1	1B	27	IN	IN	IN	IN

Note: ‘CU’ is PORT C upper nibble; ‘CL’ is PORT C lower nibble.

5.4 GROUP 1 CONFIGURATION & DATA

GROUP 1, PORT A DATA
BADR3 + 4h
READ/WRITE

7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0

GROUP 1, PORT B DATA
BADR3 + 5h
READ/WRITE

7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0

GROUP 1, PORT C DATA
BADR3 + 6h
READ/WRITE

7	6	5	4	3	2	1	0
C7	C6	C5	C4	C3	C2	C1	C0
CH3	CH2	CH1	CH0	CL3	CL2	CL1	CL0

GROUP 1 CONFIGURATION

BADR3 + 7h
READ/WRITE

7	6	5	4	3	2	1	0
-	-	-	D4	D3	-	D1	D0

Refer back to Section 5.3 and Table 5-2 for information on this register.

5.5 GROUP 2 CONFIGURATION & DATA

GROUP 2, PORT A DATA
BADR3 + 8h
READ/WRITE

7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0

GROUP 2, PORT B DATA
BADR3 + 9h
READ/WRITE

7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0

GROUP 2, PORT C DATA
BADR3 + Ah
READ/WRITE

7	6	5	4	3	2	1	0
C7	C6	C5	C4	C3	C2	C1	C0
CH3	CH2	CH1	CH0	CL3	CL2	CL1	CL0

GROUP 2 CONFIGURE
BADR3 + Bh
READ/WRITE

7	6	5	4	3	2	1	0
-	-	-	D4	D3	-	D1	D0

Refer back to Section 5.3 and Table 5-2 for information on this register.

5.6 GROUP 3 CONFIGURATION & DATA

GROUP 3, PORT A DATA
BADR3 + Ch
READ/WRITE

7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0

GROUP 3, PORT B DATA
BADR3 + Dh
READ/WRITE

7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0

GROUP 3, PORT C DATA
BADR3 + Eh
READ/WRITE

7	6	5	4	3	2	1	0
C7	C6	C5	C4	C3	C2	C1	C0
CH3	CH2	CH1	CH0	CL3	CL2	CL1	CL0

GROUP 3 CONFIGURE
BADR3 + Fh
READ/WRITE

7	6	5	4	3	2	1	0
-	-	-	D4	D3	-	D1	D0

Refer back to Section 5.3 and Table 5-2 for information on this register.

6 SPECIFICATIONS

Power consumption

+5V Operating	2.2A typical, 3.35A max

Digital Input / Output

Digital Type	8255 emulation, Mode 0
Output:	74S244
Input:	74LS373
Configuration	8 banks of 8, 8 banks of 4, programmable by bank as input or output
Number of channels	96 I/O
Output High	2.4 volts min @ –15mA
Output Low	0.5 volts max @ 64 mA
Input High	2.0 volts min, 7 volts absolute max
Input Low	0.8 volts max, –0.5 volts absolute min
Power-up / reset state	Input mode (high impedance)

Environmental

Operating temperature range	0 to 70°C
Storage temperature range	–40 to 100°C
Humidity	0 to 90% non-condensing

7 ELECTRONICS AND INTERFACING

This brief introduction to the electronics most often needed by digital I/O board users covers a few key concepts.

IMPORTANT NOTE

WHENEVER AN 82C55 (OR EMULATION) IS POWERED-ON OR RESET, ALL PINS ARE SET TO HIGH-IMPEDANCE INPUT. FOLLOWING STANDARD TTL FUNCTIONALITY, THESE INPUTS WILL TYPICALLY FLOAT HIGH, AND MAY HAVE ENOUGH DRIVE CURRENT TO TURN ON EXTERNAL DEVICES.

The implications of this is that if you have output devices such as solid state relays, they may be switched on whenever the computer is powered on or reset. To prevent unwanted switching and to drive all outputs to a known state after power on or reset, pull all pins either high or low through a 2.2 K resistor.

7.1 PULL UP & PULL DOWN RESISTORS

Whenever the board is powered on or reset, the control register is set to a known state. That state is all ports go to the input state.

The nature of the input means it will typically float high. However, depending on the drive requirements of the device you are driving, they may float up or down. Which way they float is dependent on the characteristics of the circuit and the electrical environment; and may be unpredictable. This is why it often appears that the board outputs have gone 'high' after power up. The result is that the controlled device gets turned on. That is why you need pull up/down resistors.

Shown in Figure 7-1 is a digital output with a pull-up resistor attached.

The pull-up resistor provides a reference to +5V. The value of 2.2K ohms requires only 2.3 mA of drive current.

If the board is reset and enters high impedance input, the line is pulled high. At that point, both the board AND the device being controlled will sense a high signal.

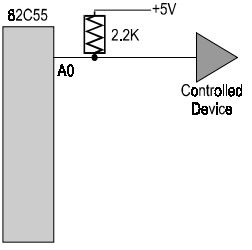

Figure 7-1. Pull-up Resistor

If the board is in output mode, the board has enough power to override the pull-up/down resistor's high signal and drive the line to 0 volts.

Of course, a pull-down resistor accomplishes the same task except that the line is pulled low when the board is reset. The board has enough power to drive the line high.

The PCI-DIO96H has positions for pull-up/down resistors in Single Inline Packages (SIPs). The positions, marked PORT#A, B and C, are located adjacent to the I/O connectors.

A 2.2K, 8-resistor SIP is made of eight 2.2K resistors all connected with one side to a single common point, the other side of each to a pin protruding from the SIP. The common line to which all resistors are connected also protrudes from the SIP. The common line is marked with a dot and is at one end of the SIP.

The SIP may be installed as pull-up or pull-down. At each location, PORT#A, B & C on the PCI-DIO96H series boards, there are 10 holes in a line. One end of the line is +5V, the other end is GND. They are marked HI and LO respectively. The eight holes in the middle are connected to the eight lines of a port 1 through 4, A, B, or C.

A resistor value of 2.2K is recommended. Use other values only if you have calculated the necessity of doing so.

UNCONNECTED INPUTS FLOAT

Keep in mind that unconnected inputs float (typically, but not reliably, high). If you are using the PCI-DIO96H board for input, and have unconnected inputs, ignore the data from those lines.

You do not have to tie input lines, and unconnected lines will not affect the performance of connected lines. Just make sure that you mask out any unconnected bits in software!

7.2 TTL TO SOLID STATE RELAYS

Many applications require digital outputs to switch AC and DC voltage motors on and off, or to monitor AC and DC voltages. These AC and high DC voltages cannot be controlled or read directly by the TTL digital lines of a PCI-DIO96H.

Solid State Relays, such as those available from Measurement Computing Corp. allow control and monitoring of AC and high DC voltages and provide up to 4000VAC isolation. Solid State Relays (SSRs) are the recommended method of interfacing to AC and high DC signals.
The most convenient way to use solid state relays and a PCI-DIO96H board is to use a Solid State Relay Rack. An SSR Rack is a circuit board with input buffer

amplifiers that are powerful enough to switch the SSRs. The buffer amplifiers and SSRs are socketed. The standard buffer amplifiers are inverting types, meaning that a low input from a DIO 82C55 outputs a high to the SSR which turns it on ("closes" the SSR output). If desired, non-inverting amplifiers can be specified

The outputs of the PCI-DIO96H are sufficient to drive SSRs directly. If desired, you can drive DR-OAC OR DR-ODC modules that are mounted on DIN rails.

7.3 VOLTAGE DIVIDERS

If you wish to measure a signal that varies over a range greater than the input range of a digital input, use a voltage divider to drop the voltage of the input signal to the level the digital input can measure.

Ohm's law states:

Voltage = Current * Resistance

Thus, any variation in the voltage drop for the circuit as a whole will have a *proportional* variation in all the voltage drops in the circuit.

In a voltage divider, the voltage across one of the resistors in a circuit is proportional to the voltage across the total resistance in the circuit (Figure 7-2).

When designing a voltage divider, choose two resistors with the proper proportions relative to the full scale of the digital input and the maximum signal voltage.

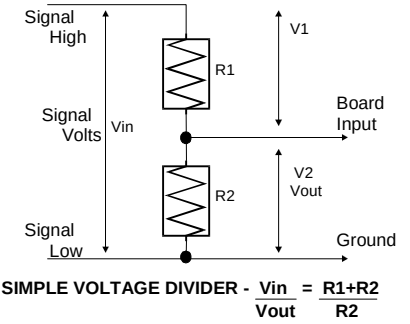

Figure 7-2. Voltage Divider

The formula for voltage attenuation is:

$$\text{Attenuation} = \frac{R1+R2}{R2}$$

The variable *Attenuation* is the proportional difference between the signal voltage max and the full scale of the analog input.

$$2 = \frac{10K+10K}{10K}$$

For example, if the signal varies between 0 and 10 volts, and you wish to measure that with a PCI-DIO96H board with a full scale range of 0 to 5 volts, the *Attenuation* is 2:1, or just 2.

$$R1=(A-1)*R2$$

For a given attenuation, pick a handy resistor and call it R2, then use this formula to calculate R1.

Digital inputs can readily use voltage dividers. For example, if you wish to measure a digital signal that is at 0 volts when off and 24 volts when on, you cannot connect that directly to the PCI-DIO96H digital inputs. The voltage must be dropped to 5 volts max when on. The Attenuation is 24:5 or 4.8. Use the equation above to find an appropriate R1 if R2 is 1K. Remember that a TTL input is 'on' when the input voltage is greater than 2.5 volts.

IMPORTANT NOTE

The resistors R1 and R2 dissipate power in the divider circuit according to the equation Current (I) = Voltage / Resistance and Power (W) = I^2 x R. The higher the value of the resistance (R1 + R2) the less power dissipated by the divider circuit. Here is a simple rule:

For attenuation of 5:1 or less, no resistor should be < 10K.

For attenuation of greater than 5:1, no resistor should be < 1K.

EC Declaration of Conformity

We, Measurement Computing Corporation, declare under sole responsibility that the product:

PCI-DIO96H	Digital I/O board
Part Number	Description

to which this declaration relates, meets the essential requirements, is in conformity with, and CE marking has been applied according to the relevant EC Directives listed below using the relevant section of the following EC standards and other normative documents:

EU EMC Directive 89/336/EEC: Essential requirements relating to electromagnetic compatibility.

EU 55022 Class B: Limits and methods of measurements of radio interference characteristics of information technology equipment.

EN 50082-1: EC generic immunity requirements.

IEC 801-2: Electrostatic discharge requirements for industrial process measurement and control equipment.

IEC 801-3: Radiated electromagnetic field requirements for industrial process measurements and control equipment.

IEC 801-4: Electrically fast transients for industrial process measurement and control equipment.

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