

# CS203 Fall '18 - Lab 3

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Due: 28 November 2018, 1159 pm PST

## 1. Objective

The goal of lab 3 is to measure the effective memory bandwidth on three machines

## 2. STREAM Tool

The STREAM tool is available at <https://www.cs.virginia.edu/stream/>

Get familiar with it. Use it to measure the effective memory bandwidth on three machines of your choice.

## 3. (12 points) Report Results

	A	B	C
CPU	Intel Core i7 (I7-3820QM)	Intel Core 2 Duo (P8600)	Intel Core i5 (I5-6200U)
Clock (GHz)	2.7 GHz	2.4 GHz	2.3 GHz
Main Mem (MB)	8192 MB	8192 MB	8192 MB
Mem Clock (MHz)	1600 MHz	1066 MHz	2133 MHz
Nominal BW (GB/s)	12.8 GB/s	8.533 GB/s	17.067 GB/s
Average measured BW (GB/s)	9.539 GB/s	3.872 GB/s	5.530 GB/s
L1 D\$ (KB)	32 KB/core	32 KB/core	32 KB/core
L2 (D\$) (KB)	256 KB/core	3072 KB (shared)	256 KB/core
L3\$ (KB)	8192 KB (shared)	N/A	3072 KB (shared)

First: TysonLast: LovelessSID: 861118716First: SouryaLast: RoySID: 861243493

#### 4. (10 points) BONUS Question

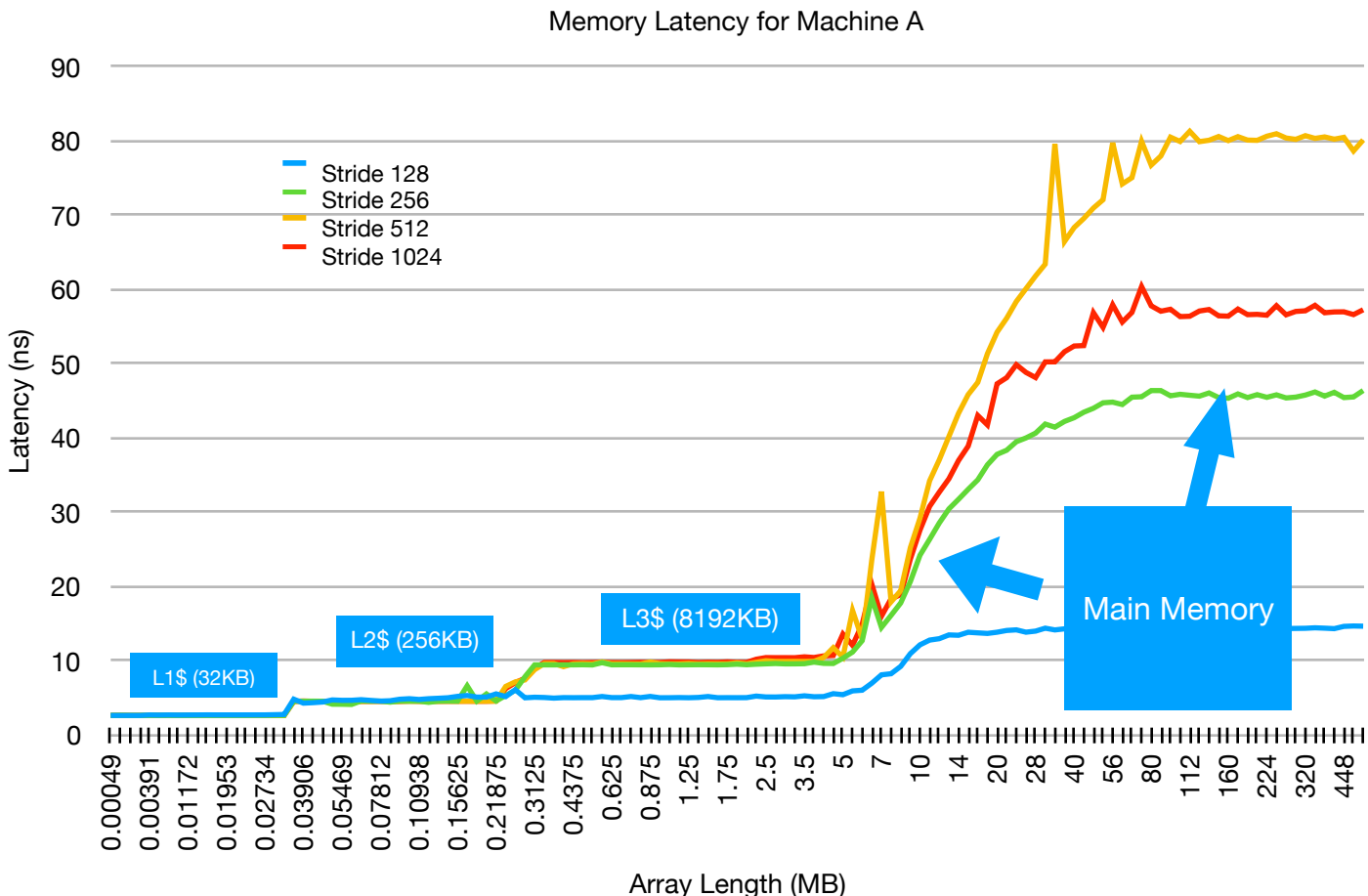
This bonus question will count as Lab 4.

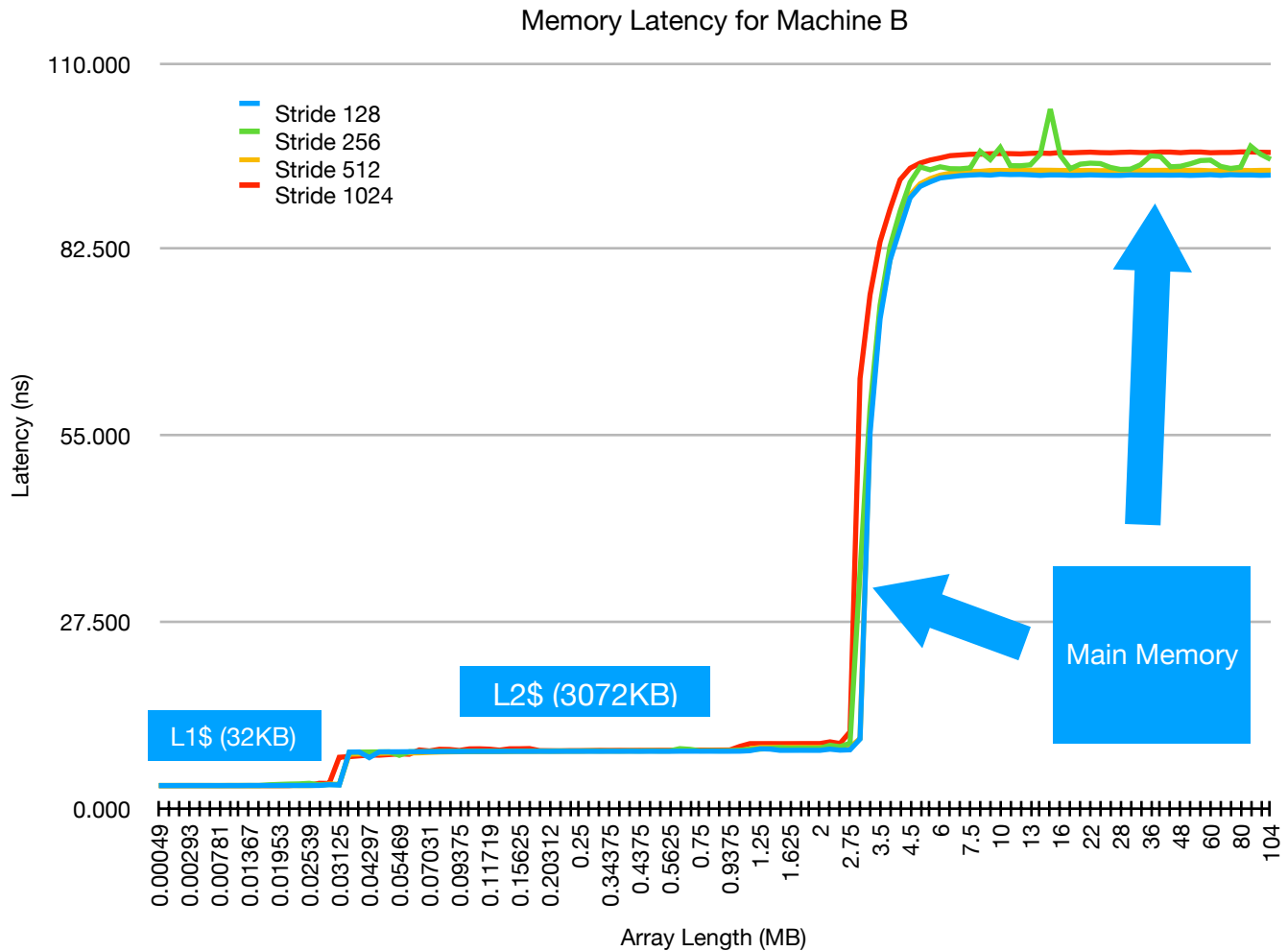
Can you modify the stream.c code, or write or find another code, to measure the latencies of the various cache levels?

Report must include your code as well as the results for two machines. Submit as one zip file to iLearn.

Meet with the TA to demonstrate your code after you submit it. An announcement will be sent on iLearn.

We modified the stream.c code to include the `lat_mem_rd`<sup>1</sup> benchmark from `lmbench3`. `lmbench3` was built for Linux systems, and several functions used are incompatible with other \*nix systems, such as macOS. Hence, many modifications to the source were required to allow the latency benchmark to run on our systems. The test was run on machines A and B with strides of 128, 256, 512, and 1024, with large enough arrays to completely fill last level cache. For Machine C, we only report a stride of 256. Stride values higher than the cache line size eliminate any prefetching the system might be optimizing with, so results for different stride values vary. The below graphs show the change in latency as each level of the memory hierarchy reaches capacity. The final table shows the results at 256 stride for all three machines.





Average latency measured using a stride of 256.

Average Latency(ns)	Machine A	Machine B	Machine C
L1\$	2.7 ns	3.4 ns	2.4 ns
L2\$	4.6 ns	8.3 ns	7.3 ns
L3\$	9.7 ns	N/A	20.4 ns
Main Memory	45.5 ns	95.2 ns	65.3 ns