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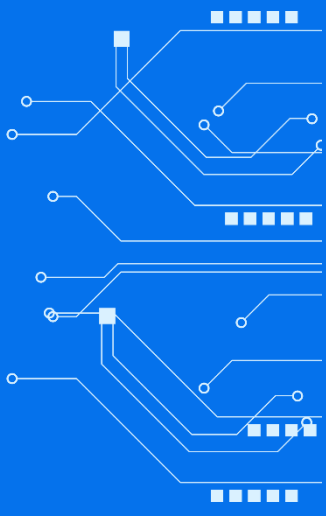
Product Data Sheet

Rev.1.4 2022/11/9

S3KM111L

Smart mmWave Sensor Series



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S3KM111L

1 General Description

The S3KM111L is an integrated single-chip mmWave sensor SoC based on FMCW radar transceiver technology. It works in the 24 GHz K-band with up to 1 GHz modulation bandwidth in every single frequency sweeping chirp.

The S3KM111L offers a low-cost fully integrated solution for all critical mmWave functions with full transceiver and signal processing path, including full K-band RF transceiver, on-chip pattern generator, PLL, and ADC. The pattern generator supports multiple frequency sweeping modes with different time-frequency waveforms, e.g. saw-tooth and triangular waveforms. The pattern generator and PLL support fast chirp mode up to 8 kHz chirp rate. The digitized signals from the receiver chain can be serialized via multiple output interfaces.

The device is packaged in a 32 pin 4 mm × 4 mm leadless ROHS compliant QFN package for easy interfacing to a wide range of antenna board technologies.

2 Main Features

- 24 GHz K-band highly integrated FMCW radar sensor SoC
- Up to 1 GHz bandwidth FM tuning range
- Integrated signal generator, low phase noise PLL， transmitter, receiver, baseband, and ADC
- One transmit channel and one receive channel
- TX maximum output power: 12 dBm
- RX noise figure: 10.5 dB
- Phase noise @ 1 MHz offset: -97 dBc/Hz
- Built-in 2.5 MHz throughput rate ADC with 16 bits resolution
- Support flexible power supply modes
- Built-in hardware accelerator for FFT and filtering
- Chip configuration interface support: I2C/SPI/UART
- Data output interface support: SPI/UART data
- Easy hardware design: 4 × 4 mm^2 QFN32 package for ultra-compact and low-cost PCB design
- Junction temperature range of –40°C to 105°C

3 Applications

- Smart Home Radar sensor
- Robotics
- Proximity and Position sensor
- Motion detector
- Gesture recognition
- Vital signs monitoring

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4 Block Diagram

The RF and analog subsystem implements the FMCW (frequency-modulated continuous-wave) transceiver system with one transmitter (TX), one receiver (RX), synthesizer, mixer, and baseband. Gain controls are applied to both transmitter and receiver to adjust the whole link budget to work in different scenarios. The baseband section includes intermediate frequency (IF) programable amplifiers, filters, and ADCs. A built-in DSP accelerator can process the IQ ADC's raw data with Range FFT or Doppler FFT.

S3KM111L can be configured via I2C/SPI/UART interface, and DSP accelerator processed data can be serialized and outputted via SPI or UART interface.

Figure 4-1 presents an illustration of the design of S3KM111L.

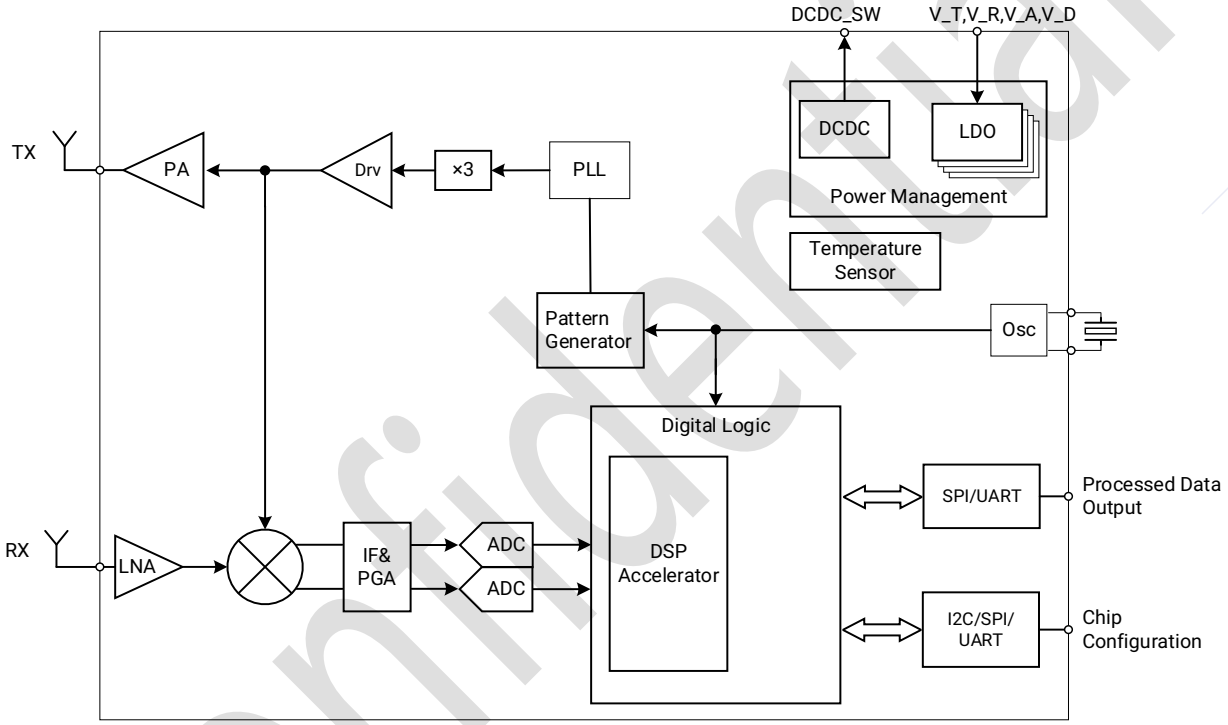


Figure 4-1 S3KM111L diagram

5 Terminal Configuration and Description

5.1 Pin Diagram

The outlook of S3KM111L is shown in Figure 5-1.

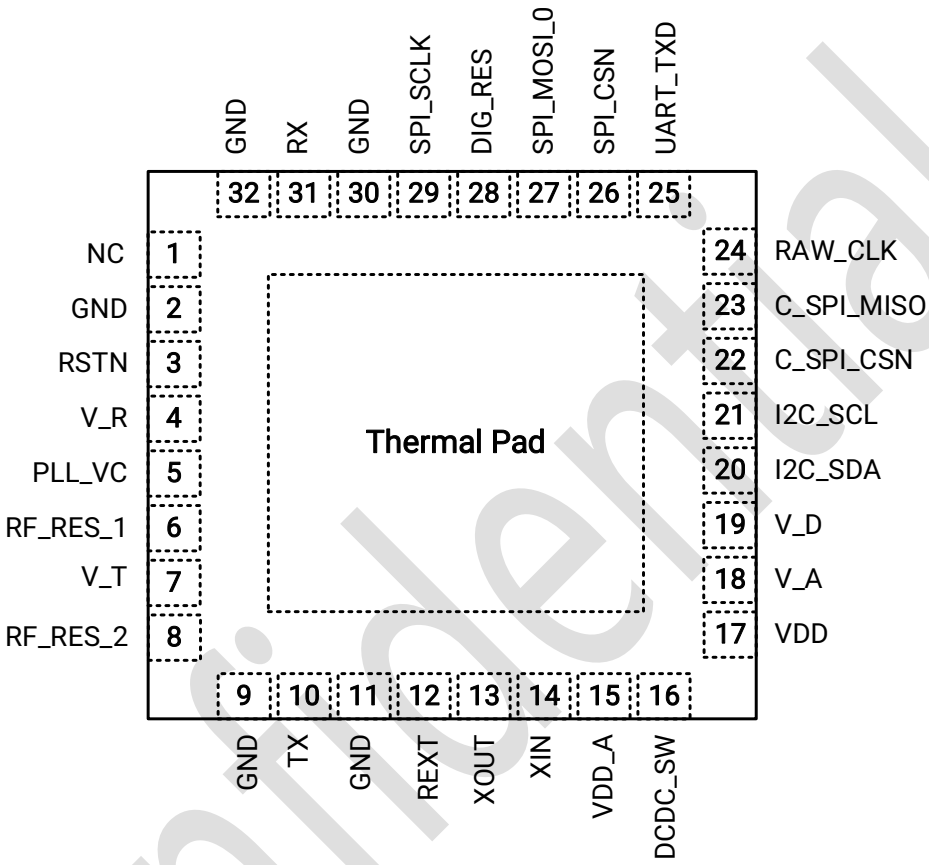


Figure 5-1 Pin diagram QFN32 (top view)

5.2 Signal Descriptions

Information of each pin is given in Table 5-1.

Table 5-1 Signal descriptions

Signal Name	BALL_NO	Type	Description
NC	1	NC	No electrical connection internally. It may be left floating or connected to ground
RSTN	3	IN	External hardware reset input: a logic low on this pin resets the device, causing internal digital circuit to take on their default states
V_R	4	Power	1.6 V analog power supply for RX sections
PLL_VC	5	IN	Connected to external loop filter to drive the internal VCO.
RF_RES_1	6	OUT	Reserved RF pin, connect to Pin 8
V_T	7	Power	1.6 V analog power supply for TX sections

RF_RES_2	8	IN	Reserved RF pin, connect to the Pin 6
TX	10	OUT	Single-ended transmitter output port
REXT	12	IN	Current bias circuit input, connect to ground with a bias resistor
XOUT	13	OUT	Crystal oscillator output port
XIN	14	IN	Crystal oscillator or external clock input port
VDD_A	15	Power	3.3 V power supply for analog domain
DCDC_SW	16	OUT	DCDC regulator switch node. Connect to the power inductor
VDD	17	Power	3.3 V power supply for the DCDC converter and digital domain
V_A	18	Power	1.6 V power supply for analog circuits
V_D	19	Power	1.6 V power supply for digital circuits
I2C_SDA	20[1]	OD	Configuration_I2C_SDA: configuration channel I2C data I/O (open drain)
		IN/OUT	Configuration_SPI_MOSI: configuration SPI channel master-out/ slave-in data
		IN	Configuration_UART_RX: configuration UART channel receiver
I2C_SCL	21[1]	IN	Configuration_I2C_SCL: configuration I2C channel clock
		IN/OUT	Configuration_SPI_SCLK: configuration SPI channel serial clock
		OUT	Configuration_UART_TX: configuration UART channel transmitter
C_SPI_CSN	22	IN/OUT	Configuration_SPI_CSN: configuration SPI channel chip select enable. Connect to ground with a 3.3 kΩ resistor if not use configuration SPI.
C_SPI_MISO	23[1]	IN/OUT	Configuration_SPI_MISO: configuration SPI channel data master-in/ slave-out
		IN	Chip pin mux function, see Table 5-2
RAW_CLK	24	IN	Chip pin mux function (internally pull up), see Table 5-2
UART_TXD	25[1]	OUT	Data_UART_TX: data UART channel transmitter, 115200 baud rates
		IN	Chip pin mux function (internally pull up), see Table 5-2
SPI_CSN	26	OUT	Data_SPI_CSN: data SPI channel chip select enable
SPI_MOSI_0	27[1]	OUT	Data_SPI_MOSI [0]: data SPI channel data output
		IN	I2c address high bit configuration, see Table 5-4
DIG_RES	28[1]	IN	I2c address low bit configuration, see Table 5-4
		OUT	GPIO output, target detect. High: target exists; low: no target
SPI_SCLK	29	OUT	Data_SPI_SCLK: data SPI channel clock
RX	31	IN	Single-ended receiver input port
GND	Thermal PAD, 2, 9, 11, 30, 32	GND	Ground

Note:

[1] There are pin multiplexing functions in Pin 20, Pin 21, Pin 23, Pin 25, Pin 27, Pin 28.

5.3 Pin Mux Function

The S3KM111L have 6 pins (Pin 20, Pin 21, Pin 23, Pin 25, Pin 27, Pin 28) supporting multiplexing functions, all

these multiplex function pins, in exception of Pin 28, should be properly set to Selected Configuration Mode by Pin 23/Pin 24/Pin 25 configuration status during S3KM111L's power up or hardware reset's chip settling time. Pin 28's target detect function is controlled by register setting.

Table 5-2 Function Mode Selection Setup - chip configuration setting

Pin 23	Pin 24	Configuration Mode
Low	Low	UART
Low	High	I2C
High	Low	SPI
High	High	SPI

Table 5-3 Function Mode Selection Setup – data communication setting

Pin 25	Processed Data Output Mode
High	SPI & UART

When configuration mode is set as I2C communication, Pin 27 and Pin 28 should be set to configure the slave chip's address during S3KM111L power up or hardware reset's chip settling time. Up to 4 devices can share the same I2C bus in I2C configuration mode.

Table 5-4 I2C device address

Pin 27	Pin 28	I2C Slave Device Address
Low	Low	7'b010_0000
Low	High	7'b010_0001
High	Low	7'b010_0010
High	High	7'b010_0011

5.4 Chip Configuration Pin States Configuration

The S3KM111L configuration mode is determined by Pin 23 and Pin 24 configuration states, Pin 25 must keep at logical high during the chip settling time. Pin 23 ~ Pin 25 configuration states are fully determined by the external voltage applied on the pin during the chip settling time. Pin 23 and Pin 24 configuration has 2 states: low and high. Setting "Low" when the pin is connected to ground with a 3.3 kΩ resistor; setting "High" when the pin is connected to VDD with a 10 kΩ resistor. Pin 24 and Pin 25 can be float when setting "high" as they are internally pulled up.

After the chip settling time, Pin 23 ~ Pin 25's external applied voltage should be released, as the chosen configuration mode and processed data output mode are triggered.

6 Functional Description

6.1 Transceiver Section

The S3KM111L provides one transmitter, and transmitter parameters can be set via I2C/SPI/UART configuration channel, and directly controlled by the waveform generator. The transmitter can deliver RF power of maximum 12 dBm via the TX port and support programmable transmitter output power for system optimization.

The S3KM111L provides one receiver, which consists of an LNA, mixer, LPF filters, PGA, ADC, and decimation

filter. The baseband subsystem has one quadrature mixer, dual channels IF and ADC chains to provide complex I and Q outputs for DSP processing.

6.2 Waveform Generator Section

The waveform generator provides a linear frequency chirp, and frequency deviation from 0 MHz to 1000 MHz. CW mode is also supported in the waveform generator. The waveform generator provides a sequence of frequency chirps with precise timing. An indicative timing of each frequency chirp is shown in Figure 6-1.

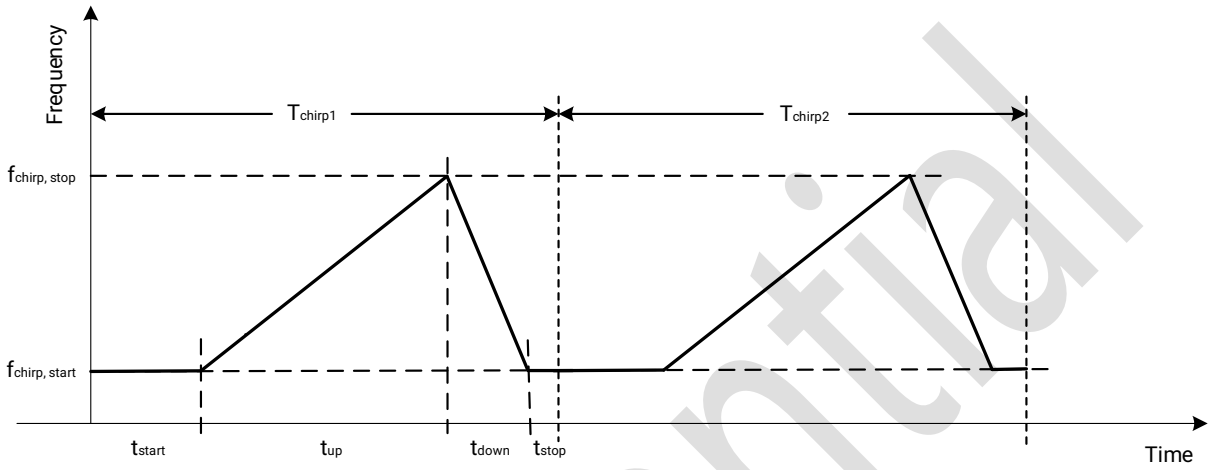


Figure 6-1 Timing parameters in a frequency chirp

The S3KM111L works in continuous sensing mode, each frame starts from t_{pre}, which the waveform generator is initialized to prepare the chirp generation, t_{pre} is programable and typically 20 µs. Then TX output port sends given numbers of chirps for target sensing. After the last chirp of a frame, the S3KM111L can enter low power mode during the NOP time denoted as $t_{\_NOP}$ in Figure 6-2.

If the register 0x41[1] bit4 is set to 0, the RF transceiver (PA, LNA) and baseband (ADC, LPF&PGA) circuits will automatically power down in each frame's NOP time $t_{\_NOP}$ and return to work at next t_{pre} period. During the NOP time, PD time is S3KM111L's fully power down time, S3KM111L takes $t_{\_2pd}$ time of typical 22 µs to turn to low power mode or vice versa.

[1] For register information please refer to S3KM111L Technical Reference Manual.

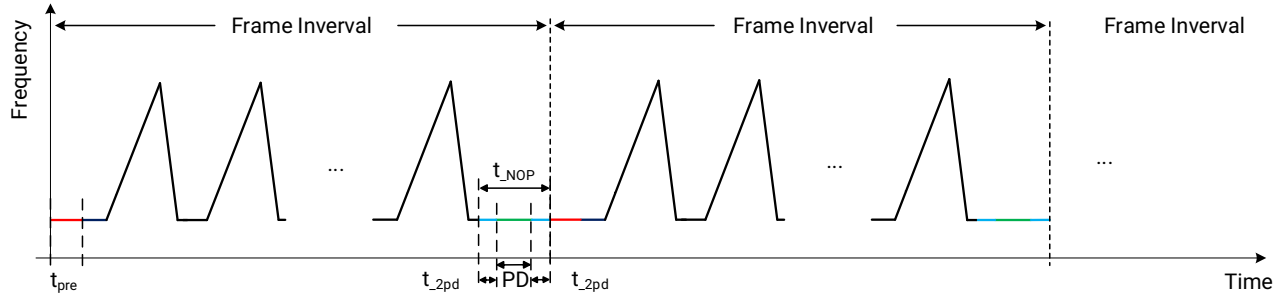


Figure 6-2 Continuous sensing mode

6.3 DSP Accelerator

The S3KM111L integrates Range FFT and Doppler FFT DSP accelerator, the typical DSP flow diagram is shown in Figure 6-3.

The output of the DSP accelerator can be selected as Range FFT data, Doppler FFT data or Doppler FFT Peak data by the data output format configuration.

The I/Q raw data output from RX channel ADC is processed by the DSP accelerator. In DSP accelerator, the raw data is down sampled firstly, and 3 configuration modes are supported for Down sampling: continuous sampling mode, 1/2 down sampling mode, and 1/4 down sampling mode. The down sampled data will go to the Range FFT process, the FFT window supports 64/128/256 points. If Doppler processing is selected, Range FFT processed data will pass an IIR high pass filter for cluster removing; then processed by Doppler FFT process, the sampling points support 16x64/64x16/8x128/32x32 points; finally, the Doppler FFT Peak outputs as the last optional DSP processing stage.

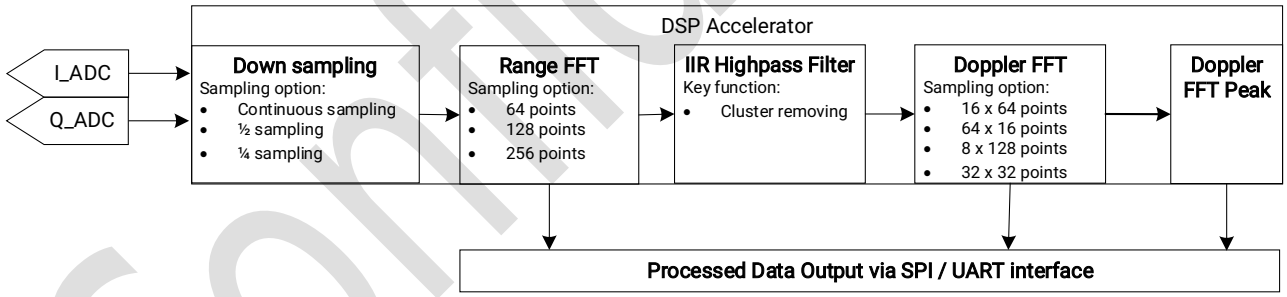


Figure 6-3 DSP accelerator data flow

The S3KM111L also supports a simplified mode for target identification at Pin 28 if the target identification function is turned on; when the DSP accelerator identifies a moving target existing, Pin 28 outputs a logical High, otherwise Pin 28 keeps at logical Low.

6.4 Power Supply Section

The S3KM111L 3.3 V power supply domain is based on an available supply voltage of nominal 3.3 V on PCB board, the 3.3 V power supply is converted into a 1.6 V supply by means of on-chip DCDC circuits or an external DCDC. The S3KM111L supports two power supply modes: single 3.3 V power supply mode and dual power supply (3.3 V and 1.6 V) mode.

3.3 V power supply domain should be properly equipped with a 100 nF capacitor as close as possible to the

power pins for better PSRR.

Pin DCDC_SW is an output pin of the internal DCDC buck converter, and it should connect to a 22 μH power inductor and a 22 μF capacitor as the internal DCDC's output filter. The inductor and output capacitor together provide a low pass filter. The power inductor should be a low ESR power inductor, as in the reference of SWPA252012S220MT. The output capacitor allows the use of ceramic capacitors with low ESR. These capacitors provide low output voltage ripple and are thus recommended. To keep its resistance up to high frequencies and to achieve narrow capacitance variation with temperature, it is recommended to use X7R or X5R dielectric.

6.5 Temperature Sensor

A 10-bit temperature sensor is provided in S3KM111L for temperature monitoring.

7 Electrical Characteristics

7.1 Absolute Maximum Ratings

In accordance with the Absolute Maximum Rating System (IEC 60134).

Table 7-1 Absolute Maximum Ratings [1]

Parameter	Description	Min.	Max.	Unit
VDD_{max}	3.3 V power supply max input	-0.5	3.7	V
$V\_1.6_{max}$	1.6 V power supply (when internal DCDC is not used) max input	-0.5	3.7	V
RF_in_{max}	Externally applied power on RX	-	0	dBm
RF_OUT_{max}	Externally applied power on TX	-	16	dBm
Analog Input and Output voltage	Externally applied voltage at PLL_VC, REXT, XIN, XOUT, DCDC_SW ports	-0.5	3.7	V
Digital Input and Output voltage	Externally applied voltage at RSTN, I2C_SDA, I2C_SCL, C_SPI_MOSI, C_SPI_CSN, RAW_CLK, UART_TXD, SPI_CSN, SPI_MOSI_0, DIG_RES, SPI_SCLK ports	-0.5	3.7	V
T_J	Junction temperature range	-40	125	°C
T_{STG}	Storage temperature range	-40	125	°C

Note:

[1] All voltages with respect to ground

[2] This value is for an externally applied signal level on the TX. Additionally, a reflection coefficient up to Gamma = 1 can be applied on the TX output.

Attention: Stresses exceeding those Max. and Min. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

7.2 ESD Ratings

Table 7-2 ESD Ratings

Model		Value	Unit
V_{ESD}	HBM: Human body model	+/-2000[1]	V
	CDM: Charge device model	+/-500[2]	V

Note:

[1] According to ANSI/ESDA/JEDEC standard, Method JS-001-2017

[2] According to ANSI/ESDA/JEDEC standard, Method JS-002-2014

7.3 Thermal Resistance

Table 7-3 Thermal resistance

Parameter	Description	Min.	Typ.	Max.	Unit
$R_{\theta JA}$	The junction-to-ambient thermal resistance	-	47	-	°C/W

Note:

[1] $T_j = T_A + R_{\theta JA} \times P_{total}$, where P_{total} is the power consumption of the chip and T_A is the environment temperature in the still air.

7.4 Recommended Operating Conditions

Table 7-4 Recommended operating conditions

Parameter	Description	Min.	Typ.	Max.	Unit
VDD_A	3.3 V power supply for analog domain	3.0	3.3	3.6	V
VDD	3.3 V power supply for DCDC and digital domain	3.0	3.3	3.6	V
V_T, V_R, V_A, V_D	1.6 V power supply when the internal DCDC is bypassed	1.5	1.6	1.7	V
VIH	Voltage input High	2.3	-	VDD	V
VIL	Voltage input Low	0	-	0.8	V
VOH	Voltage output High	2.45	-	VDD	V
VOL	Voltage output Low	0	-	0.45	V
T_J	Operating junction temperature range	-40	-	105	°C

7.5 Power Supply Characteristics

7.5.1 Power Supply Modes

S3KM111L has internal low PSRR DCDC module and can support 2 power supply modes: 3.3 V single power supply mode, and 3.3 V/1.6 V dual power supply mode.

7.5.1.1 3.3 V Single Power Supply Mode

S3KM111L can utilize the internal low PSRR DCDC module, connect VDD_A and VDD to external 3.3 V power supply, and connect DCDC_SW as 1.6 V power supply to V_T, V_R, V_A, V_D.

7.5.1.2 3.3 V/1.6 V Dual Power Supply Mode

S3KM111L has 2 fully independent power supplies (3.3 V and 1.6 V), if internal DCDC is not used, connect VDD_A and VDD to external 3.3 V power supply, and connect V_T, V_R, V_A, V_D to external 1.6 V power supply.

7.5.2 Power Consumption

Data in Table 7-5 are measured under 25°C ambient temperature, single power supply mode, applied external voltage refers to typical value in Table 7-4.

Table 7-5 Average power consumption

Parameter	Condition	Description	Min.	Typ.	Max.	Unit
P_{total}	1TX1RX 50% duty cycle	Average power consumption in single power supply mode, all the circuits work at default setting mode and all the circuits are on.	-	210	-	mW

Data in Table 7-6 are measured under 25°C ambient temperature when the internal DCDC is used, applied external voltage refers to typical value in Table 7-4.

Table 7-6 Maximum Current Ratings at Power Terminals

Parameter	Supply Name	Description	Min.	Typ.	Max.	Unit
Current consumption	VDD_A	All analogue and digital domain activated	-	-	23	mA
	VDD		-	-	106	mA

Data in Table 7-7 are measured under 25°C ambient temperature when the internal DCDC is bypassed.

Table 7-7 Maximum Current Ratings at Power Terminals

Parameter	Supply Name	Min.	Typ.	Max.	Unit
Current Consumption	VDD_A	-	-	22	mA
	VDD	-	-	12	mA
	V_T	-	-	128	mA
	V_R	-	-	30	mA
	V_A	-	-	32	mA
	V_D	-	-	10	mA

7.6 Dynamic Performance

Unless otherwise specified, the following conditions apply: single power supply mode, VDDA and VDD are connected to 3.3 V. T_{case} = 25°C. Reference plane on PCB 1.6 mm from bump center; input source and output load impedance at 50 Ω. All RF parameters are measured in an application board, relevant information is to be added.

Table 7-8 RF performance

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
Z_Out	TX output load impedance		-	50	-	Ω
$POut_{max}$	TX maximum output power	0x6D = 0x9dc0 0x72 = 0x3ea0	10	-	12	dBm
F_Out	TX output frequency range		24	-	25	GHz
P_Out	TX recommended output programable power range		-5	-	13	dBm
Z_In	RX input load impedance		-	50	-	Ω
S_{11}_RF_{in}	RX input return loss		-	-	-10	dB

NF	RX noise figure	RX including RF and ADC	-	10.5	-	dB
IP1dB	RX RF Input 1 dB compression point (RX chain including ADC)	30 dB gain, 24 GHz	-	-26	-	dBm
		24 dB gain, 24 GHz	-	-20	-	dBm
G_RF_{RX}	Recommended gain range of RF in RX		20	-	31	dB

Table 7-9 Baseband performance

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
Res_ADC	ADC resolution		-	16	-	bit
f_ad	ADC conversion rate		-	2.5	-	MHz

Table 7-10 Pattern Generator and PLL performance

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
F_Ref	PLL input reference frequency		-	25	-	MHz
BW_PLL	PLL bandwidth	with off-chip filter parameters as follow: R1 = 430 Ω, C1 = 22 nF, C2 = 2.2 nF	-	65	-	kHz
PN_{1MHz}	phase noise at 1 MHz offset @ TX output port		-	-97	-	dBc/Hz
BW_Chirp	FMCW chirp bandwidth @ TX output port		-	-	1	GHz
R_Ramp	FMCW chirp ramp rate		-	-	15	MHz/μs

Table 7-11 DCDC performance

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
f_{sw}	Internal DCDC switching frequency	Single power supply mode	400	500	650	kHz

7.7 Timing and Switching Characteristics

7.7.1 Start-up Sequence

The start-up sequence is depicted in Figure 7-1. If S3KM111L works in single power supply mode, no power sequence restriction as V_T/V_R/V_A/V_D are supplied by internal DCDC and those pins' power up sequences are also controlled by internal power management block. If S3KM111L works in dual power supply mode, the V_T, V_R, V_A, and V_D pins should be powered up after VDD in roughly 1.2 ms. After a rough time of 3.1 ms (T_{start}), the crystal oscillator starts up. An interval of roughly 0.4 ms after T_{start} is needed before releasing the internal RSTN. The interval of roughly 0.5 ms after T_{start}, crystal oscillator stabilizes the 25 MHz clock outputs, chip configuration and data communication mode has been confirmed, Pin 23 ~ Pin 25 pin mux function selection control can be released. Then, after the time of $T_{settling}$ (~0.4 ms), chip configuration command can be sent into S3KM111L. Finally, after roughly 0.2ms, all function blocks are ready.

The VDD power up to Pin 23 ~ Pin 25 pin mux function selection control released is roughly 3.6 ms, the VDD power up to chip configuration communication ready is typically 4 ms.

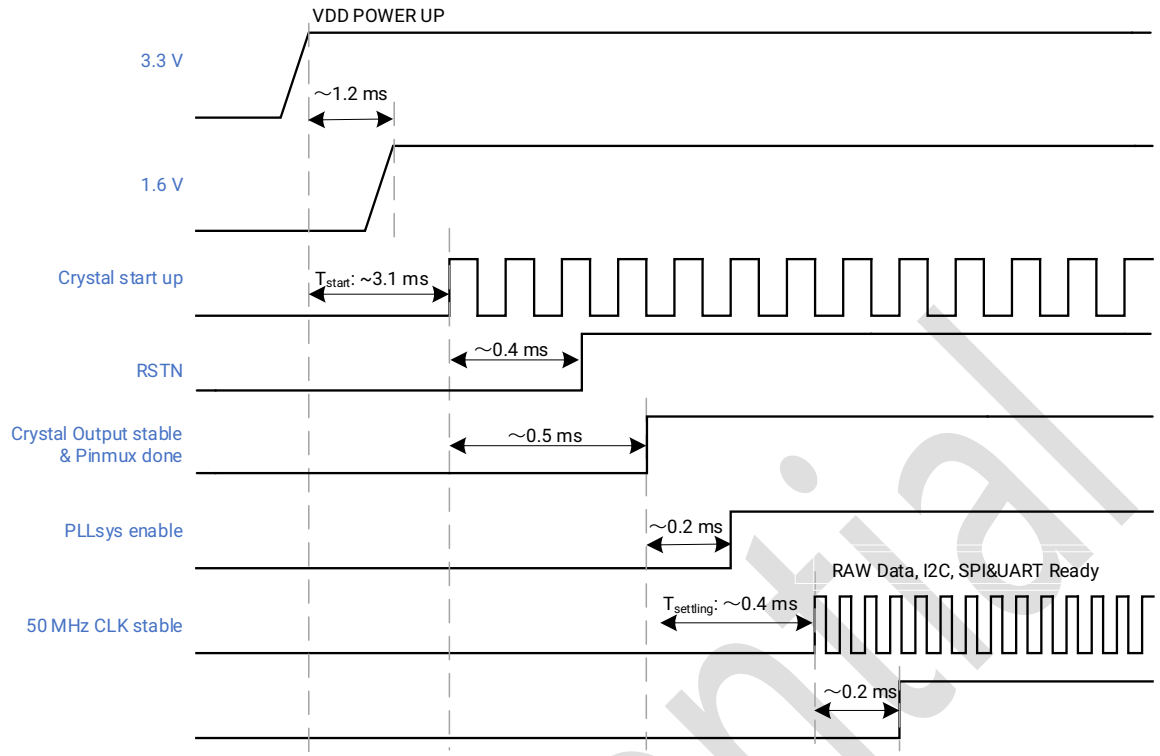


Figure 7-1 Power up timing and sequence

7.7.2 Hardware Reset Timing

S3KM111L chip configuration can be set during both initial power up and hardware reset.

Hardware reset requires an external reset pulse shown in Figure 7-2. If hardware reset is active, all S3KM111L internal registers value will be reset to their default values, all the chip's configuration needs to be re-configured after the reset finishes.

Hardware reset activates when Pin RSTN is triggered by logic low, the Pin 23 ~ Pin 25 should be connected to proper logic inputs to guarantee the chip entering target function mode (check Table 5-2 and Table 5-3) , before Pin RSTN gets a logic high. The Pin 23 ~ Pin 25 should keep the logic level of 0.1 ms after the RSTN rising edge of logic high. Then, Pin 23 ~ Pin 25 pin mux function selection control can be released. The chip is accessible for configuration. T_{RST} is recommended to be greater than 2 ms.

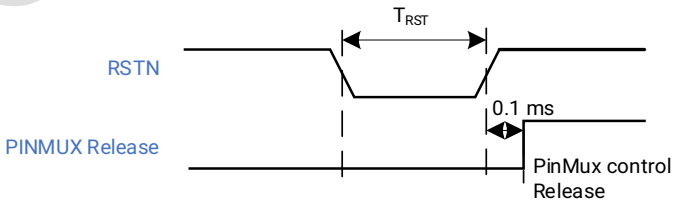


Figure 7-2 Reset pulse width

7.8 External Clock and Crystal Characteristics

S3KM111L requires an external clock source (that is, a 25 MHz crystal or external clock input) for initial boot and as a reference for the internal PLL driving the whole device. Since the feedback resistor is on chip, only a

crystal and the capacitors Ct1 and Ct2 need to be connected externally, in the case of fundamental mode oscillation. Figure 7-3 shows the crystal implementation.

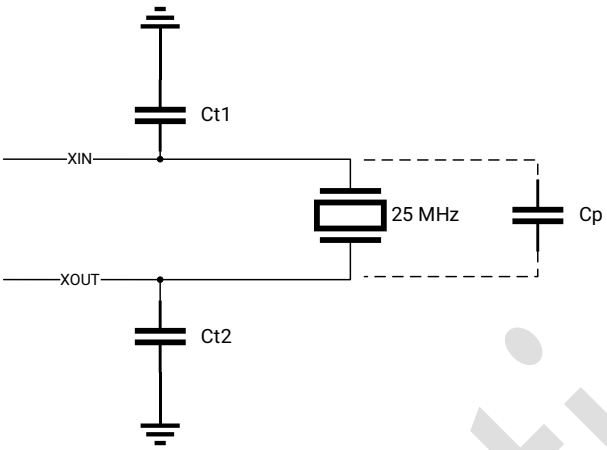


Figure 7-3 Crystal implementation

The load capacitors Ct1 and Ct2 in Figure 7-3 should be chosen such that Equation 1 is satisfied. C_L in the equation is the load specified by the crystal manufacturer. All discrete components used to implement the oscillator circuit should be placed as close as possible to the associated oscillator XIN and XOUT pins.

$$C_L = \frac{Ct1 \text{ x } Ct2}{Ct1+Ct2} + Cp \qquad \text{Equation 1}$$

Table 7-12 shows the electrical characteristics of the clock crystal.

Table 7-12 Crystal electrical characteristics

Parameter	Description	Min.	Typ.	Max.	Unit
f_P	Parallel resonance crystal frequency	-	25	-	MHz
C_L	Crystal load capacitance	5	10	12	pF
C_p	Crystal shunt capacitance	-	-	2	pF
ESR	Crystal ESR	-	-	50	Ω
Temperature range	Expected temperature range of operation	-40	-	85	°C
Frequency tolerance	Crystal frequency tolerance [1][2][3]	-50	-	50	ppm

Note:

[1] The crystal manufacturer's specification must satisfy this requirement

[2] Includes initial tolerance of the crystal, drift over temperature, aging and frequency pulling due to incorrect load capacitance.

[3] Crystal tolerance affects radar sensor accuracy.

The clock signal becomes available after the crystal signal level stabilizes, typically 3 ms after the S3KM111L is activated.

An AC external clock signal may be applied to S3KM111L as the reference clock. The clock is fed to XIN pin only, and XOUT pin should be floated. The electrical characteristic of the external clock signal is shown in Table 7-13. The incoming clock signal should be AC-coupled to the XIN pin, using a 2 pF capacitor.

Table 7-13 External clock signal specifications

Parameter	Description	Min.	Typ.	Max.	Unit
f_s	External clock signal frequency	-	25	-	MHz
Amp	AC clock signal amplitude	0.5	-	1.5	V(pp)
Duty cycle	Duty cycle of clock signal	-	50%	-	
Frequency tolerance	Crystal frequency tolerance	-50	-	50	ppm
PN	Phase noise at 1 kHz	-	-	-135	dBc/Hz
	Phase noise at 100 kHz	-	-	-150	dBc/Hz
	Phase noise at 1 MHz	-	-	-150	dBc/Hz

8 Interface and Peripherals

S3KM111L has 2 types of digital communication interfaces: chip configuration interface and processed data output interface.

8.1 Chip Configuration Interface

The S3KM111L chip configuration mode is determined by Pin 23 and Pin 24 status during the power up or hardware reset period. S3KM111L has 3 types of configuration communication modes: I2C, SPI, and UART.

8.1.1 I2C for Configuration

S3KM111L I2C module works as a slave terminator, and has following features:

- The I2C-interface is an I2C-bus compliant interface with open-drain pins;
- The I2C-bus interface supports Fast-mode with bit rate up to 400 Kb/s;
- Bidirectional data transfer between masters and slaves;
- Support up to 4 I2C device addresses.

8.1.1.1 I2C Timing Characteristic

Table 8-1 I2C timing parameter

Symbol	Parameter	Min.	Typ.	Max.	Unit
f_{scl}	SCL clock frequency	-		400	kHz
$t_{HD;STA}$	Hold time (repeated) START condition	0.4	-	-	μs
t_{LOW}	Low time of the SCL clock	0.4	-	-	μs
t_{HIGH}	High time of the SCL clock	0.4	-	-	μs
$t_{SU;STA}$	Set-up time for a repeated START condition	0.1	-	-	μs
$t_{HD;DAT}$	Data hold time	0	-	-	ns
$t_{SU;DAT}$	Data set-up time	50	-	-	ns
t_r	Rise time of both SDA and SCL signals	20	-	300	ns
t_f	Fall time of both SDA and SCL signals	20	-	300	ns
$t_{SU;STO}$	Set-up time for STOP conditions	0.1	-	-	μs
t_{BUF}	BUS free time between a STOP and START condition	1			μs

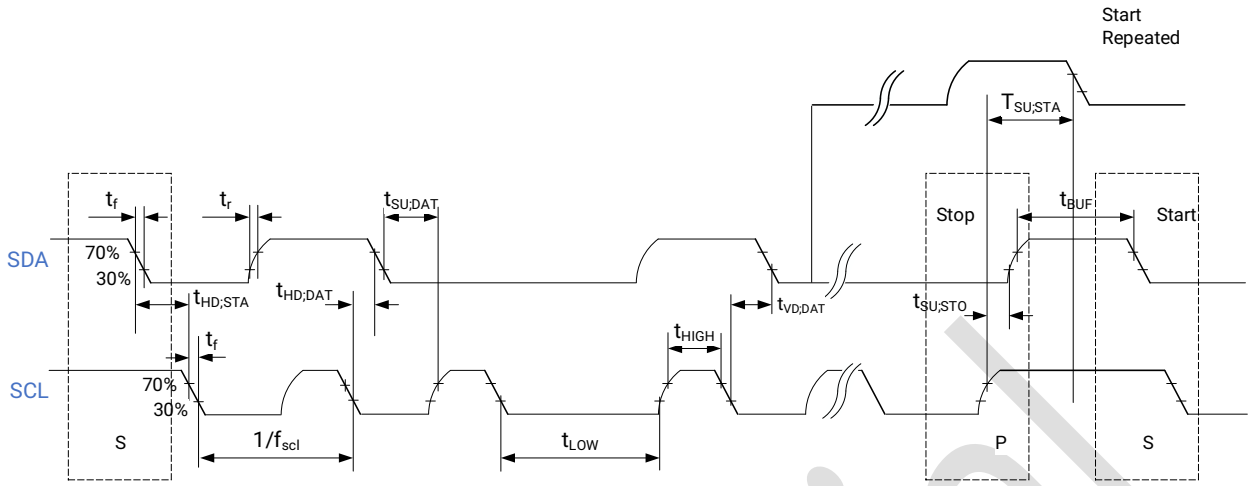


Figure 8-1 I2C timing diagram

The data on the SDA must be stable during the t_{HIGH}, and can only change when the clock signal is low.

Table 8-2 lists the acronyms used in I2C functionality.

Table 8-2 I2C abbreviations

Acronym	Description
SA[6:0]	The 7 bits slave address
SRN[7:0]	Slave Internal Register Number
DATA[7:0]	Data Word
R / $\overline{W}$	Read/Write (0 = data from master to slave, 1 = data from slave to master)
ACK	Acknowledgement
NACK	Non-Acknowledgement (=1)
S	Start condition (initiated by master)
Sr	Repeated Start condition (initiated by master)
P	Stop condition (initiated by master)

8.1.1.2 I2C Interface Data Protocol

The S3KM111L Configuration_I2C interface operates in byte data format. Start and Stop condition are generated by external master terminator, and depicted as S and P part in 错误!未找到引用源。. The first byte after the Start condition consists of a 7-bit slave address followed by the R / $\overline{W}$ bit.

R / $\overline{W}$ = 0: The master writes data to the addressed slave.

R / $\overline{W}$ = 1: The master reads data from the slave.

One extra clock dedicated for acknowledgement (ACK) is inserted after each byte. If the ACK is inserted by the slave after the first byte from the master, it is followed by 8 bits of data from the transmitter (master or slave, depending on the R / $\overline{W}$ bit). After the data bits have been transferred, the receiver inserts an ACK bit.

To ignore the readback message, the master terminator must send a no-acknowledge (NACK) bit at the acknowledge clock time on the bus.

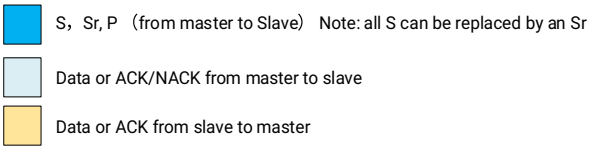


Figure 8-2 I2C color conventions

8.1.1.3 I2C Write

A typical I2C write for chip configuration is depicted in Figure 8-3.

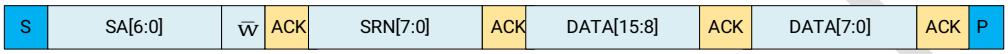


Figure 8-3 I2C configuration communication Write

8.1.1.4 I2C Read

In a read sequence (bit R / $\overline{W}$ = 1), after each data byte, the master responds with an acknowledgement (ACK). After the last data byte, the master responds with a non-acknowledgement (NACK). A typical I2C read for chip configuration is depicted in Figure 8-4.

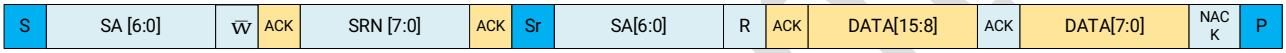


Figure 8-4 I2C configuration communication Read

8.1.2 SPI for Configuration

S3KM111L chip configuration SPI supports full duplex transfers and has following features:

- Maximum SPI speed of 2.08 Mbit/s;
- Synchronous serial communication;
- Slave operation at mode 00.

8.1.2.1 Configuration SPI Interface Timing Characteristic

Table 8-3 Configuration SPI timing parameter

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$T_{c(sck)}$	Clock period		480	-	-	ns
T_{sck_high}	Clock high time		160	-	-	ns
T_{sck_low}	Clock low time		320	-	-	ns
$T_{h(CSN)}$	Chip select hold time		320	-	-	ns
$T_{su(SI)}$	SPI MOSI input setup time		40	-	-	ns
$T_{h(SI)}$	SPI MOSI input data hold time		40	-	-	ns
$T_{a(SO)}$	SPI data output access time		0	-	-	ns
$T_{dis(SO)}$	SPI data output disable time		0	-	-	ns
$T_{h(SO)}$	SPI data output hold time		40	-	-	ns

$T_{v(SO)}$	SPI MOSI data output valid time		-	-	120	ns
T_{cs_sck}	SPI CSN setup time		160	-	-	ns
T_{sck_cs}	SPI CSN hold time		160	-	-	ns
T_{cs_cs}	SPI CSN disable to next CSN enable time		320	-	-	ns
POL_{clk}	SPI clock polarity (CPOL)		-	0	-	
ϕ_{clk}	SPI clock phase (CPHA)		-	0	-	

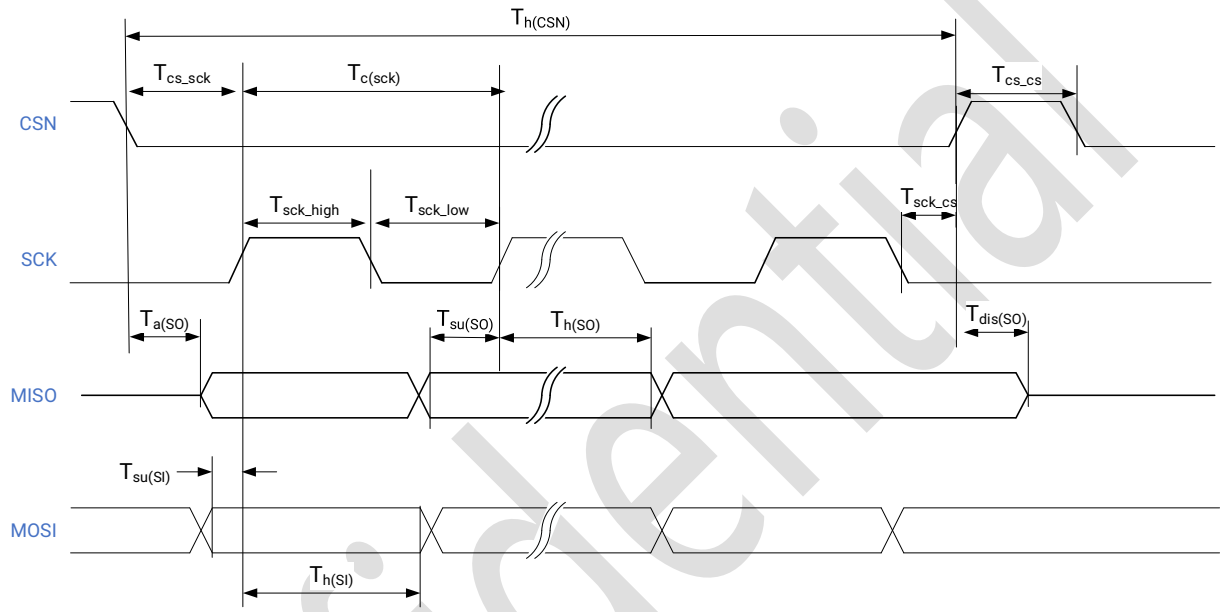


Figure 8-5 Configuration SPI interface timing diagram

8.1.2.2 Configuration SPI Interface Data Protocol

S3KM111L configuration SPI interface works on 4-wire communication mode, the control is based on a combination of a single SPI protocol handler, with several register interfaces within each sub-block.

Pin nomenclature for interfacing to a host MCU is as follows: “SCLK” is the serial clock input at a maximum bus signaling rate of 2.08 Mbps; “MOSI” (Master Out Slave In) is the serial input to write serial data into S3KM111L; “MISO” (Master In Slave Out) is the serial output for data to be read from S3KM111L; and “CSN” (Chip Select) is the select pin for Write and Read operations.

The S3KM111L SPI operates in byte data format. The data frame starts from R / $\overline{W}$, then 7 bits A0 ~ A6 follows, 2 bytes data will be read or written in the communication process.

R / $\overline{W}$ = 0: The master writes data to the addressed slave;

R / $\overline{W}$ = 1: The master reads data from the slave.

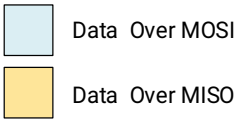


Figure 8-6 SPI color conventions

8.1.2.3 SPI Write

The SPI interface can be used to write into a single 16-bit register. A typical SPI Write for a chip configuration data is depicted in Figure 8-7. The Write operation starts with R / $\overline{W}$ bit, then follows the Register address (7 bits), and a payload message of 16-bit, therefore requires a transfer from external controler to S3KM111L.

Figure 8-7 SPI configuration Write

8.1.2.4 SPI Read

The MISO interface timing is shown in Figure 8-8. The interface protocol shown below is valid only if the first bit over MOSI (R / $\overline{W}$ bit) is set to '1'.

Figure 8-8 SPI configuration Read

8.1.3 UART for Configuration

S3KM111L chip configuration UART interface has both TX and RX lane, and typical data communication speed is 115.2 kbps.

8.1.3.1 Configuration UART Interface Timing Characteristic

Table 8-4 Configuration UART interface timing parameter

Symbol	Parameter	Min.	Typ.	Max.	Unit
Bd	Baud Rate	-	115200	-	bps

8.1.3.2 Configuration UART Interface Data Protocol

The S3KM111L configuration UART interface is based on a combination of a single UART protocol handler and several register interfaces within each sub-block.

Pin nomenclature for interfacing to a host controller is as follows: "Configuration_UART_RX" is the serial input to write serial data into S3KM111L; "Configuration_UART_TX" is the serial output for data to be read from S3KM111L.

The S3KM111L UART interface operates in asynchronous communication mode with no clock pin. The data frame starts from a start bit ('0'), then followed with 8 bits data payload with additional one parity bit, and ends in one stop bit.

During the UART configuration operation, data sent to S3KM111L should contain one parity bit and S3KM111L will not check the parity; data sent from S3KM111L will add 1-bit odd parity.

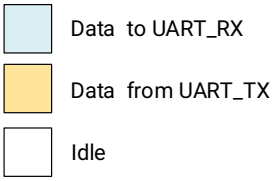


Figure 8-9 UART color conventions

8.1.3.3 Configuration UART Write

The UART interface can be used to write into a single 16-bit register. A typical UART chip configuration is depicted in Figure 8-10. The configuration operation command is composed of 3 sections, the first section sends the 7 bits slave address and 1-bit R / $\overline{W}$; the next 2 sections write the data value to the slave address. A payload message of 16-bit data is divided into 2 sections (low bits and high bits) and follows the rule that starts from the start bit ('0'), then 8 bits data follows, and ends in a parity check bit and a stop bit.

The data write or read enable bit locates at the slave address section.

R / $\overline{W}$ = 0: The master writes data to the addressed slave.

R / $\overline{W}$ = 1: The master reads data from the slave.

S: start bit

PA: parity check bit

P: stop bit

I: idle bits

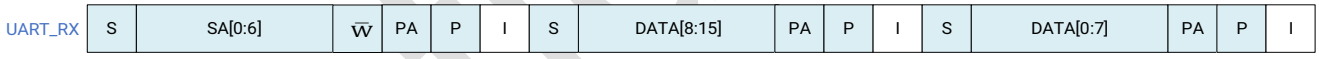


Figure 8-10 UART configuration Write

8.1.3.4 Configuration UART Read

The Read operation timing is shown in Figure 8-11. The interface protocol shown below is valid only if the first bit over UART_RX (R / $\overline{W}$ bit) is set to 'R'.

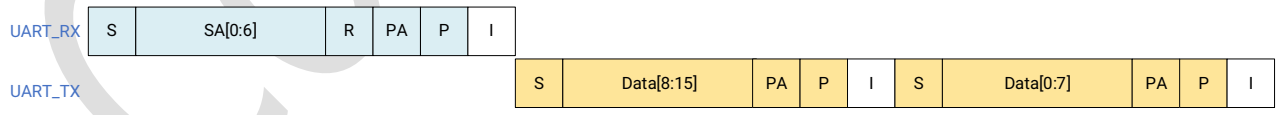


Figure 8-11 UART configuration Read

8.2 Chip Data Communication Interface

The S3KM111L data communication mode is determined by Pin 25 status during the power up or hardware reset period. The S3KM111L has 2 types of data communication modes: SPI and UART. SPI and UART interfaces send the DSP processed data out to the receiver.

8.2.1 SPI for data communication

The S3KM111L chip data communication SPI interface works in master mode, and has a single lane MOSI.

It only supports data output with frames of FFT data flowing from the master to the slave, and has following features:

- Maximum SPI speed of 16.67 Mbit/s;
- Master operation, mode 00.

8.2.1.1 Data Communication SPI Interface Timing Characteristic

Table 8-5 Data communication SPI timing parameter

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$T_{c(sck)}$	clock period		60	-	640	ns
T_{sck_high}	clock high time		20	-	-	ns
T_{sck_low}	clock low time		40	-	-	ns
$T_{\_h(MO)}$	SPI MOSI data output hold time		0	-	-	ns
$T_{\_v(MO)}$	SPI MOSI data output valid time		15	-	-	ns
T_{cs_scl}	SPI CSN setup time		60	-	-	ns
T_{scl_cs}	SPI CSN hold time		40	-	-	ns
T_{cs_cs}	SPI CSN disable to next CSN enable time		120	-	-	ns
POL_{clk}	SPI clock polarity (CPOL)		-	0	-	
ϕ_{clk}	SPI clock phase (CPHA)		-	0	-	

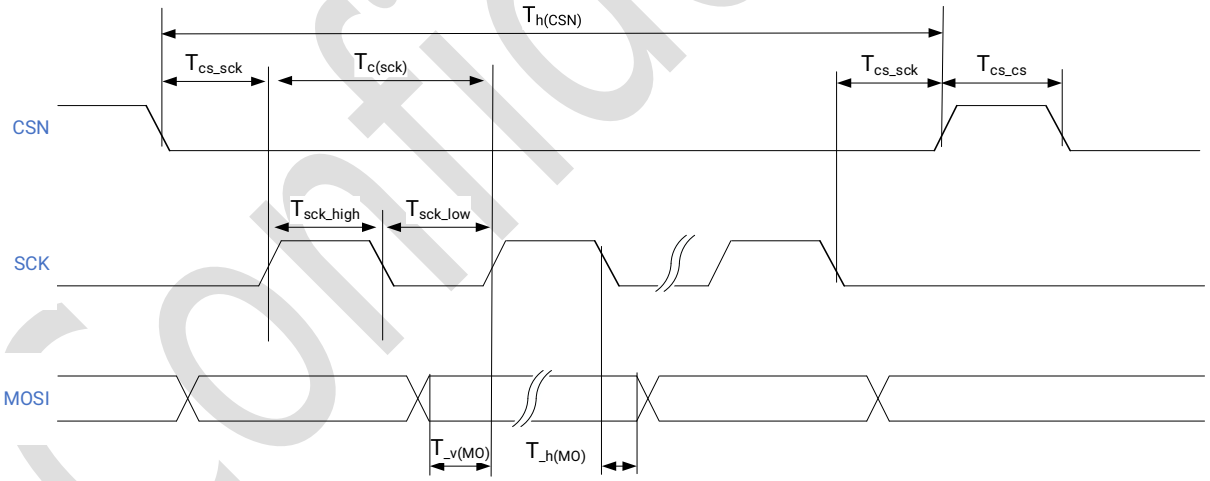


Figure 8-12 Data communication SPI interface timing diagram

The data SPI outputs are not guaranteed during the period of chip configuration. All the data transmitted out through the DATA_SPI channel follow the format shown in Figure 8-13.

Figure 8-13 Data channel transmission

8.2.1.2 Data Communication SPI Output for Range FFT

When Range FFT data SPI output mode is selected by chip configuration command, the chip will transfer Range FFT data. Pin nomenclature for interfacing is as follows: Pin 29 “SCLK” is the serial clock output; Pin 27 “MOSI[0]” (Master Out Slave In) is the serial output to read out serial data from S3KM111L; and Pin 26 “CSN” (Chip Select) is the select pin for Read operations.

The S3KM111L data communication SPI operates in 32 bits format. The data frame starts from the header Dword (32 bits); then all the FFT data is sent out, high 16 bits represent real part of the FFT data, low 16 bits represent imaginary part of the FFT data; finally, the tail Dword(32 bits) will valid the check_sum and terminate the data output.

The transfer is under MSB first sequence and the Range FFT data type is signed integer. Table 8-6 shows the data protocol.

Table 8-6 Range FFT data frame format

Header[Dword 0]	‘b1010 1010	‘b 00	‘b 11	FFT_chirp_index[19:11] [1]	‘b 00	CFG_FFT_TX_MAX[8:0] [2]
Data [Dword 1]	FFT real data 0 [31:16]			FFT Imaginary data 0 [15:0]		
Data [Dword 2]	FFT real data 1 [31:16]			FFT Imaginary data 1 [15:0]		
Data [Dword …]	FFT real data … [31:16]			FFT Imaginary data … [15:0]		
Data [Dword m]	FFT real data m-1 [31:16]			FFT Imaginary data m-1 [15:0]		
Tail [Dword m+1]	Check_sum [31:16] [3]			‘b 00	‘b 11	FFT_chirp _index [11:8] [4]	‘b 0101 0101

Note:

[1] FFT_chirp_index[19:11]: the chirp sequence number in one frame, start from “0” in each frame.

[2] CFG_FFT_TX_MAX[8:0]: the number of m (the total FFT transferred points) +1 in this chirp

[3] Check_sum[31:16]: sum of all data in this frame, and equals to the value of low 16 bits sum result.

[4] FFT_chirp_index[11:8]: the chirp sequence number in one frame, it equals to FFT_chirp_index[19:11]’s low 4 bits value.

8.2.1.3 Data Communication SPI Output for Doppler FFT

When Doppler FFT data SPI output mode is selected by chip configuration command, the chip will transfer Doppler FFT data. Pin nomenclature for interfacing is as follows: Pin 29 “SCLK” is the serial clock output; Pin 27 “MOSI[0]” (Master Out Slave In) or Pin 28“MOSI[1]” is the serial output to read out serial data from S3KM111L; and Pin 26 “CSN” (Chip Select) is the select pin for Read operations. DFFT is short for “Doppler FFT” in the following diagrams and tables.

The S3KM111L data communication SPI operates in 32 bits format. The data frame starts from the header Dword (32 bits); then all the FFT data are sent out, the high 16 bits represent real part of the FFT data, and the low 16 bits represent imaginary part of the FFT data; finally, the tail Dword (32 bits) will valid the check_sum and terminate the data output.

The data transfer is under MSB first sequence and the Doppler FFT data type is signed integer. Table 8-7 illustrates the Doppler FFT data format.

Table 8-7 Doppler FFT data frame format

Header[Dword 0]	'b1010 1010	'b 10	'b 11	'b 1111	DPL_frame_cnt[15:0] [1]
Data [Dword 1]	DFFT real data 0 [31:16]				DFFT Imaginary data 0 [15:0]
Data [Dword 2]	DFFT real data 1 [31:16]				DFFT Imaginary data 1 [15:0]
Data [Dword ...]	DFFT real data … [31:16]				DFFT Imaginary data … [15:0]
Data [Dword 1024]	DFFT real data 1023 [31:16]				DFFT Imaginary data 1023 [15:0]
Tail [Dword 1025]	Check_sum [31:16] [2]				'b 0101 0101 0101 0101

Note:

[1] DPL_frame_cnt[15:0]: Doppler frame sequence number, start from 0, cycling between 0 and 0xFFFF.

[2] Check_sum [31:16]: sum of DFFT data in one frame, and equals to the value of low 16 bits sum result.

8.2.1.4 Data Communication SPI Output for Doppler FFT Peak

The S3KM111L can transfer Doppler FFT peak data with data SPI, where Pin 27 is the data output bus MOSI[0]. The transfer is under MSB first sequence and the Doppler FFT data type is signed integer.

Table 8-8 Doppler FFT peak data frame format

Header[Dword 0]	'b1010 1010			'b 01	'b 00	'b 00 0000 0000 0000		CFG_LEN_RPT [5:0] [1]
Data [Dword 1]	0	DFFT_MAX0_DIDX [30:24]	0	DFFT_MAX0_RIDX [22:16]		RESERVED [15:0]		
Data [Dword 2]	DFFT_MAX0_VALUE [31:0]							
Data [Dword 3]	RESERVED [31:0]							
Data [Dword 4]	0	DFFT_MAX1_DIDX [30:24]	0	DFFT_MAX1_RIDX [22:16]		RESERVED [15:0]		
Data [Dword 5]	DFFT_MAX1_VALUE [31:0]							
Data [Dword 6]	RESERVED [31:0]							
Data [Dword ...]	Data ...							
Data [Dword (3m-2)]	0	DFFT_MAXm_DIDX [30:24] [2]	0	DFFT_MAXm_RIDX [22:16] [3]		RESERVED [15:0]		
Data [Dword (3m-1)]	DFFT_MAXm_VALUE [31:0] [4]							
Data [Dword (3m)[5]]	RESERVED [31:0]							
Tail [Dword (3m+1)]	Check_sum [31:16] [6]					'b 01	'b 00	'b0000	'b 0101 0101

Note:

[1] CFG_LEN_RPT [5:0]: Length of Data Dwords payload; max value is 27;

[2] DFFT_MAXm_DIDX [30:24]: DFFT peak location, Doppler FFT index;

[3] DFFT_MAXm_RIDX [22:16]: DFFT peak location, Range FFT index;

[4] DFFT_MAXm_VALUE [31:0]: DFFT peak value; This value is the modulus value of 2DFFT at the corresponding position;

[5] 3m: Data Dword payload max number, equals to the value of CFG_LEN_RPT [5:0];

[6] Check_sum [31:16]: Sum of all data in this frame, and equals to the value of low 16 bits sum result.

8.2.2 UART Output for Data Communication

The S3KM111L data communication UART interface only has TX lane, and the electrical characteristics are shown in Table 8-9.

Table 8-9 Data communication UART interface electrical characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
Bd	Baud Rate	4.8	-	256	kbps

The S3KM111L DATA_UART_TX interface can also transfer Range FFT data, Doppler FFT data, and Doppler FFT peak. DATA_UART_TX sends out the data with an odd parity bit.

DATA_UART_TX can send data frame illustrated in Table 8-6, Table 8-7, and Table 8-8, and transmit all the data in byte, the format is from DW0's highest byte to the lowest byte, then goes to the next DW, until the last DW. Each byte is from LSB to MSB.

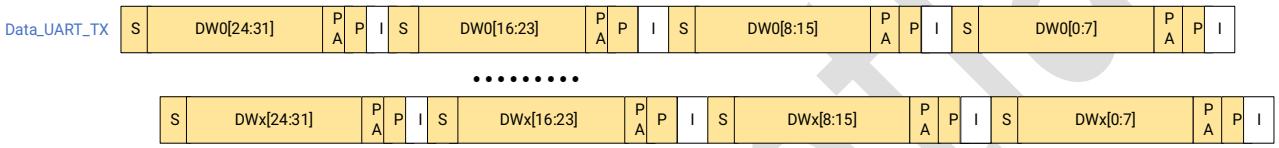


Figure 8-14 UART output data timing

Note:

[1] DWx: the last DW of the data frame.

9 Application Information

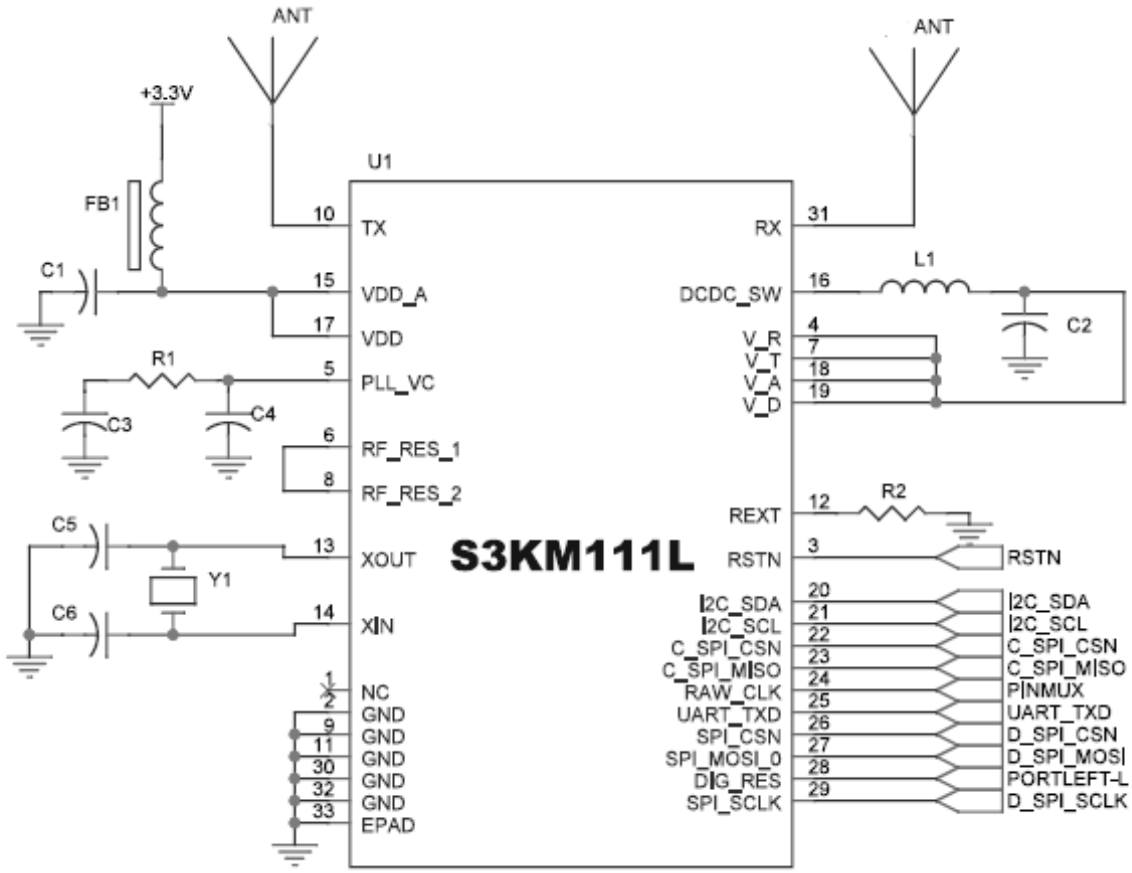
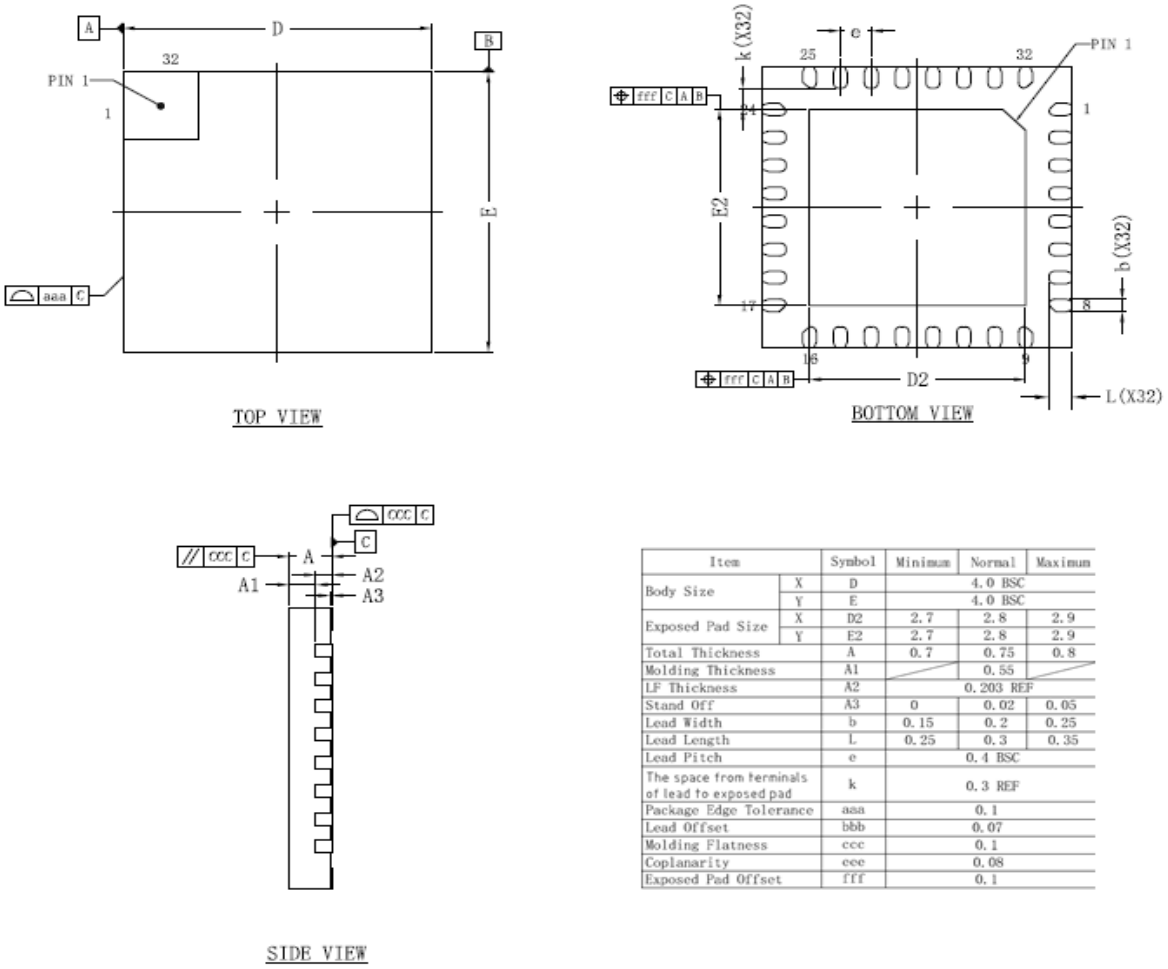


Figure 9-1 mmWave sensor application schematic

Table 9-1 External component suggestions

Component	Description	Value	Remarks
ANT	PCB patch antenna	24 GHz antenna	
FB1	Ferrite bead	GZ1005D310TF	
C1	Ceramic capacitor	100 nF	X7R
C2	DCDC output ceramic capacitor	22 μF	X5R
L1	DCDC output power inductor	22 μH	SWPA252012S220MT, ±20%, DCR < 1.7 Ω, Isat > 500 mA
R1	Loop filter resistor	430 Ω	±5%
C3	Loop filter ceramic capacitor	22 nF	±5%, X7R
C4	Loop filter ceramic capacitor	2.2 nF	±5%, X7R
R2	Resistor	12.4 kΩ	±1%
C5, C6	Capacitor	12 pF	±5%, C0G
Y1	Crystal	25 MHz	<50 ppm

10 Package Outline



Item		Symbol	Minimum	Normal	Maximum
Body Size	X	D		4.0 BSC	
	Y	E		4.0 BSC	
Exposed Pad Size	X	D2	2.7	2.8	2.9
	Y	E2	2.7	2.8	2.9
Total Thickness		A	0.7	0.75	0.8
Molding Thickness		A1		0.55	
LF Thickness		A2		0.203 REF	
Stand Off		A3	0	0.02	0.05
Lead Width		b	0.15	0.2	0.25
Lead Length		L	0.25	0.3	0.35
Lead Pitch		e		0.4 BSC	
The space from terminals of lead to exposed pad		k		0.3 REF	
Package Edge Tolerance		aaa		0.1	
Lead Offset		bbb		0.07	
Molding Flatness		ccc		0.1	
Coplanarity		eee		0.08	
Exposed Pad Offset		fff		0.1	

Figure 10-1 Package description

11 Handling Information

ESD CAUTION	
	**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

12 References

1. AN10015: S3KM111L Hardware Design Guide
2. RM10001: S3KM111L Technical Reference Manual

13 Revision History

Revision	Date	Data Sheet Status	Contents
1.0	2020/7/24	Objective Data Sheet	Initial official release
1.01	2020/9/1	Objective Data Sheet	Update frequency range; Update the table for Doppler FFT; Update the diagram for Doppler FFT
1.02	2020/9/24	Objective Data Sheet	Update I2C timing diagram; Add digital data output notice in application tips
1.1	2021/1/28	Objective Data Sheet	Update package description and introduction of cascade mode
1.2	2021/3/24	Objective Data Sheet	Update Range FFT, Doppler FFT, Doppler FFT Peak data format
1.3	2022/08/29	Objective Data Sheet	Data Sheet structure update
1.4	2022/11/9	Product Data Sheet	Fix some typos and delete original Figure 8-2; Re-arrange section 7.7.1 and 7.7.2; Modify timing and sequence diagrams

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