Lab 3 – Sequential BCD Counter

ENGIN 341 – Advanced Digital Design
University of Massachusetts Boston

Overview

In this lab students will design a sequential up-down Binary to Decimal (BCD) Counter. This will be achieved using sequential circuit design and clock division. The resulting output will be displayed on a two-digit seven segment display.

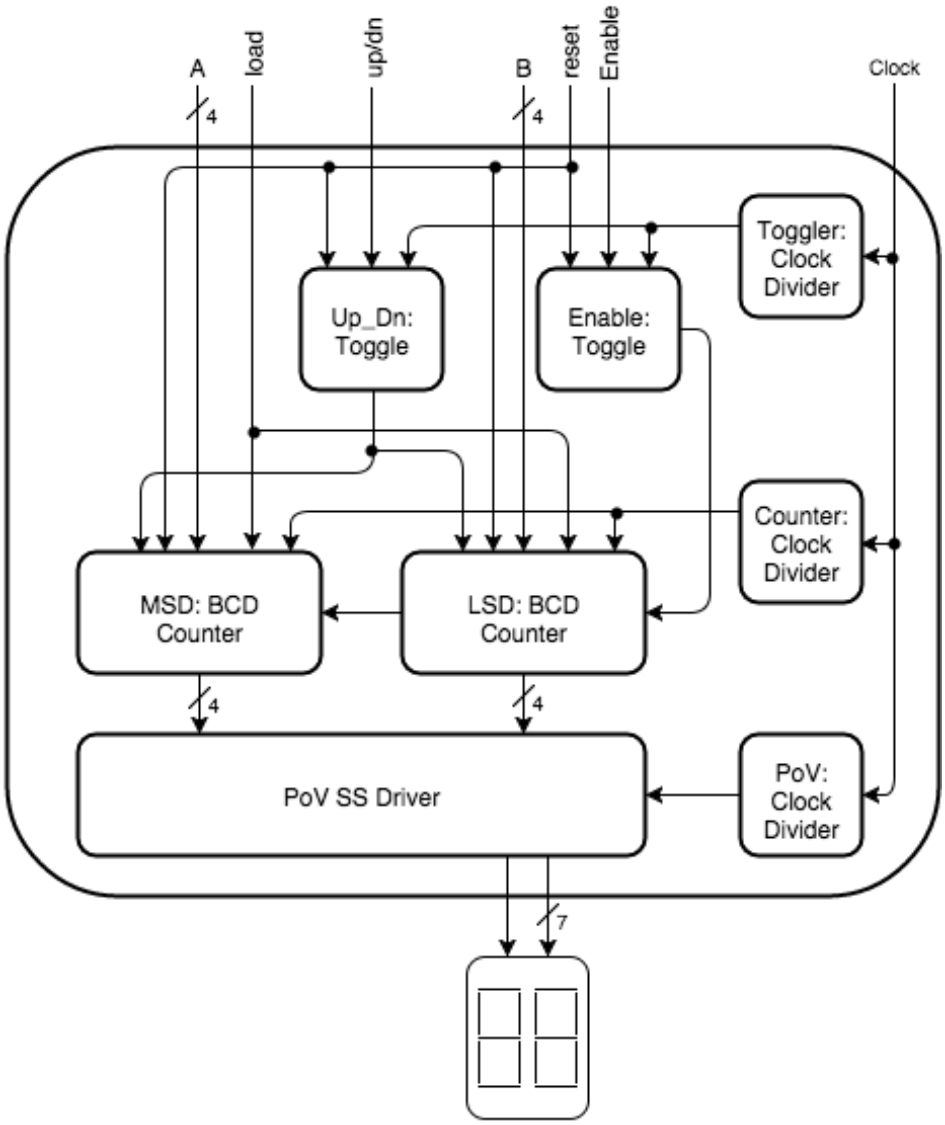

Figure 1. Lab 3 Block Diagram. Each block is an instance of one of the 4 components called by the Top Level file.

Lab Work

1. Refer to the **Lab 3 – Detailed Instructions** to do the following:

2. Write a VHDL module for a generic Clock divider.

3. Write a VHDL module for a *Persistence-of-Vision* (PoV) driver that allows the 7-Segment display to be used for visualizing two-digit values.

4. You have been given a working module for the *BCD_Counter* and *toggler* used within the Lab3 design. Using the Diagram in Figure 1, Write a Lab3.vhd file that instantiates and interconnects two BCD counters, two push button toggle modules, three clock division modules, and a PoV 7-Segment Driver. **Use Generics when possible.*
    a. The ZYBO provides an onboard clock that runs at 125MHz. This is too fast for both the counter and *PoV_SS Driver.* Three separate *Clk_Dvd* modules will be required, with different speeds. Choose the appropriate values to bring the counter's clock to 1 clock strike per second, and refer to the *SS Display Reference Manual* to determine the required speed for your *PoV* module's clock. Use a 1ms clock period for the *toggler* modules.
    b. Synthesize the design. Then use the *I/O Planning* tool to design the constraints file. Refer to the *Zybo Reference Manual* and Table 1 when assigning the pins.

5. **DEMO:** Program the ZYBO with the completed Two Digit Counter and verify its functionality using the the following tests, also show a timing diagram of the expected behavior and the actual behavior of the following operations:
    a. Reset to 0
    b. Load in the value 19
    c. Count up to 22
    d. Count down to 15
    e. Reset to 0
    f. Count down to 89
    g. Load in the value 67
    h. Count up to 72

6. **LAB REPORT:** In your Lab write-up, answer the following questions:
    a. What are the output frequencies of your three *Clk_Dvd* modules, and how did you come up with those values?
    b. Explain how the *Persistence of Vision Driver* works in your design.
    c. You have been provided the *toggler* and *BCD_Counter* modules. Look over the code for each module and explain how they function using pseudo code.

Deliverables

Your Lab 3 project directory, containing all sources, simulation waveforms, bit files, timing diagram and lab write-up are to be turned in as a zip file labeled *"ENGIN341_LAB3_LastName_FirstName.zip".*