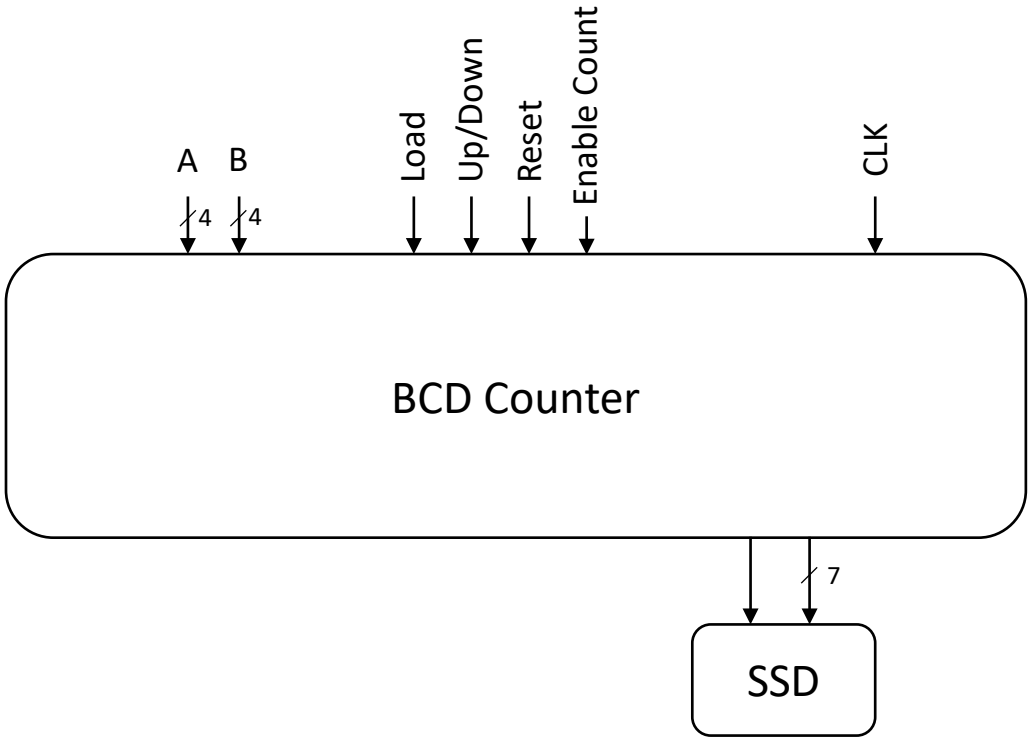
Lab 3 – Sequential BCD Counter

ENGIN 341 – Advanced Digital Design

University of Massachusetts Boston

Design Description

In this lab, students will use the PMODSSD seven segment display to visualize a 2-digit binary converted decimal (BCD) value and implement the logic necessary to (a) reset the value, (b) load a value, and (c) count up or down. The four on-board pushbuttons will be used as input to reset the counter to 0, load the value from the current switch settings, specify whether you are counting up or down, and enable the counter which will count with a frequency of 2Hz. When loading a new value, you will use the current setting of the 4 onboard switches to load a decimal value into the "ones" digit and the current setting of the 4 PMOD switches to load a decimal value into the "tens" digit. Note that the Zybo board's onboard clock is 125 MHz.



Pre-lab objective: *Design Formulation*

In the pre-lab portion of this lab, you are tasked with formulating the structure of a design implementation for the design description above. This implies that you will evaluate the required input/output for the system, the internal components, and the interconnection of components. In your pre-lab design formulation, depict this module and describe the internal components. Be sure to include open questions if there are aspects of the design that are not clearly identified in the design description above.