Wishbone Slave wbs1: I2C

The original I2C module provided a generic I2C interface with a wishbone bus slave that is described in the file “RUv0a/doc/I2C_specs.doc”. The current module wraps this wishbone bus to provide a simpler interface for the specific I2C devices used in the power module prototype and GBTx ASIC and thus loses some generality. The current mapping of the slave at address 0x0xx is as follows:

Address	Data	
0x00	“Address”	r/w “Address” to GBTx “indirect address” register
0x01	“Data”	Write “data” to GBTx I2C register pointed to by 0x00 and increment 0x00
0x02	“Data”	Write “data” to Power Module I/O module
0x03 – 0x07	“Data”	Write Power Unit Current DAC (write-only)
0x08 – 0x0b	“Data”	Write Power Unit Output Voltage Potentiometer (write-only)
0x0c	“Data”	Store/recall Power Unit output voltage Pot values
0x0d	“Data”	Write Power Unit Bias voltage Potentiometer (write-only)
0x10 – 0x17	“Data”	r/w Power Unit ADC

For details of these transactions and the data required, please see the power unit documentation from Alberto Collu.