Wishbone Slave wbs3: GBT-SCA

The registers of wishbone slave 3 wrap the GBT-SCA module registers. The GBT-SCA module generates the EC bits of the GBT frame to control the SCA chip. The original code of the SCA control module was provided by Alessandro Caratelli (CERN GBT SCA team) and modified and extended by Erno David and J. Schambach. The slave address of these registers are at 0x2xx:

Write:	Reg 0:	Control		
		bit 4:	= start send	
		bits(3:0)	= 0	send packet HDLC + payload
			= a	HDLC CONNECT packet
			= b	HDLC RESET packet
			= c	HDLC TEST packet
	Reg 2:	DATATX(15:0)		SCA HDLC payload send
	Reg 3:	DATATX(31:16)		
	Reg 4:	DATATX(47:32)		
	Reg 5:	DATATX(63:48)		
	Reg 6:	bit 0	= enable	
Read:	Reg0:	bit 0	= acknowledge of send	
		bit 15	= Interrupt	
	Reg 1:	Status		read clears Interrupt bit in Reg 0
	Reg 2:	DATARX(15:0)		SCA HDLC payload received
	Reg 3:	DATARX(31:16)		
	Reg 4:	DATARX(47:32)		
	Reg 5:	DATARX(63:48)		
	Reg 6:	bit 0	= enable	

The 64 bits of DATATX/DATARX are mapped as follows:

Tx:

regSCA_ch_in	DATATX(7:0)	Channel
regSCA_Tr_in	DATATX(15:8)	Tr. ID
regSCA_cmd_in	DATATX(23:16)	Command
regSCA_len_in	DATATX(31:24)	Length
regSCA_Data0_in	DATATX(39:32)	D0
regSCA_Data1_in	DATATX(47:40)	D1
regSCA_Data2_in	DATATX(55:48)	D2
regSCA_Data3_in	DATATX(63:56)	D3

Same for Rx:

regSCA_ch_out	DATATX(7:0)	Channel
regSCA_Tr_out	DATATX(15:8)	Tr. ID
regSCA_cmd_out	DATATX(23:16)	Error
regSCA_len_out	DATATX(31:24)	Length
regSCA_Data0_out	DATATX(39:32)	D0
regSCA_Data1_out	DATATX(47:40)	D1
regSCA_Data2_out	DATATX(55:48)	D2
regSCA_Data3_out	DATATX(63:56)	D3