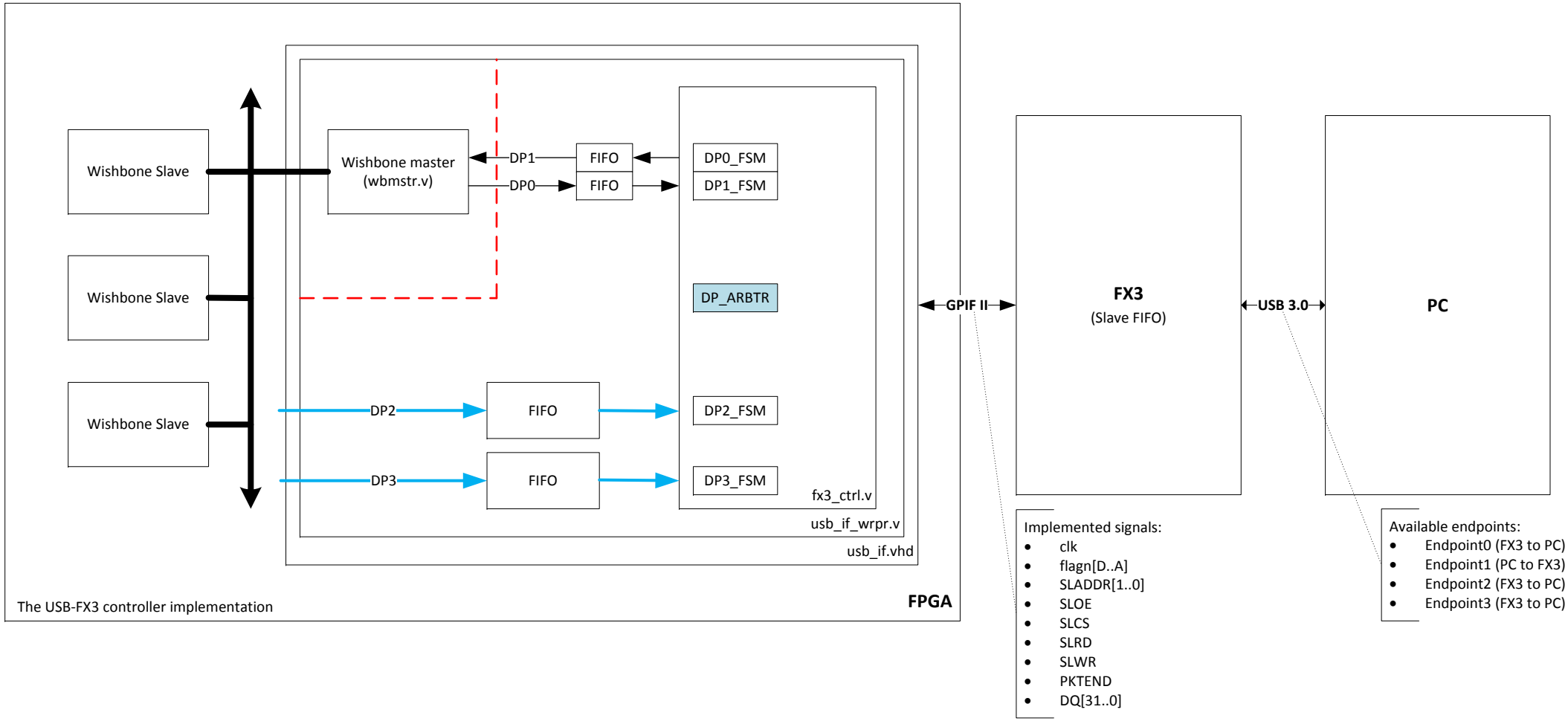
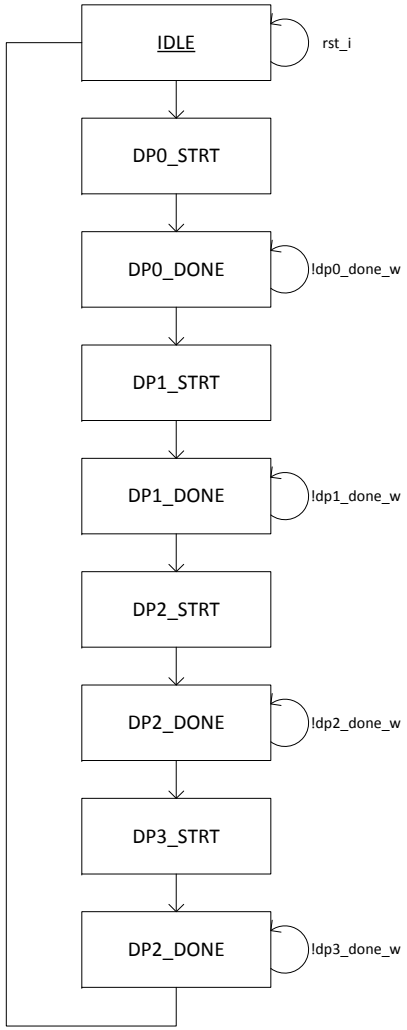
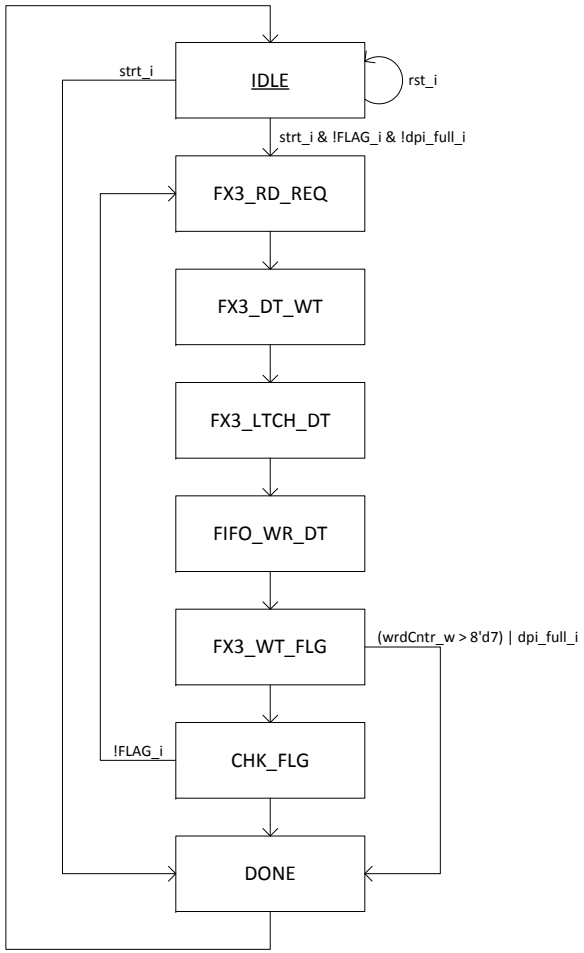

Wishbone Slave
Wishbone Slave
Wishbone Slave
Wishbone master
(wbmstr.v)
DP1
DP0
FIFO
FIFO
DP0_FSM
DP1_FSM
DP_ARBTR
DP2
FIFO
DP2_FSM
DP3
FIFO
DP3_FSM
fx3_ctrl.v
usb_if_wrpr.v
usb_if.vhd
The USB-FX3 controller implementation
FPGA
GPIF II
FX3
(Slave FIFO)
USB 3.0
PC
Implemented signals:
clk
flagn[D..A]
SLADDR[1..0]
SLOE
SLCS
SLRD
SLWR
PKTEND
DQ[31..0]
Available endpoints:
Endpoint0 (FX3 to PC)
Endpoint1 (PC to FX3)
Endpoint2 (FX3 to PC)
Endpoint3 (FX3 to PC)

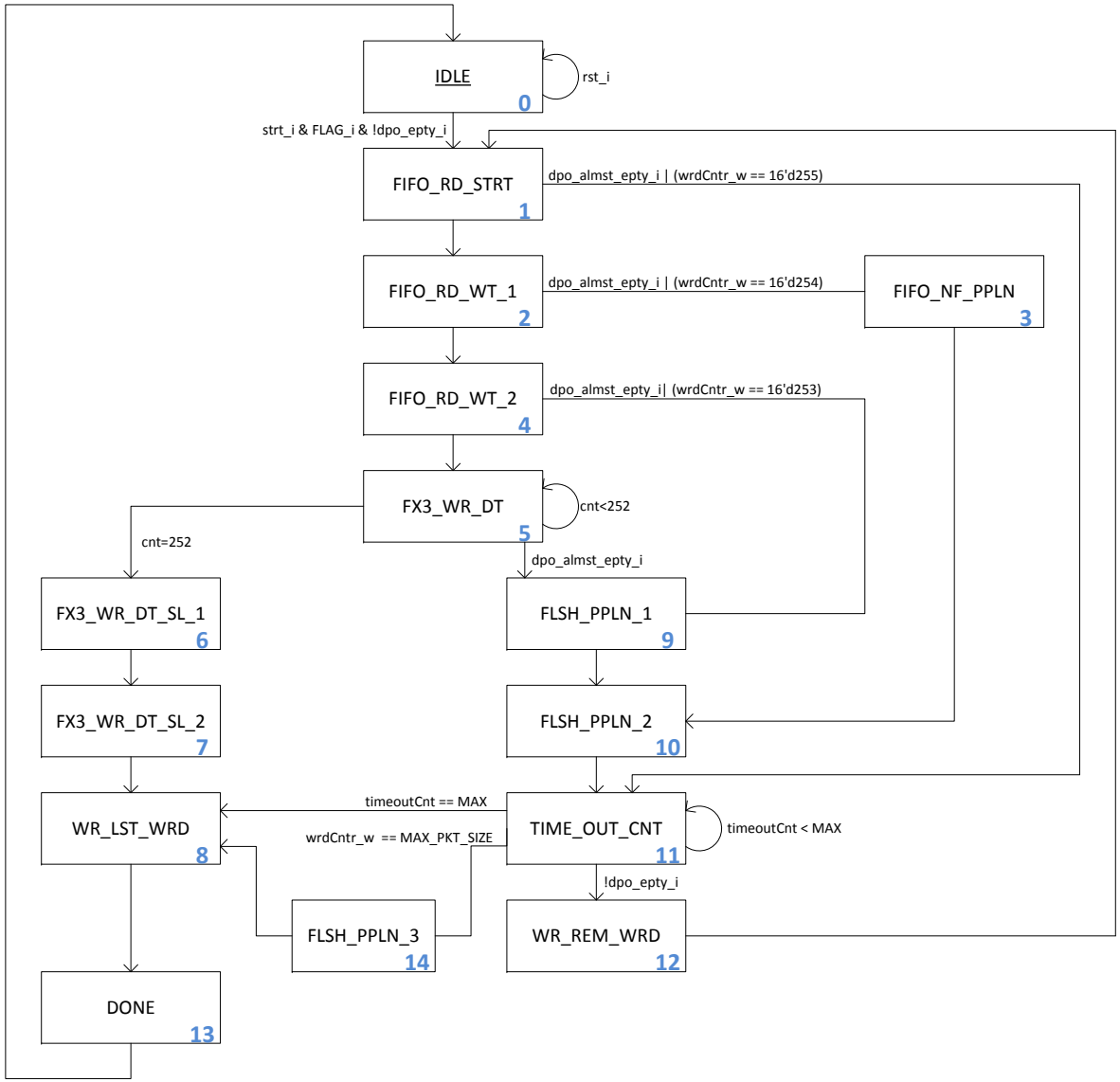
DP_ARBTR FSM Diagram



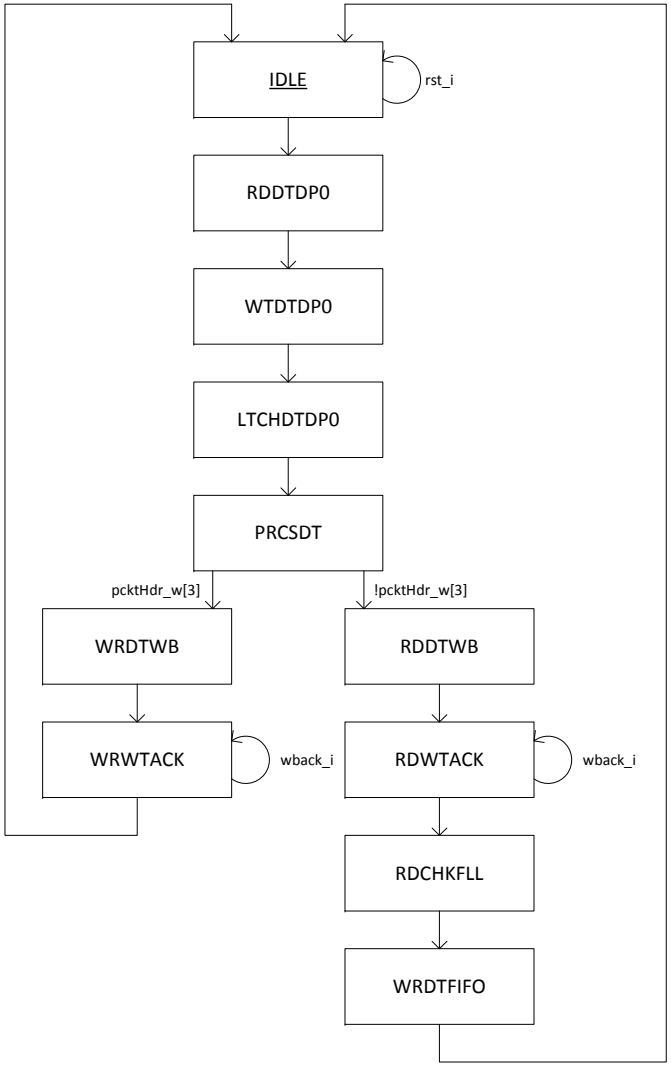
DPI FSM Diagram



DPO FSM Diagram



WBMSTR FSM Diagram



USB word protocol

- PC –FPGA (endpoint DP1):
  - Writing to a register

  - Initiate Read from a register

- FPGA-PC (endpoint DP0):
  - Response from reading a register: