Wishbone Slave wbs4: GBT_FPGA

The registers of wishbone slave 4 are used for the VIO signals of the GBT_FPGA module. This wishbone slave is at slave address 0x3xx. The currently defined registers are:

Read:

Register	Bit	
0	0	MGT Link Ready
	1	RX WordClk Ready
	2	RX FrameClk Ready
	3	gbtRx Ready
	4	gbtRx IsData
	5	gbtRx ReadyLost Flag
	6	gbtRx DataErrorSeen Flag
	15:7	0
1	0	TxIsData
	15:1	0
2	2:0	TestPatternSelect
	15:3	0
3		DataErrorCtr(15:0)
4		DataErrorCtrL(31:16)
5		LinkLostCtr(15:0)
6		LinkLostCtrL(31:16)
7		GbtxDataErrorCtr(15:0)
8		GBTxDataErrorCtrL(31:16)
9		LinkLostCtrDis(15:0)
10		LinkLostCtrDisL(31:16)

Write:

Register	Bit	
0	0	General Reset
	1	reset Tx
	2	reset Rx
	3	reset gbtRx DataErrorSeen Flag
	4	reset gbtRx ReadyLost Flag
	15:5	
1	0	Tx IsData
	15:1	
2	2:0	TestPatternSelect
	15:3	
3	0	DataErrorCtr enable
	15:1	
4	any	DataErrorCtr Reset
5	0	LinkLostCtr enable
	15:1	
6	any	LinkLostCtr Reset
7	0	GBTxDataErrorCtr enable
	15:1	
8	any	GBTxDataErrorCtr Reset

Note: LinkLostCtrDis counts only once for each of consecutive LinkLost errors. This counter is also controlled by writes to register 5 and 6 (i.e. has no separate enable and reset).