

CLAS12 Silicon Vertex Tracker

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Abstract

For the 12 GeV upgrade of Jefferson Laboratory, a Silicon Vertex Tracker (SVT) has been designed for the CLAS12 spectrometer using single-sided microstrip sensors fabricated by Hamamatsu. The sensors have a graded angle design to minimize dead areas and a readout pitch of 156 μm , with intermediate strips. Each double-sided SVT module hosts three daisy-chained sensors on each side with a full strip length of 33 cm. There are 512 channels per module, read out by four Fermilab Silicon Strip Readout (FSSR2) chips, featuring data-driven architecture, mounted on a rigid-flex hybrid board. The modules are assembled on the barrel using a unique cantilevered geometry to minimize the amount of material in the tracking volume. The paper is focused on the design, qualification of the performance, and experience in operating and commissioning the tracker during the first year of the data taking.

1. Physics Requirements and Technical Specs

Essential parts of the CLAS12 physics program, such as the measurement of proton distribution functions, require tracking of low-momentum particles with a few percent momentum resolution and about one degree angle resolution at large angles [1]. Stable operation of the tracker at instantaneous luminosities up to $10^{35}\text{cm}^{-2}\text{s}^{-1}$ for the nuclear targets is required over periods of several years. This is achieved by the central tracker, installed inside the CLAS12 5 T superconducting solenoid magnet providing a highly uniform field in the tracking volume and acting as a Möller electron shield. Silicon detector technology provides an excellent match to the central tracking system in the CLAS12 configuration, where small space and high luminosity operation is needed for accurate measurements of exclusive processes at high momentum transfer. The silicon energy band gap (1.12 eV at room temperature) is large enough to have a low leakage current due to electron-hole pair generation, while it is small enough to allow production of a large number of charge carriers per unit energy loss of the ionizing particles. The large energy loss per traversed length of the ionizing particle (3.8 MeV/cm for a minimum ionizing particle) due to the high material density (2.33 g/cm³) leads to production of measurable

signals in thin detectors. Because of high mobility of electrons and holes, the silicon detectors can be used in high-rate environments, with charge collection times in the order of ns. The expected integrated luminosity per year in CLAS12 is 500 fb^{-1} . The radiation dose for the forward CLAS12 Silicon Vertex Tracker (SVT) sensors (carbon target) is 2.5 Mrads.

SVT provides tracking capabilities in the central detector region by measuring recoil baryons, large angle pions, kaons, and protons with tracking efficiency $\geq 90\%$, transverse momentum resolution $\delta p_T/p_T \leq 5\%$, and angular resolution for polar angles $\delta\theta \leq 10\text{--}20 \text{ mrad}$ (within $35^\circ\text{--}125^\circ$) and azimuthal angles $\delta\phi \leq 5 \text{ mrad}$ (within $\geq 90\%$ of 2π). The CLAS12 central detector consists of the SVT as the inner detector, surrounded by the Barrel Micromegas Tracker (BMT), the Central Time-Of-Flight system (CTOF), and the Central Neutron Detector (CND). The required momentum resolution is provided by the SVT while the BMT improves polar angle resolution due to the strips crossing at 90 degrees. Tracks match up with hits in the CTOF system for β vs. p measurements (particle identification). The SVT allows reconstructing detached vertices, e.g. $K_s \rightarrow \pi^+\pi^-$, $\Lambda \rightarrow \pi^- p$, $\Xi \rightarrow \Lambda\pi$, for an efficient experimental program in strangeness physics.

To satisfy the physics requirements on track momentum resolution, the SVT must have low mass inside the acceptance region. The SVT module position tolerances should be within 20, 500, and 100 μm across the module, along the module, and along the beam, respectively.

2. Design

2.1. Barrel layout and support structure

The SVT comprises 21504 channels of wire-bonded triplets of p-on-n AC-coupled single-sided silicon micro-strip sensors in six layers (three concentric polygonal regions that have 10, 14, and 18 double-sided modules positioned at radii of 65, 93, and 120 mm). The SVT is enclosed by a Faraday cage with an inner radius of 57 mm (with 6 mm clearance to the inner shell of the target scattering chamber) and an outer radius of 133 mm. To minimize multiple scattering, a unique module design with extra long 33 cm strips has been developed to reduce the material budget to about 1.4% of a radiation length per region (two silicon planes) for normal incidence tracks, which is essential for tracking at low momenta [2]. No module services such as cooling lines, power, readout, and slow control cables were placed in the tracking volume. The module dimensions are 41.9 cm \times 4.2 cm \times 0.39 cm. All of the SVT modules are identical to minimize production costs. There are no overlaps of adjacent modules and minimal clearance between them to satisfy material budget and acceptance constraints.

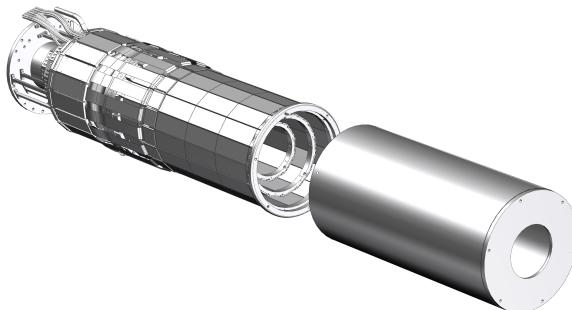


Figure 1: Layout of the barrel and the Faraday Cage. Copper supports are shown in yellow. Supports are bolted directly to the cold plate. The silicon sensors are shown in green.

The modules are mounted between upstream and downstream rings (see Fig. 1). For each region the upstream ring is attached to the cold plate with screws.

The upstream support ring provides a mounting surface for the modules on the upstream end of the detector. It also provides a conduction path for heat to be transferred from the modules to the coolant flowing through the cold plate.

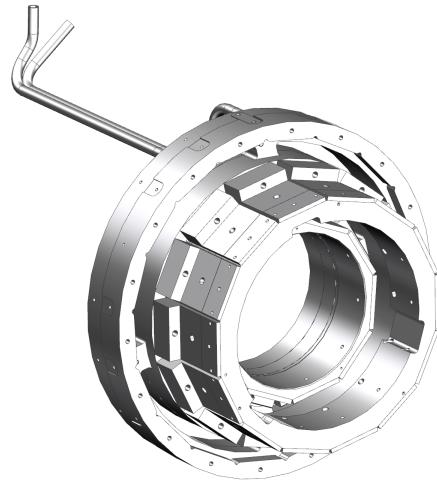


Figure 2: Upstream support ring attached to the cold plate.

The SVT modules are cantilevered off a chilled cold plate, designed to provide mechanical support and to remove heat generated by the electronics, located at the upstream end of the module outside of the tracking volume (see Fig. 2). The cold plate is bolted to the mounting tube that is attached to the insertion cart with the support tube.

The cold plate and upstream ring are attached to the mounting tube. The mounting surfaces of the upstream and downstream rings are machined closely coupled in a single step to guarantee planarity. The modules in the vertical and near vertical positions provide stiffness to the downstream ring and to a region as a whole. The regions are shifted along the beam axis to match the required angular coverage. The downstream support rings are made from PolyEther Ether Ketone (PEEK) [3].

2.2. Module design

The SVT uses single-sided 320- μm thick microstrip sensors fabricated by Hamamatsu, mounted on each side of the module (see Fig. 3). All modules have 3 types of sensors: H (Hybrid), I (Intermediate), and F (Far). The sensors were cut from 6 inch wafers with resistivity of 5 k Ω and <100> surface orientation, with 2 sensors per wafer to maximize the yield. All sensors have the same size, 112 \times 42 mm. There are three

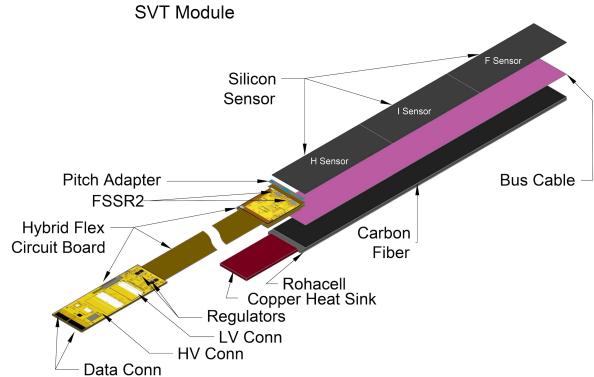


Figure 3: Layout of an SVT module.

daisy-chained sensors per layer (six per module) with a 110 μm gap between them.

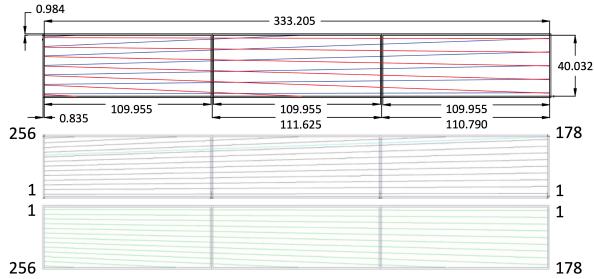


Figure 4: Sensor strip layout.

Each layer has 256 strips with linearly varying angles of 0° - 3° (constant ϕ pitch of $1/85^\circ$) to minimize the dead sensor area. The first readout strip is parallel to the longitudinal axis of the module; the last readout strip has an angle of 3° with respect to this axis (see Fig. 4). Because of the constant ϕ pitch, the lengths of the readout strips of the modules vary from 0.5 cm to 33 cm. At the hybrid side, the intermediate strip pitch is $78 \mu\text{m}$ and the readout pitch is $156 \mu\text{m}$. The strip-to-pitch ratio is 0.256 for all three types of sensors. Fig. 5 shows the cross-sectional view of the sensor. The aluminum strip width is $26 \mu\text{m}$ and is AC-coupled via the SiO_2 layer to the $20\text{-}\mu\text{m}$ wide $p+$ implant strips, which are $1.2 \mu\text{m}$ below the aluminum strips. The total strip capacitance at 1 MHz is below 1.3 pF/cm and coupling capacitance above 10 pF/cm . Electrical specs of the sensors are shown in Table 1 [4]. The implant strips are grounded via $1.5 \text{ M}\Omega$ polysilicon resistors. The unpassivated aluminum backplane (ohmic contact) is connected to the positive side of the power supply; the n -bulk volume of the sensor is depleted via the highly doped n^{++} layer. The guard ring is surrounding the sensitive area to re-

Full depletion voltage	$40 < V < 100$
Interstrip capacitance	$< 1.2 \text{ pF/cm}$
Leakage current (at depletion V)	$< 10 \text{ nA/cm}^2$
Strip to backplane capacitance	$< 0.2 \text{ pF/cm}$
Interstrip isolation (at 150 V)	$> 1 \text{ G}\Omega$
Resistance of aluminum strips	$< 20 \text{ }\Omega/\text{cm}$
Coupling capacitance	$> 20 \text{ pF/cm}$
Value of polysilicon bias resistor	$1.5 \text{ M}\Omega$
Single strip DC current	$< 2 \text{ nA}$

Table 1: Electrical specs of the sensors.

duce the surface currents from the edges of the detector. The 42-mm width of the sensor accommodates 256 readout strips and the 1 mm keep-out zones along the edge of the sensor.

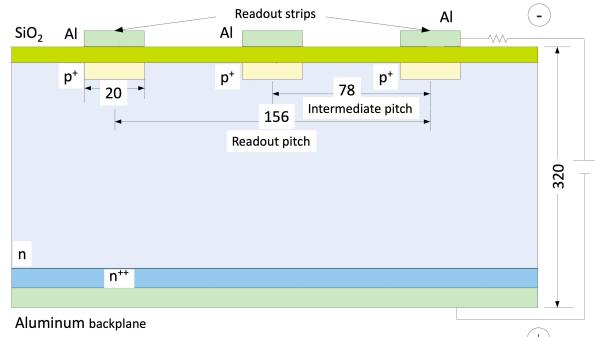


Figure 5: Cross-sectional view of a sensor showing the different layers and the spacing of the strips (the dimension units are in μm).

The sensors are mounted on a backing structure composed of Rohacell 71 core, 78 μm thick bus cable, and carbon fiber (see Fig. 6). The carbon fiber skin is made from Mitsubishi type K13C2U fibers oriented in a quasi-isotropic (45/-45/0) pattern. To ensure adequate electrical conductivity, it is co-cured with the bus cable, made from a Kapton sheet with 3- μm thick and 0.5-mm wide copper traces; one side provides high voltage (HV) to the sensors, a 6×6 mm copper mesh on the other side grounds the carbon fiber. The Rohacell core under the hybrid board is replaced by a copper heat sink to remove ~2 W of heat generated by the ASIC preamplifier chips. At the downstream end of the module, the Rohacell core is replaced by a PEEK insert. The cross-section of the active area of the module is shown in Fig. 7.

A pitch adapter matches the $156\text{ }\mu\text{m}$ sensor readout pitch to the $50\text{ }\mu\text{m}$ FSSR2 bonding pad pitch. The pitch adapter [5] is a glass plate 41.5×4 mm (tolerance of

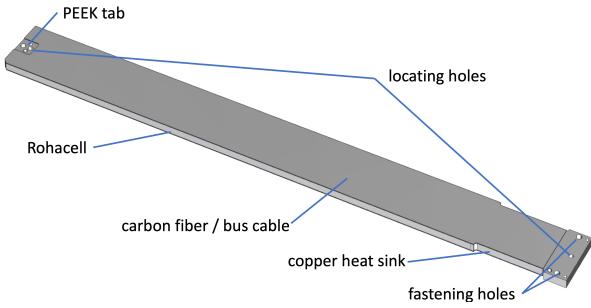


Figure 6: The module backing structure.

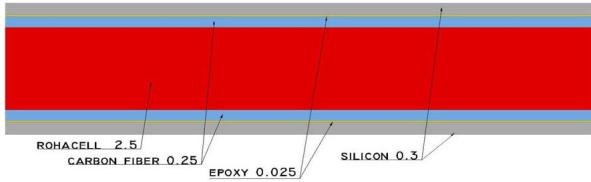


Figure 7: The cross-section of the module. The dimensions are in mm.

50 μm), with metal traces made of aluminum and copper alloy. The alloy improves electromigration hardness and bonding. The metal layer is sputter deposited. The passivation silicon oxide layer protects the soft aluminum traces from damage. There are two fiducials on the pitch adapter edge next to the sensor and three on the edge next to the hybrid to facilitate alignment. No more than one open trace or two short-circuited traces are allowed per pitch adapter. A section of the pitch adapter is shown in Fig. 8.

Both sides of a module are instrumented with a read-out system by a single rigid-flex Hybrid Flex Circuit Board (HFCB) located on the upstream end of the module (see Fig. 9). The HFCB provides bias to the silicon sensors, and power and control lines to four FSSR2 ASICs located at the edge of the hybrid, two on the top

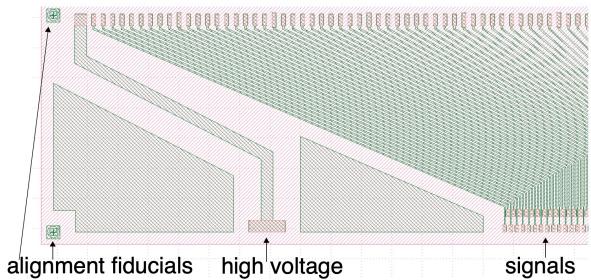


Figure 8: One end of the pitch adapter mask, showing the alignment fiducials, wire bonding pads, and traces.

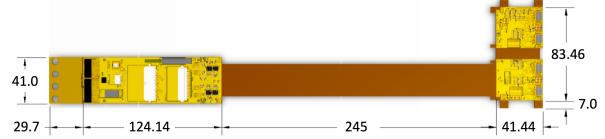


Figure 9: Hybrid Flex Circuit Board (HFCB). The level one connect board (left side) is connected to the hybrid area (right side).

and two on the bottom side. The ASICs are glued to pads on their substrates with conductive epoxy. These pads are the reference for the analog return for the chips. The hybrid area of each HFCB (42 x 82 mm) consists of two rigid boards (top and bottom hybrids) connected by a 10 mm-long wing flex High Density Interconnect (HDI) cable wrapped around the backing structure (see Fig. 10). The transition line from the rigid board to the flex cable was strengthened. Both hybrids connect to the module electrically using micro-bonding technology for the signals and bias return, and solder connection for the detector bias and module support ground. The sensors, the pitch adapters, and the HFCB are glued to both sides of the backing structure.

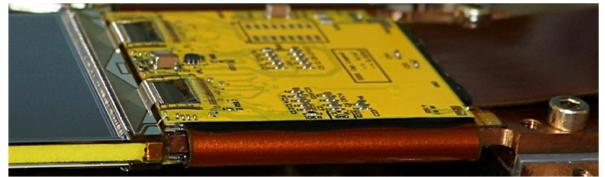


Figure 10: The wrapping of the HFCB from the top to the bottom silicon layers.

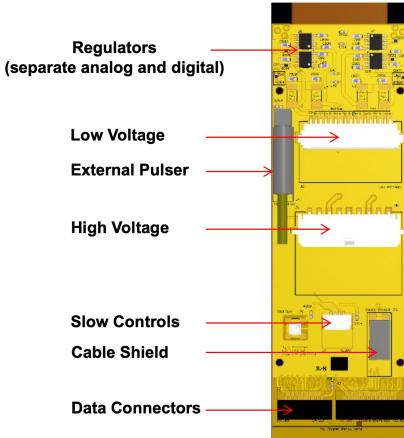


Figure 11: HFCB level one connect board.

Module services are provided via the level one connect (L1C) board (125 x 41 mm) coupled to the hybrid area via the upstream flex HDI cable (245 mm). The upstream flex HDI cable is routed through 10 mm radial slots in the cold plate. The L1C board hosts two high density Nanonics connectors for data and control lines, Molex Micro-Fit 9-pin connector for high voltage (~85 V) bias to the sensors, AMP Mini CT 17 pin connector for low voltage (2.5 V) power to the ASICs, hybrid temperature connector, external pulser connector, and four voltage regulators (see Fig. 11). The L1C board is mounted to the support tube on its own support structure designed to keep each L1C board positioned in line with its module.

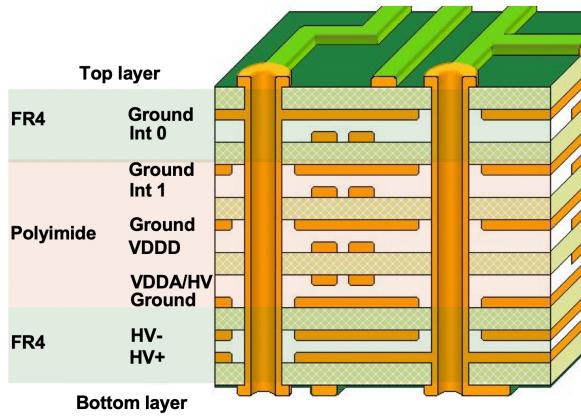


Figure 12: HFCB 12-layer stack-up.

The HFCB layer stack up (see Fig. 12) consists of six layers of flexible polyimide sandwiched between two triple layers of rigid FR4 (Flame Retardant glass-reinforced epoxy laminate material). The stack up varies from section to section, the flexible sections (wing and upstream flex) only contain the polyimide, whereas the rigid areas contain all 12 layers. This variation in stack up provides the ability to instrument both the top and bottom sides of each module and to pass through the cold plate to the L1C board mounted on the support structure. The two outer layers of the flex stack are the top and bottom shields, which are solid copper pours used to improve signal integrity by providing shielding and references for the differential signals. The top and bottom layers are made from 1 oz copper, while all the inner layers are made from 0.5 oz copper. The thickness of the rigid boards is 1.42 mm and the thickness of the flex cable is 0.5 mm.

Design of the HFCB reflects recommendations given by the experts in low noise electronics during the SVT technical reviews. Separate planes are provided for ana-

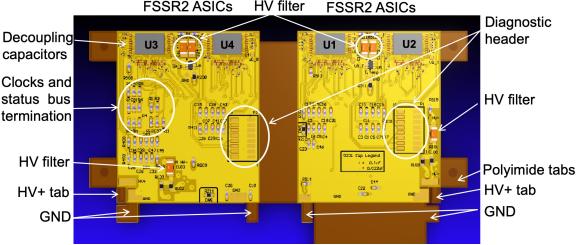


Figure 13: Hybrid side of the HFCB.

log (VDDA) and digital (VDAA) power on each side of the hybrid. To reduce noise on these planes, all chip voltage lines are decoupled from the low voltage (LV) return with capacitors near the chips. High voltage filter circuits and the bridging of the high and low voltage return lines are located close to the ASICs (see Fig. 13). Decoupling capacitors for power transmission are placed at the transitions between the flex and rigid materials. All data, clock, status, and register traces (Int0 and Int1) are routed with no crossing of the splits in the reference planes. All clock traces are separated from other differential signals by guard traces that are stitched to the ground planes with vias. The trace width of the guard is 10 mils. No clock signals are routed under the chips to minimize cross talk. All power lines are decoupled from the ground (GND) using 2.2 or 4.7 μ F capacitors close to a transition in the printed circuit board (PCB) material (flex to rigid). Sensor bias lines are separated from the data lines by the guard traces. The clocks are terminated at the end of the pair line with two 50 Ω resistors in series between the low voltage differential signal (LVDS) pair, with a 0.1 μ F termination capacitor at the node between the resistors and the ground. There are temperature sensors located between the two FSSR2 chips on each side of the HFCB for monitoring purposes. In the hybrid areas, the bottom layer is used to transfer heat from the chips to a copper insert built into the module support core.

Thermal and structural final element analysis (FEA) on the SVT detector elements was performed using ANSYS [6]. The deflection in the detector was analyzed for an individual module and for a region as a whole. The deflection was calculated based on gravitational load on the module. On the upstream end the module was assumed to be fixed since it is fastened to the upstream support ring of the detector. On the downstream end a simply supported condition was assumed since it is supported by the downstream ring. The maximum deflection of a module due to gravity is 14 μ m (see Fig. 14) due to excellent mechanical rigidity of silicon sensors

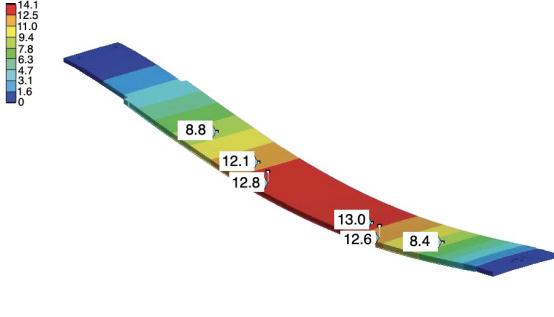


Figure 14: Deflection of an individual horizontally oriented SVT module due to gravity.

and carbon fiber support. The deflection of the downstream ring is less than $7 \mu\text{m}$. The vertical modules in the barrel minimize the deflection in the downstream ring making it a fairly rigid structure. The deflection of the entire SVT is $230 \mu\text{m}$.

For the thermal analysis, the module was modeled with the copper support and the heat sink insert. The heat output from each module is about 2.5 W . Cooling the cold plate with coolant flowing in the copper tubes that are brazed into the cold plate at -20°C , at a rate of 2 liters per minute, results in a temperature differential of the coolant between the inlet and outlet of the cold plate to be less than 1°C . The temperature distribution on the module is shown in Fig. 15. The maximum temperature of the sensors at the readout end is -10°C . The variation in temperature from the upstream end of the Hybrid sensor to the downstream end of the Far sensor is about 1°C . All components of the cooling system are outside of the tracking volume.

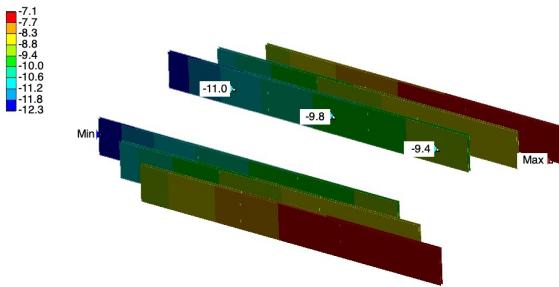


Figure 15: Temperature distribution along the SVT module.

2.3. Module Assembly and Quality Assurance (QA)

The position resolution of the detector can be compromised if the alignment is not known. Due to tight

material budget restrictions there is no room for an individual module adjustment system. Strict positional tolerances are imposed so that minimal corrections need to be made to the measurements. Therefore, both the position of the sensors with respect to each other and with respect to the alignment points are measured and controlled during module production. A mechanical survey was carried out before electrical testing to check that the module fits within a well-defined envelope and to ensure no interference with adjacent modules on the support structure. The SVT modules were assembled at the Fermilab Silicon Detector Facility and tested at Jefferson Lab. Prior to installation on a module, all components were inspected and tested as part of the quality assurance procedure.

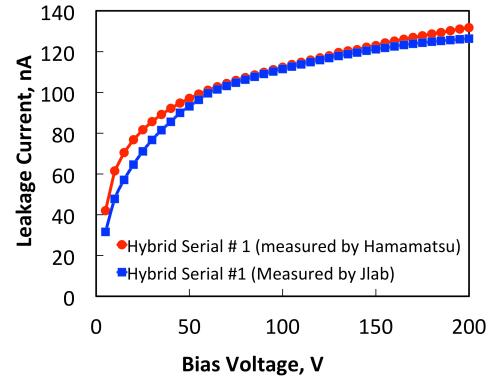


Figure 16: Typical IV-curve of the silicon sensor.

Sensor characterization was initially carried out by the manufacturer and later confirmed by the reception testing at Jlab and Fermilab. Fig. 16 shows the typical IV-curve for the hybrid-type sensor. Sensor leakage currents and the number of bad strips were within the specs and matched the data supplied by the vendor.

The measurements of sensor full depletion voltage were done by testing the dependence of its capacitance on the reverse bias voltage. Fig. 17 shows good agreement of the data obtained at different test facilities. The full depletion voltage data were found to be within the specs.

The initial tests for continuity, shorts, and current draw on the FSSR2 chips were done by TestEdge, Inc on the wafer level prior to the dicing. The yield was 99%, 8 failures out of 520 chips. A more detailed testing of individual chips after the dicing was performed at JLab. Fig. 18 shows the probe card used for the quality assurance of the readout chips. The measurement procedure included register testing (read/write), loading and reading back the mask, measuring channel inefficiency,

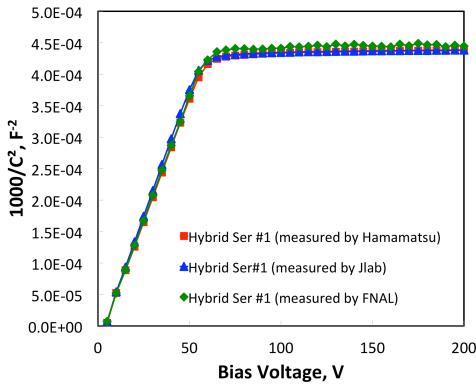


Figure 17: Comparison of CV plots of the sensor done by the vendor with measurements at JLab and Fermilab.

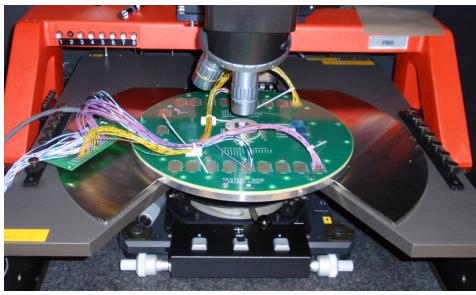


Figure 18: FSSR2 testing in the probe station.

gain, noise, and threshold dispersion. 330 chips were tested with yield over 90%. No additional dead channels have been observed in the modules produced from the tested chips.

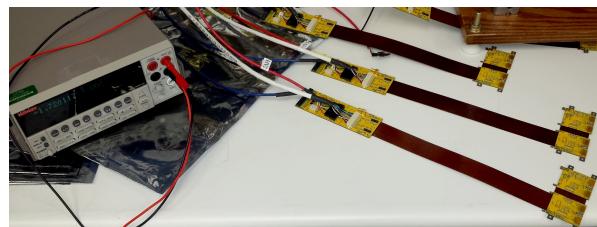


Figure 19: Electrical test of the HFCBs.

Fabrication and primary quality control of the HFCBs were done by Compugetics. A variety of mechanical mock ups using different 12-layer stack-ups were used to evaluate the bend radius of the wing flex cable. Boards passed the bending test were sent to the Micro-Craft company for a comprehensive automated electrical testing. HFCB assembly was done by Compugetics inc. using automated pick-and-place component mounting system with thermal profiling reflow system, and au-

335 tomatized inspection process. Reception test at JLab included visual inspection, resistance measurements, and burn-in. Acceptance testing of the HFCBs at JLab is shown in Fig. 19.



Figure 20: Bus cable routing.

340 Fabrication of the backing structure was done in the carbon fiber laboratory at Fermilab. To make a bus cable skin for the backing structure, the bus cable panel was laminated on the sheet of the carbon fiber and co-cured in the oven at 250 F. The layout of the six bus cables on a panel has a minimum of 5.05 mm between adjacent cables on the panel to allow for the 1/8-inch diameter routing bit (see Fig. 20). After the routing step the components of the bus cable (two bus cable skins and Rohacell core) were examined under the microscope and selected for the next fabrication step.



Figure 21: Assembling the backing structure in the mold.

350 To assemble the backing structure, a mold and an epoxy that cures at room temperature were used (see Fig. 21). The backing structures were cured on a precision jig to satisfy the required tolerances. Backing structure flatness was within 250 μ m.

355 Each module has two pairs of mounting and fiducial holes in the copper heat sink and one in the PEEK insert (see Fig. 22). After a module was fabricated, the positions of these fiducial holes were measured with respect to the fiducial marks etched on the sensor.



Figure 22: Assembled backing structure.

360 The holes for the mounting pin have a tight diameter tolerance and are used for module alignment. The slot
365 in the PEEK insert has a tolerance of $5 \mu\text{m}$. To accurately control the width of the backing structure, post-
machining of the width at the downstream end and near
370 the pitch adapter is done. After post-machining of the
precision edge, any foam exposed due to that process
375 was encapsulated with 3M DP190 epoxy. QA procedure
for the backing structures included CMM inspection of
flatness and precision width, testing bus cable HV and
ground connections. Module dimensions and mounting
holes were within the specs. The edges of the backing
structure are covered with Kapton tape to insulate the
carbon fiber from the back side of the sensors (Fig. 23). It
was found during testing of the pre-production modules
that without the tape the thin carbon fibers could
create a parasitic path from the backing structure ground
to the sensor bias contact.

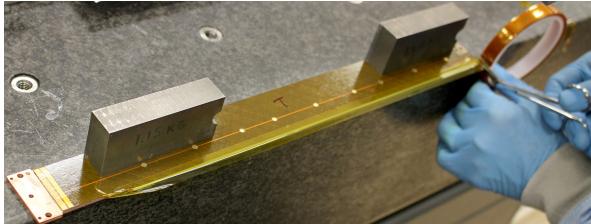


Figure 23: Insulating the edges of the backing structure.

380 Installation of the HFCB onto the backing structure
385 was done in a special fixture (see Fig. 24). Backing
390 structure was pinned to the base plate with alignments
400 tabs on the HFCB setting its position. Bottom side glued
405 and allowed to cure. HV and GND tabs were soldered
410 to bus cable, then the backing structure was flipped over
for glueing of the top side of the HFCB, followed by
soldering the HV and GND tabs and cutting off the align-
ment tabs. Visual inspection and electrical testing were
done by the JLab crew.

390 Sensor placement was done in the fixture shown in
Fig. 25. The backing structure with mounted HFCB was
395 attached to the fixture with a clamp. The vacuum chan-
nels in the fixture were used to ensure the planarity of
the backing structure. The epoxy glue was spread on the

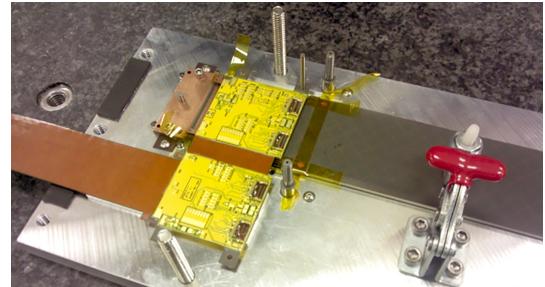


Figure 24: Installation of the HFCB onto the backing structure.

surface of the backing structure, then the sensors were placed and aligned within few μm with respect to the insert and sensor fiducials in the coordinate measuring machine (CMM). The weight block wrapped in Kapton tape was holding the sensor during the curing process. Sensor alignment and flatness were within the specifications, most sensors were aligned within $5 \mu\text{m}$.

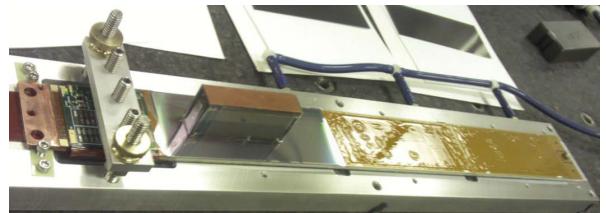


Figure 25: Mounting the sensors on the backing structure.

400 After installation of the HFCBs and pitch adapters,
the module was placed in a carrier box designed to al-
low storage of partially and fully fabricated modules
(see Fig. 26). The design of the carrier box provides
secure mounting of the double-sided module using the
location pins with the screws in the copper and PEEK
405 inserts. The flex cable is secured with a clamp. The
module can be powered, cooled (using a passive heat
sink), and operated in the carrier box. The carrier box
allows access to both sides of the module to facilitate
410 inspection and debugging.



Figure 26: SVT module carrier box.

Wire-bonding of the backing structure, sensors, pitch
adapters, and the readout chips was done on the same

fixture which was used for sensor placement. Functionality of the readout was performed after the wire-bonding step on each side. Fig. 27 shows an SVT module being wire-bonded. Visual inspection of the wire-bonds was part of the module quality assurance procedure.



Figure 27: Wire-bonding of the SVT module.

Module performance tests were done at various stages during module production at Fermilab. A 420 72-hour burn-in test was done on all the modules before the shipment. All modules were shipped with the individual travelers containing the part numbers and the survey 425 data for the module components, the results of the quality assurance measurements and calibration data. The tested modules were transported to Jefferson Lab in carrier boxes inside a cushioned container with a shock logger (Fig. 28), mounted in a wooden crate on the shock absorbers. Quality assurance measurements were 430 repeated during the reception test and assembly of the SVT at Jefferson Lab.



Figure 28: Modules in the container before shipment.

2.4. Detector integration and commissioning

Barrel integration took place at Jefferson Lab. The regions were assembled in sequence. The assembly was 435 done in a vertical position on a square table with suspension and leveling system. Positioning the barrel vertically allows access to all modules of the region being

assembled and facilitates strain relief of the cables during testing. Region 1 (innermost region) was assembled first, followed by Regions 2 and 3. The modules were mounted on the dowels inserted in the rings by holding the module by the two handling rods that were screwed into the inserts (see Fig. 29).

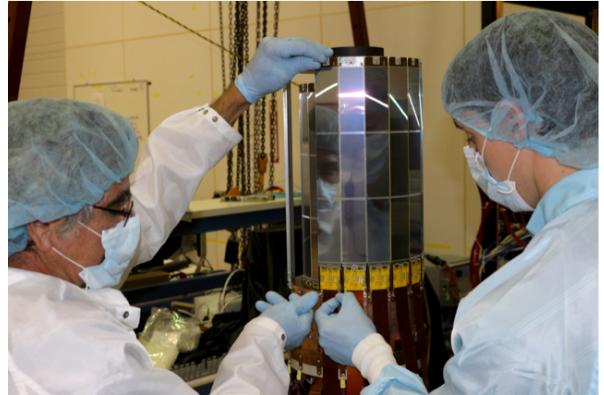


Figure 29: SVT assembly in progress.

Fig. 30 shows he close-up photo of the adjacent modules on the barrel, demonstrating the two readout chips encapsulated on 3 sides, wire-bonded to the HFCB, the pitch adapter, and the sensor. The barrel installation procedure was tested successfully, no modules were damaged during the region integration.

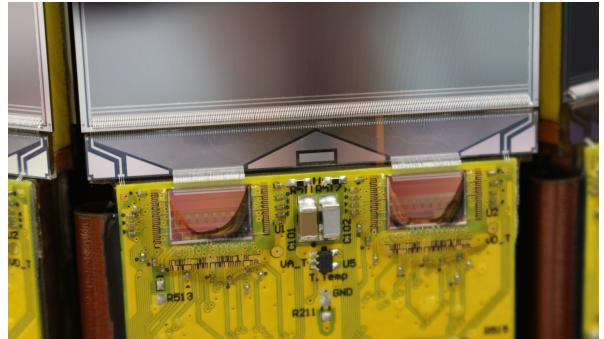


Figure 30: The close-up photo of the adjacent modules on the barrel.

The upstream support ring is fastened to the cold plate by a single screw for each of the copper module supports. This ensures good thermal contact between the inserts on the cold plate and the module supports of the upstream support ring. A layer of thermal grease was applied between the mating surfaces. The cold plate and upstream ring were then mounted to a mounting tube. The larger flange on the mounting tube rests on the assembly table.

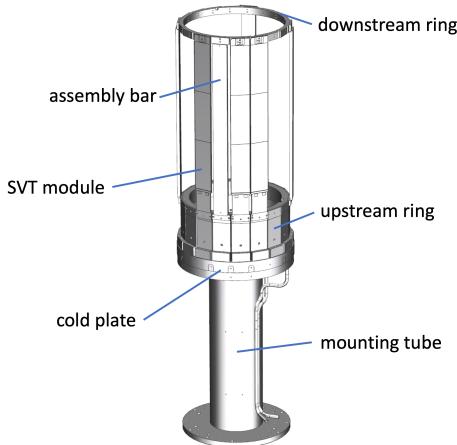


Figure 31: Region assembly schematic.

The downstream ring is supported by four aluminum region assembly bars (see Fig. 31) fastened to it to provide stiffness to the ring during assembly. These bars have accurately positioned holes and precision mounting surfaces to position the downstream ring. As the modules are mounted around the polygonal rings the assembly bars were replaced by the modules one at a time. The mounting surfaces of the upstream and downstream rings were machined simultaneously to reduce twist in the module that could result from the two surfaces not being co-planar. The holes for locating pins and tapped holes for fasteners on the upstream and downstream rings were also added at this stage. Once the downstream ring is in position, a CMM was used to establish a coordinate system for the detector and a central axis for the detector based on fiducials machined onto the flange of the mounting tube and the tooling plate on the downstream ring. The downstream ring has holes in it for accommodating the dowels and screws used for locating and mounting the module on the downstream end. The module has a slot machined into it that accommodates the locating dowel. This constrains the module in the tangential direction without constraining it in the axial direction. The other holes were used for surveying the module location and for handling the module during assembly. There are three fiducial points on each module, two on the upstream copper insert, and one on the downstream PEEK insert. The Fig. 32 shows the inner Faraday cage and the downstream end of region 1 modules with plastic dowels and the screws in the PEEK insert holding the module on the downstream ring. Also seen the fiducial hole and the screw hole for the mounting rod used to hold the module during the installation. The design of the backing structure provided

2 soldering pads for the surface-mounted decoupling capacitors. Results of the common mode testing demonstrated that they were not necessary and the capacitors were not staffed.

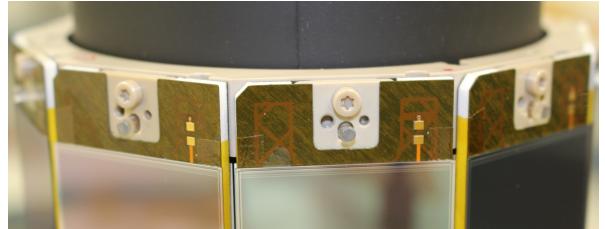


Figure 32: Downstream support of the module.

The rings of each region are independent from each other to prevent over-constraining the assembly. When the inner region was assembled, a light-tight Faraday cage was installed, nitrogen was flushed through it, and the modules were cooled with a portable chiller. The chiller was using water as coolant and the temperature was set to 10°C. The process of installing the Faraday cage is shown in Fig. 33. The space between the inner shell of the cage and region 3 sensors is small. A system of 3 aluminum rails was installed on the assembly table to guide the cage over the barrel and preserve the shape of the carbon shell during the installation.



Figure 33: Installing the Faraday cage.

The barrel was placed in the dark box and tested for functionality and noise performance. Fig. 34 shows the L1C boards of region 1 attached to the mounting tube with cables connected. The slow controls and the interlock system was in place to protect the SVT during the test.

After confirming the stable operation of the inte-

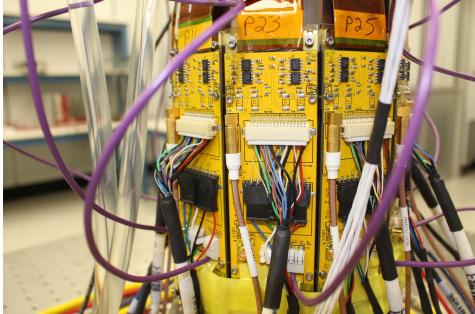


Figure 34: Cable connections during the performance test.

grated modules, the assembly proceeded with the next region. First, the upstream ring was mounted using the region assembly fixture. The fixture has a mounting ring suspended on the vertical rods which can slide in vertical and horizontal directions. The upstream ring was attached to the mounting ring, moved on the rails in the fixture, slid over the inner region and secured to the cold plate with the screws. This design allows an entire region to be removed as a unit, rather than module by module. Fig. 35 shows the process of region disassembly. Regions 1 and 2 are still integrated and mounted on the assembly table. Region 3 is removed and placed on a dedicated support structure on the cart.

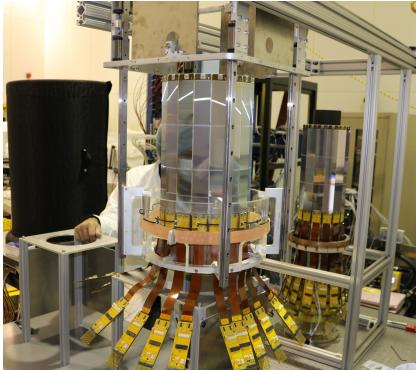


Figure 35: Region disassembly.

Upon completion the assembly of each region, the locations of the fiducials on the downstream and upstream rings were measured with respect to the coordinate axes with a precision of $\sim 20 \mu\text{m}$ using a FaroArm Quantum CMM. The displacements between the measured and ideal positions of the fiducials are within a fraction of a mm in X, Y, and Z axes. Fiducial displacement in XY plane is shown in Fig. 36. The misalignment shifts of survey positions from the ideal geometry were taken

into account by the alignment software.

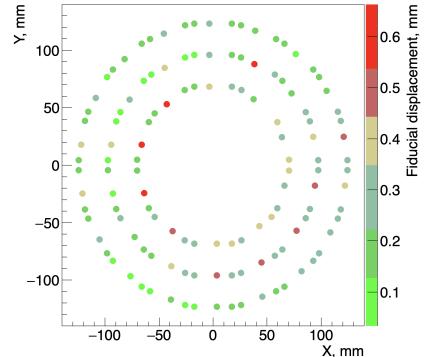


Figure 36: Fiducial displacements in XY plane measured in the survey.

After placement of each module on the support, all the modules on the support were re-tested to find and resolve problems with cables routed on the outside of the cylinder.



Figure 37: Assembled barrel.

Fig. 37 shows the barrel after integration mounted on the assembly bench.

After assembling each region the functionality of the integrated modules was checked. When barrel assembly was complete, it was moved to the transportation cart and rotated to a horizontal position using a special transition fixture. Fig. 38 shows the model of the cart with the SVT barrel mounted on the transition fixture in vertical and horizontal positions. Fig. 39 shows the process of rotating the assembled barrel. Safety locks of the fixture prevented accidental moves of the barrel during the rotation procedure.

The SVT support tube was mounted on the integration cart (see Fig. 41) using a crane and a mounting fix-

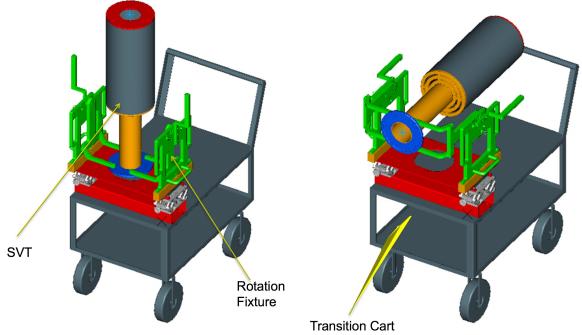


Figure 38: Barrel rotation with the transition fixture.



Figure 39: Rotating the assembled barrel.

ture placed on the parallel rails. The adjustment links on the cart allow for the SVT to be aligned with the support tube. Fig. 40 shows attaching the SVT barrel to the support tube using the transition fixture. The fixture allows fine adjustment of the barrel in vertical and horizontal directions. The survey of the fiducials on the support structure was performed and alignment of the barrel was done by shimming the support tube and adjusting the mounting fixture links.



Figure 40: Attaching the SVT barrel to the support tube.

The mounting fixture with attached barrel was moved

to one side of the integration cart and locked into place. At this time, all cables and cooling lines were connected to the SVT (see Fig. 42). The cable bundles were secured to the support tube using the nylon eyebolts on the tube and connected to the readout electronics crates.

The detector was tested and commissioned with cosmic rays. The integration cart was enclosed in a protective cover, the wheels were placed in the suspension pods, and the cart was transported to the experimental hall on a truck. In the hall the SVT was craned off the integration cart and mounted on the service cart. The cart hosts all detector services and is movable along the beam axis for easy maintenance.

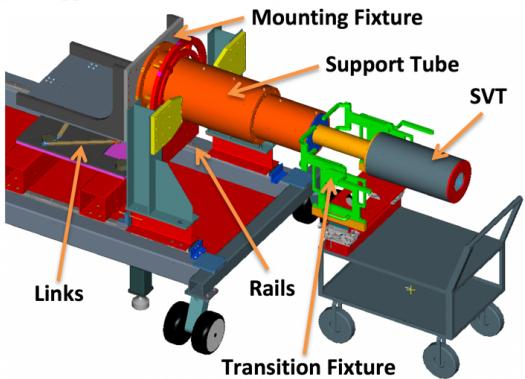


Figure 41: Integration cart.

After installation in Hall B, the SVT was tested with the services that are used to operate the SVT during data-taking. A series of runs was performed with and without the beam and with and without the magnetic field, four configurations in all. For each of these configurations, the tests for the module performance were repeated. Tests at later stages were aimed at finding problems with data acquisition and services, such as with the power supplies and cables, in order to ensure that no common mode noise was added to the system due to improper grounding and shielding.

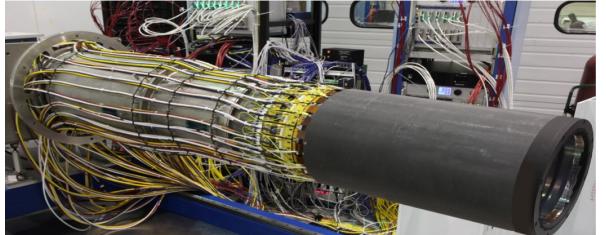


Figure 42: SVT barrel after integration.

3. Hardware Components and Construction

3.1. Cooling and air purging system

The SVT regions are cantilevered off a chilled cold plate that is designed to remove the heat generated by the electronics and to provide operational conditions for the sensors. External cooling has been chosen over internal cooling (tubes in the modules) to keep the amount of material in the active area as low as possible. The front-end electronics provide 5 W per module, with the 42 total modules producing 210 W. The HFCB flex cables are routed through 10 mm slots in the cold plate. The cold plate (see Fig. 43) includes a copper plate with brazed copper 0.25 in inner diameter tubes and a PEEK plate on the upstream side. The sensors are cooled by cold air. The coolant lines to and from the cold plate are placed inside of 0.5 in diameter nylon tubes. Air flows inside the 0.5 in tubes, outside the coolant tubes, to cool the air. The air flows out of the 0.5 in tubes through the holes in the cold plate, into the sensor area.

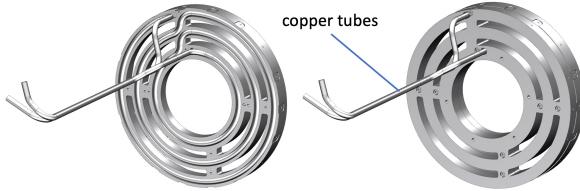


Figure 43: Copper tubing lines brazed to the copper cold plate (left) and the fully assembled cold plate (right).

Coolant (Dynalene HC50) is flowing with a rate of 2 liters per minute at a temperature of -25°C. The cold plate upstream cover is made of PEEK plastic. Dry air flowing through the slots in the cold plate is cooled by the liquid coolant circulating in the tube inside the air purging line (see Fig. 44). With 100 liters per minute of chilled air flow across the cold plate, the sensors are cooled to the operational temperature of -10°C. The Faraday cage cap on the downstream end has 4 holes to ensure the flow of cold air along the barrel.

The outer shell of the Faraday cage is insulated with 3-mm-thick neoprene sheet. The barrel is protected from environment humidity by purging dry air between the scattering chamber and the inner shell of the Faraday cage and between the outer shell of the Faraday cage and the protective plastic cover (see Fig. 45).

3.2. Slow controls and detector monitoring

Ambient conditions inside the detector are monitored by temperature and humidity sensors installed on the

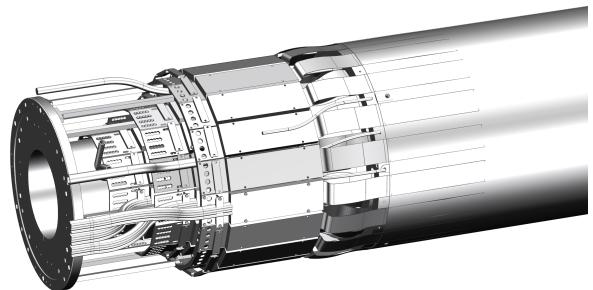


Figure 44: Dry air flows past connectors, through the slots in the cold plate, into the Faraday cage, past sensors, and out through the holes in the cap.

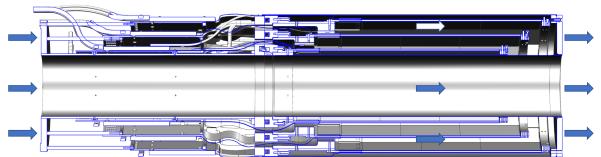


Figure 45: Cross section of the SVT detector showing the dry air flow.

upstream rings (see Fig. 46). There are 3 ambient sensor boards glued in the dedicated slots on the inner side of the rings in regions 2 and 3. There are 2 temperature and 2 humidity sensors on each board for redundancy.

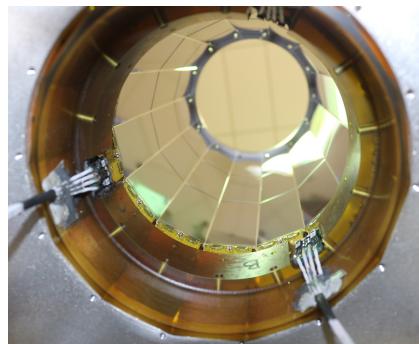


Figure 46: Ambient sensor boards mounted on the upstream rings.

Safe operation of the tracker is ensured by Experimental Physics and Industrial Control System (EPICS)-based real-time monitoring of all important operation parameters and status of the hardware components [7]. The software and hardware interlocks continuously monitor the critical system parameters. A multi-level user interface provides safe operation of the SVT by the shift crew and all necessary tools for the system experts (see Fig. 47).



Figure 47: User interface for the SVT slow controls overview.

The SVT Hardware Interlock System (HIS) is a backup system designed to protect the detector from damage in case the main control system fails or if network communication is lost. This is a standalone system independent from the main EPICS-based slow controls system and does not rely on network communications to safeguard the SVT detector. The HIS is based on the National Instruments CompactRIO (cRIO) Programmable Automation Controller (PAC) platform. cRIO is a reconfigurable embedded control and acquisition system. The cRIO system's hardware architecture includes I/O modules, a reconfigurable field-programmable gate array (FPGA) chassis, and an embedded controller. The HIS monitors key detector parameters and takes corrective action if a monitored signal is outside of pre-programmed limits. The signals monitored include: HFCB temperature, ambient and detector temperature, humidity, and dew point, coolant flow, pressure, temperature, and coolant leak detection (see Fig. 48).

Under fault conditions, the hardware interlock system disables the MPOD HV/LV crates via the front panel connector on the MPOD controller. When disabled by the HIS, the EPICS controls are overridden and all channels of the MPOD crate ramp down at their pre-programmed rate. A reset of both the HIS and the EPICS MPOD control is needed in order to re-power the HV and LV channels. Under fault conditions, the HIS shuts off the AC power to the SVT chiller.

The HIS is the last line of protection for the detector. If the main EPICS slow controls system works correctly,

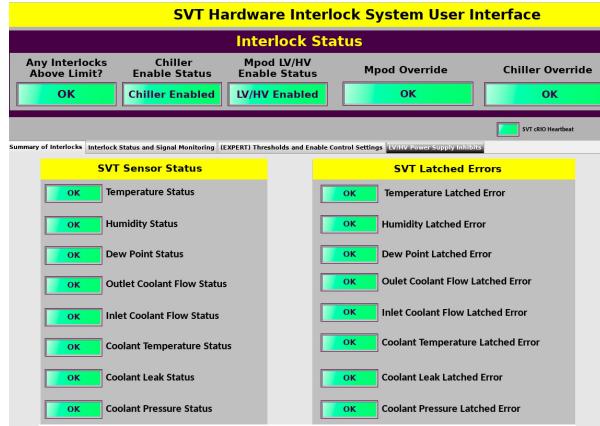


Figure 48: User interface for the SVT hardware interlock system (HIS).

the HIS shall never need to take corrective action to protect the detector. The trip levels for the hardware interlock system are slightly out of bounds from the EPICS trip levels to prevent both systems from tripping at the exact same level. The EPICS slow controls system (if working correctly) shall always trip first before the HIS. The current status of the slow controls and interlocks is reported on the CLAS alarm handler.

The front panel of the HIS has two interlock keys. These keys allow system experts to update the cRIO system while the SVT detector is powered. These keys are normally locked in the enabled position during detector operation. The user interface to the HIS allows the operator to remotely monitor the SVT and to set interlock trip levels. The user interface is also used to reset the system after an interlock trip event.

The performance and stability of the system is tested at various operation temperatures. The observed sensor leakage currents are below 400 nA in normal operating conditions with coolant at -20°C. Humidity inside the barrel is kept at 2% by purging dry air. All critical detector operational conditions (currents, voltages, ambient sensor readings, interlocks etc.) are recorded in a MYA database [8] to evaluate system performance and stability.

Java-based data quality monitoring tools were developed to check detector performance both online and offline. The SVT detector monitoring interface is shown in Fig. 49. The tools allow for checking the status of track reconstruction and performance of the individual modules. Individual sensors can be selected from the SVT layout canvas on the left side of the interface. On the right side specific set of histograms can be selected with the tabs. The selected tab shows the distribution of

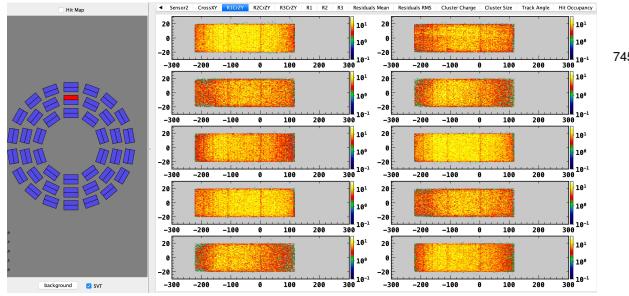


Figure 49: SVT detector monitoring interface.

the crosses for the first SVT region. The gaps between the sensors are visible.

4. Electronics

4.1. Grounding and shielding

In a comprehensive noise analysis, different configurations for the grounding were studied, to define and validate the final scheme. The signal from the aluminum readout strip is input to the FSSR2 ASIC. The returns of the floating high and low voltage supplies are isolated from the Hall B ground. To maintain the reference voltage level of the carbon fiber, the copper mesh on one side of the bus cable is connected at the hybrid area of the HFCB to the return line of the low voltage. Modules are read out by the FSSR2 ASICs located on the hybrid area of the HFCB. Power and readout connections are made at the L1C. There is no coupling of power or return lines of different modules – each module is independent of the other modules. All modules are electrically isolated from the detector support structure. Each crate in the system has a safety ground. To shield against electromagnetic interference, the cable shields – signal, power, slow control, and pulser – of each module are connected together at the L1C. The L1Cs of all modules are located at the entrance of the Faraday cage, and from each of the L1Cs a cable connects the shields to the Faraday cage, which in turn are connected by a single cable directly to the Hall B central ground (see Fig. 50). The SVT is placed inside a Faraday cage that comprises the cold plate, a forward disk, and a cylindrical carbon shell.

Common mode is of particular concern in digital read-out systems as it cannot be measured on an event-by-event basis thus a correction for common mode is impossible. It can only be estimated statistically. It is important to ensure that the input noise of the modules does not increase with services successively added to the system, as that would indicate problems in the

grounding scheme and common-mode noise has been introduced into the system. The analysis of the common mode noise validated the decisions made on grounding and shielding of the HFCB and the detector.

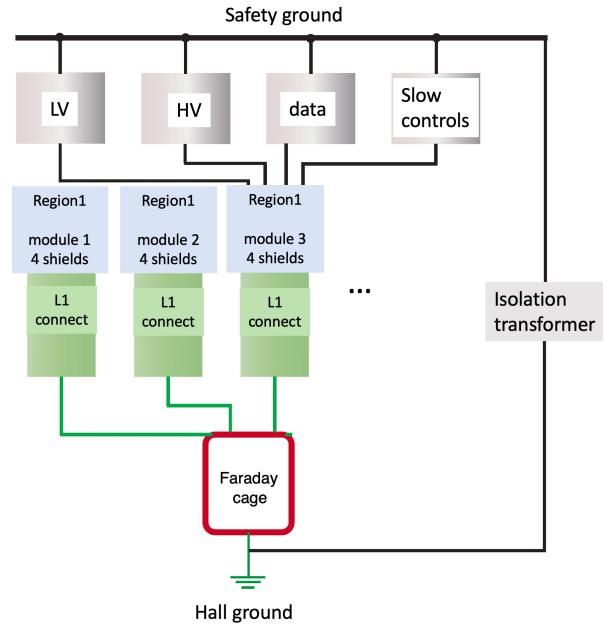


Figure 50: SVT shielding scheme.

4.2. Power supplies

Each side of a module has a high voltage channel, 80 V ($40 \mu\text{A}$), and two low voltage channels, 2.5 V (0.3 A). To power the FSSR2 ASICs and to bias the modules, Wiener's Universal Multi-channel Low and High Voltage System (MPOD) crates are used. The crates are 19 inches tall, rack-mountable, and capable of housing 10 low voltage Wiener cards or 10 high voltage Iseg cards, or a combination of the two (see Fig. 51). The output voltage channels of the cards are floating. All power supply channels have programmable voltages, ramp rates, and limits. Hardware limits on voltage and current can be set on each card. Local control of the crate and cards is available on the LCD front panel; remote control is facilitated by a 10/100 Ethernet connection.

For low voltage, the Wiener eight-channel low voltage cards are used. These cards have a peak-to-peak voltage (V_{pp}) ripple of 10 mV and are capable of providing up to 8 V at 5 A per channel via a 2 x 37-pin, sub-D connector. Each output channel has a 12-bit voltage setting and measurement resolution, as well as a 12-bit current monitoring resolution. To bias the modules, the



Figure 51: Wiener MPOD LX crate with mixed low and high voltage modules.

ISEG high precision, 16-channel high voltage cards are used. These cards have a V_{pp} ripple of 5 mV and are capable of providing up to 500 V at 10 mA via a Redel multi-pin connector. Each output channel has a 21-bit voltage setting and measurement resolution, as well as a 21-bit current monitoring resolution. Clean power, provided by shielded isolation transformers, is used for the high and low voltage power supplies.

5. Signals and Readout

5.1. Front-End Readout Electronics

There are 512 channels per module read out by FSSR2 chips, mounted on a hybrid. The FSSR2 ASIC has been developed at Fermilab for the BTeV experiment [9]. The chip (see Fig. 52) features a data-driven architecture (self-triggered, time-stamped). Each of the 128 input channels of the FSSR2 ASIC has a preamplifier, a shaper that can adjust the shaping time (50–125 ns), a baseline restorer (BLR), and a 3-bit ADC (see Fig. 53). The period of the clock called the beam crossing oscillator (BCO) sets the data acquisition time.

If a hit is detected in one of the channels, the core logic transmits pulse amplitude, channel number, and time stamp information to the data output interface. The data output interface accepts data transmitted by the core, serializes it, and transmits it to the data acquisition system. Thus, an irregular data flow is converted into data synchronized with the main clock frequency of the system. No time is allotted for transmitting stored information in the FSSR2 working cycle, i.e., the data arrive at the chip output directly after the signal is detected. The signal reception board should be permanently ready for receiving data, since the data can arrive at any moment. Therefore, the chip can operate only as a part of

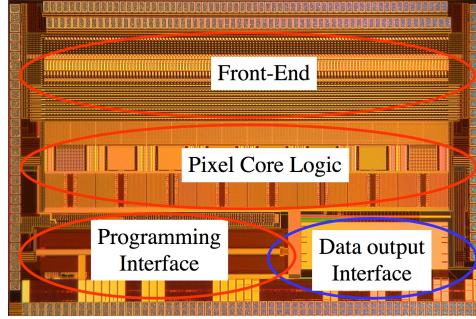


Figure 52: FSSR2 ASIC with the different functional areas labeled.

the software – hardware complex with the external controller tuned for the data waiting mode (time-variable data flow).

To send the 24-bit readout words one, two, four, or six LVDS serial data lines can be used. Both edges of the 70 MHz readout clock are used to clock data, resulting in a maximum output data rate of 840 Mb/s. The readout clock is independent of the acquisition clock. Power consumption is ≤ 4 mW per channel. The FSSR2 is radiation hard up to 5 Mrad. The choice of the readout chip was driven by its architecture and good noise performance at high capacitive load of long SVT strips.

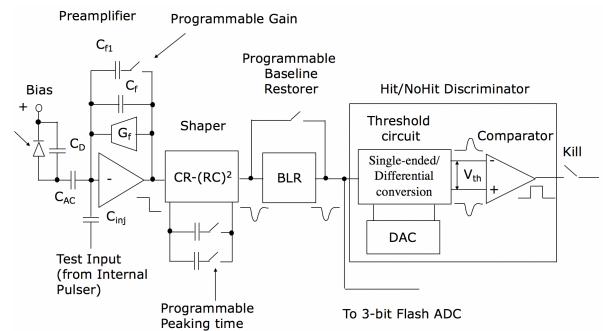


Figure 53: FSSR2 analog channels.

Each FSSR2 ASICs has six LVDS pairs with a source synchronous clock to transmit event data. The VSCM supports receiving data from all six LVDS pairs of each FSSR2 ASIC running at 70 MHz double data rate (DDR) (840 Mb/s from each FSSR2). Xilinx Spartan 6 FPGAs are used to buffer and deserialize data from two FSSR2 ASICs each. Four of these FPGAs are used to support eight FSSR2 ASICs' simultaneous data streams coming from two HFCB interfaces; the FPGAs in turn send their information to the master FPGA where the event builder resides.

The FSSR2 ASICs' architecture is such that it sends out 24-bit data words if a channel has a hit or a 24-bit status word if the channel does not have a hit (idle state) within a BCO clock cycle. The FSSR2 ASICs transmit these data over six lines. First, the data is deserialized. The 24-bit data words are appended with 8 bits to make the time range longer, and the 32-bit words are correlated to the trigger, which is generated by other detectors. The status words are suppressed to minimize the data size of an event. However, the status words are monitored to diagnose the performance of individual FSSR2 ASICs. Each channel has a memory cell for writing a single event. If the data on the event arrive into the cell, the channel is disabled, and the data presence signal is sent into the controller. The controller interrogates the channel with the detected event and produces a data word. The data are transmitted in a short time interval, and, after that, the channel is again ready for receiving signals. Under relatively low rates, when the interval between events is longer than the time required for reading a single event, data losses are absent.

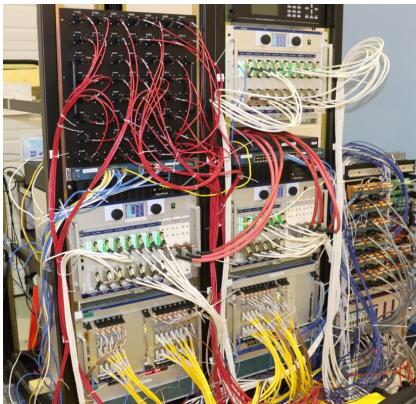


Figure 54: The SVT test stand installed in the clean room.

5.2. Back-End Readout

The four FSSR2 ASICs on the HFCB communicate with the VXS architecture-based segment collector module (VSCM), which configures the FSSR2 ASIC registers, provides analog calibration pulses to the FSSR2 ASICs, sets/monitors proper control signals (clock, reset, status), and acquires serialized event data from the FSSR2 ASICs. Each VSCM can interface with two HFCBs. Up to 16 VSCM cards can reside in a VXS crate. When multiple VSCM cards are used, additional cards, the Trigger Interface (TI), and Signal Distribution

(SD), are required to ensure event and timing synchronization. The VSCM supports a stand-alone mode, useful when only one or two HFCBs are used. The event builder of the VSCM uses the BCO clock timestamp from the data word of each FSSR2 ASIC and matches it to the timestamp of the global system clock, given by the CLAS12 trigger. The FSSR2 ASIC data is tagged with a global trigger timestamp (48 bits, 8 ns resolution). Since the BCO clock is derived from the global system clock, triggers received by the VSCM enable the event builder to extract hits with specific BCO timestamps that fall in a programmable time window within which the event could have occurred. When a trigger is received, the data words from the FSSR2 ASICs are copied to an event buffer and pushed into an event FIFO. These events can be read out in order with other modules in the system while event-level synchronization across all modules in the system is maintained. The VME interface provides for event readout, access to the configuration registers on the VSCM, bridges access to the registers of the FSSR2 ASICs, and provides an interface to the CPU. The A32 address space, 2 MB in size, is dedicated to the event builder FIFO, which can be read using single-cycle and block transfer VME protocols. Block transfer protocols are used for event readout; the 2eSST protocol planned for use is to maximize performance. The 2eSST protocols provide 200 MB/s sustained transfer rate and supports the proprietary Jefferson Lab token-passing scheme that allows a single direct memory access (DMA) operation on the CPU to transfer data from all VSCM modules sequentially, eliminating overhead (compared to individual board transfers). The VSCM is set up to extract event data within a programmable lookback window of $\sim 16 \mu\text{s}$ relative to the received trigger. The calibration pulser circuit provides a 2 Vpp dynamic range, up to 125 MS/s, and 14-bit resolution (for pulse height steps in sub mV increments). The bandwidth is sufficient to allow 10 ns rise times to be delivered over 15 feet of 50Ω coax cable terminated with 50Ω . Two independent pulser outputs are provided to drive both HFCB modules. The pulser signal phase can be placed in a deterministic phase relationship to the BCO clock that drives the FSSR2 ASIC.

During the SVT integration and testing a full-featured test stand (Fig. 54) accommodating production services (power supplies, DAQ, slow controls, alarm handler, purging, and cooling system) for the whole detector was installed in the clean room.

5.3. Expected Noise Performance

Sensor thickness and total length of the strips (33 cm) are defined by the technical requirements on the detector acceptance and energy spectrum of the registered tracks. The signal generated in 320 μm sensors is about 24000 electrons which makes essential to minimize all sources of noise and control the cross-talk.

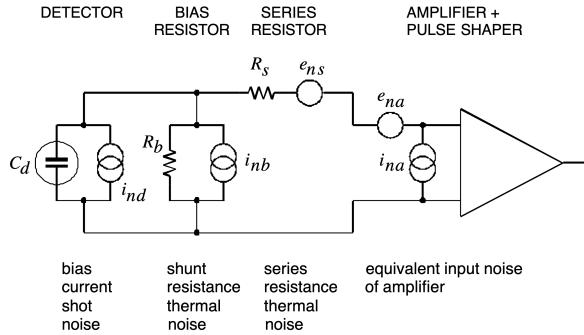


Figure 55: Equivalent noise circuit diagram. Serial noise sources are shown as voltage sources and parallel sources as current sources.

The equivalent circuit diagram of a silicon strip sensor with connected readout electronics is shown in Fig. 55 [10]. A single channel (3 daisy-chained strips) with capacitively coupled readout is represented by its total capacitance C_{tot} , a coupling capacitance C_c , the resistance of the connection line to the amplifier R_s , the bias resistor R_b and a filtering capacitance of the bias circuit C_b . The SVT sensor is measuring the charge deposited by the particles, thus the noise is quoted in terms of the Equivalent Noise Charge (ENC), defined as the charge that, if injected in the input, gives a signal-to-noise ratio of 1. All the noise sources of a circuit can be summarized and represented by a noise voltage v_{ni} appearing on the input of the amplifier. Internal capacitance of the amplifier C_i is connected in parallel to C_{tot} . The dependence of the ENC Q_n on the input capacitance can be parametrized as [11]:

$$Q_n^{RMS} = a + C_{tot} \cdot b, \quad (1)$$

where $a = v_{ni}^{RMS} \cdot (C_f + C_i)$, $b = v_{ni}^{RMS}$, and C_f is the feedback capacitance of the amplifier.

Parallel shot noise from reverse bias current I_b through the strip:

$$\frac{1}{q_e} \frac{e}{\sqrt{8}} \sqrt{2q_e I_b \tau} \approx 108 \cdot \sqrt{I_b [\mu\text{A}] \tau [\text{ns}]}, \quad (2)$$

where q_e is charge of the charge carriers and τ is the characteristic shaping time.

Parallel noise from shunt resistance R_b :

$$\frac{1}{q_e} \frac{e}{\sqrt{8}} \sqrt{\frac{4kT}{R_b \tau}} \approx A \cdot \sqrt{\frac{\tau [\text{ns}]}{R_b [M\Omega]}}, \quad (3)$$

where k is the Boltzmann constant and T is the temperature, A is the temperature dependent factor equal to 24 at 20°C and 22.5 at -10°C.

Series noise from metal strip resistance R_s :

$$\frac{1}{q_e} \frac{e}{\sqrt{8}} \sqrt{4kT \frac{R_s}{3\tau} C_{tot}} \approx B \cdot C_{tot} [\text{pF}] \cdot \sqrt{\frac{R_s [\Omega]}{\tau [\text{ns}]}} , \quad (4)$$

where B is the temperature dependent factor equal to 14 at 20°C and 13 at -10°C.

For non-irradiated sensors the shot noise from the measured sensor reverse bias current 0.05–0.4 μA (256 strips) at -10–20°C is within 20-50 electrons with the shaping time 125 ns and can be neglected. As demonstrated in expressions (3) and (4), the detector noise does not change much when sensors are cooled up to -10 °C. The contribution from the shunt resistance is about 200 electrons with shaping time 125 ns. Total capacitance of the strip C_{tot} including the wire bonds and the pitch adapter is ~45 pF. Metal strip (33 cm) resistance is ~230 Ω , which gives an estimate for the series noise ~850 electrons.

Fig. 56 shows the results of the FSSR2 noise measurements performed on a single-chip test board with discrete capacitors connected to the amplifier confirming linear dependence of the noise on the total capacitive load of the amplifier in the equation (1). The contribution from the amplifier itself is the dominant source of noise, mainly caused by shot noise and thermal noise on the current path of the transistors. Adding all sources of noise gives an estimate for the total ENC for the SVT channel ~1500–1600 electrons.

6. Calibration

Since the SVT modules are designed with a binary readout system, the analog channel response cannot be measured directly. Instead, the analog response is reconstructed by injecting a calibration charge on the channel and measuring the corresponding occupancy over a range of threshold values.

The output signals from the FSSR2 chip can be converted to charge using either internal or external calibration pulses. Because external pulser can be set to higher frequency than internal pulser without affecting the calibration process, external pulser circuit was added to the

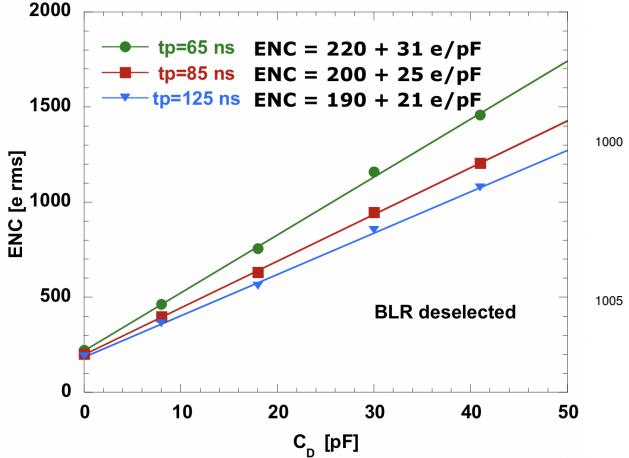


Figure 56: FSSR2 ENC vs. detector capacitance at different shaping time settings.

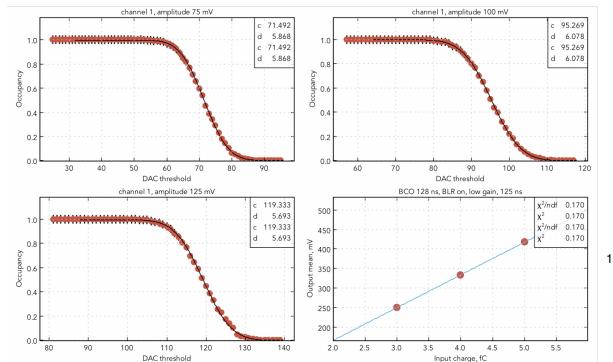


Figure 57: Threshold scan on a single representative SVT channel.

HBCB and the VSCM. Noise is measured using external, low frequency calibration charge injected in the absence of signal. The injected charge is shaped and amplified in the analog circuitry to form an output signal. The discriminator threshold determines whether or not the output signal corresponded to a hit. The probability that the injected charge produces a hit depends on the setting of the discriminator threshold. The average hit probability is measured by repeating the process of injecting charges and counting the fraction of readout triggers that produced a hit. This measurement is repeated over a range of threshold settings to produce an occupancy plot.

The occupancy plots are measured setting the pulser amplitude at fixed values and changing the comparator thresholds. Each point of an occupancy plot represents the percentage of times that the comparator fires for a

certain value of injected charge. In Fig. 57 presented three occupancy plots taken at different pulser amplitudes and the response plot showing the linear dependence of the output pulse height on the input charge in the operation region of the preamplifier. In between the high and low threshold regions, the occupancy curve is described by an error function, or S-curve, which can be fitted to the occupancy histogram for each channel, producing a mean value (discriminator threshold) and standard deviation (noise). The conversion from mV to electrons is performed considering a nominal value for the FSSR2 injection capacitance of 40 fF.

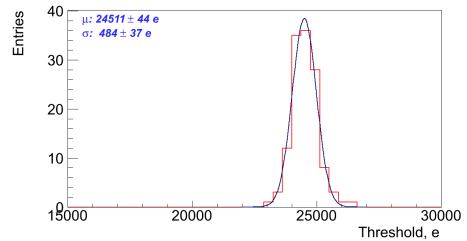


Figure 58: Typical threshold dispersion within a chip.

Threshold charge must be the same across the channels in a detector, otherwise the track-finding algorithms would be biased by the potential extra hits. Any spread in the response among the different channels of a chip results in a spread of the efficiency and noise occupancy which degrades effective performance. This leads to a requirement that the channel-to-channel variations in threshold and noise are kept to a minimum. Threshold dispersion is defined to be a standard deviation of the distribution of means obtained from the parameters of the complementary error function fit. The noise and threshold dispersion constants for each individual detector channel are measured and the values are used by the zero-suppression algorithms implemented in the core logic of the FSSR2 and by calibration procedures to identify defective channels. A comparison of the noise for 33 cm strips with the threshold spread demonstrates that the threshold spread is negligible compared to the noise and does not affect the efficiency and noise occupancy (see Fig. 58). The threshold dispersion agrees with expectations for the FSSR2 chip for the chosen settings.

SVT calibration data are stored in CLAS12 calibration database. The channel calibration table has columns corresponding to sector, layer, chip ID, mean, channel status (good, noisy, open, dead, or masked), ENC, gain, offset, V_{t50} (threshold at 50% occupancy), and the threshold. There are 21504 rows in the channel

calibration table. The ENC and gain are calculated using a calibration amplitude equal to 100 DAC. The chip calibration table has columns corresponding to layer, sector, chip ID, ENC (electrons), gain (mV/fC), offset (mV), the threshold at 50% occupancy (V_{150} , mV), threshold dispersion (electrons), chip gain (low, high), BLR mode (off, on), BCO time (ns), shaper time (ns), 8 ADC thresholds in DAC. There are 168 rows in the chip calibration table.

1045 7. Local reconstruction

The extraction of signals is done with a threshold set based on the signal-to-noise ratio. A hit is created when a pulse height on a channel exceeds a certain signal-to-noise ratio. To account for particle hits with signals shared by adjacent channels due to capacitive coupling, when the signals of neighboring strips exceed a threshold, they are added to the cluster. The number of strips in a cluster is called cluster size or cluster strip multiplicity. In a binary readout system, where the position information is derived from the strip with the highest pulse height, the root mean square of the spatial resolution is given by the readout pitch divided by square root of 12. FSSR2 is a binary chip and the 3-bit ADC is provided for the calibration purposes. Although the precision of the digitized pulse height is poor, it is still possible to use this information in the reconstruction to improve the spatial resolution compare to binary signal processing. The cluster position is determined from the centroid of the signal amplitudes by a center-of-gravity method using charge sharing between neighboring strips due to capacitive coupling.

8. Simulation

8.1. Detector simulation

A realistic model of the SVT has been developed, 1070 describing the location and composition of all modules, with material description based on the engineering drawings and assembly procedures, and confirmed by the survey measurements during integration. The SVT design and module layout were validated by Geant-4-based simulated detector performance studies demonstrating compliance with the technical requirements and 1075 engineering models. A 3D view of the simulated geometry of the SVT sensors is shown in Fig. 59. The SVT model is described in the simulation article of this volume.

According to the results of GEANT simulation of 1080 the SVT, a resolution of 50 μm in the bending plane

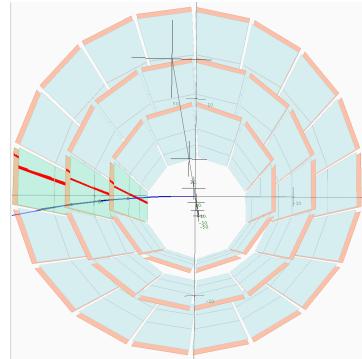


Figure 59: 3D view of the simulated SVT detector geometry.

is needed to measure, with a precision better than 5%, tracks with momentum up to 1 GeV (see Fig. 60) [12, 13]. At low momenta the degradation of the resolution is caused by multiple scattering.

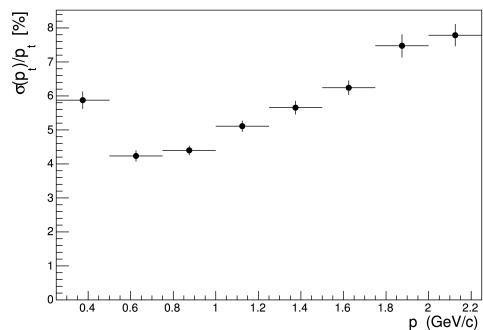


Figure 60: Simulated SVT momentum resolution.

Centroid residual distribution for the simulated muon tracks generated in the interval 0.5–2 GeV is shown in Fig. 61. Cluster centroids were calculated based on the charge weighting method. The spacial resolution of the sensors in the transverse plane using the ideal SVT geometry with no misalignments was found to be about 30 μm .

8.2. Backgrounds, energy deposition, dose rates

Radiation-induced bulk and surface detector damage studies have been conducted with charged hadrons, leptons, neutrons, and γ -ray photons. The radiation damage produced by different particles with different energies are scaled under the assumption of the Non-Ionizing Energy Loss (NIEL) hypothesis as the radiation damage in the silicon bulk depends only on the

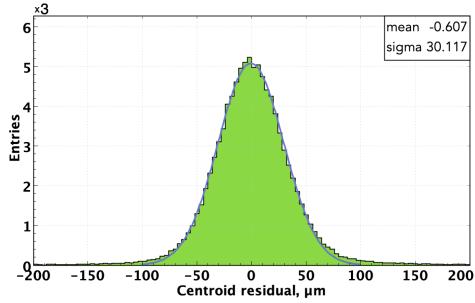


Figure 61: Simulated centroid residual distribution for the SVT module.

non-ionizing energy loss. The damage caused by different particles is referenced to the damage from 1 MeV neutrons. The standard value for the NIEL of 1 MeV neutrons is 95 MeVmb.

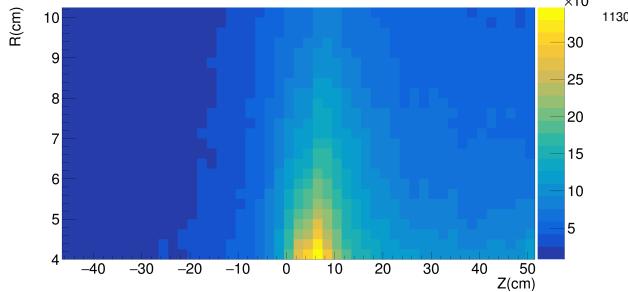


Figure 62: Accumulated 1MeV equivalent neutron fluence for the lead target.

To calculate the effects of different target configurations on the SVT detector, FLUKA [14, 15] simulations have been performed. In order to include the hadron electro-nuclear production, a dedicated source term has been used to enhance the physics production from the target, since it is a key in radiation estimates for targets with radiation length below 4%. To assess the radiation damage to the SVT, the accumulated 1MeV neutron equivalent fluence has been recorded corresponding to the planned run conditions. For the experiment with lead target, the expected exposure was 240 h at beam current of 38 nA with electron beam energy of 6.6 GeV (Fig. 62). For deuterium target, the study has been done for the accumulated charge of 108 mC at 11 GeV (Fig. 63). In both scenarios the expected doses should not cause substantial degradation of the silicon sensors.

FLUKA simulations of radiation damage levels have been performed in terms of 1MeV equivalent neutron fluence and high energy hadron equivalent fluence

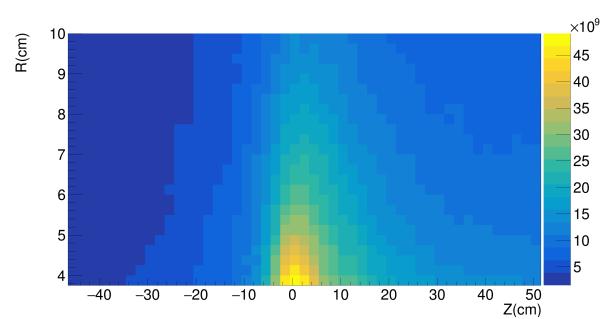


Figure 63: Accumulated 1MeV equivalent neutron fluence for the deuterium target.

which is proportional to the rate of Single Event Effects (SEE) [16]. Estimated levels of radiation damage in radial direction are presented in Fig. 64) for liquid hydrogen and carbon targets at nominal beam currents. Also shown the radiation levels for the tagger magnet yoke during the beam tuning (see the beam line section in this volume).

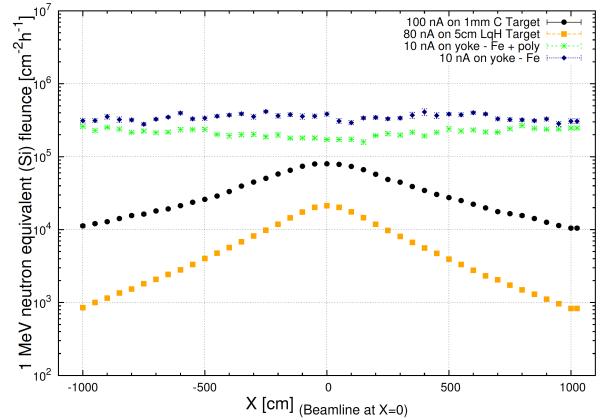


Figure 64: Estimated levels of radiation damage in radial direction in terms of 1MeV neutron equivalent fluence in silicon.

Simulations of beam-related backgrounds were performed for several thicknesses of a tungsten shielding cylinder around the CLAS12 target covering the first SVT layer.

Fluences, radiation doses, and 1 MeV neutron damage rates in the SVT were calculated for different particles. Rates were estimated for liquid hydrogen, liquid deuterium, carbon, iron, and lead targets. For each event, 124,000 electrons going through the target within a 248.5-ns time window were simulated. This corresponds to the full CLAS12' $10^{35} \text{cm}^{-2} \text{s}^{-1}$ luminosity on

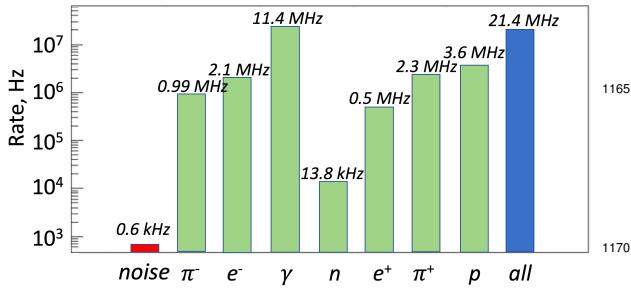


Figure 65: Rates in the first SVT layer for a 5-cm long liquid hydrogen target at the nominal CLAS12 operating luminosity of $10^{35} \text{ cm}^{-2} \text{s}^{-1}$.

a 5-cm-long liquid-hydrogen target at 11 GeV beam energy. Rates in the first SVT layer for a liquid-hydrogen target are shown in Fig. 65. For carbon target at a threshold of 40 keV the hadronic rate was estimated to be 5 MHz (total rate 40 MHz) with strip hit rates of 3.1 kHz (region 1), 2.2 kHz (region 2), and 1.7 kHz (region 3). The energy deposited in layer 1 for the electromagnetic and the hadronic particles is shown in Fig. 66. At a threshold of 30 keV, 92% of the electromagnetic background is rejected while preserving 99.5% of the signals coming from the hadrons [17].

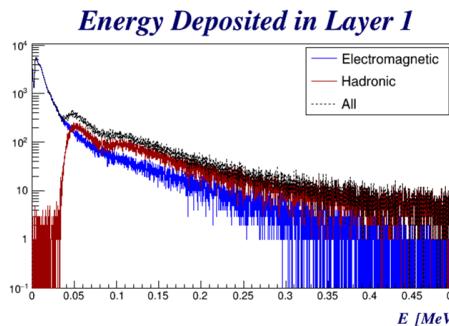


Figure 66: Energy deposited in the SVT layer 1 for electromagnetic and hadronic particles for a liquid hydrogen target at the nominal CLAS12 operating luminosity.

A tungsten shield 51 μm thick is installed on the target scattering chamber. The shield consists of 2 sheets mounted over the top and bottom halves of the foam cylinder referenced to the SVT common ground. The SVT rates and radiation damage benefit from the inclusion of the tungsten shield. The rates have been compared with physics run data at several beam currents. There is a good agreement between the real and the simulated data.

While the gamma fluences / doses show a dramatic decrease with the introduction of shielding, the total fluences and doses decrease significantly for the thinner configuration and do not vary much for thicker tungsten (see Fig. 67). The photon radiation dose becomes negligible for 50 μm or more of tungsten with total 1 MeV equivalent radiation dose about 65 krad per year on a liquid-hydrogen target. For 15 years of running the experiment on a carbon target the estimated radiation dose for the sensors is 2.5 Mrad (with 50 % operation) [17].

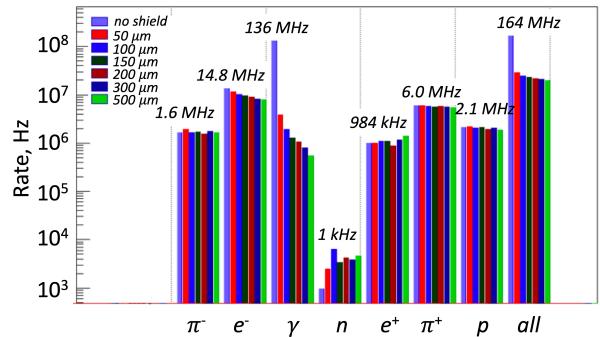


Figure 67: Rates in the first SVT layer for different tungsten shield thickness from 50 to 500 μm for a liquid hydrogen target at the nominal CLAS12 operating luminosity. No energy threshold cut applied.

8.3. Magnetic Field

Due to the constraints on the maximum length of the cables, the readout, slow controls, and power supply crates are installed on a movable service cart within few meters from the detector. To assess the potential impact of the solenoid field on the SVT DAQ, a magnetic field map was simulated for the location of the power supply and readout crates. Fig. 68) shows that the maximum strength of the field for the crates is at an acceptable level of 100 G.

9. Performance

9.1. Module testing

Detailed quality assurance procedures were developed for testing the modules during assembly at Fermilab, reception tests at Jefferson Lab, tracker integration, and commissioning. At each stage the results were compared with previous measurements. Module performance was tested by calibration procedures. No significant correlated noise has been observed between the channels of the same chip, chips of the same module or

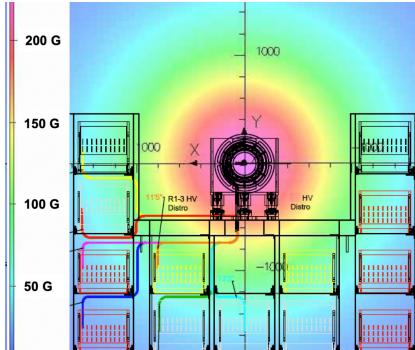


Figure 68: Solenoid field map at the location of the SVT service cart.

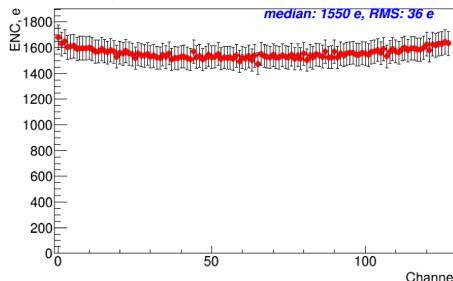


Figure 69: Typical input noise on a single chip of an SVT module.

closely placed modules. The measured average channel noise (see Fig. 69) is comparable with the estimated contributions of different noise sources. The gain dispersion measured on the channels is within the specs of the readout chip (see Fig. 70). To verify operational stability and functionality of the module at low temperature with active cooling, a performance test was conducted at -20 C using a sealed container and a module in a carrier box.

Longer silicon strips have higher capacitance and thus a higher input noise (see Fig. 71). Noise calibration accounts for the different strip lengths and pitch adapter layouts that affect the input capacitance of the preamplifier. The mean noise values scale linearly with strip length which confirms that the noise is dominated by the strip capacitance and not by coherent noise pickup of the system. The channel noise has a linear dependence on the strip length with the offset p_0 about 400 electrons (with shaper at 125 ns) corresponding to the ENC for the shortest strips and the slope p_1 of 27 electrons, consistent with FSSR2 noise measurements at comparable capacitive load taken on a single-chip test board with

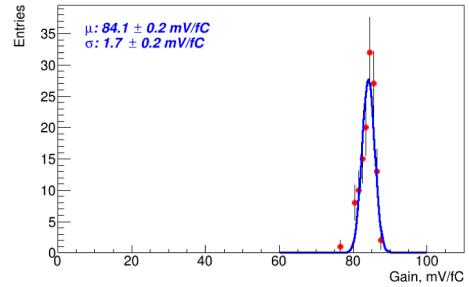


Figure 70: Distribution of the gain for the channels of one representative FSSR2 ASIC.

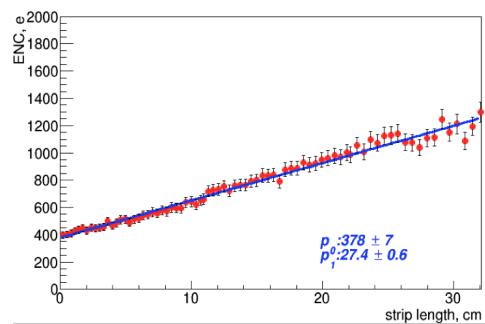


Figure 71: Input noise vs. strip length.

discrete capacitors (see Fig. 56).

The noise occupancy histogram with no charge injection is shown in Fig. 72. It probes the tail of the noise distribution, which can show effects masked by the higher occupancy at low thresholds. A MPV of the signal peak from a MIP corresponds to a 100th DAC bin. The equivalent noise charge of the SVT channels is shown in Fig. 73. The peak is ~1600 electrons, the shoulder on the left side corresponds to the shorter strips. The channel noise allows setting a 3 σ threshold at the 30 keV level.

The detector response and full readout chain calibration was done with γ and β sources, cosmic muons, electron beam, and proton beam. The output from the 3-bit ADC is not allowing to get a good resolution of the pulse height. To increase the number of bins in the cluster charge distribution, a sliding window method was used, combining the data taken for the same time window in several runs with discriminator thresholds set for the required binning. When using signals from minimum ionizing particles, like cosmic rays or ^{90}Sr β source, the signal distribution is fitted with a Landau-Gauss convolute. The detector response to minimum ionizing particle (MIP) was about 24000 elec-

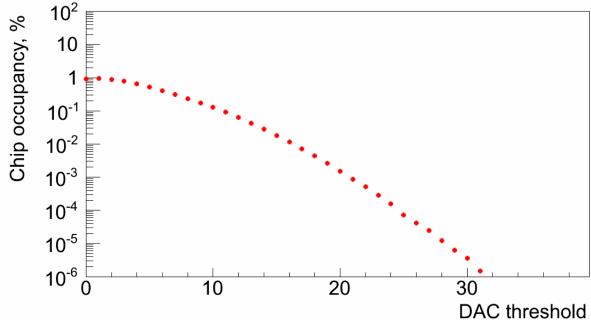


Figure 72: Channel noise occupancy vs. DAC hit/no-hit threshold (in DAC bins, one DAC bin corresponds to 3.5 mV).

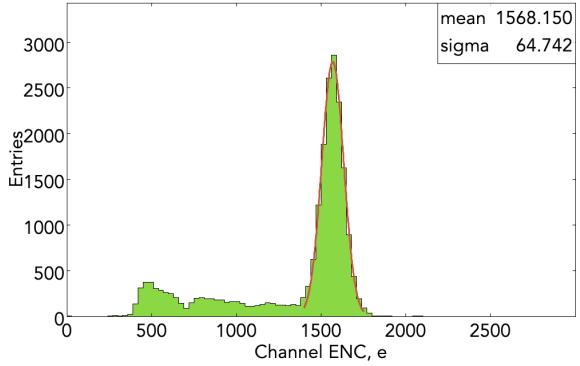


Figure 73: SVT ENC for all channels. The main peak corresponds to the full length strips (33 cm). The shoulder on the left side corresponds to the shorter strips.

tron, which is what is expected for the $320\ \mu\text{m}$ thick sensor. The results of absolute gain calibration with a γ source (Am^{241}) are shown in Fig. 74. The signal peak is in good agreement with the expected position (marked with an arrow).

9.2. Integration and system checkout

To verify performance of the integrated detector, data acquisition chain, power services, and cooling system, as well as the detector control and data acquisition software, the final detector system was installed in the clean room and used at all stages of tracker integration and commissioning. The SVT was operated for several months under environmental conditions close to the ones in the experimental hall. Defects known before the integration of the system were reestablished. 99.9% of channels were operational after the detector integration.

The noise behavior was found to be within expectations and well understood. The dependence of the noise on the environmental temperature and humidity

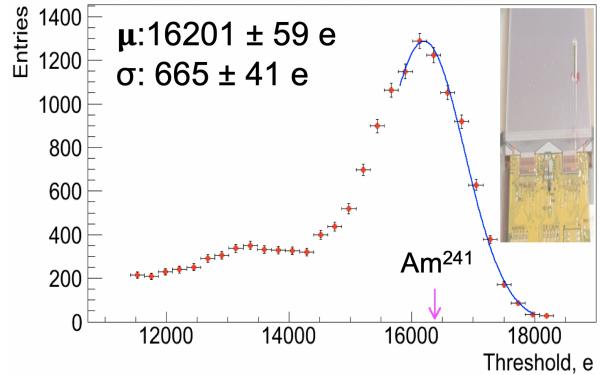


Figure 74: Signal from $\text{Am}^{241}\ \gamma$ source.

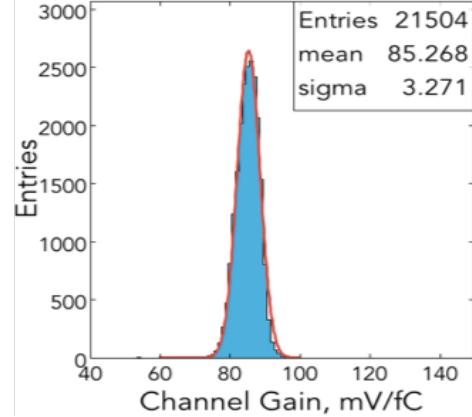


Figure 75: Distribution of gain for the SVT channels.

is small. The noise performance in the experimental hall was comparable with the results taken in the clean room during integration. No significant correlated noise has been observed between the channels of the same chip, between the chips of the same module, or between the closely placed modules. The front-end electronics performed reliably, and no chip failures were observed. The distribution of gain was uniform and stable for all channels (see Fig. 75).

In the hall the SVT was dismounted from the integration cart, craned to the space frame level in horizontal position using the mounting brackets on the support tube and the counter weight system to balance the weight of the cables which remained connected to the modules and coiled around the support tube during this operation. The support tube was attached to the central tracker service cart with alignment system for final adjustment of the SVT along the beam line. The cart hosts the crates for the power supplies, back-end electronics, slow controls, and the dry air distribution system. The



Figure 76: SVT detector installed in the experimental hall before being integrated with the CLAS12 detector.

service cart is placed on the wheels and can be moved along the beam line on the rails, providing access to the detector during maintenance. The power, network, gas, and cooling lines are long enough to allow the cart to be moved up to 5 m upstream. Fig. 76 shows the SVT detector after installation in the experimental hall. All modules were found to be fully functional after transportation from the assembly site and installation on the beam line.

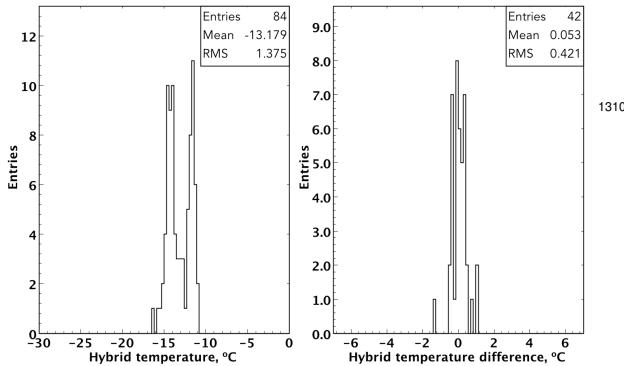


Figure 77: Hybrid temperatures (left) and the difference in temperature between the two sides of the module with coolant at -26 °C (right).

Temperature variation of the SVT modules measured by sensors mounted on the hybrids with coolant at -26 °C is shown in Fig. 77 (left). In these operating conditions the module temperatures were uniformly distributed within the region, with lower temperatures close to the cooling lines. Region 3 temperatures were slightly higher than in the inner regions. The temperature difference between the two sides of a module is within 1°C as shown in Fig. 77 (right). Sensor leakage currents remained at the same low levels after installation (see Fig. 78). Thermal cycling of the modules verified the robustness of the bond wires.

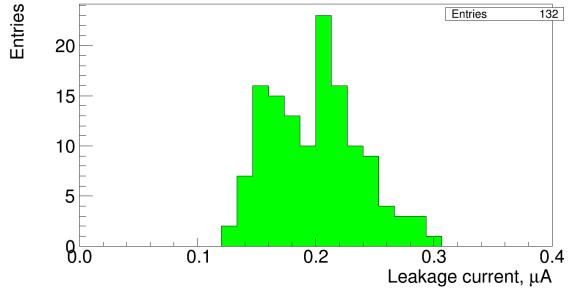


Figure 78: Sensor leakage currents after detector integration.

9.3. Commissioning with cosmic rays

Cosmic ray tests of the SVT have been used to test track reconstruction routines for the SVT, qualify the geometrical precision of detector assembly by track based alignment methods, establish correct readout, good noise performance, full response for the entire detector, measure the inter-strip couplings, study the time evolution of the detector response. Once the reception tests of the first assembled modules were complete, a cosmic test stand was assembled (Fig. 79) to verify the expected performance of the detector. Four SVT modules were stacked vertically between the two trigger paddles. Evaluation of the signal to noise ratio and capacitive coupling confirmed the estimates and validated the full readout chain calibration data.



Figure 79: Cosmic test stand.

Cosmic data during detector integration in the clean room were taken in the standalone mode using the self triggering feature of the FSSR2 readout chip in coincidence logic. VSCM boards reading the SVT modules located at the top and bottom halves of the horizontally placed barrel provided the trigger signals via signal distribution of two VXS crates. The coincidence of signals from the trigger interface boards of both crates was taken as the cosmic trigger. The response of the chan-

nels was uniform, and performance results obtained during tracker integration were confirmed. The angular distribution of the cosmic muons reconstructed in the SVT is shown in Fig. 80.

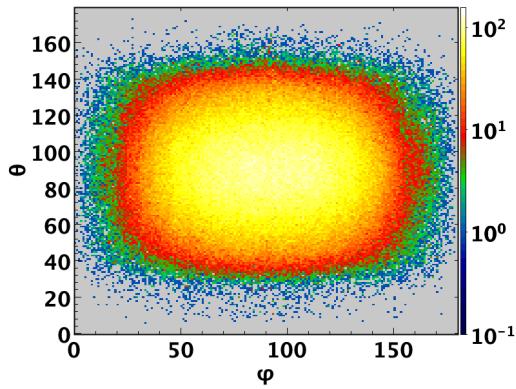


Figure 80: Angular distribution of the cosmic muons reconstructed in the SVT.

After installation of the SVT in the hall and checkout of detector services and readout system, a trigger from the CTOF detector was used to collect cosmic data for the CLAS12 central detector. A cosmic muon reconstructed in the central detector is shown in Fig. 81. The 1330 SVT is the inner detector, surrounded by the BMT, the CTOF, and the CND. Yellow circles represent crosses (matched hits on both sides of the module) in the SVT and green circles correspond to the clusters in the Micromegas detector. Both tracking detectors have the same number of layers. The SVT has small angle stereo strips on the two sides of a module, and the BMT has interleaving layers of the strips along the beam axis and arcs at the fixed radii. Between the physics data taking runs more cosmic trigger data were collected for 1340 calibration and performance studies. A hit map for the SVT channels during the cosmic run is shown in Fig. 82. Lower hit occupancy on the right side of the map is due to the shorter strips at this side of the sensors.

The charge sharing among two adjacent strips was 1345 studied using the η -function, defined for the 2-strip clusters as the ratio of the pulse height of the left strip to the pulse height of the cluster. Fig. 83 shows the η -function obtained from the measurement of on-track clusters from the cosmic muons. The granularity of the 1350 pulse height after the digitization is coarse due to the 3-bit ADC of the readout chip. There is a pronounced peak in the center between the two readout strips where all the charge is collected by the intermediate strip. Because of capacitive coupling, signals on these intermediate strips are partially transferred to the readout strips.

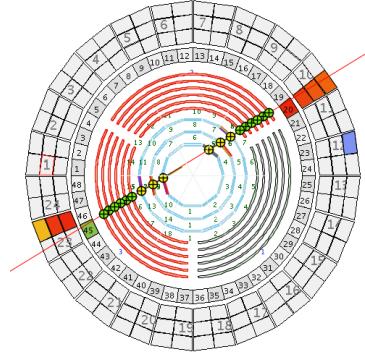


Figure 81: Cosmic muon reconstructed in the CLAS central detector.

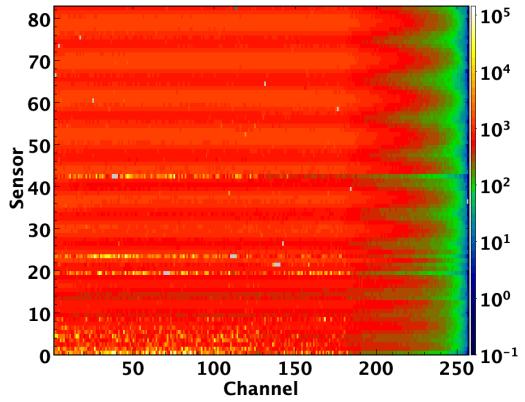


Figure 82: Monitoring SVT hit map during a cosmic run showing module vs. strip number.

Strip multiplicity of the clusters (cluster size) in the cosmic run is shown in Fig. 84. The size of the clusters is lowest in the innermost region and is increasing with radius due to a larger local track angle (the tracks, triggered by the CTOF, crossing the barrel far from the beam line).

Cosmic muons are an important source for calibration and alignment. Their trajectories are sensitive to misalignments of different tracker parts. The cosmic muons significantly improve the alignment precision. A preliminary alignment of the SVT was done using the sample of several millions of the cosmic muon tracks taken without solenoid magnetic field. With exception of the modules located at the shallow angle to the vertical axis, the acquired sample provided adequate statistics of the tracks to extract the misalignment data. The tracks crossing the sensors at large inclination angles and low energy tracks subject to multiple scattering were rejected. Additional requirement on the χ^2 per de-

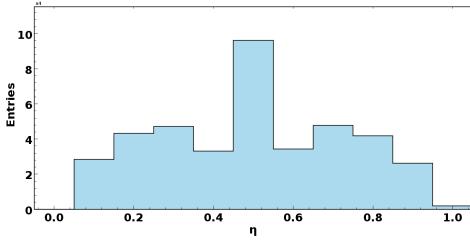


Figure 83: η -function for the two-strip clusters.

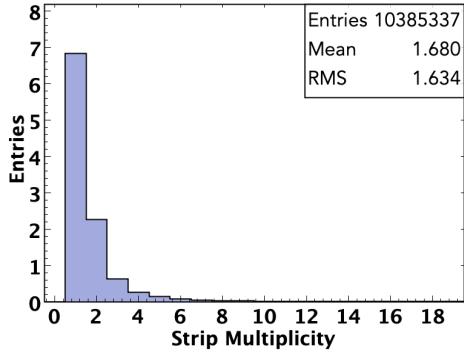


Figure 84: Strip multiplicity of the clusters in the cosmic run.

gree of freedom of the track fit was applied to reject tracks effected by the outlier hits. The spacial residuals before (blue) and after (red) the alignment procedure (see Fig. 85) are expected to provide the designed momentum resolution.

9.4. Commissioning with beam

Performance of the SVT module has been studied at Fermilab in a beam test with 120 GeV protons. SVT module in the plastic carrier box was mounted vertically behind the CMS pixel beam telescope (8 planes, $\approx 6 \mu\text{m}$ track position uncertainty, $2 \times 2 \text{ cm}$ active area), used as the trigger and the tracker. Beam test setup is shown in Fig. 86. Production SVT DAQ has been exercised at different event rates. Event block mode has been tested up to 100 k protons per 4 sec spill with no busy time. Signal-to-Noise ratio was in agreement with results with radioactive sources and cosmic muons. Measured cluster charge distribution is shown in Fig. 87. Several millions triggers have been taken at different discriminator thresholds. Expected position resolution of the silicon sensors was confirmed.

The front-end electronics performance and noise occupancy of the detector were studied during physics data taking. No interference with other CLAS12 subsystems were found. The data quality and detector op-

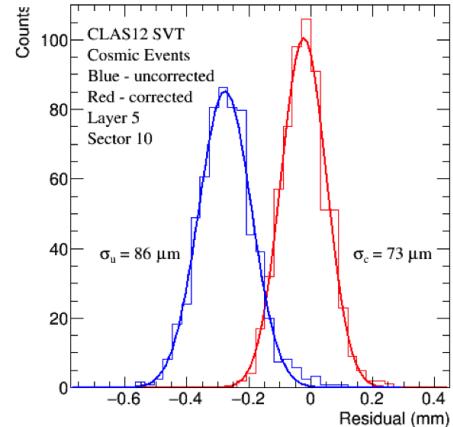


Figure 85: Residuals for one of the SVT sensors before (blue) and after (red) alignment.



Figure 86: Beam test setup.

erational stability were verified with both online and offline monitoring packages. There were occasional FSSR2 chip latch-ups observed after the start of a new run. These latch-ups were traced by improper configuration of the chips and fixed by adding additional resets to the run start sequence.

Tracks reconstructed in the CLAS12 central detector during a physics run are shown in Fig. 88. The level-1 trigger latency is finely tuned to match the CLAS12 trigger delays. Single Event Monitor (SEM) error checking implemented in the VSCM firmware allows real-time monitoring of the readout errors induced by the radiation. Relatively minor single event upsets were recorded in the SVT readout electronics with no latch-ups or single event burn-outs observed. The SEM recorded events are correlated with beam conditions in the experimental hall during the run. SVT readout and power supply crates did not require rebooting. No readout or data corruption issues were observed [18].

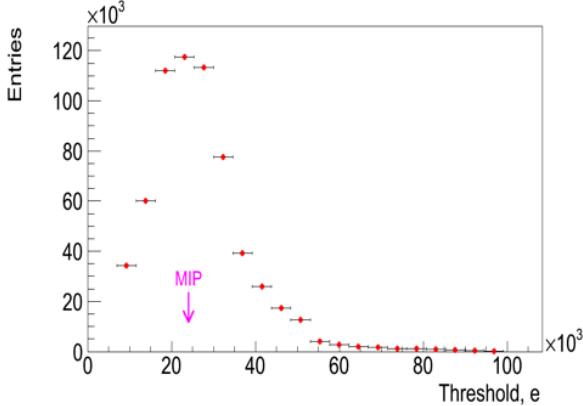


Figure 87: Cluster charge distribution from 120 GeV protons.

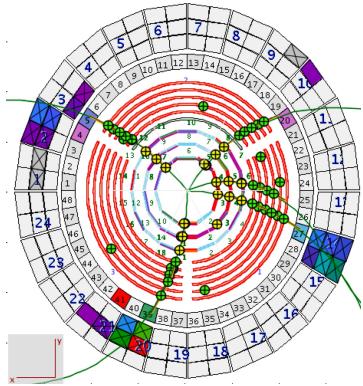


Figure 88: Multi-track event reconstructed in the CLAS12 central detector during a physics run.

FSSR2 readout chip does not provide the timing information from the hit. Reading the time stamp associated with a hit was implemented in the VSCM board. The time stamp is synchronized with the "Got Hit" pulse from the chip when the pulse height reaches the threshold set for the first discriminator of the ADC. Timing of the SVT hits referenced to the CTOF timing are shown in Fig. 89. The data correspond to the time difference between the SVT and the CTOF time stamps for the SVT hits which were associated with a track. Applying a cut on this difference can be used to remove background and noise hits in the track seeding algorithm.

Radiation induced energy levels in the middle of the band gap are causing an increase of thermally generated electron-hole pairs. The sensor leakage current in-

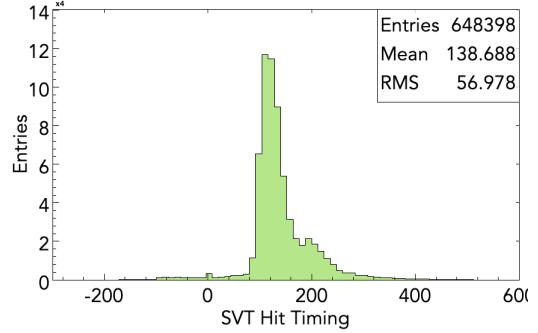


Figure 89: SVT hit timing referenced to the CTOF time in a physics run with the hydrogen target.

creases with the absorbed flux:

$$\Delta I_R = \alpha \Phi, \quad (5)$$

where Φ is the particle fluence and $\alpha \approx 2 \cdot 10^{-17}$ A/cm [11]. The increased leakage current is increasing the noise and heating up the sensor, which, in turn, will further increase the leakage current. When the temperature increases beyond a critical temperature where the cooling can not maintain a stable temperature this will result in thermal runaway. After accumulating a large hadron fluence, the SVT requires low temperature operation to avoid thermal runaway induced by the sensor leakage current. Fig. 90 shows thermal runaway in the 2 innermost layers of the SVT received the highest radiation dose. Leakage currents in other layers were stable. The monitoring data correspond to the period after a physics run with liquid hydrogen target, when there was no beam in the hall for extended time. The leakage currents became stable when the coolant temperature was decreased.

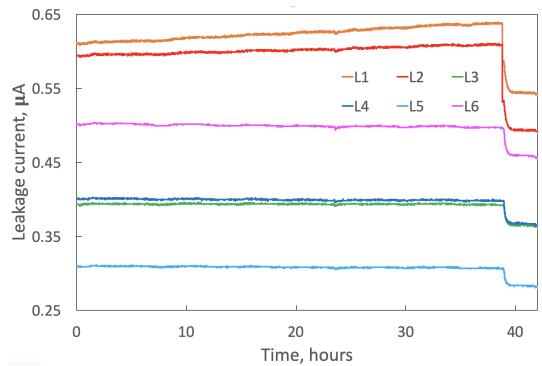


Figure 90: Thermal runaway in the SVT inner layers (L1 and L2).

Fig. 91 shows monitoring plots for the average sensor leakage currents in the SVT layers during the data taking with liquid deuterium target. For the first few hours in the time period shown there was no beam in the hall and the currents were stable. Currents in all the layers are increasing with time when beam is present. The jumps in the leakage current of a layer between two values correspond to beam trips. The largest difference between beam-on and beam-off levels and the rate of current increase is in the inner layers. The data were taken at 50 nA beam current.

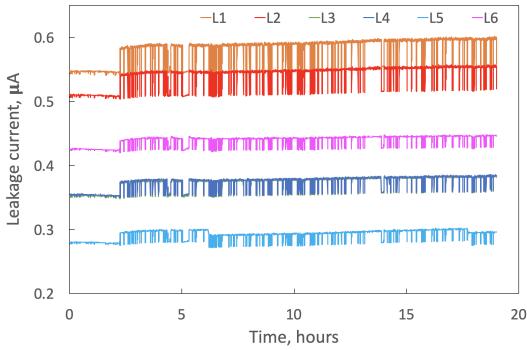


Figure 91: Monitoring plots of the sensor leakage currents in the SVT layers during the run with liquid deuterium target.

Comparison of the rates of leakage current increase with different targets is shown in Fig. 92. The rate of current increase with liquid deuterium target was about 1 nA per hour. Corresponding rate for liquid hydrogen target was 0.06 nA per hour. The data were taken at 50 nA beam current corresponding to the instantaneous luminosity of $0.7 \times 10^{35} \text{ cm}^{-2} \text{s}^{-1}$ per nucleon.

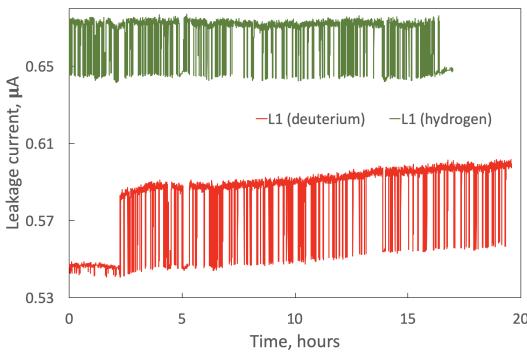


Figure 92: Average sensor leakage currents in the SVT layer 1 during the runs with hydrogen and deuterium targets.

The rate of current increase for the hydrogen target

was much smaller.

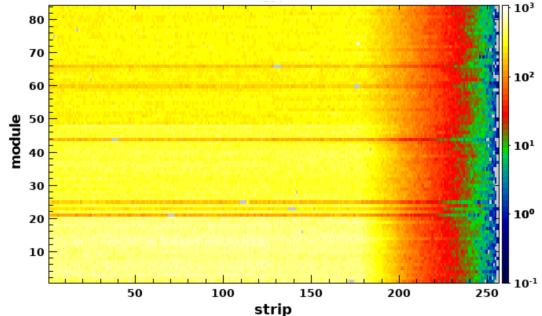


Figure 93: SVT hit map during a physics run with the hydrogen target.

After a year of running several sensors developed pinholes (the strips with DC current through the damaged dielectric (oxide) between aluminum strip and implant, resulting in a high current flowing into a channel) observed as groups of adjacent hot channels. The performance of the charge amplifying chip is deteriorated by the high current flowing into a channel. The bias voltage on these sensors has been lowered to reduce noise and abnormally high leakage currents (high occupancy regions on the map). The increased leakage current is reduced by lowering the detector temperature. The detector is kept below -10 C to freeze the reverse annealing interleaved with short periods at room temperature for the beneficial annealing. A hit map of the SVT from a physics run is shown in Fig. 93. Sensors with pinholes are seen on the map as darker horizontal lines due to reduced efficiency (under-depleted sensors) with strips of masked hot channels with no hits.

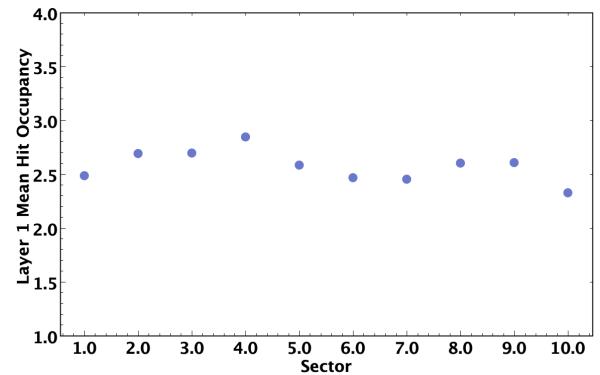


Figure 94: Mean hit occupancies for the sectors of the innermost SVT layer with hydrogen target at 50 nA beam current.

Fig. 94 shows average hit occupancy per event in the

innermost SVT layer for the data taken with hydrogen target at nominal beam current of 50 nA. The hits are uniformly distributed among the sectors with occupancies close to 1% (each sensor has 256 strips).

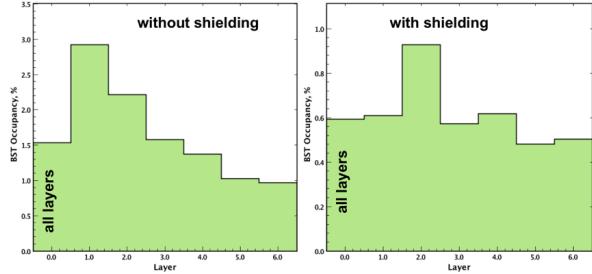


Figure 95: Hit occupancies with and without the 50 μm -thick tungsten shield installed outside of the target scattering chamber.

The impact of the tungsten shield on the SVT occupancy is shown in Fig. 95. Occupancies in all SVT layers are substantially lower, which results in better tracking performance due to reduced combinatorics. The effect of the shield on momentum resolution is negligible [19]. For the liquid hydrogen target the occupancy in the innermost layer of the SVT is approximately 1%, decreasing to 0.5% in the outermost layer. There is no hit efficiency loss due to the dead time of the readout system at such occupancies.

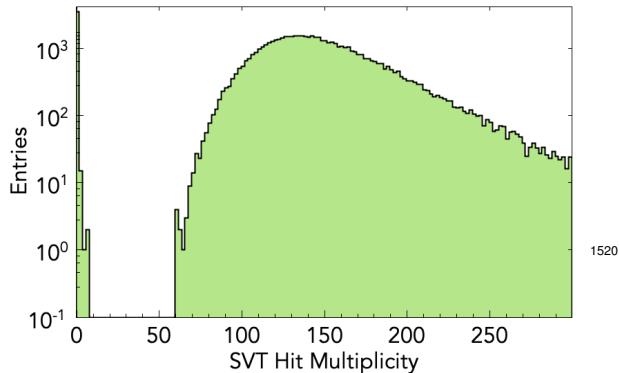


Figure 96: SVT hit multiplicity during the liquid hydrogen run at 50 nA beam current.

Noise performance of the SVT during the physics data taking is demonstrated in Fig. 96, showing the SVT hit multiplicity during the liquid hydrogen run at nominal 50 nA beam current. The main peak is at about 130 hits per event which corresponds to 0.6% detector occupancy. The narrow peak on the left side represents SVT

occupancy when there was no beam in the hall. The plot confirms good signal-to-noise ratio of the detector.

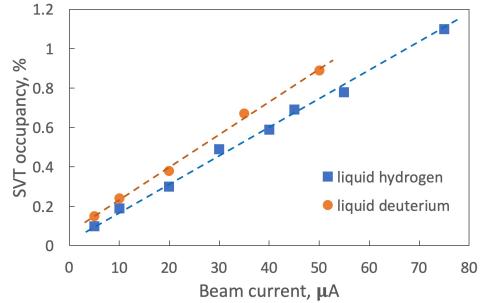


Figure 97: SVT occupancy vs. beam current for hydrogen and deuterium targets.

Fig. 97 shows SVT occupancy vs. beam current for hydrogen and deuterium targets. The production data were taken at 50 nA. The SVT occupancy increases linearly with luminosity and remains at low levels not causing a substantial drop in the track finding efficiency.

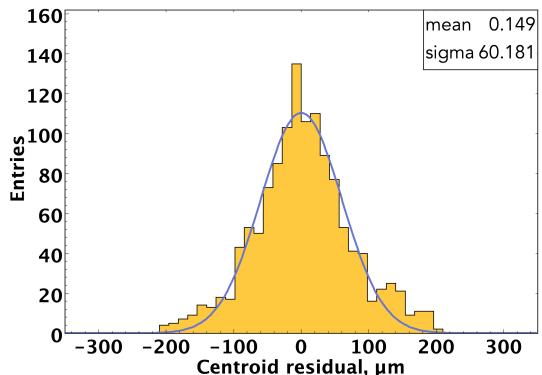


Figure 98: Centroid residual for one of the SVT sensors after preliminary tracker alignment.

A series of dedicated central tracker alignment runs was done at low beam current without magnetic field. The alignment data were collected when position of the central detector subsystems or the target has changed. In addition to the track-based alignment, the data from the mechanical survey of the fiducials were also recorded when the detectors were moved. Centroid residual for one of the SVT sensors after preliminary tracker alignment is shown in Fig. 98. Sensor spacial resolution is close to the specs.

10. Conclusions

The SVT is installed in the CLAS12 spectrometer in Hall B of Jefferson Lab, and the performance of mod-

Detector/module	Strip length, cm	ASIC	ENC _{675 e}
ATLAS barrel	13	ABCD3A	1500
CMS TOB OB1	18	APV25	1100
CDF Run 2b L0	24	SVX4	1600
CLAS12 SVT	33	FSSR2	1600 ¹⁵⁸⁰

Table 2: ENC of the silicon strip modules.

ules measured during detector integration has been confirmed. No channels were lost during the installation. The SVT barrel has been electrically tested with the number of defective channels of 0.1%, well within the specification. The chip average ENC noise is uniform, ~ 1600 e, on par with the leading silicon strip trackers (see Table 2). There is no evidence of coherent noise between the modules and other components. The tracker has been commissioned with cosmic rays and integrated as part of the CLAS12 central detector. Experience in operating and commissioning the tracker has been gained during the first year of operation. The tracking performance was studied with beam data and matches the physics requirements.

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