Packet Chasing: Spying on Network Packets over a Cache Side-Channel

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Abstract

This paper presents Packet Chasing, an attack on the network that does not require access to the network, which works regardless of the privilege level of the process receiving the packets. A spy process can easily probe and discover the exact cache location of each buffer used by the network driver. Even more useful, it can discover the exact sequence in which those buffers are used to receive packets. This then enables packet frequency and packet sizes to be monitored through existing cache side channels. This enables both covert channels between a sender and a remote spy with no access to the network, as well as direct attacks that can identify the web page access patterns of a victim on the network.

1 Introduction

Modern processors employ increasingly complex microarchitectural techniques that are carefully optimized to deliver high performance. However, this complexity often breeds security vulnerabilities, as evidenced recently by Meltdown [1] and Spectre [2]. This paper explores the vulnerable side effects of another sophisticated high performance microarchitectural technique –*Intel® Data Direct I/O* (DDIO) [3] implemented in most server-grade Intel processors to accelerate network packet processing. Further, it presents new high resolution covert and side channel attacks on the network I/O traffic, which while possible without DDIO, are considerably more effective in the presence of DDIO.

The widespread adoption of multi-gigabit Ethernet and other high-speed network I/O technology such as Infiniband has highlighted the critical importance of processing network packets at high speed in order to sustain this newly available network throughput, and further improve the performance of bandwidth-intensive datacenter workloads. Consequently, most Intel server-class processors today employ DDIO technology that allows the injection and subsequent processing of network packets directly in the processor's last level cache (LLC), bypassing the traditional DMA (Direct Memory Access) interface. DDIO is invisible to software, including OS drivers, and is always enabled by default.

The key motivation behind DDIO is the fact that modern server-class processors employ large LLCs (~20MB in size), thereby allowing the network stack to host hot data structures and network packets in-process completely within the LLC, reducing trips to main memory. By eliminating redundant memory transfers, DDIO has been shown to provide substantial improvements in I/O bandwidth and overall power consumption [3–6]. Although Intel restricts allocating more than 10% of the LLC for DDIO to prevent cache pollution, it neither statically reserves nor dynamically partitions a dedicated portion of the cache for DDIO.

However, despite its seemingly benign intention to accelerate network packet processing, DDIO has a previously unknown vulnerable side effect that this paper exposes. On a DDIO host, incoming network packets from a remote client and application data structures from processes on the local host contend for the shared LLC, potentially evicting each other in the event of a cache conflict. In this paper, we show that such a contention provides significant leakage for cache side channel attacks to perform covert communication and/or infer network behavior, with virtually zero access to the network stack. In particular, we describe a new class of covert- and side-channel cache attacks, dubbed *packet chasing* that exploits this contention by creating arbitrary conflicts in the LLC using carefully constructed memory access patterns and/or network packet streams.

We further show that the location (in cache) of packet buffers used by the network driver, *and the order in which they are filled*, are easily discovered by an attacker, greatly minimizing the amount of probing necessary to follow the sequence of packets being chased.

The *packet chasing*-based covert channel we describe in this paper allows a spy process running covertly alongside a server daemon on the local DDIO host to receive secret messages from a trojan process running on a remote client across the network, by causing deterministic contention in the last-level cache. We show that such a covert means of communication is feasible, and is achievable at a high bandwidth, despite the fact that the trojan process only sends broadcast packets over the network and that the spy process is completely isolated from the network-facing server daemon (potentially cross-container and cross-VM), and further lacks any access to the network stack.

In addition to the covert channel, we describe a novel *packet chasing*-based side-channel attack that leverages a local spy process running alongside a web server. In our experiments, the spy is on the client side alongside of a browser like firefox, enabling it to fingerprint a remote victim's website accesses without having access to the network.
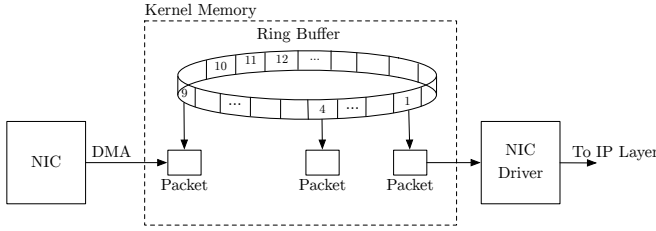
Figure 1. The shared ring buffers between NIC and the device driver.

In particular, this attack enables an attacker to recognize the web activity of the victim based on packet size patterns.

The major contributions of this paper are as follows: It shows that (1) with DDIO turned on, the location of the packet buffers for a common network driver are easily discovered, (2) the size of each packet sent (in cache block increments) is also discoverable, (3) the sequence in which the discovered buffers are repeatedly accessed can also be deduced, (4) covert channels can be created between a trojan sending packets on the network and a spy on another machine, and (5) the sequence/pattern of packet sizes can leak sensitive information across a side channel, such as a trace of web access activity.

2 Background and Related Work

This section provides background on network packet handling, DDIO and related network optimizations, network and I/O based attacks, and cache attacks.

2.1 Journey of a Network Packet

When an application sends data through the network, it usually sends a stream of data; and it is the responsibility of the transfer layer to break the large messages into smaller pieces that the network layer can handle. The Maximum Transferable Unit (MTU) is the largest contiguous block of data which can be sent across a transmission medium. For example, the Ethernet MTU is 1500 bytes, which means the largest IP packet (or some other payload) an Ethernet frame can carry is 1500 bytes. Adding 26 bytes for the Ethernet header results in a maximum frame of 1526 bytes.

When the NIC driver initializes, it first allocates a buffer for receiving packets and then creates a descriptor which includes the receive buffer size and its physical memory address. It then adds the receive descriptor to the receive ring (rx ring), a circular buffer shared between the driver and the NIC to store the incoming packets until they can be processed by the driver. The driver then notifies the NIC that it placed a new descriptor in the rx ring. The NIC reads the content of the new descriptor and copies the size and the physical address of the buffer into its internal memory. At this step, the initialization is done and the NIC is ready to receive packets.

As shown in Figure 1, upon receiving incoming packets, the NIC, using Direct Memory Access (DMA), copies packets to the physical addresses provided in the rx ring, then sends an interrupt to notify the driver. The driver drains the new packets from the rx ring and puts each of them into a kernel data structure called a socket buffer (skb) to begin their journey through the kernel networking stack up to the application which owns the relevant socket. Finally, the driver puts the receive buffer back in the rx ring to be used for future packets.

2.2 Direct Cache Access and Data Direct I/O

A number of technologies have been employed to improve network I/O performance by improving the memory subsystem [3, 7]. Direct Cache Access (DCA) [7] enables the NIC to provide prefetch hints to the processor's hardware prefetcher. DCA requires that memory writes go to the host memory and then the processor prefetches the cache lines specified by the memory write. DCA needs to be initialized upon system startup. The I/O device driver configures the DCA by setting up the appropriate DCA target ID for the device. The I/O device then encapsulates that information in PCIe Transaction Layer Packet (TLP) headers which then trigger a hardware prefetch to the processor cache [8]. DCA has been part of the Linux Kernel since 2007 and version 2.6.24 [9].

The Intel Sandy-Bridge-EP microarchitecture introduced Data Direct I/O (DDIO) technology [3] which transparently pushes the data from the NIC or other I/O devices directly into the last level cache. Before DDIO, I/O data was always sent through the memory; inbound data is written by the I/O device into memory, and then the data is either prefetched before access or demand fetched into the cache upon access by the processor. With DDIO, however, DMA transactions for an I/O allocated region go directly to the last level cache, and they will be in dirty mode and only written to memory if they get evicted [10, 11].

While DCA and DDIO are shown to be successful at reducing the cache miss rates in many scenarios [3, 7], if the device has large descriptor rings, they can result in worse performance as useful data can be evicted from the cache and will have to be fetched again later [12]. In addition, as we show in this paper, these technologies potentially open up new side channels and vulnerabilities since the packets are brought directly into the LLC, which is shared by all cores in the processor.

2.3 Network-Based Covert-Channels

The literature abounds with network-based covert channels that require some network protocol as carrier and encode the data into a protocol feature [13–18]. For example, covert channels can be formed by encoding data in unused or reserved bits of frame or packet headers [17–20], such as the TCP Urgent Pointer which is used to indicate high priority

data [18]. In the TCP protocol, Initial Sequence Number (ISN) is the first sequence number and is selected arbitrarily by the client. Rowland proposed shifting each covert byte by 26 bits to the left and directly using it as the TCP ISN [21]. Abad [14] shows that the IP header checksum field can also be exploited for covert communication, and further proposes encoding the secret information into the checksum field and adding the content of an IP header extension to compensate the checksum modification, chosen such that the modified checksum will be correct. Other header fields such as address fields [15] and packet length [17] are also exploited to build covert channels. In addition to the header field, packet rate and timing [15, 20], packet loss rate [16] and packet sorting [22] are also used to build covert channels.

Many of these covert-channels are based on non-standard or abnormal behaviour of the protocol and can be detected and prevented by a simple anomaly detection method [13]. In addition, all of these network-based covert channels require the receiver to have access to the network and be able to receive packets, while the receiver in our packet chasing attack does not need any access or permission to the network.

2.4 Cache Attacks

Cache-Based side-channel attacks, also known as cache attacks, are the most common class of architectural timing channels, and are shown to be successful at building covert communication channels [23, 24], revealing secret information such as cryptography keys [24–27], keystroke [28], and web browsing data [29, 30]. A cache attack typically involves a victim process and a spy process that share a cache memory. For example in PRIME+PROBE [24, 29], the spy process, by monitoring cache usage of the victim, tries to learn which cache sets are accessed by the victim. In the PRIME part, the attacker fills one or more cache sets with its own cache blocks, simply by accessing its data. Then, the attacker waits for a time interval and lets the victim execute and use the cache. By accessing the cache, the victim will evict some of the attacker's blocks. Finally, at the PROBE part, the attacker measures the time it takes to load each set of cache blocks. If the attacker observes an increase in the memory access latency for a cache line, she can infer that the victim has accessed that line. Since the PROBE phase touches all the attacker's cache blocks, it makes the cache set ready for subsequent observations and acts as the next PRIME.

To perform these attacks in a fine time granularity, the attacker has to target specific sets in the last level cache. As such, she has to know how the addresses map into the sets in the LLC. But, starting with the Sandy Bridge microarchitecture [31], Intel uses a new design for the last-level cache in which they split the LLC into multiple slices, one for each core (See figure 2). An unpublished hash function maps the physical addresses to the slices, which supposedly distributes the physical addresses uniformly among the cores. However, this hash function has been successfully reverse-engineered
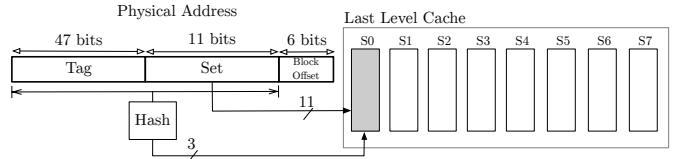
Figure 2. Intel's complex indexing of modern last level cache.

for many different processors in Intel's Sandy Bridge [32–34], Ivy Bridge [33, 35], and also Haswell [33, 36] architectures.

In addition to PRIME+PROBE, multiple other variants of cache attacks are also proposed [25–27]. FLUSH+RELOAD [26] uses Intel's CLFLUSH instruction to flush a target address out of the cache, and then, at the measurement phase, the attacker "reloads" the target address and measure its access time. However, it relies on shared memory between the spy and the victim and precise timers. PRIME+ABORT [27] exploits the Intel transactional memory extension (TSX) hardware to build a timer-free last level cache attack.

Several defenses have been proposed in the literature to mitigate cache timing channels [37–40]. These mitigation strategies include identifying the leakage in software [41], dynamically detecting the attack [42], closing the channels at hardware design time [37–39], dynamic cache partitioning [40, 43, 44], strict reservation of physical cores to security-sensitive threads [45], randomization [43], memory trace obliviousness [46, 47], and cache state obfuscation using decoy load micro-ops [48].

2.5 Security of I/O Devices and Drivers

A number of security attacks have been published that target device drivers [49–51]. Thunderclap [50] describes an attack that subverts the Input-Output Memory Management Unit (IOMMU) protections to expose the shared memory available to DMA-enabled I/O peripherals. Zhu et al. [52] demonstrate another attack that bypasses IOMMU and compromises the GPU driver to exploit GPU microcode to gain full access to CPU physical memory. To address these vulnerabilities, researchers focus on isolating device drivers, and to make operating systems secure when a device driver is buggy or has code which is intentionally malicious [53, 54]. Tiwari et al. [55] propose a full system which includes an I/O subsystem and a micro-kernel that enable isolation and communication by monitoring and controlling the information-flow of the system.

3 Packet Chasing: Setting up the Attack

System Setup. We perform our analysis and attack on Intel's Gigabit Ethernet (IGB) driver version 5.3.5.22 [56] loaded into Linux Kernel version 4.4.0-142. We run the attack on a Dell PowerEdge T620 [57] server which uses Intel I350 network adapter [8] and is operated by two Intel Xeon CPU

E5-2660 processors. Each processor has a 16-way 20 MB last level cache with 16384 sets. To perform Prime+Probe on the last level cache, we use the Mastik Micro-Architectural Side-Channel Toolkit Version 0.02 [58]

Always-miss Scenarios. When monitoring last level cache access time, we observe that a non-negligible number of cache sets always exhibit misses, even when we constantly prime the caches sets with a high frequency. So, it could not be from external noise. This is likely because Intel has set aside some blocks for special purposes, making the effective associativity of those sets lower than the assumed value of 16. In most cases, we can eliminate this problem by constructing eviction sets for lower levels of associativity.

Our attack consists of two phases. One is an offline phase where the attacker recovers the sequence of the buffers and an online phase where the attacker uses that information to monitor the incoming packets.

3.1 Deconstruction of the NIC Driver

While the code samples of this subsection are specific to Intel's Gigabit Ethernet (IGB) driver, we note that the insights are generalizable.

Size and Number of RX Ring Buffers The original Ethernet IEEE 802.3 standard defines the minimum Ethernet frame size as 64 bytes and the maximum as 1518 bytes, with the maximum being later increased to 1522 bytes to allow for VLAN tagging. Since the driver and the NIC don't know the size of incoming packets beforehand, the NIC has to allocate a buffer that can accommodate any size. The IGB driver allocates a 2048 byte buffer for each frame and packs up to two buffers into one 4096 byte page which will be synchronized with the network adapter. For compatibility, it is recommended [59] that when the device drivers map a memory region for DMA, they only map memory regions that begin and end on page boundaries, which are guaranteed also to be cache line boundaries. Further, the rx ring buffer is used to temporarily hold packets while the host is processing them. Increasing the number of buffers in the ring can reduce the packet drop rate but increases the host memory usage and the cache footprint. Therefore, while the maximum size supported by Intel's I350 adapter is 4096 buffers, the default value in the IGB driver is set to 256.

The linux kernel, in the DMA API, provides two different types of DMA memory allocation for device drivers. Coherent (or consistent) memory and streaming DMA mappings. Coherent memory is a type of DMA memory mapping for which a write by either the device or the processor can be visible and read by the processor or device without the need to explicitly synchronize and having to worry about caching effects. But, the processor has to flush the write buffers before telling devices to read that memory [59]. Therefore, consistent memory can be expensive on some platforms as it invariably entails a wait due to write barriers and flushing of

```
static bool igb_add_rx_frag(rx_buffer, skb){
    ...
    size = rx_buffer->size;
    page = rx_buffer->page;
    if (likely(size <= IGB_RX_HDR_LEN)) {
        memcpy(__skb_put(skb, size), page, size);
        /* we can reuse buffer as-is,
        just make sure it is local */
        if (likely(page_to_nid(page) == numa_node_id()))
            return true;
        /* this is a remote page and cannot be reused*/
        put_page(page);
        return false;
    }
    /* only if packet is large */
    skb_add_rx_frag(skb, page);
    return igb_can_reuse_rx_page(rx_buffer, page);
}
```

Figure 3. The IGB driver function that adds the contents of an incoming buffer to a socket_buffer which will be passed to the higher levels of networking stack. The function returns true if the buffer can be reused by the NIC.

```
bool igb_can_reuse_rx_page(rx_buffer, page){
    /* avoid re-using remote pages */
    if (unlikely(page_to_nid(page) != numa_node_id()))
        return false;
    /* if we are only owner of page we can reuse it */
    if (unlikely(page_count(page) != 1))
        return false;
    /* flip page offset to other buffer */
    rx_buffer->page_offset ^= IGB_RX_BUFSZ;
    /* bump page ref count before it's given to the stack */
    get_page(page);
    return true;
}
```

Figure 4. The IGB driver function that checks if the driver can reuse a page and put it back into the rx ring buffer.

buffers [59]. While the buffers themselves are mapped using streaming DMA mapping, the ring descriptors are mapped using coherent memory. So, the device and the driver could have the same and synchronous view of the ring descriptors. Also, this makes the writes to the rx descriptor ring expensive. Therefore, in order to avoid changing the content of rx descriptors, drivers after receiving packets usually reuse the buffers instead of allocating new buffers. So the drivers usually allocate the buffers once and reuse them throughout the life cycles of the driver.

Figure 3 shows the part of the IGB driver code that is called upon receiving packets and whose job is to add the contents of the rx buffer to the socket buffer which will be passed to the IP layer. If the size of the packet is less than a predefined threshold (256 by default) then the driver copies the contents of the buffer and then tries to recycle the same buffer for future packets. If the buffer is allocated on a remote NUMA node, then the access time to that buffer is much more than

if the buffer was allocated in a local NUMA node. Therefore, to improve performance, the driver deallocates the remote buffer and re-allocate a new buffer for that rx ring descriptor. If the packet size is larger than 256, then instead of the direct copy, the IGB driver attaches the page as a fragment to the socket buffer. Then it calls the *igb_can_reuse_page* function shown in Figure 4. In this function if two conditions are met, then the driver flips the *page_offset* field, so that the device only use the second half of the page. The first condition is again the same condition that the driver checks for small packets. But, the second condition, which is also unlikely, is specific to large packets which prevents re-using the page if the other half of the page is still being processed in the kernel stack and the driver is not the only owner of that page.

To conclude, in the common scenarios, the driver uses a small number of ring buffers (256) on 256 distinct pages, each of them half-page aligned and it continually reuses these buffers typically until the next system reboot or networking restart. In addition, the order of the ring descriptors will never change throughout the execution of the driver code. Therefore, as long as the driver reuses the buffers for descriptors, the order of the buffers remains constant.

3.2 Recovering the Cache Footprint of the Ring Buffer

The ultimate goal of the Packet Chasing attacker is to gain size and temporal information about incoming packets by spying on the last level cache memory. To this end, we perform PRIME+PROBE on the last-level cache. But blindly probing all cache sets doesn't give us much information. This is because when you prime and probe the entire last level cache, your probe time gets limited by the time it takes to access the entire cache, which in this case is about 12 million CPU cycles, too long to gain any useful information about incoming packets. Long probe time also makes the attack more susceptible to background noise, as the probability of observing irrelevant activity on the cache line increases.

However, from the previous subsection, we know that the buffers that store packets in kernel memory are page-aligned. That means we only need to probe the sets that the page-aligned addresses are mapped to. Having 4KB page size implies that the lowest 12 bits of the starting addresses are zero. So the lowest 6 bits of the set indexes are zero (Also see Figure 2). That limits us to 32 sets in each slice for a total of 256 possible sets. Using the Mastik toolkit, we find these sets and construct eviction sets for them, which are essentially a stream of addresses guaranteed to replace all other data from the 16 cache blocks in a set. With these, we have the ability to monitor all 256 cache sets that are potential candidates for buffer locations.

While all the NIC rx buffers map to one of the page-aligned cache sets that we obtain, the distribution of this mapping is not uniform, which means that some of the rx buffers
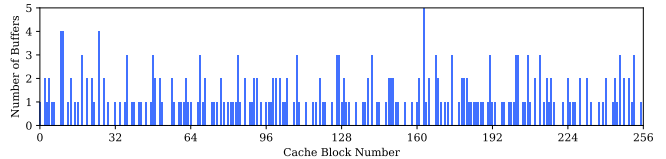

Figure 5. An example of how the NIC ring buffers are mapped to to the page-aligned cache sets.
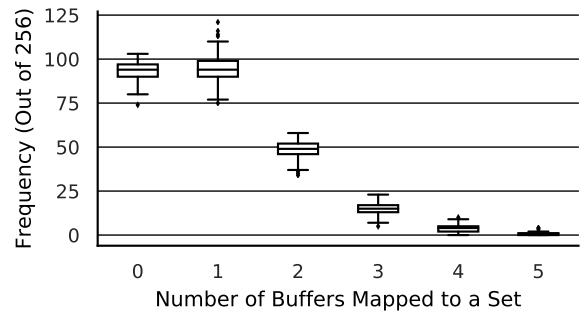

Figure 6. Frequency of the ring buffers that map to same sets, measured for 1000 instances. Zero represents the number of sets that are page aligned but none of the ring buffers is mapped to those.

are mapped to the same cache set. To show an example of such conflict in the cache sets, we instrument the driver code to print the physical addresses of the ring buffers. Figure 5 shows this non-uniform mapping for just one instance of the buffer allocation in NIC. Horizontal axes shows one of the page-aligned cache sets and on the Y axis, we show the number of NIC buffers that map to each page-aligned cache set. In this example, we see that 5 NIC buffers are mapped to cache set number 165 while none of the NIC buffers are mapped to cache block 65.

Figure 6 further analyzes this mapping which shows the result of performing the same experiment across multiple instances of driver initialization. For around 35% of the page-aligned sets, there is no co-mapped NIC buffer, while there are only 5 out of 1000 instances in which we see more than 4 buffers mapped to the same page-aligned cache set.

By narrowing down the number of monitored cache sets to only 256, we are able to see a clear footprint in the cache when the NIC device is receiving packets, as shown in Figure 7. In this experiment, we rely on a remote sender who is on the same network with the spy and constantly sends broadcast Ethernet frames to the network. To this end, we use Linux raw socket [60] that generates broadcast Ethernet frames with arbitrary sizes. These frames get discarded in the driver since the protocol field is unknown. Thus, the effect that we see is only caused by the driver/adaptor accessing the buffers, without any activity of the kernel networking
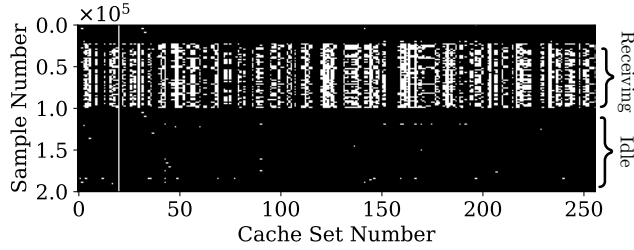
Figure 7. Monitoring all the page-aligned sets while receiving packets. A white dot shows at least one miss (activity) on a cache set in a sample interval

Figure 8. Cache footprint of packets with different sizes while probing the addresses that map to the location of the first three blocks in the packet buffer page. A white dot indicates at least a miss in a set.

stack. At around sample 25k, the sender starts sending packets and it continues to do so until sample 100k. In some cache sets, e.g., cache set number 53, we don't see any activity and that is because none of the NIC buffers are mapped to those sets. On the other hand, on some cache sets, e.g., cache set number 21, we see activity regardless of whether the packets are arriving at the NIC, due to the always-miss scenario described in Section 3.

The packet chasing attacker, with the ability to distinguish between an idle system vs. when there are incoming packets, establishes a leaking channel that can be exploited to covertly communicate secret data over the network. This is more difficult in the presence of other cache activity, but this action need only be done once between system reboots, so this can be done in the middle of the night, or the attacker can patiently wait for the system to become idle. We can further extend the bandwidth of this leaking channel by differentiating the receiving streams based on frame sizes. Since the incoming packets are stored in contiguous rx buffers, using the same way that we construct the eviction sets for the page-aligned cache sets, we construct eviction sets for the second cache blocks in the page. All the second cache blocks in the pages are mapped to one of these 256 cache sets. Similarly we find the sets for the third and fourth cache blocks of the pages. This now allows us to recognize not just the presence of a packet, but also the size of the packet.

Figure 8 shows the result of a simple experiment where we send packets of different sizes and test our ability to detect packet size. On the columns we have 4 different runs with constant packet sizes being sent, from one cache block (64 bytes) to 4 cache blocks (256 bytes). On the rows we show detection on 4 different cache eviction sets, block 0 to block 3 which are targeting the first to fourth blocks in the page-aligned buffers. As expected, we see clear activity on the diagonal and above, and no activity below the diagonal. The only exception is 1-block packets which exhibit activity on block 1 as well as on block 0. This is because there is a performance optimization in the driver code that prefetches the second block of the packet regardless of the packet sizes. The reason for this optimization is that most Ethernet packets
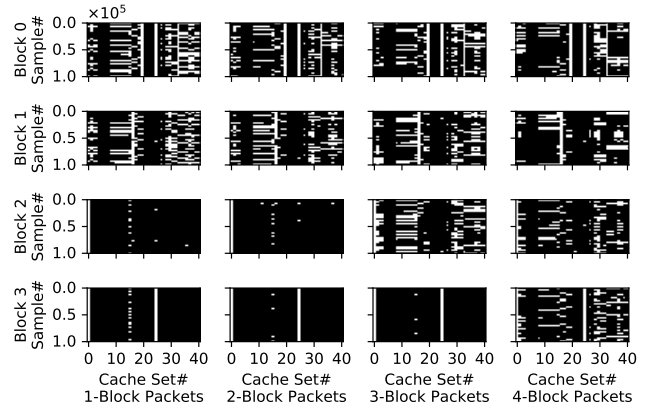
have at least two blocks, and 64-byte packets (0-Block Packet) are only common in control packets that don't have payloads such as TCP acknowledge packets.

The attack distinguishes a stream of packets with different sizes from each other, and that could be used to construct a remote covert channel (More details in Sec 4) with 1950 bytes-per-second bandwidth by only detecting a stream of small packets vs. stream of large packets (essentially, a binary signal). However, we can turn this to a more powerful channel if we differentiate sizes with finer granularity, essentially sending multiple bits of information per packet. The following subsection describes the method that we use to further narrow down the monitored sets while we perform Prime+Probe.

3.3 Chasing Packets over the Cache

The attacker has to probe all 256 page-aligned sets at once to detect incoming packets only because she doesn't know which buffers get filled first, and then probe more sets to detect packet size. However, if we know the order in which the buffers get filled in the driver, then we can actually chase the packets over the cache by only probing the cache sets corresponding to the next expected buffer, building a powerful high-resolution attack. We show that it is possible to almost fully recover the sequence of the buffers by performing an offline statistical analysis phase. Since the buffers are always recycled and then get back to the ring, the order of the buffers in the ring is maintained during the lifetime of the driver.

Algorithm 1 describes the SEQUENCER procedure that we use to recover the sequence. It consists of three steps. First, in the GET_CLEAN_SAMPLES step, we gather cache probe

Algorithm 1 Ring Buffer Sequence Recovery

```
 1: procedure Sequencer
 2:     samples ← get_clean_samples(Nsets, Nsamples)
 3:     graph ← build_graph(samples)
 4:     sequence ← make_sequence(graph)
 5:     return sequence
 6: end procedure
 7: procedure get_clean_samples(Nsets, Nsamples)
 8:     monitor_list ← [0..Nsets]
 9:     samples ← repeated_probe(Nsamples, monitor_list)
10:     for all x ∈ monitor_list do
11:         if activity(samples[x]) > activity_cutoff then
12:             replace x in monitor_list with the 2ⁿᵈ block of the page
13:             goto: 3
14:         end if
15:     end for
16:     return samples
17: end procedure
18: procedure build_graph(samples)
19:     curr← 0, prev← 0
20:     for i ∈ {0, …, SAMPLES} do
21:         for all cand ∈ monitor_list do
22:             if samples[i][cand] < miss_threshold then        ▷ no activity
23:                 continue
24:             end if
25:             if curr≠ prev then                               ▷ no self-loop
26:                 graph[prev][curr][cand]← graph[prev][curr][cand]+1
27:                 (prev, curr)←(curr, cand)
28:             end if
29:         end for
30:     end for
31:     return graph
32: end procedure
33: procedure make_sequence(graph)
34:     root ← get_root(graph)
35:     sequence ← [], (prev,curr) ← root
36:     repeat
37:         sequence.push(curr)
38:         (next,weight)← get_max_weight(graph[prev][curr])
39:         if weight < weight_cutoff then
40:             break
41:         end if
42:         graph[prev][curr][next] ← 0                          ▷ mark as visited
43:         (prev, curr) ← (curr, next)
44:     until (prev, curr) ≠ root
45:     return sequence
46: end procedure
```

samples for *Nsets* cache sets. To this end, we start with constructing the eviction sets for the page-aligned NIC buffers. However, as mentioned in Section 3, sometimes we have always-miss scenarios on some sets, which is easily observed a priori. For those sets, we simply use the second cache block of a page-aligned buffer instead of the first one.

After that, we start building a complete weighted graph with the nodes being the monitored cache sets and the weights on the edge that connect node x to node y are the number of times that we observe an activity on y which was immediately followed by an activity on node x, as visualized in the leftmost graph in Figure 9. To deal with the problem

that multiple buffers can map to the same cache set, when we build the graph, we maintain one node history for each edge. This allows the algorithm to distinguish between the activity on two or more different buffers that map to the same cache set by their successor cache sets. So, for example in Figure 9, two different buffers are mapped to cache set number 2. These buffers occupy location numbers 93 and 193 in the ring buffer. Therefore, in the final sequence, we have two different instances of cache set number 2, one that is followed by cache set 3 and the other that is followed by cache set 1.

The final step, Make_Sequence, is to traverse the graph we build in the previous steps, starting from a random node, and continuing to move forward until we reach the same node. Note that since the final sequence is a *ring* in which the *in-degree* and the *out-degree* of each node is exactly one, the choice of the starting node doesn't change the outcome of the procedure.

While this procedure can recover the sequence of the buffers that are mapped into *Nset*, it can only do so if we monitor a limited portion of the page-aligned cache sets (we were successful up to 64 cache sets). This is because the probe time gets longer than what is required to detect the order of the incoming packets, if we include more sets in our monitor list. So we first find the sequence for 32 cache sets, then we repeat the Sequencer procedure with the first 31 nodes (node 0 to node 30) plus a candidate node (e.g, 32) and we try to find the location of the candidate in the sequence. Then, we repeat the same procedure for the nodes 1 through 31. We repeat the procedure until we find a place in the sequence for all cache sets.

Sometimes two consecutive buffers are mapped into one set. For example, consider the case that buffers number 93 and 98 are mapped into the set 2 in Figure 9. With our approach, we don't capture these cases in the first round, but starting from the beginning, we can find a place for them if we have a representative node, in the graph that we traverse, that maps to a buffer which is between these two, e.g., buffer number 94.

We measure Levenshtein distance [61] to quantify the distance between the sequence that we obtain and the ground truth actual sequence that we get from driver instrumentation. The Levenshtein distance between two sequences is the minimum number of single-character edits (i.e., insertions, deletions or substitutions) needed to change one sequence into another. We see the results of such experiments in Table 1. Fine-tuning the probe rate is a rather challenging task as it needs to be long enough that the activity of each incoming packet touches only one sample, and needs to be small enough to not lose the temporal relation between the incoming consecutive packets. Otherwise, we see a drop in accuracy of the obtained sequence. However, in our covert-channel construction, in many of our attack scenarios, we
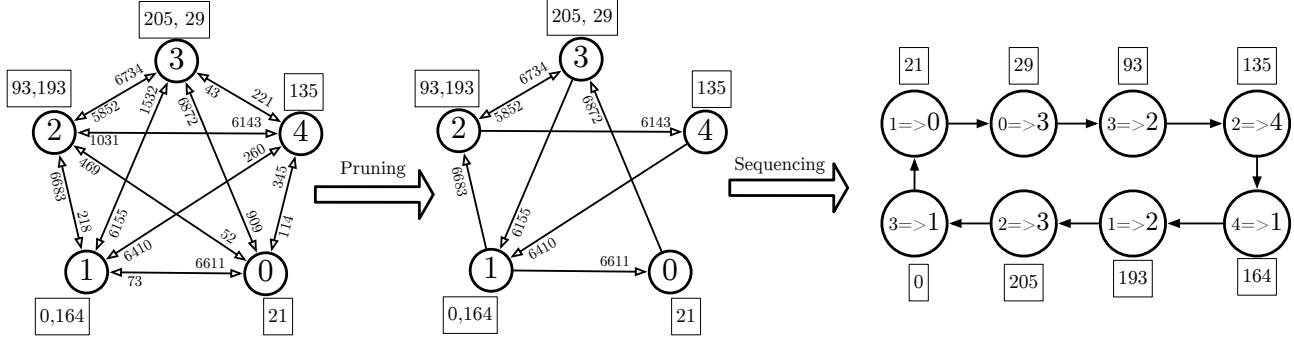
Figure 9. Pruning and sequencing of the set graph to get the order of ring buffers. Each node represents a set in the attacker address space. Numbers in squares are the sequence number of the associated ring buffers that map to same set.

only need find buffers that are in different parts of the ring, so small errors in the sequence is tolerable.

During the profiling period we rely on a remote sender whose only job is to constantly send packets. However, the spy can recover the sequence even without the help of the external sender, as long as the system is receiving packets. In fact, noise (extra packets not sent by co-operating sender) in this step only help the spy.

4 Packet Chasing: Receiving Packets without Network Access

In this section we show the effectiveness of the Packet Chasing attack by constructing a covert channel over the network.

Threat Model. We assume a simple threat model where a remote trojan attempts to send covert messages through the network, to a spy process located in the same physical network. As shown in Figure 10, the spy process is inside a container and does not have root privileges, neither in the container nor in the host OS, and is also not permitted to use the networking stack. The trojan process has the ability to send packets to the physical network, but there is no authorized method to communicate with spy.

Table 1. Summary of experiments for sequence recovery

Results		
Measure	Value	CI
Levenshtein Distance	34.7	[22, 51]
Error Rate (%)	13.5	[8.5, 19.9]
Longest Mismatch	5.7	[3, 9]
Time (Minutes)	238	[230, 244]
Parameters		
Parameter	Value	
Number of Samples	100,000	
Number of Monitored Set	32	
Packet Rate (packet/s)	0.2M	
Probe Rate (probe/s)	8000	
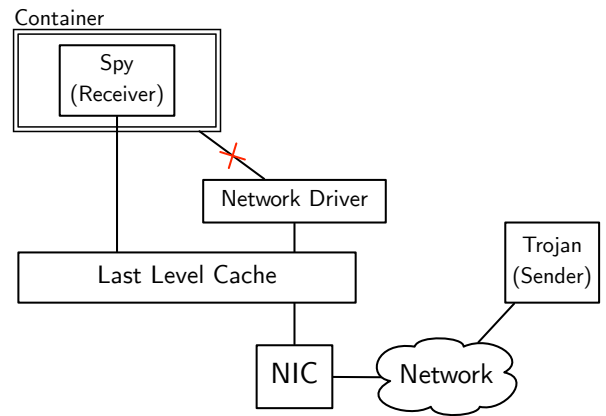
Figure 10. Remote covert communication scenario.

Channel Capacity. To build a framework for quantitatively comparing different encoding and synchronization schemes, we follow the methodology described in [24] and measure the channel bandwidth and error rate of transferring a long pseudo-random bit sequence with a period of $2^{15} - 1$. The pseudo-random bit sequence is generated using a 15-bit wide linear feedback shift register (LFSR) that covers all the 2^{15} sequences, except the case that all bits are zeros. This allows us to spot various errors that might happen during the transmission including bit loss, multiple insertion of bits, or bit swaps [24].

Data Encoding and Synchronization. The spy first chooses x, one of the page-aligned cache sets that only one of the ring buffers is mapped to. Finding such a page-aligned cache set is not challenging using the approaches described in Section 3. Then the spy process finds the cache sets to which the addresses $x + 64$, $x + 2 * 64$, and $x + 3 * 64$ are mapped. In other words, it finds the cache sets for the second, third, and fourth cache blocks of the page-aligned buffer. As described in Section 3, the spy process knows the set index bits for these sets, but the outcome of the hash function (slice bits) are not known. To find out the exact slice, the spy process

executes a trial and error procedure in which it selects one of the eight slices based on the activity on the sets. After this step, the initialization is done and the spy process constantly monitors the found cache lines.

The spy process, at time frame *n*, sends 256 (the length of the ring buffer) packets of size $(S + 2) * 64$ to transmit the symbol S. Since we operate on the network and the latency is fluctuating frequently, we cannot use return-to-zero self-clocking encoding [24], rather we choose to use a synchronized clock encoding scheme in which the first block of the buffer acts as a clock to synchronize the spy with the trojan. We explore the bandwidth and error rate for two cases: First, we encode one binary symbol in each packet, i.e., we send either 64-byte packets that encode "0", or we send 256-byte packets that encode "1". Second, we send a ternary symbol in each packet, i.e, we send 64-byte packets to encode "0", 192-byte packets to encode "1", and 256-byte packets to encode "2".

For example, Figure 11 shows a part of a sequence that the spy receives in a real experiment. In this experiment, the trojan transmits sequence "2012012012..." and the spy collects one sample from the three cache sets in every 200, 000 cycles. When decoding, the spy uses a window of three samples to distinguish between different values. This is because sometimes we see the cache activity of one packet (one symbol) that spans across two cycles (the wide peaks in the figure). The spy process should not decode these cases into two different symbols. In addition, having a window helps if the activity on the sets get skewed because of the delay of arriving packets. The first set is used as a clock to synchronize the parties, therefore the activity on the other two sets can show the transmitted values. Monitoring the activity of the two sets only gives us three different symbols because by sending a 3-block packet, we have a compulsory activity on set 2.

To estimate the error rate, we use edit Levenshtein distance [61] between the sent and received data for the pseudo random bit sequence. Figure 12 shows the bandwidth and error rate of our coding schemes as well as the effect of varying the probe rate, i.e., the time that we wait between consecutive probes. The bandwidth of the channel is almost constant with different probe rates. This is because the limitation here is the line rate. We are using 1000Mb/s Ethernet link and transmitting a collection of packets whose average size is 192 Bytes. The maximum frame rate for the packets with frame size of 192 is around 500,000 frames per second [62]. Since we are sending one symbol per 256 packets, therefore our maximum bandwidth is theoretically bounded at 1953 symbols per second. By coding three symbols, this packet chasing covert channel can reach a bandwidth of 3095 bps. The error rate, however, is reduced as we reduce the probe time. That is because with a longer wait time between two consecutive probes, we raise the probability of capturing irrelevant background activity on the sets. When we use
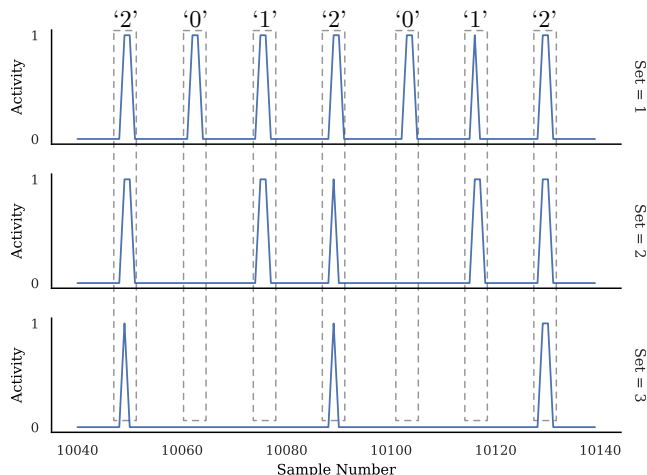
Figure 11. Spy process decodes the transmitted sequence based on the monitored activity on the probed sets. Set 1 acts as the clock and the activity is one for a set if we find at least one miss in the blocks in the eviction set of the probed set.

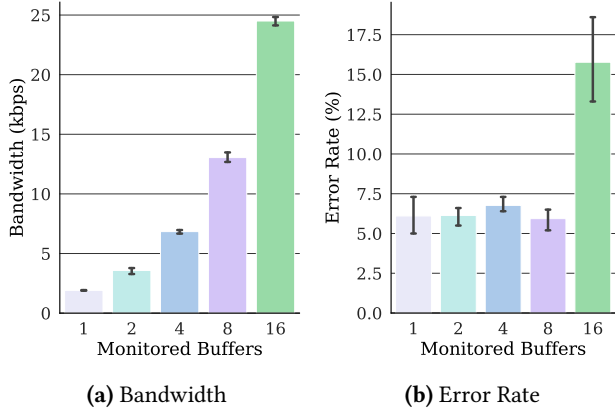**(a)** Bandwidth **(b)** Error Rate
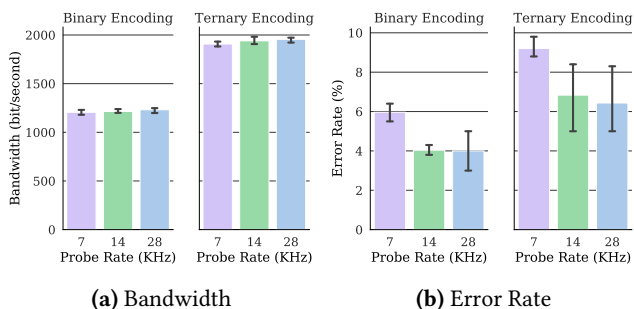
Figure 12. Bandwidth and error rate of the remote covert channel for binary and ternary encoding and various cache probe rates.

Binary encoding, we use the samples from both *set 2* and *set 3* and if they both have activity during a window, we decode as "1". Therefore, the error rate is slightly less than the Ternary encoding.

Exploiting Ring Buffer Sequence Information. If we know the ordering of the buffers, this mechanism is easily extended to send more than one symbol per 256 packets. In this case, the trojan can send one covert message every *256/n* packets by dividing the ring buffer into *n* sections of similar sizes by selecting *n* buffers that are ideally *256/n* apart. The selected buffers should be among the buffers that are mapped to only one of the page-aligned cache sets. Then the spy starts monitoring the selected sets and their adjacent blocks to detect the size of the packets that are filling these buffers.
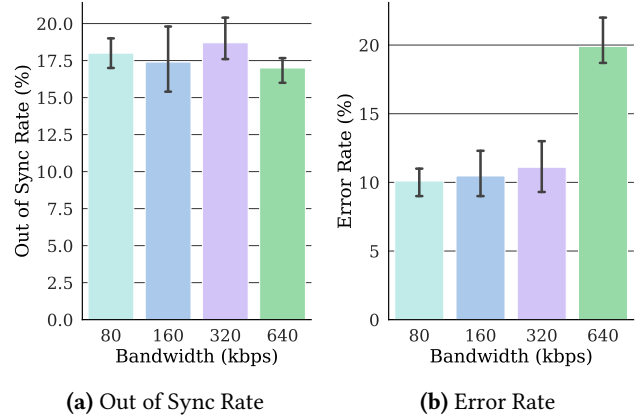
This process can multiply the capacity of the covert channel as shown in Figure 13. This figure shows the bandwidth

(a) Bandwidth   **(b)** Error Rate

Figure 13. Bandwidth and error rate of the remote covert channel for the spy that uses the ring's sequence information.

(a) Out of Sync Rate   **(b)** Error Rate

Figure 14. Bandwidth and error rate of the remote covert channel for the spy that uses the ring's sequence information.

and the error rate for the cases that the spy monitors a different number of buffers in the ring. For each of these buffers the spy probes three cache sets that are associated to the first, third, and fourth cache blocks of the packets that fill these buffers. For the case that there is only one monitored buffer, the trojan sends one covert message with 256 packets, and for the case of 16, the trojan sends a new message every $256/16 = 16$ packets. The bandwidth of the channel almost doubles when we double the number of monitored buffers and it goes up to 24.5 kbps for the case of 16 monitored buffers. The error rate remains almost constant until the time between incoming packets gets close to the time between two consecutive probes. Note that when we have more sets in our monitored list, each probe takes more time and this decreases the probe rate. Furthermore, with the increased number of monitored buffers, it becomes harder to find the buffers that are n buffers apart in the ring and also do not share the cache set with any other buffer in the ring. For these reasons, we see a jump in the error rate when we monitor 16 buffers of the ring. Note that these and subsequent results also account for inaccuracies incurred when we deconstruct the ring sequence.

Figure 14 shows the result of another experiment in which we actually chase the packets using the sequence. We probe one buffer at a time and as soon as we detect an activity on the probed buffer, we move to the next buffer in the sequence. The *out-of-sync* rate is the rate by which packet chasing misses one packet, and therefore it has to wait until completion of the whole ring, or the next time a packet fills that buffer, to get synchronized again. The bandwidth is controlled by the rate that the sender sends the packets and the error rate is calculated on the synchronized regions of the transmission. The figure shows that the out-of-sync rate is almost constant for different packet rates. That is because when we probe just one set, the resolution of probing is higher than the time between consecutive packets. In

addition, the frequency at which we get out-of-sync is a function of the quality of the sequence that we obtain. The error rate jumps at 640 kbps, which is because at that speed the packets start to arrive out-of-order at the receive side.

Detectability and Role of DDIO/DCA   The packets that carry the covert messages are hard to detect and filter as they can be regular broadcast packets, e.g., DHCP and ARP, and they are not even required to be destined for the machine that host the spy. This is because, with DDIO/DCA, the network adapter directly transfers the packets into the last level cache of the processor, and only after this will the driver examine the header of each frame and discard the packets that do not target any protocol that is hosted in that machine.

5   Packet Chasing: Exploiting Packet Size Detection

In this section we present a sample application for a Packet Chasing attack, in which we use the high resolution samples of packet sizes to gain information on the co-located user's browsing data. For example, the spy could be waiting for the victim to enter a particular website before initiating some action such as a password detection attack.

This simple attack consist of two phases. First, the offline phase in which the adversary generates traces of packet sizes for different websites of interest, then processes these traces and calculates a representative trace for each website, which is just a point-wise average of the packet sizes, resulting in a vector of these points (average packet size) over time.

In preparation for the attack, the attacker builds the sequence of the ring buffers, as previously described. After that, the attacker enables spy mode in which she constantly monitors the first two cache blocks of the first buffer in the sequence until she finds a window in which there are activities on both block 0 and block 1. This indicates that a packet is filling that buffer. Then, similar to the receiver in the covert

channel, on each detected activity the attacker moves to the next buffer in the sequence. Each time, the attacker monitors the first 4 block of the first half-page of the buffer as well as the first 4 block of the the second half-page of the buffer. That is because the driver switches between the halves of the pages when there is a large packet (See Section 3.1). This enables the attacker to distinguish between packets with 4 level of sizes. After collecting the samples of packet sizes, the spy feeds the collected vector into a simple correlation-based classifier which calculates cross-correlation [63] of the collected samples with the representatives of different target websites.

Figure 15 shows an example of the signals that we obtain by Packet Chasing and the actual packet sizes that are captured using tcpdump [64] packet analyzer. The websites are accessed using Mozilla Firefox version 68.0.1. The figure shows how packet size, even in cache block granularity, can be an identifier for the webpages that are being accessed. The packets are usually congested on the two sides of the spectrum, they are either carrying a very large message that got fragmented into MTU-sized frames, or they are small control packets [65]. But the last packet of the large messages can fall anywhere between 1-block to MTU, giving us a good indicator of the webpages. In addition, combining packet sizes with the temporal information that Packet Chasing obtains from the packets, gives us enough information to distinguish between webpages. We evaluate our fingerprinting attack using a small closed world dataset with 5 different webpages: facebook.com, twitter.com, google.com, amazon.com, apple.com. In our experimentation with 1000 trials, Packet Chasing detects the correct website with average of 89.7% accuracy. We use a simple classifier in this experiment, but given the challenges for this particular attack, a classifier that is tolerant of noise as well as slight compression or decompression of the vectors would be likely to improve these results.

6   Potential Mitigation

In this section, we discuss potential hardware and software mechanisms that one could employ to help mitigate the attack. All come with some performance impact.

Cache Isolataion. Any method that eliminates cache side channels would stop this attack, including isolating the LLC so that partitions (slices) are not shared between cores. But that comes at a significant performance cost [40, 43, 44], which is why cache side channels remain.

Disabling DDIO/DCA. DDIO enables these attacks because it ensures the header and the payload appear in the cache simultaneously, greatly simplifying the detection of packet size. Without this, however, attacks are still possible. If we can detect the presence of packets (headers are always accessed immediately and will appear in the cache in sequence),

we can still establish a covert channel with inter-arrival timing. We could also send types of packets where the reading/processing of the payload is quick and deterministic, again allowing us to distinguish sizes.

Randomizing the Buffers. While Packet Chasing exploits the sequence by which the packets fill the ring buffers to boost the resolution of the side- and covert-channels, we show that attacks are still possible, without knowing the sequence of the buffers (Section 4). However, randomization does significantly reduce the channel bandwidth. The cost of randomization could be quite high, as the driver and network adapter would now need to constantly synchronize on the address of the next buffer. Because our attack setup takes some time, though, it may only be necessary to permute the buffer order at semi-regular intervals, thus limiting the overhead.

Increasing the Size of the Ring. In the absence of sequence information, the required probing of the cache scales with the size of the ring if the attacker wants to catch every packet. Thus a combination of occasional reshuffling of the ring, and a larger ring, may be effective in making the probe set larger enough to make the attack difficult to mount cleanly without picking up significant noise.

7   Disclosure

We disclosed this vulnerability to Intel, explaining the basic substance of the vulnerability and offering more details.

8   Conclusion

This paper presents Packet Chasing, an attack that detects the frequency and size of packets sent over the network, by a spy process that has no access to the network, the kernel, or the process(es) receiving the packets. This attack is not enabled by the DDIO network optimization, but is greatly facilitated by it. This work shows that the inner workings of the network driver are easily deconstructed by the spy process setting up the attack, including the exact location (in the cache) of each buffer used to receive the packets as well as the order in which they are accessed. These two pieces of information dramatically reduce the amount of probing the spy must do to follow the network packet sequence.

This information enables several possible covert channels between a remote sender and a spy anywhere on the network, with varying bandwidth and accuracy tradeoffs. It also enables a side channel leakage attack that can detect the web page access activity of a victim process.

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(a) facebook.com

(b) twitter.com

(c) Recovered facebook.com

(d) Recovered twitter.com
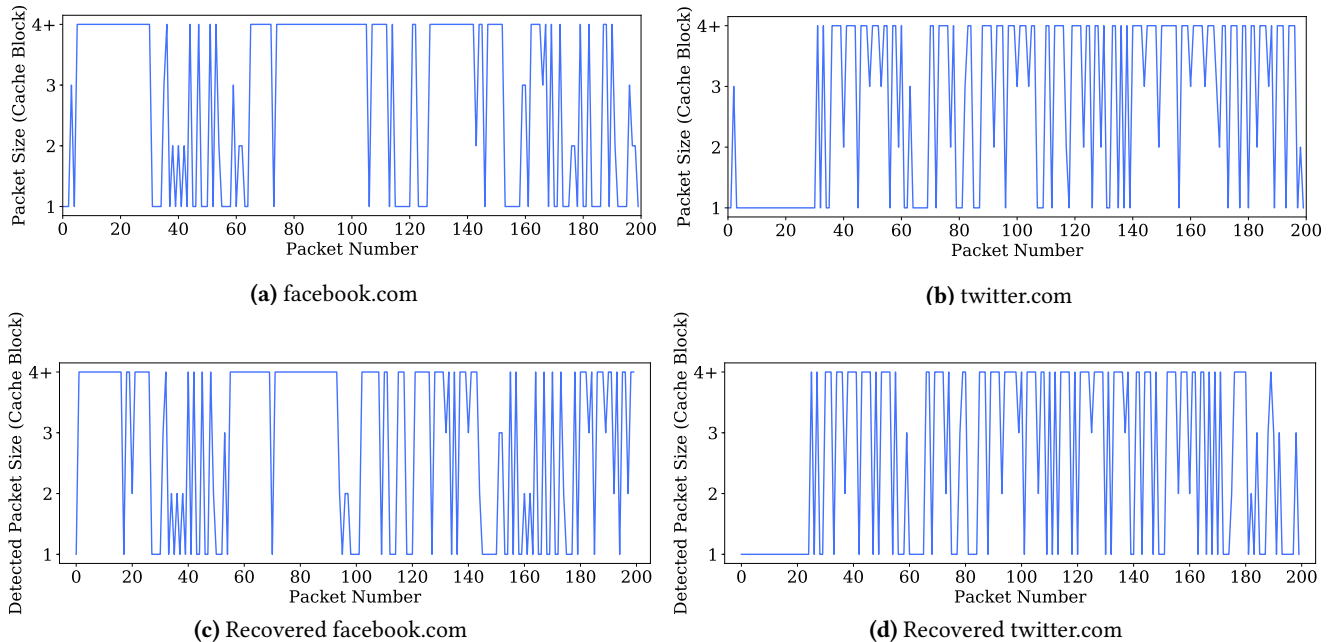
Figure 15. Packet size detection for website fingerprinting. Shows original packet sizes versus the recovered packet sizes by Packet Chasing for the first 200 packets of the websites.

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