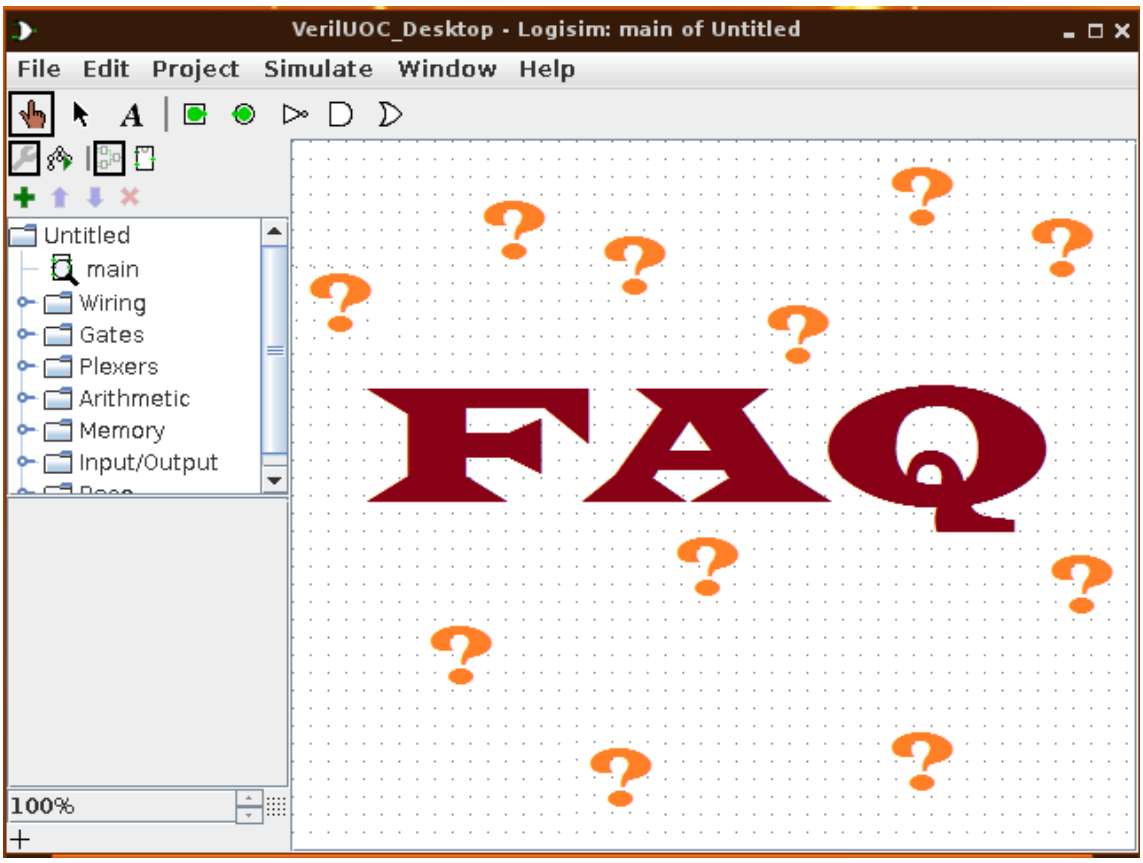
Frequently Asked Questions and Issues Related to VerilUOC_Desktop



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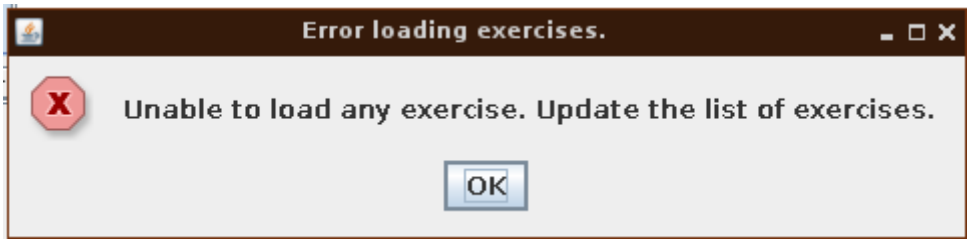
Questions and Answers – Problems and Solutions

1. Question: As VerilUOC_Desktop is stored in a *.jar* file, I conclude that VerilUOC_Desktop has been developed in Java. Would be possible to install and run VerilUOC_Desktop on a computer with Java installed, without using the virtual machine?

Answer: No. Although it is true that VerilUOC_Desktop has been developed in Java, many of its features rely on applications and services that are installed on the virtual machine. Therefore, if VerilUOC_Desktop would run outside the virtual machine, those functionalities would not be available or would produce an incorrect behavior.

2. Problem: I get the message below when I run the command **`Simulate -> Verification.`** It seems the list of exercises should be updated.



Solution:

Probably the mysql database service has stopped or is not working properly. Do the following:

1. Close VerilUOC_Desktop.

2. Open a terminal (**`Applications → Utilities → Sakura Terminal`**) in the virtual machine and run:

```
sudo /etc/init.d/mysql   start
```

3. **IF** the output of the command is "Mysql already running." **THEN** run in the terminal:

```
sudo /etc/init.d/mysql   restart
```

4. Open VerilUOC_Desktop and click again **`Simulate -> Verification`**.

3. Question: May I get a PDF version of the documentation listed in the VerilUOC_Desktop wiki?

Answer: No, there is not a PDF version of this documentation, and we do not foresee to generate it.

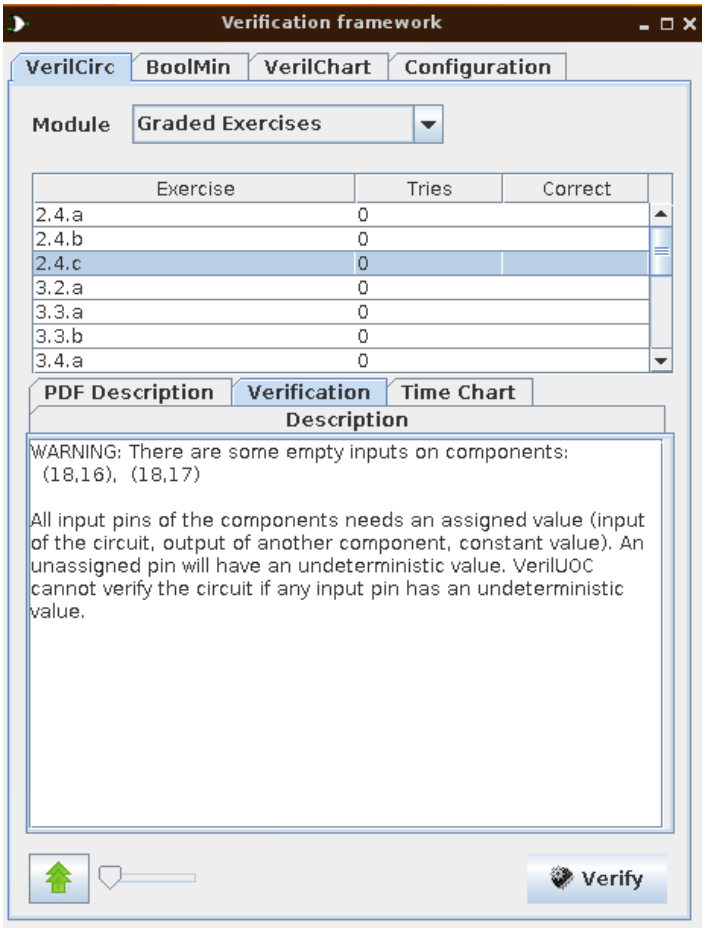
4. Question: If I am designing a circuit with Logisim and I need information on inputs, outputs and/or operation of a particular cell, how do I get this information?

Answer: In VerilUOC_Desktop, click on **`Help → Tutorial.`** You will find detailed information about all the components.

5. Problem: I have completed the design of one of the weekly exercises and, when I try to verify it with VerilCirc I get the message (see figure):

WARNING: There are some empty inputs on components

(X, Y) Note: X and Y stand for numbers

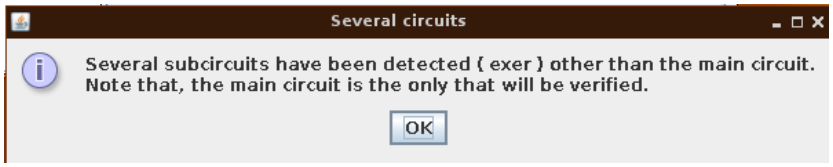


Solution: The reason is that there is some component in the circuit with inputs unconnected (floating inputs), or some output pin unconnected. Floating inputs is the most common cause.

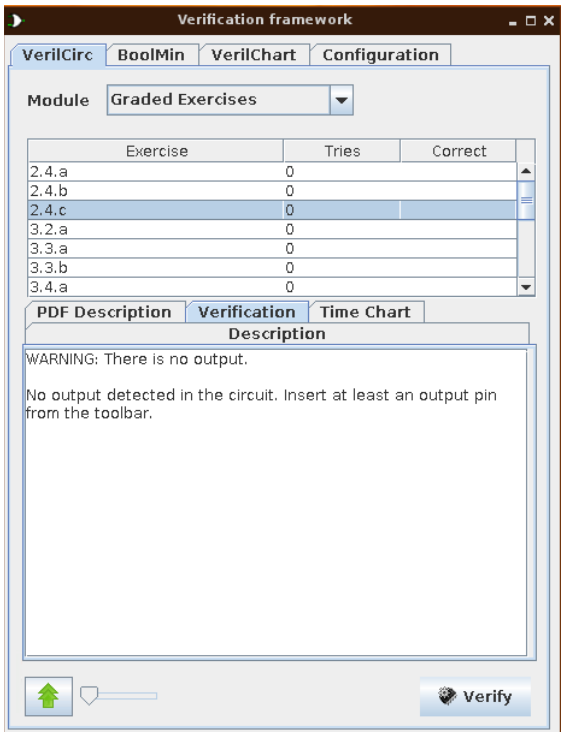
When you add a logic gate the program, Logisim selects by default a 5-input gate and, if you are using fewer inputs, some of them remain unconnected. You should define the required number of inputs for the logic gate in the "Number of Inputs" property (left menu) and select that number.

The pairs of numbers in the message indicate the coordinates of the unconnected inputs. In the Logisim window, the coordinates of the mouse position appear in the lower left corner when the icon  in the toolbar is on.

6. Problem: I have completed the design of one of the weekly exercises and, when I try to verify it with VerilCirc I get the following warning:



Then, after clicking on the **OK** button, I get a new message telling me that my circuit does not have any output (see next figure). But my circuit does actually have outputs and they are properly connected.



Solution: The most likely cause of this error is that your design is a different circuit (a subcircuit) other than the **main** circuit. In the problem statement, the name of the different circuit is **exer** (see the message in the first figure). The verification tool only verifies designs that are in the **main** circuit.

A common cause of this problem, especially when you are performing a new design, is the sequential execution of the following two commands: **File → New** and **Project → Add circuit**. Last command creates a new subcircuit for the design you want to enter which is not the **main** circuit. To avoid this situation, just run **File → New** when you want to enter a new design.

If you have already entered your design, copy your design in the **main** circuit to recover it by following these steps:

- Open VerilUOC_Desktop
- Load the file with your design (**`File → Open → file_name`**)
- Open a new, empty window (**`File → Open`**)
- In the window that displays your design:
  - * Select the whole design (**`Edit → Select All`**)
  - * Copy the design to the clipboard (**`Edit → Copy`**)
- In the empty window:
  - * Paste the design (**`Edit → Paste`**)
  - * Click in the editing background to unselect the elements of the circuit
- Close the window that contains the original design (**`File → Close)`**.
- In the window that contains the pasted design, save the circuit in a new file (**`File → Save as → new_file_name`**)
- Verify the copied design with VerilCirc as usual (**`Simulate → Verification → Select the exercise → Press the Verify button`**)

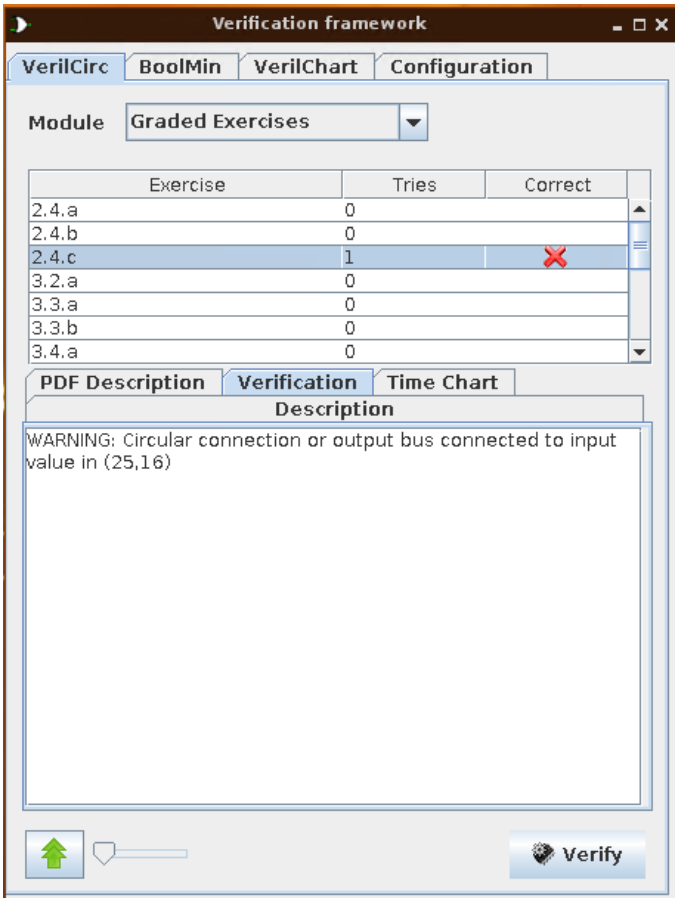
7. Problem: I have completed the design of one of the weekly exercises and, when I try to verify it with VerilCirc I get a message telling me that some inputs and/or outputs are unlabeled (unnamed). However, I named inputs and output using the *Text Tool* or *Label* command, which allows inserting labels in the circuit.

Solution: The independent labeling command should not be used to named inputs and outputs. To name an input or an output, click on it and write the name in the field **`Label`** (properties panel, bottom-left corner).

8. Problem: I have created a circuit using he circuit analysis Logisim tool (**`Project → Analyze Circuit`**). When I try to verify it I get a message telling that there are no inputs defined. But the circuit actually does have inputs.

Solution: When you use the Logisim circuit analysis tool, after pressing the **`Build Circuit`** button a form appears. In this form, the field **`Circuit Name,`** by default, has the name **main**. VerilCirc only can verify designs stored in the **main** circuit, therefore, **you should not change the name main**.

9. Problem: I have completed the design of one of the weekly exercises and, when I try to verify it with VerilCirc I get a message "**WARNING: Circular connection or output bus connected to input value in (25,16)**". What does it mean?



Solution: This error occurs when a forbidden circular connection among two or more components, usually combinational components, is found.

A circular connection is a connection between several components forming a loop. For example, let's imagine a circuit consisting of *n* cells, three of which (c_1, c_2 and c_3) are logic gates connected so that the output of c_1 is connected to an input of c_2; the output of c_2 is connected

to an input of c_3 and the output of c_3 is connected to an input of c_1. That would be a case of circular connection between c_1, c_2 and c_3.

The pair of numbers (25, 16) indicates the position of a terminal of one of the cells that are part of the circular connection. The current position of the cursor is shown in the lower left corner when the icon  in the toolbar is on. The coordinates given by the pair of numbers can be easily located by moving the cursor and watching the numbers that appear at the lower left corner of the screen.

10. Problem: I have simulated a circuit with Logisim, and it does not behave as expected. I noticed that one of the cells, namely a 3-input XOR gate, presents a malfunction: When inputs are 111 output should be 1 and the simulator produces one 0. By contrast, the 2-input XOR cell behaves correctly and if I connect a cascade of multiple XOR gates, the behavior is also correct.

Solution: Although in Boolean algebra the XOR is defined as an associative operation, and therefore $1 \oplus 1 \oplus 1 = (1 \oplus 1) \oplus 1 = 1$, in the field of digital systems coexist two definitions of the functionality of an n-inputs XOR gate:

- Output=1 when one and only one input is 1, or
- Output=1 when an odd number of inputs take the value 1 (this definition is coherent with the Boolean algebra)

By default Logisim uses the first definition, but you can change it by clicking of the property “Multiple-input Behavior” (lower left menu) and selecting “When an odd number are on”.