3 Architecting Power

In CMOS technology, dynamic power consumption is related to charging and discharging parasitic capacitances on gates and metal traces. The general equation for current dissipation in a capacitor is:

$I = V*C * f$

where I is total current, V is voltage, C is capacitance, and f is frequency.

Thus, to reduce the current drawn, we must reduce one of the three key parameters. In FPGA design, the voltage is usually fixed. This leaves the parameters C and f to manipulate the current. The capacitance C is directly related to the number of gates that are toggling at any given time and the lengths of the routes connecting the gates. The frequency f is directly related to the clock frequency. All of the power-reduction techniques ultimately aim at reducing one of these two components

3.1 Clock control

An effective way to lower the dynamic power dissipation in synchronous digital circuits is to dynamically disable the clock in specific regions that do not need to be active at particular stages in the data flow, as most of the dynamic power consumption in an FPGA is directly related to the toggling of the system clock.

Figure 3.1 illustrates the poor design practice of simple clock gating. With this clock topology, all flip-flops and corresponding combinatorial logic is active (toggling) whenever the Main Clock is active. The logic within the dotted box, however, is only active when Clock Enable = 1. Here, we refer to the Clock Enable signal as the gating or enable signal. By gating portions of circuitry as shown above, the designer is attempting to reduce the dynamic power dissipation proportional to the amount of logic (capacitance C) and the average toggle frequency of the corresponding gates (frequency f).

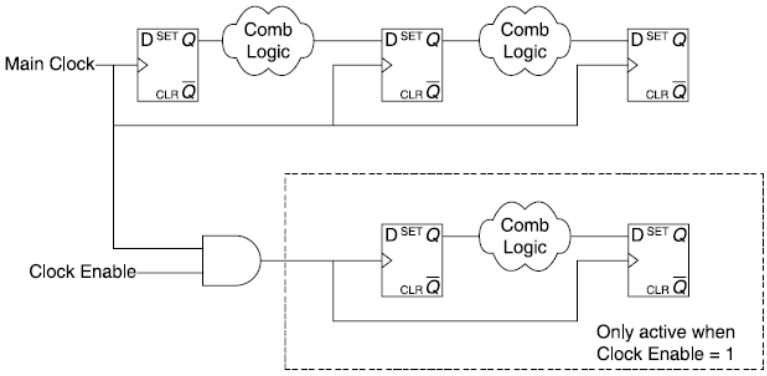

Figure 3.1: Simple clock gating: poor design practice.

When a clock is gated even in the most trivial sense, the new net that drives the clock pins is considered a new clock domain. This new clock net will require a low-skew path to all flip-flops in its domain, similar to the system clock from which it was derived.

To summarize, clock control resources such as the clock enable flip-flop input or a global clock mux should be used in place of direct clock gating. Clock gating is a direct means for reducing dynamic power dissipation but creates difficulties in implementation and timing analysis.

3.1.1 Clock Skew

In Figure 3.2, the propagation delay of the clock signal between the first flipflop and the second flip-flop is assumed to be zero. If there is positive delay through the cloud of combinatorial logic, then timing compliance will be determined by the clock period relative to the combinatorial delay + logic routing delay + flip-flop setup time. A signal can only propagate between a single set of flip-flops for every clock edge. The situation between the second and third flipflop stages, however, is different. Because of the delay on the clock line between the second and third flip-flops, the active clock edge will not occur simultaneously at both elements. Instead, the active clock edge on the third flip-flop will be delayed by an amount dC.

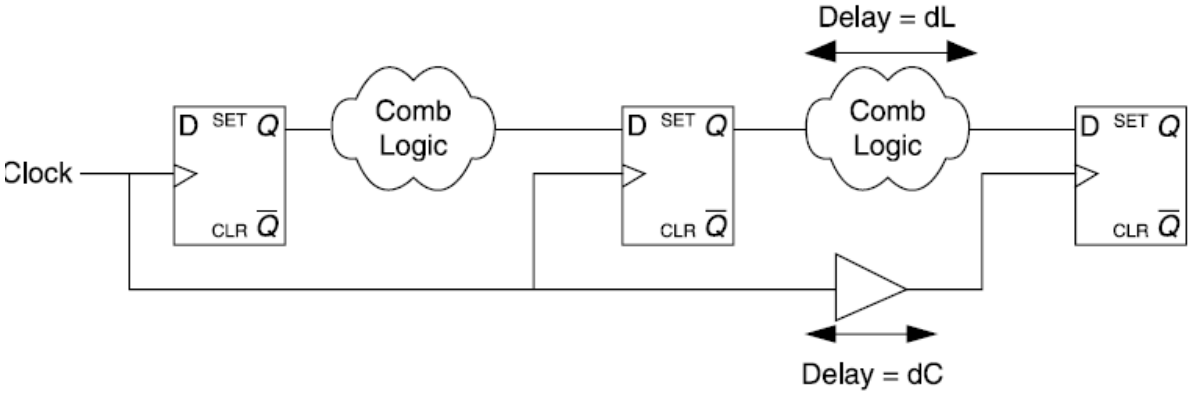

Figure 3.2: Clock Skew

If the delay through the logic (defined as dL) is less than the delay on the clock line (dC), then a situation may occur where a signal that is propagated through the second flip-flop will arrive at the third stage before the active edge of the clock. When the active edge of the clock arrives, the same signal could be propagated through stage 3. Thus, a signal could propagate through both stage 2 and stage 3 on the same clock edge! The “fly-through” issue described above will occur exactly the same way regardless of the clock frequency.

3.12 Managing skew

Clock gating can cause hold violations that may or may not be corrected by the implementation tools.

3.2 Input Control

To minimize the power dissipation of input devices, minimize the rise and fall times of the signals that drive the input.

Always terminate unused input buffers. Never let an FPGA input buffer float.#]

3.3 Reducing the supply voltage

Dynamic power dissipation drops off with the square of the core voltage, but reducing voltage will have a negative impact on performance. If this method is pursued, ensure that the timing analysis takes into consideration the lowest possible voltage on the supply rail for worst-case maximum timing.

3.4 Dual-edge triggered flip flops

Due to the fact that power dissipation is proportional to the frequency that a signal toggles, it is desirable to maximize the amount of functionality for each toggle of a high fan-out net. Most likely, the highest fan-out net is the system clock, and thus any techniques to reduce the frequency of this clock would have a dramatic impact on dynamic power consumption. Dual-edge triggered flip-flops provide a mechanism to propagate data on both edges of the clock instead of just one. This allows the designer to run a clock at half the frequency that would otherwise be required to achieve a certain level of functionality and performance.

Note that if dual-edge flip-flops are not available, redundant flip-flops and gating will be added to emulate the appropriate functionality. This could completely defeat the purpose of using the dual-edge strategy and should be analyzed appropriately after implementation.

Note: Yosys cannot synthesize dual edge triggered FFs.

3.5 Modifying terminations

There is no steady-state current dissipation with a series termination.