2.2 Control based logic reuse

Controls can be used to direct the reuse of logic when the shared logic is larger than the control logic. For instance, in *fir.sv*, MUXes and a counter are employed to select the appropriate coefficient and delayed sample that are passed to the single multiplier during each clock cycle. Figure 2.2, shows the synthesized design.

Note: the multiplier can be replaced with alternative implementations, such as a shift-and-add multiplier and a finite state machine can be utilized to control this process.

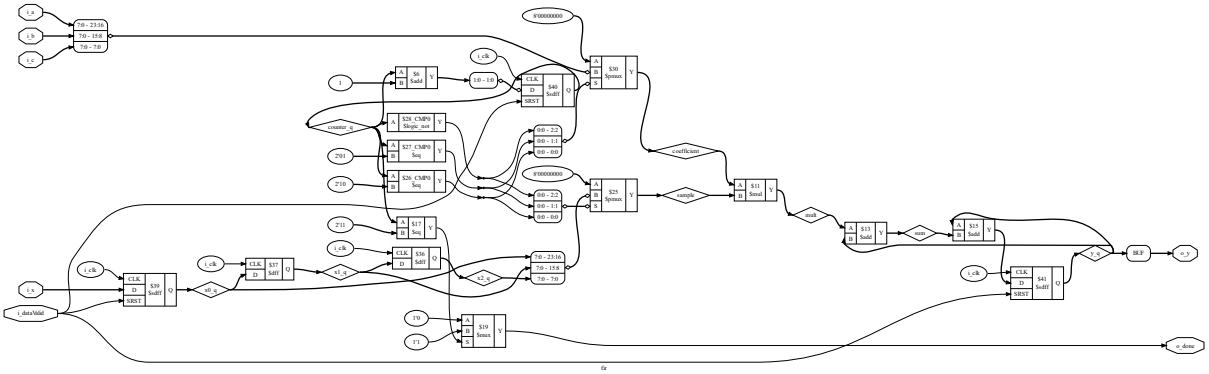

*Figure 2.2: FIR filter with one MAC that implements: Y = A*X[0] + B*X[1] + C*X[2]*