Full Custom Design of a Touchscreen Front-End in 0.18µm CMOS

Tej Sanghavi
Departmenrrt of Electrical and Electronic Engineering, Imperial College London
London, United Kingdom
tej.sanghavi17@imperial.ac.uk

***Abstract*—Integrated on almost every device nowadays, touchscreens have become a key element of consumer electronic products. These sensors have been traditionally realised by using capacitive elements, whose value varies with the user's finger presence. This article presents the development of a simple, low power, small area and relatively high-resolution front-end interface that converts a capacitance into a digital code that can be post-processed by the device CPU.**

Keywords—Capacitance to digital, time to digital converter (TDC), touchscreen interface.

I. Introduction

Over the past decade touchscreens have rapidly become the primary input mechanism for electronic systems. Their ease of use of has spurred this demand and a great deal of research has gone into this area to meet all sorts of design requirements. This article focuses on the critical front-end interface to capacitive touchscreens.

Conventionally analog to digital converters have been used to convert the capacitance to a digital value however another method which is analysed here involves the use of a TDC. Sophisticated high resolution TDCs such as the Vernier TDC [1] exist but simplistic methods can be modified to meet design requirements.

The remainder of the paper is organized such that the proposed system is introduced in the next section. In Section III, the main components of the system are analysed. Then in Section IV and V, the simulated results and layout are presented. Finally, in Section IV, future design improvements are discussed.

II. System Overview

The overall system design consists of 2 main stages to convert the capacitance of a touchscreen to a digital value. Block diagrams representing these stages are presented in Fig. 1 and Fig. 2 and their respective schematics shown in Appen. A and Appen. B.

A. Stage 1: Capacitance to time

A current mirror with a source and sink connection charges and discharges a capacitor resulting to a triangular wave output. The wave is converted to a square wave using 2 comparators with different threshold voltages; one turns on at a voltage less than V_{low} and the other at a voltage higher than V_{high}. The signals are connected to an SR Latch which results to a square wave output with a period proportional to capacitance as seen in (1).

$$T_{osc} = \frac{2(V_{high} - V_{low})C}{I} \quad (1)$$

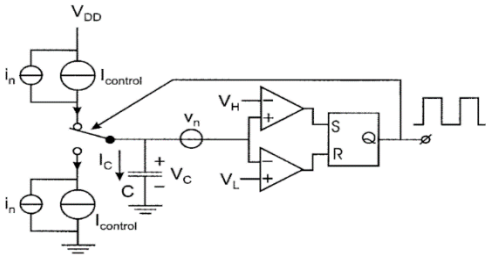


Figure 1: Stage 1 outline

Stage 2: Time to digital

A 10 MHz clock (CLK) signal samples the square wave output from stage 1 using an AND gate and each sample increments a counter which hence outputs a digital value corresponding to the pulse width of the square wave.

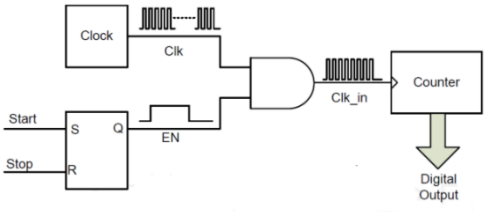


Figure 2: Stage 2 outline

The system was designed to meet the target design specifications as shown in Tab.1.

Table 1: Target Specifications

Name	Specification	Value
Area	Total Silicon Area	≤ 1 mm^2
VDD	Power Supply	1.8 V
P_{diss}	Power Dissipation	≤ 20 mW
F_{clk}	Input Clock frequency	≥ 10 MHz
C_{sensor}	Capacitance Variation	1 - 5 pF
C_{min}	Minimum Detectable Capacitance	0.5 pF
INL	Relative Error	≤ 2 %
DNL	Relative Error	≤ 2%
T	Temperature	27°C

III. Circuit Implementation

A. Stage 1

- Current Mirror: A simple current mirror design was used as shown in Appen. A. It consists of a PMOS branch to source current to charge up the capacitor, an NMOS branch to sink current from the capacitor and two other branches to sink current from the

comparators. The source and sink MOS connected to the capacitor were closely matched to ensure the same rate of charging and discharging current as shown in Appen. D however, this was limited by layout constraints. Matched MOS have a width in the order of fractions of µM and this would require multiples in the order of 100 for a common centroid design, greatly increasing area. Moreover, as their switching points are not matched shoot through occurs at the square wave edges as shown in Appen. E.

- Comparator: A well-known comparator design was used [2] consisting of 3 stages. The pre-amplification stage amplifies the input signal to improve the comparator sensitivity and isolates the input of the comparator from switching noise coming from the positive feedback stage/decision stage. The positive feedback stage determines which of the input signals is larger and the output buffer amplifies this information and outputs a digital signal. Appen. F and Appen. G shows the schematic and its associated switching waveforms.
- SR Latch: A NOR based SR Latch was selected over a NAND based one since its output doesn't change when the inputs are 0 unlike the NAND based one which results to an unstable output. In addition, via a reset pulse the circuitry in the top right corner of Appen. A forces the capacitor to begin charging when the interface is turned on.

B. *Stage 2*

- Counter: A basic counter design was implemented consisting of 7 D Flip Flops connected in a chain such that the inverted output of a DFF is connected as the CLK of the following DFF in the chain as shown in Appen. H. The negative edge of the input wave (SR Latch output) resets the counter to d'0.

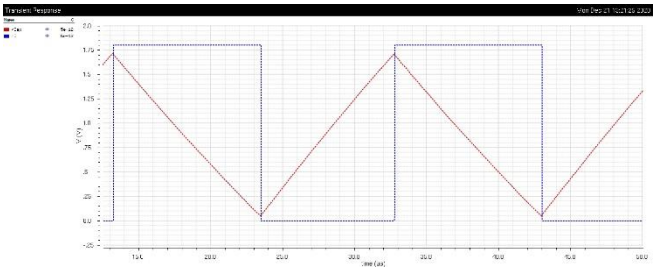
  Selecting the number of bits/DFFs of the counter is a compromise between resolution, area and power. To obtain a high resolution, the gradient of the graph in Fig. 4 should be increased such that for each 0.5 pF increment there is a larger increment in period. This corresponds to minimizing frequency of the sawtooth wave which would reduce the power draw. However, this would require having a larger number of DFFs in the counter to detect the larger range of values increasing the area.

- Latch: A 7 DFF latch was implemented to hold the value of the counter when there is no change in capacitance and hence allow a microprocessor to interface to the system and sample the digital value. This is shown in Appen. I.
- Delay: To latch the output before the digital value is reset, an inverted wave of the SR Latch acts as the store signal. Since the counter reset at the same edge a delay is needed at the input of the counter to prevent timing violations. This delay block was implemented using two inverters in series with long channels.

IV. Simulated Results

A. *Stage 1*

Referring to Fig. 3 when the capacitor is charging the square wave is low. At a voltage of 1.6 V one of the



comparators output goes high and the square wave goes high

Figure 3: Capacitor charge cycle and square wave output from SR Latch

which in turn causes the capacitor to discharge. When the capacitor voltage falls to 0.2 mV the other comparator output goes high causing the square wave to go low which in turn causes the capacitor to charge up.

The relationship between the period of the square wave and the capacitors' capacitance can be seen in Fig. 4.

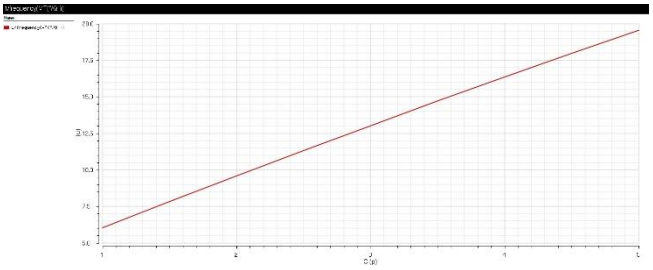


Figure 5: Square wave period vs Capacitance

B. *Stage 2*

A snapshot of the is given in Fig. 5 to give the reader a better intuition of the second stage.

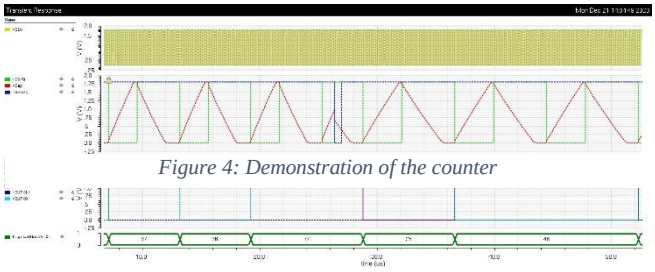


Figure 4: Demonstration of the counter

C. *Overall System*

In an ideal data converter, the output code will change at exactly LSB×(CODEn +0.5) V to give a step curve as shown by the orange graph in Fig. 6. However, in a real data converter (blue graph in Fig. 6) the transition will be shifted forwards or backwards, due to the non-linearity of the system. The differential non-linearity (DNL) and integrated non-linearity (INL) are measures of this linearity and can be calculated at the transition points of the two curves as shown in [3].

The maximum DNL and INL was obtained as 0.0925% at 44pF and 0.01% at 4.54pF. In addition, a step size of 0.02 pF

which is roughly half the minimum detectable capacitance of 0.043 ($\frac{4}{127-34}$).

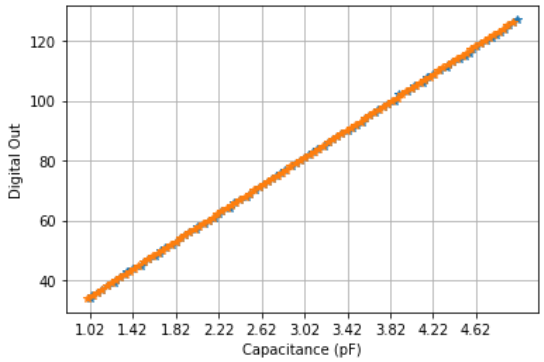
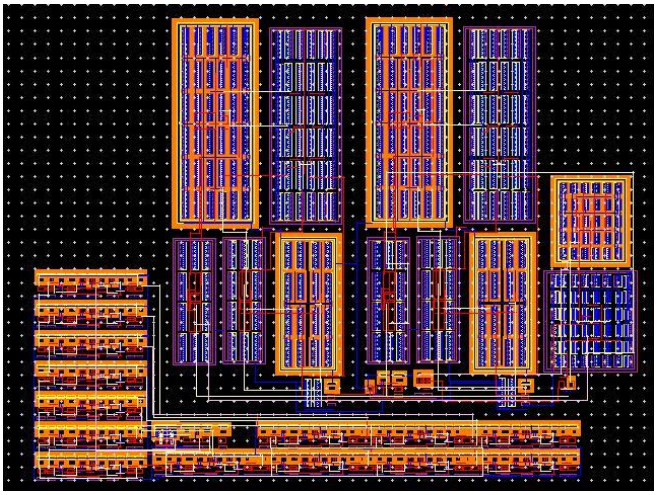


Figure 6: System output step curve

The average power draw of the system was found to be 1.05 mW with a peak power draw of 13.56 mW. As mentioned in the current mirror description, these peaks occur at the square wave edges and can be visualised in Appen. J.

V. Layout

The design was then laid out for fabrication using Cadence Virtuoso's 0.18 µM CMOS process. The overall layout can be seen in Fig. X and a larger annotated version in Appen. K. The critical analog blocks were designed using a common centroid layout and were surrounded by dummy MOS to minimise process effects and hence ensure the various respective MOS were matched. Taking a quadrilateral area around the layout, the total area is 39498µM^2



VI. Future Design Improvements

It is evident that a better current mirror design would improve system performance. For example, a cascaded current mirror can eliminate Vds variation between the source and reference MOS and hence yield better linearity. Moreover, a better topology to switch on and off the switching capacitors would eliminate the current overshoots seen. Furthermore, it would be interesting to investigate the systems output when the rate of charging the capacitor far exceeds the rate of discharging such that the triangular capacitor charging cycle becomes sawtooth. Since, the counter only needs to determine the pulse width of the output from stage 1 it is postulated that this method could still yield a period proportional to frequency and would result to a faster system. In addition, as larger pulse widths per period could be formed more accurate measurements can take place and hence a system with greater accuracy could result. In addition, it can be noticed from Fig. 4 that the digital output may vary by a single decimal value for the same capacitance. This can be attributed to partial samples being taken at a clock edge and this effect can be mitigated by using TDC with a higher resolution such as a Vernier TDC.

VII. Conclusion

This paper explored and analysed the design of a simple capacitance to digital converter which acts as the front-end interface to a touchscreen. Moreover, the system was laid out for fabrication such that simulations are expected to match real world performance. The design exceeded target specifications with future work expected to further improve the overall system performance.

VIII. References

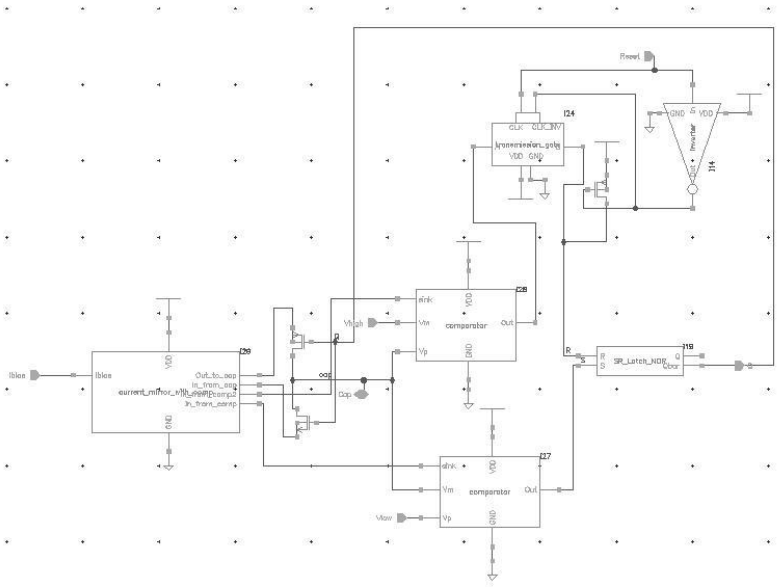
[1] C. Priyanka and P. Latha, "Design and implementation of time to digital converters," 2015 International Conference on Innovations in Information, Embedded and Communication Systems (ICIIECS), pp. 1-4, 2015.

[3] "“http://www.maximintegrated.com/app-notes/index.mvp/id/283”.".

[2] J. Baker, CMOS Circuit Design, Layout, and Simulation, Hoboken, New Jersey: John Wiley & Sons, Inc, 2010.

APPENDIX

A



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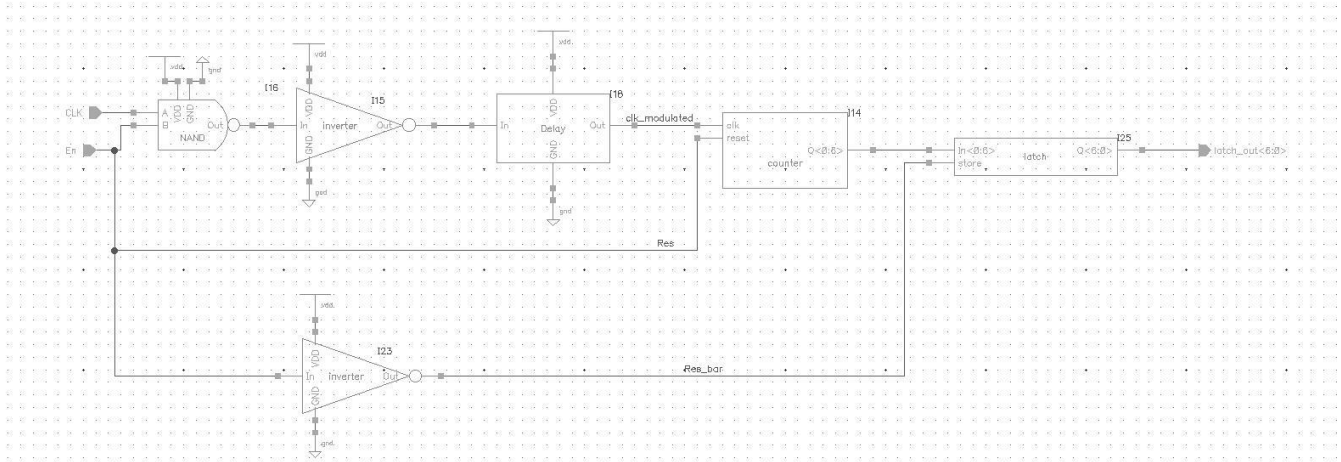

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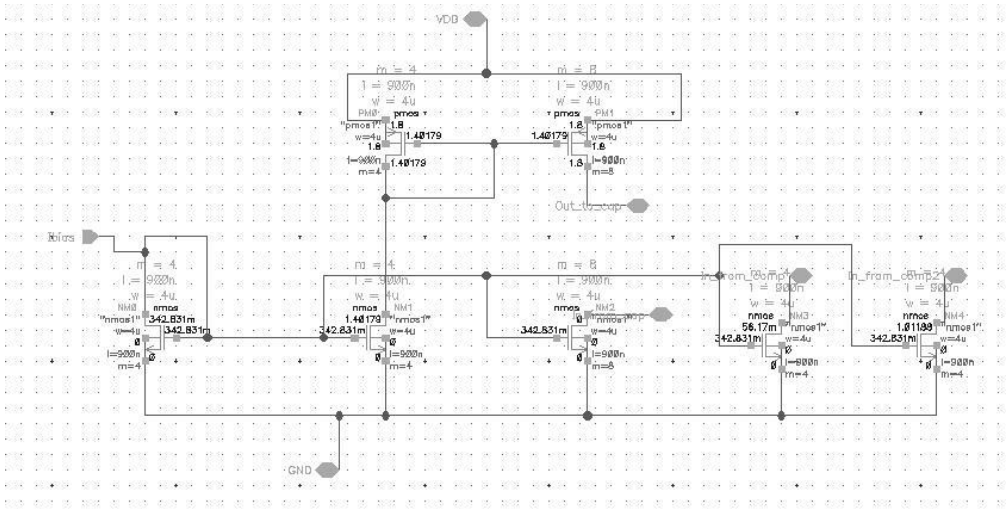

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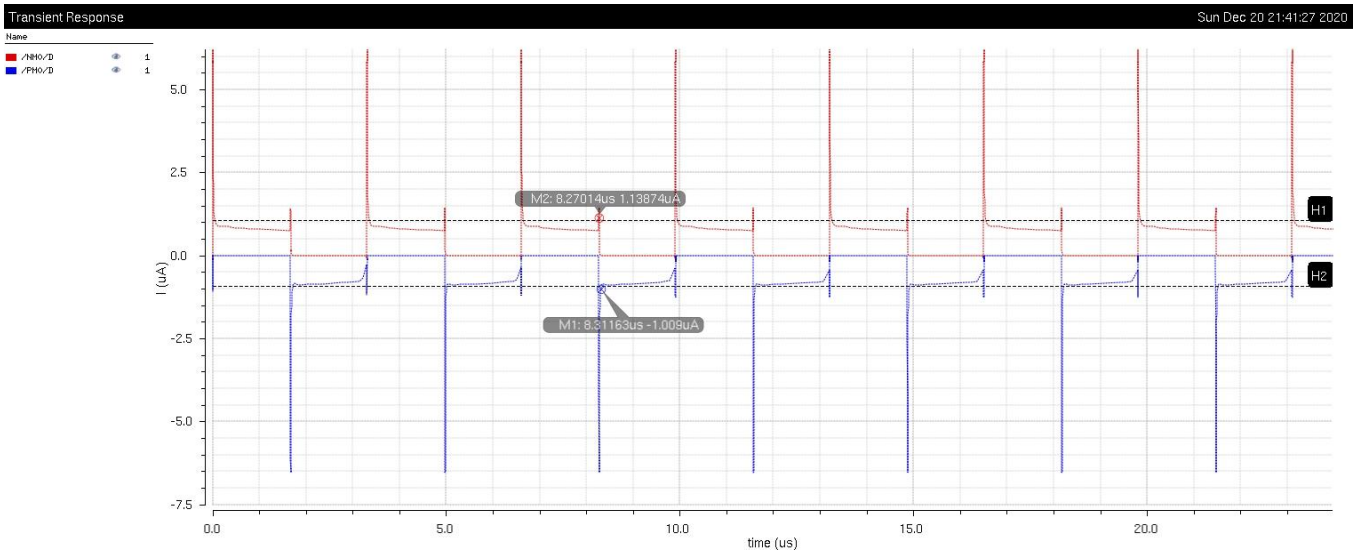
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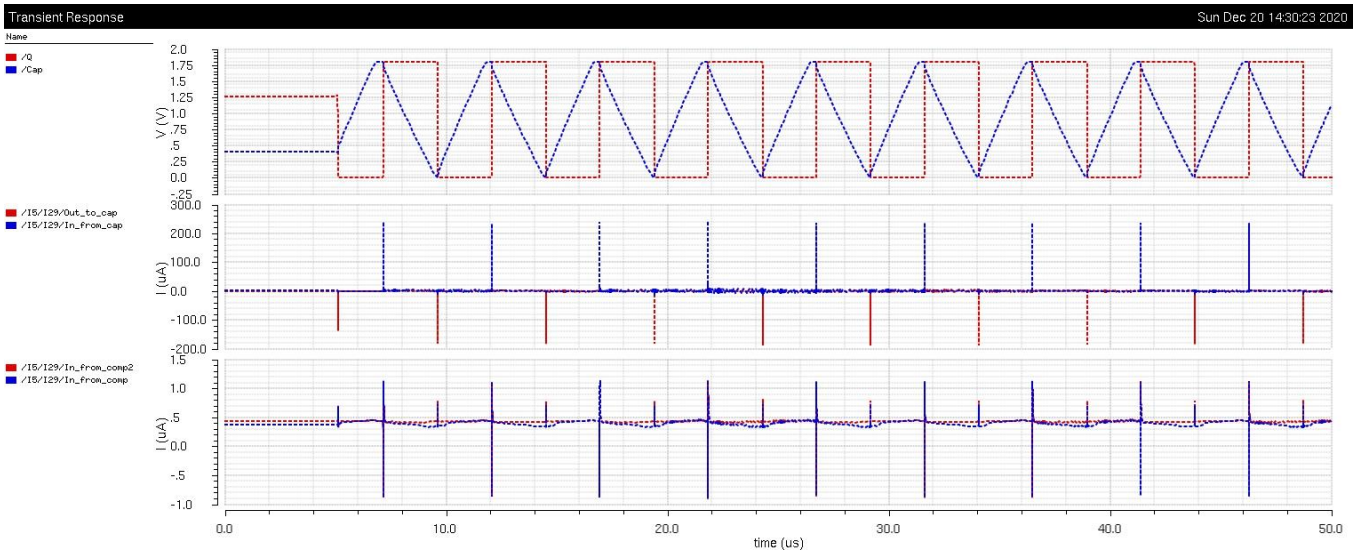
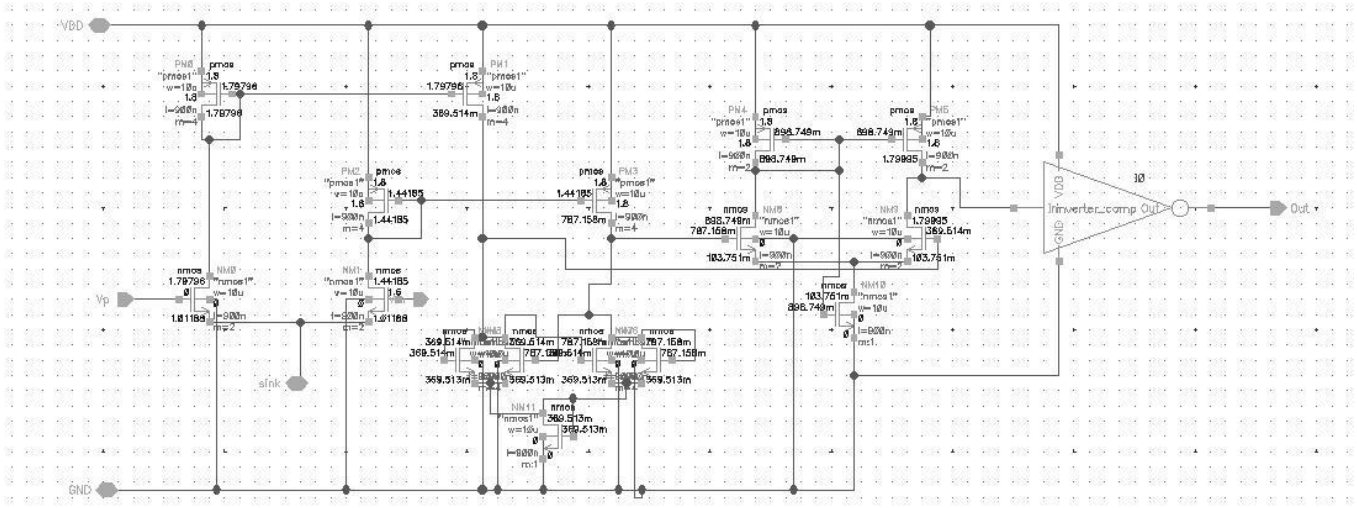
Name
/NM0/D
/PM0/D
M2: 8.27014us 1.13874uA
M1: 8.3116 3us -1.009uA
H1
H2
I (uA)
time (us)

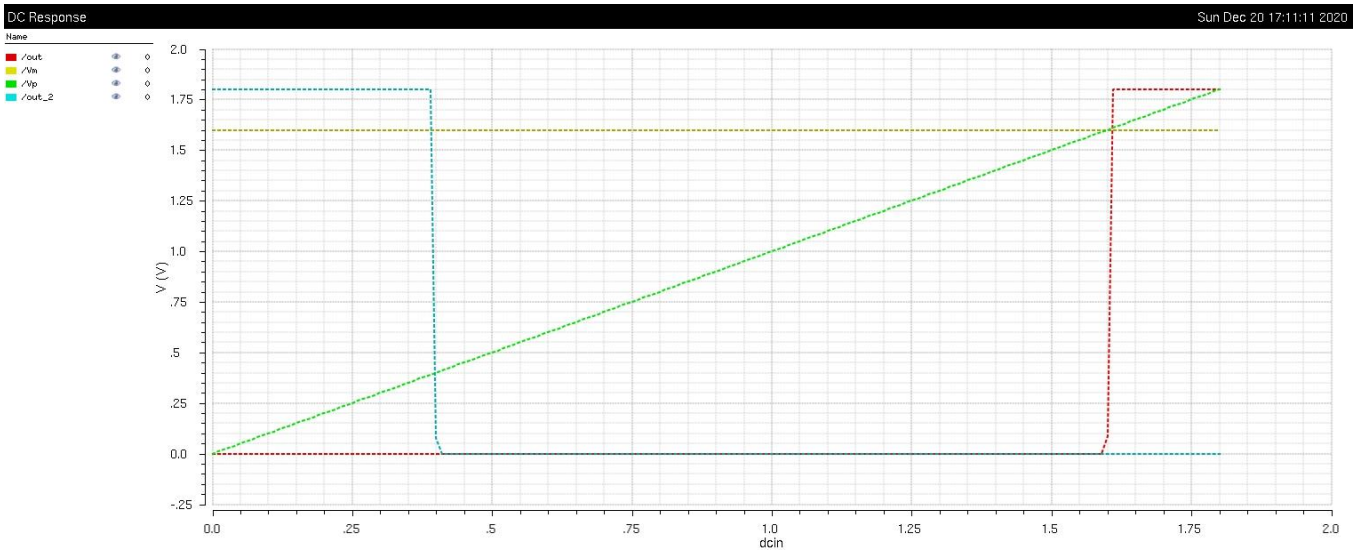
E


Transient Response
Sun Dec 20 14:30:23 2020
Name
/Q
/Cap
/I5/I29/Out_to_cap
/I5/I29/In_from_cap
/I5/I29/In_from_comp2
/I5/I29/In_from_comp
V (V)
I (uA)
time (us)

F


VBD
Vp
sink
GND
Inverter_comp
Out

G


DC Response
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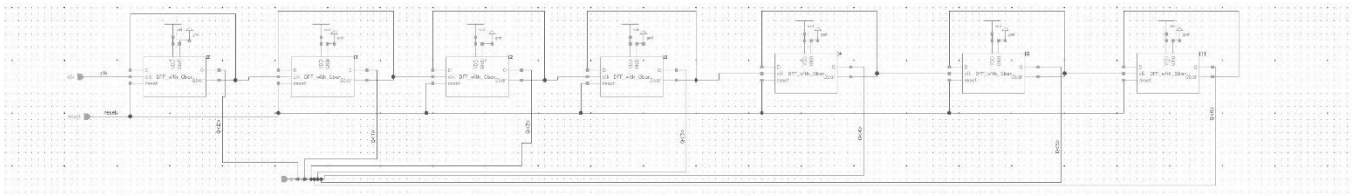
Name
/out
/Vin
/Vip
/out_2
V (V)
dcin

H



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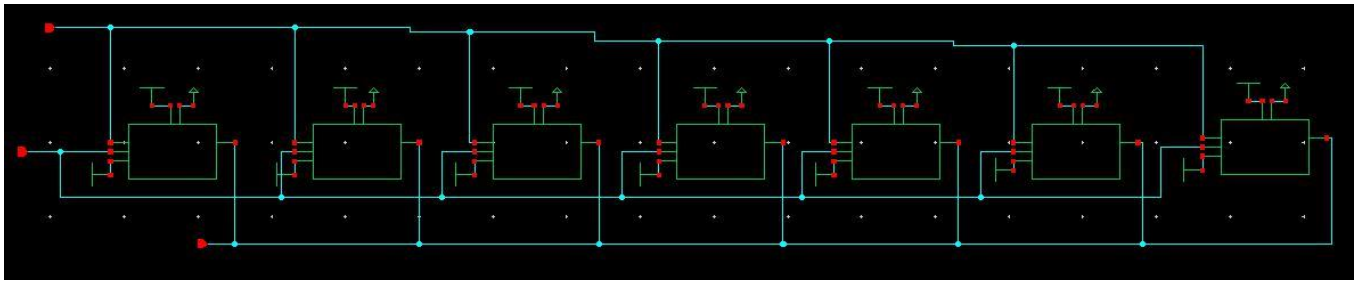
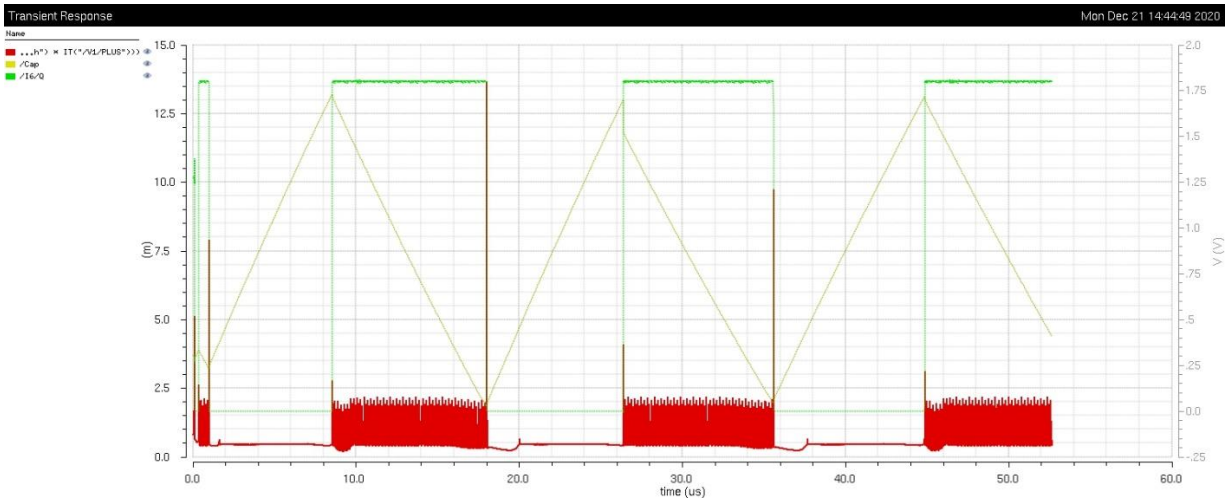


J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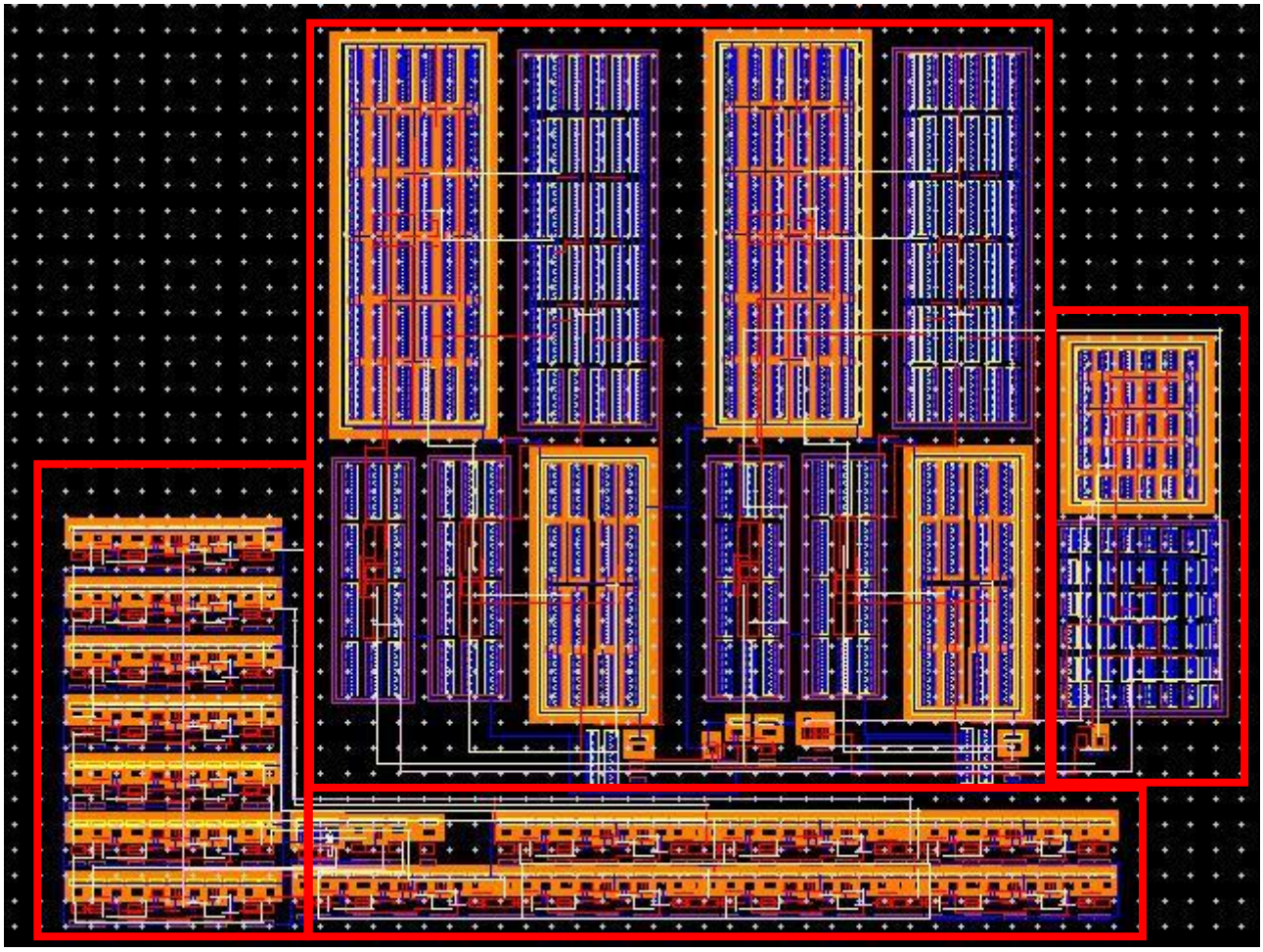
Name
/Cap
/I6/0
time (us)

K

Comparators



Current mirror

Counter

Latch