**BYOC course**

**Homework exercise #3 – GPR**

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A screenshot of a computer

Description automatically generated

In the screenshot, we observe the register values through TB\_rd\_data1 and TB\_rd\_data2 across cycles 46 to 49:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Cycle** | **Register 1** | **Register 1 Value** | **Register 2** | **Register 2 Value** |
| 46 | 12 | 0x0000cccc | 28 | 0xcccc0000 |
| 47 | 13 | 0x0000dddd | 29 | 0xdddd0000 |
| 48 | 14 | 0x0000eeee | 30 | 0xeeee0000 |
| 49 | 15 | 0x0000ffff | 31 | 0xffff0000 |

From cycles 50 to 55, the pattern changes slightly. With the TB\_Reg\_Write signal being active (1) until cycle 54, the following observations can be made:

* The value written to a register on cycle 50 is read on cycle 51 (Register 1).
* The value written on cycle 51 is read on cycle 55 (Register 2).
* The value written on cycle 52 is read on cycle 54 (Register 3).

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Cycle** | **Reg 1** | **Reg 1 Value** | **Reg 2** | **Reg 2 Value** | **Reg Write** | **Reg Write Value** |
| 50 | 1 | 0x00001111 | 2 | 0x00002222 | 1 | 0xabcd0001 |
| 51 | 2 | 0x00002222 | 1 | 0xabcd0001 | 2 | 0xabcd0002 |
| 52 | 3 | 0x00003333 | 4 | 0x00004444 | 3 | 0xabcd0003 |
| 53 | 4 | 0x00004444 | 4 | 0x00004444 | 4 | 0xabcd0004 |
| 54 | 3 | 0xabcd0003 | 4 | 0x00004444 | 5 | 0xabcd0005 |
| 55 | 2 | 0xabcd0002 | 17 | 0x11110000 | - | - |