Enhancing DC Microgrids Stability by Integrating DAB Converters with Consensus Algorithms for Bus Voltage Drop Mitigation

Advisor : Dr Pham Minh Duc

Student : Tran Nguyen Dang Khoa

DC microgrid

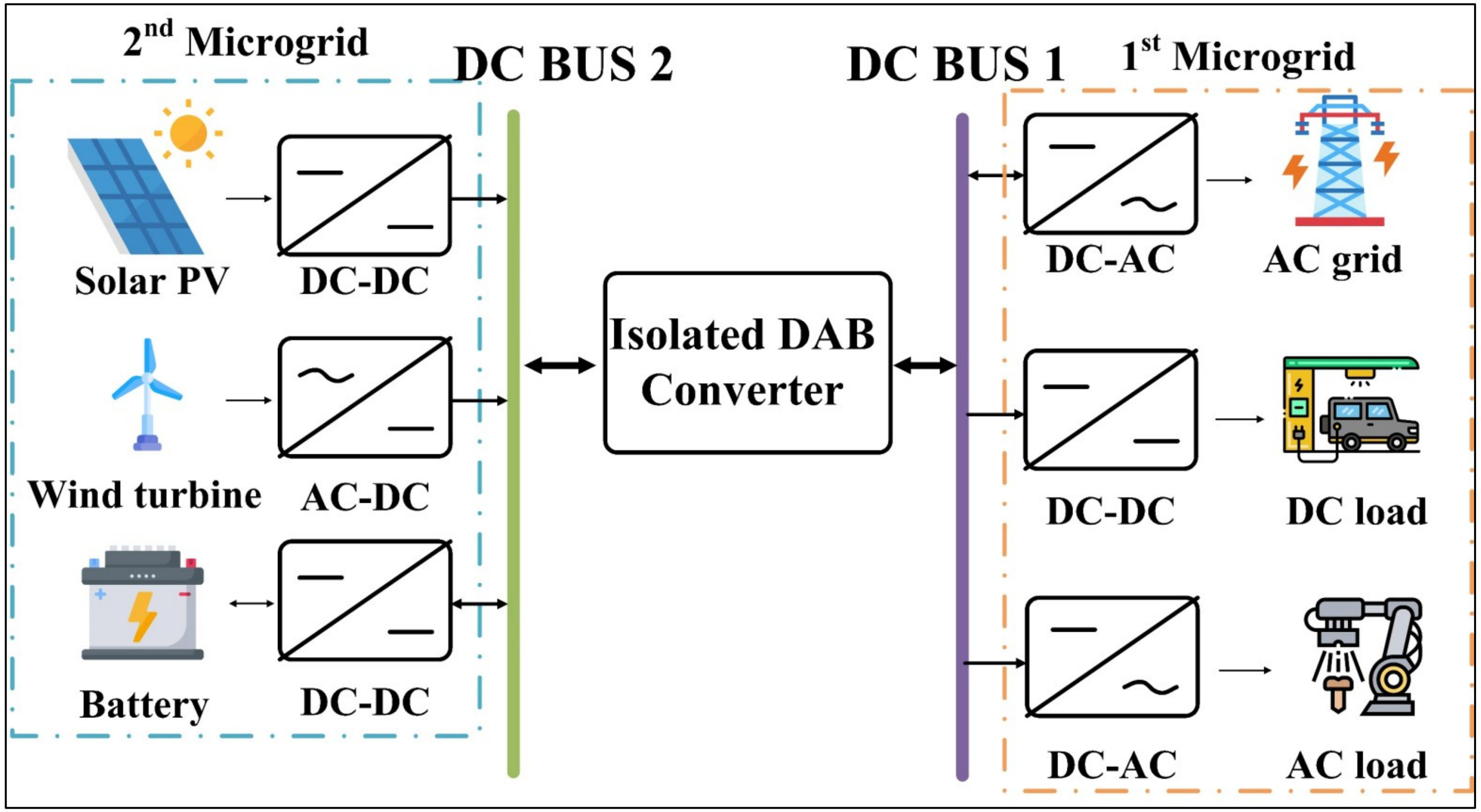


Fig. 1. Generalized structure of the DC microgrid system with isolated interlinking converter

Fig. 1 shows the generalized structure of the DC microgrid system with an isolated interlinking converter. In practice, the DC microgrid system may consist of two microgrids: one serving residential areas and another industrial one. Challenges such as high-demand spots, voltage drops, and fluctuating consumption patterns are common in this system. A major issue is managing voltage drops during overloads

DAB Converter

Phase shifts in Dual Active Bridge (DAB) control regulate power transfer and maintain efficiency, with single phase shift control simplifying operation while ensuring zero voltage switching. This study specifically explores phase shift modulation for simplicity and effective power transfer.

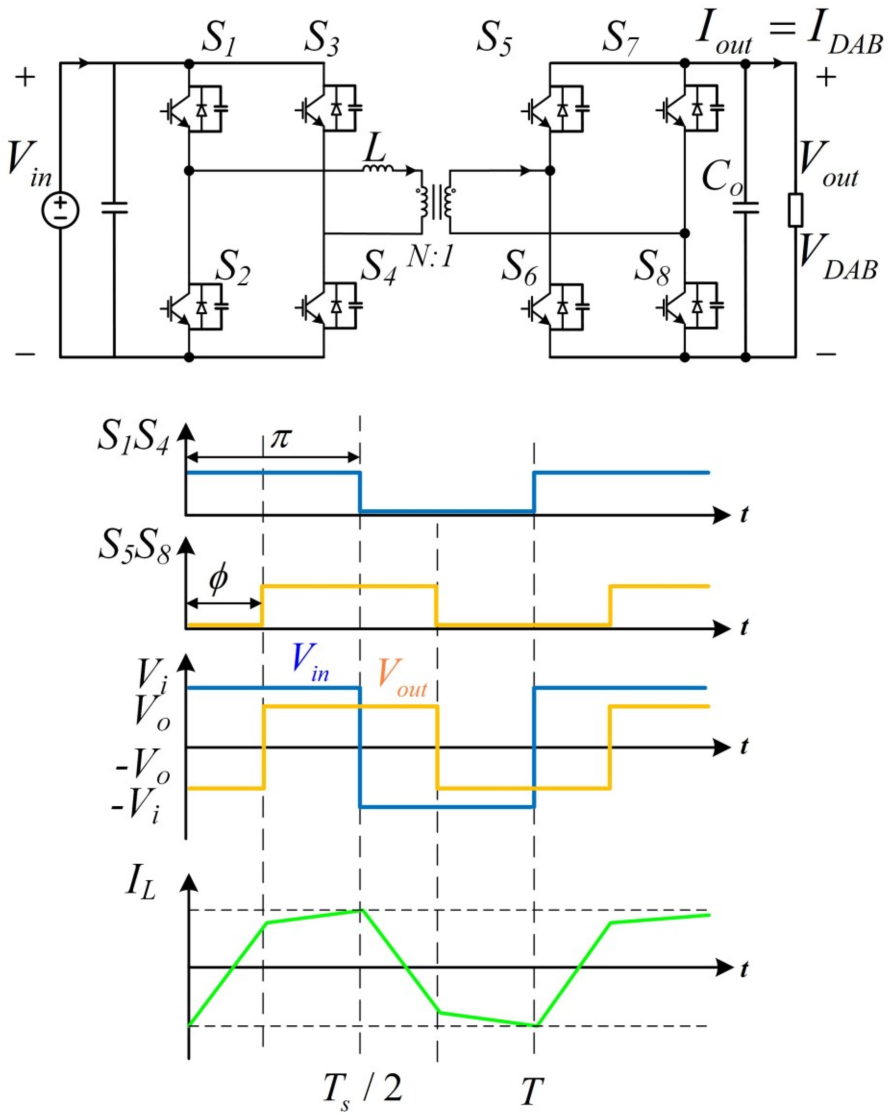


Fig. 2. DAB converter schematic and the operating state.

Example response for Consensus algorithm

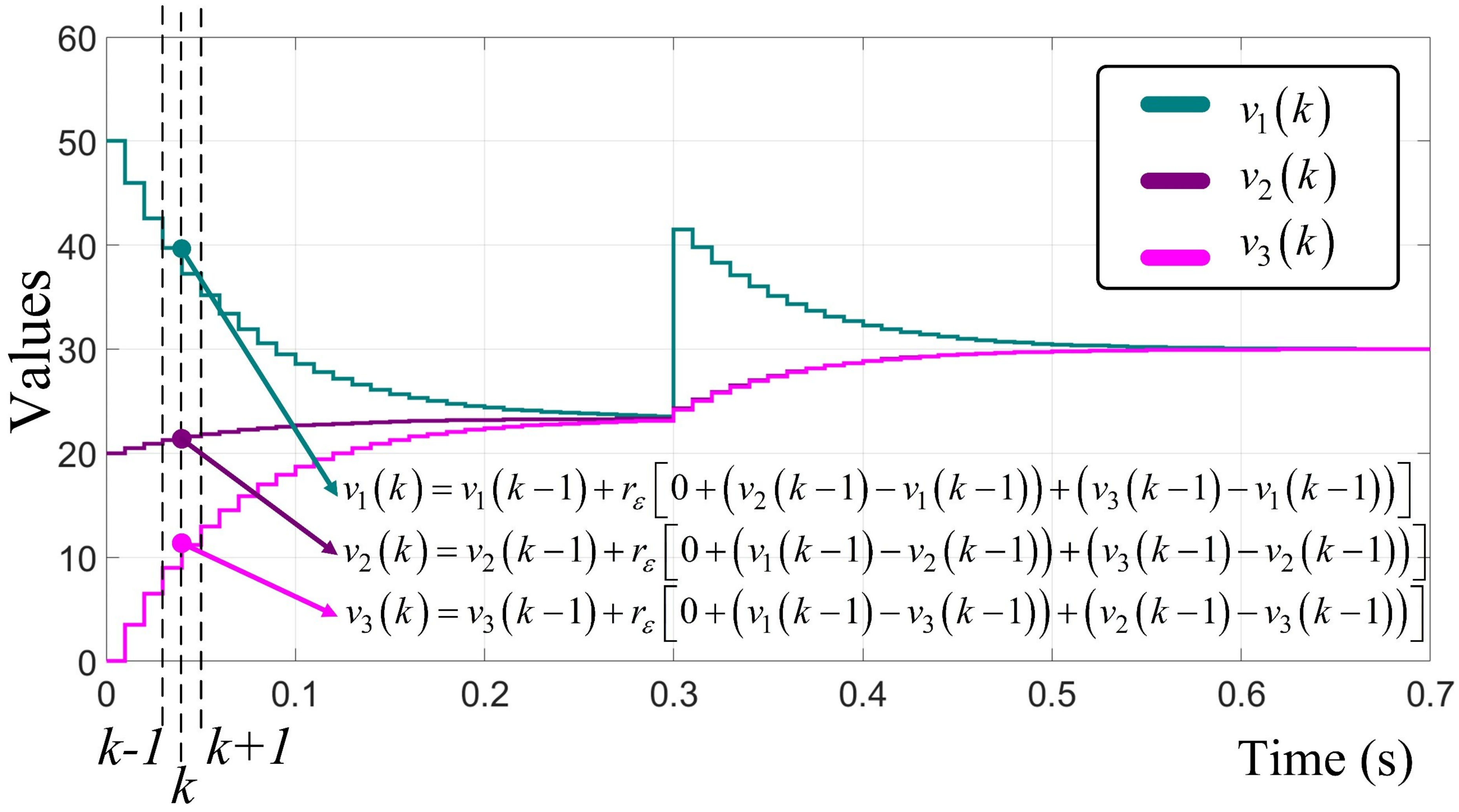


Fig. 3. Output values with discrete consensus algorithm.

Integration of Droop Control, DAB converter and Consensus

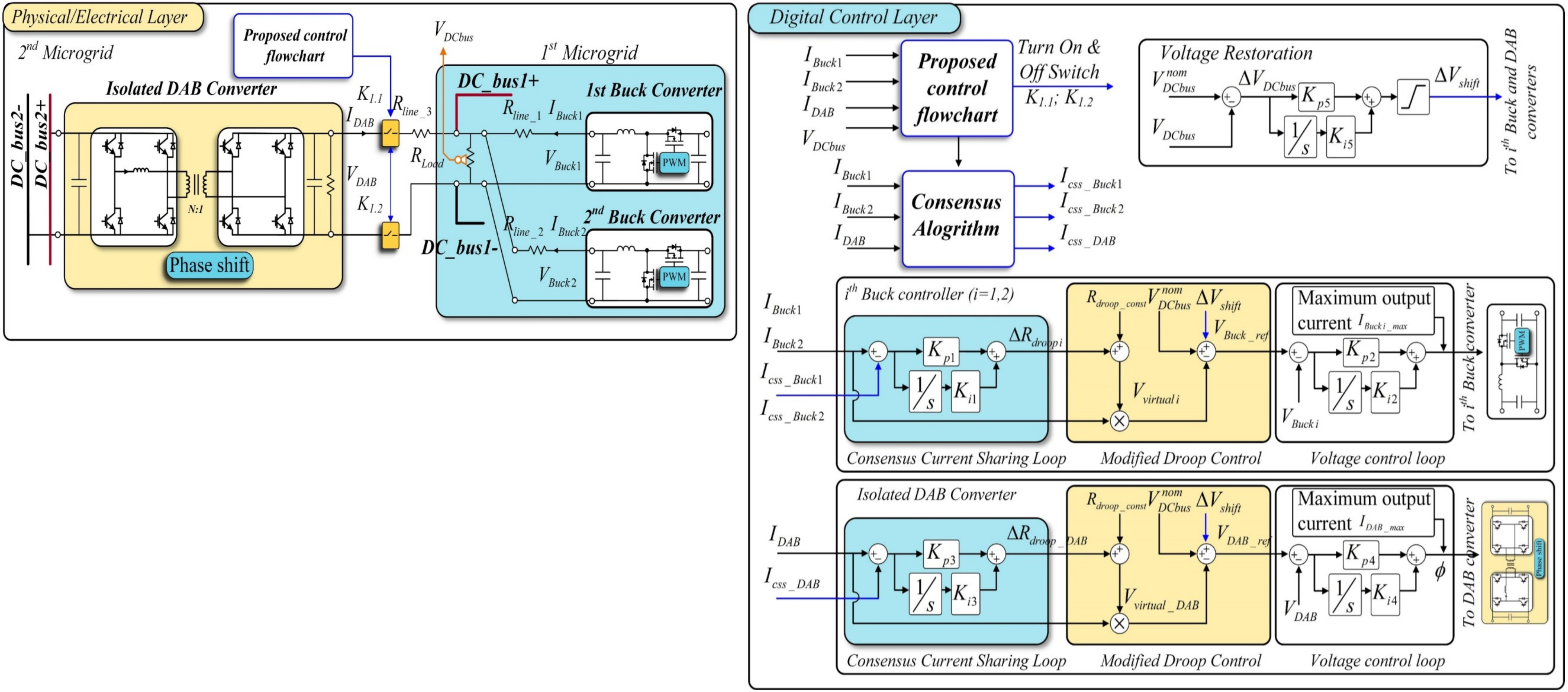
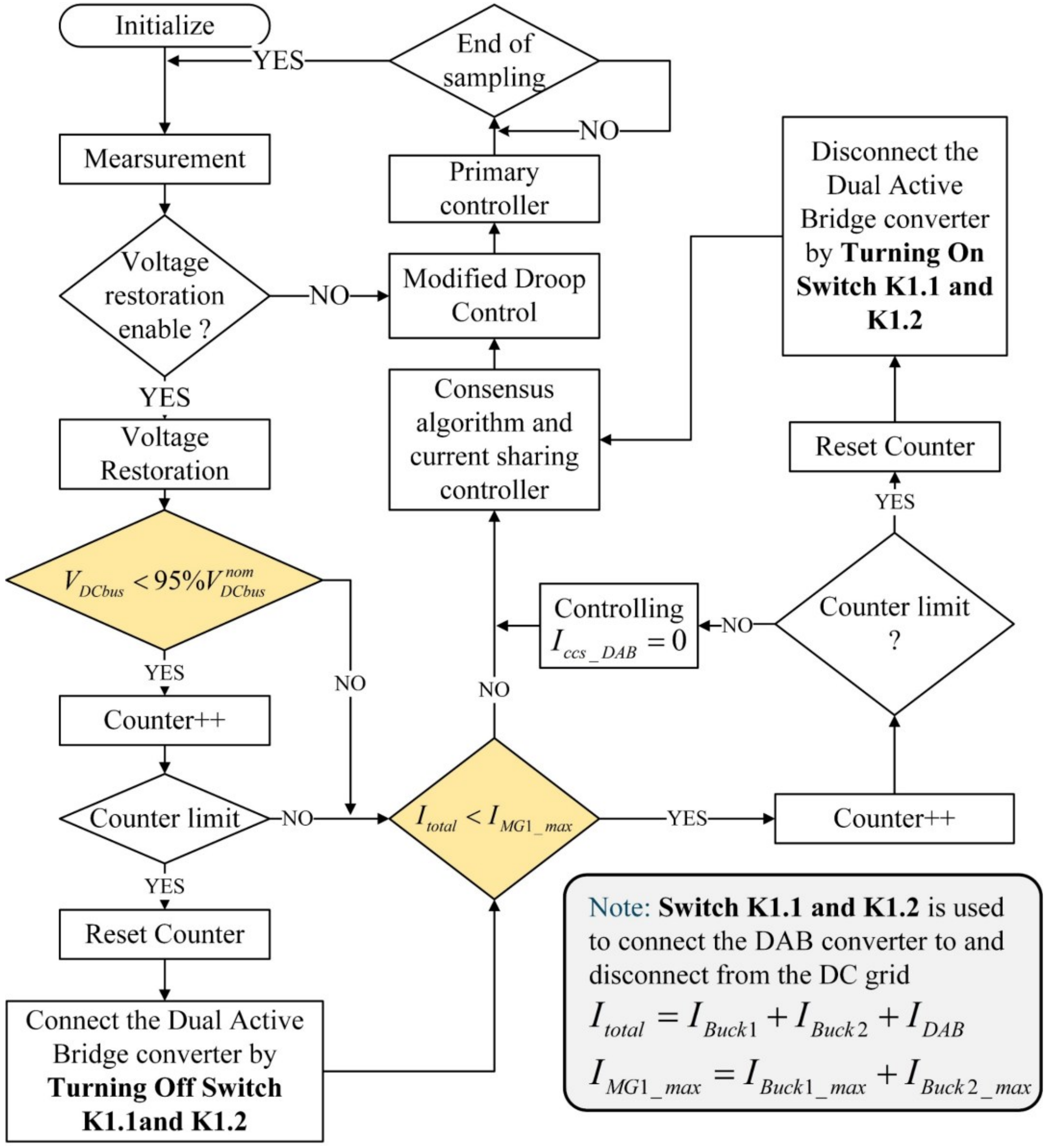


Fig. 4. Block diagram of combined DAB converter and Consensus Algorithm.

FLOW CHART



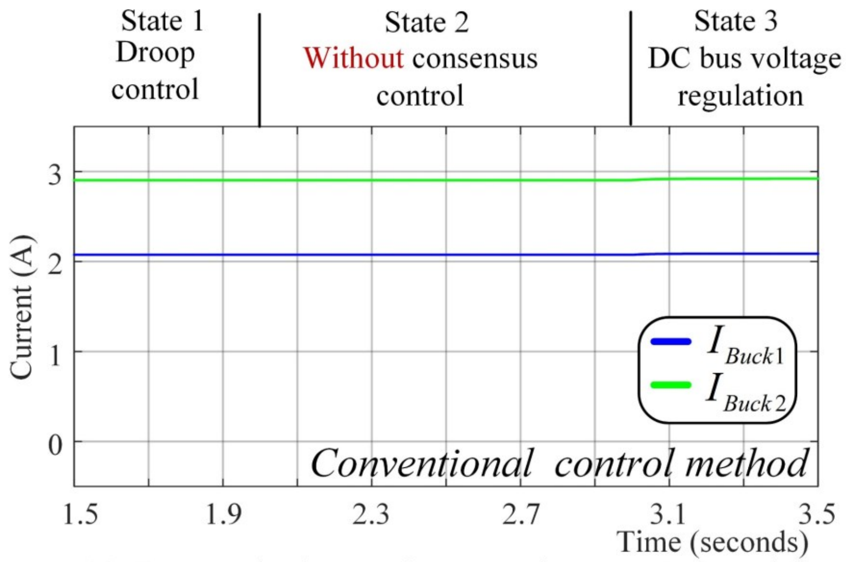
There are two conditions for turning on and off K1.1 and K1.2 along with DAB operation !

Figure 5. The proposed control flowchart.

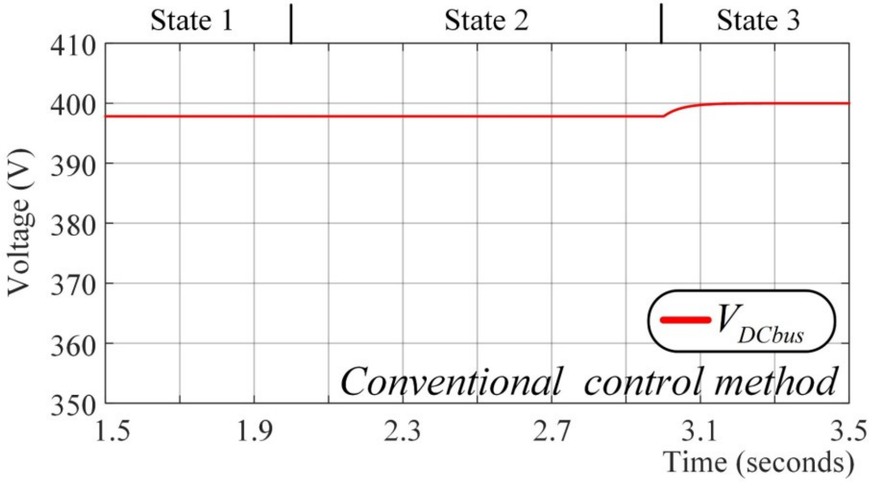
SIMULATION STATES

State 1 ($t < 2s$): The conventional droop control scheme is adopted. State 2 ($2s \le t < 3s$): The proposed consensus current control scheme with adjustable resistance is enabled. State 3 ($3s \le t < 4s$): The proposed voltage restoration is enabled. State 4 ($4s \le t < 5s$): load 2 is connected to the system which reaches the maximum output current of buck converters and reduces the DC bus voltage quality. State 5 ($5s \le t < 6s$): The additional load 3 is connected to the system to reduce the DC bus voltage smaller than 95% of the DC bus nominal voltage. The proposed control flowchart activates the DAB connection to support the 1st microgrid. State 6 ($6s \le t < 7s$): load 2 is disconnected from the system to evaluate the disconnection process of the DAB converter with the proposed control flowchart.

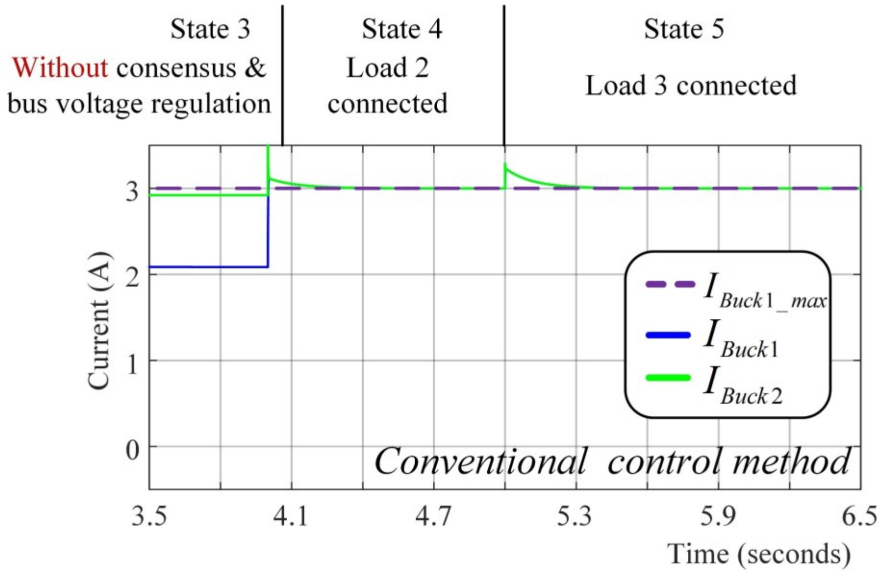
Conventional response in 5 States



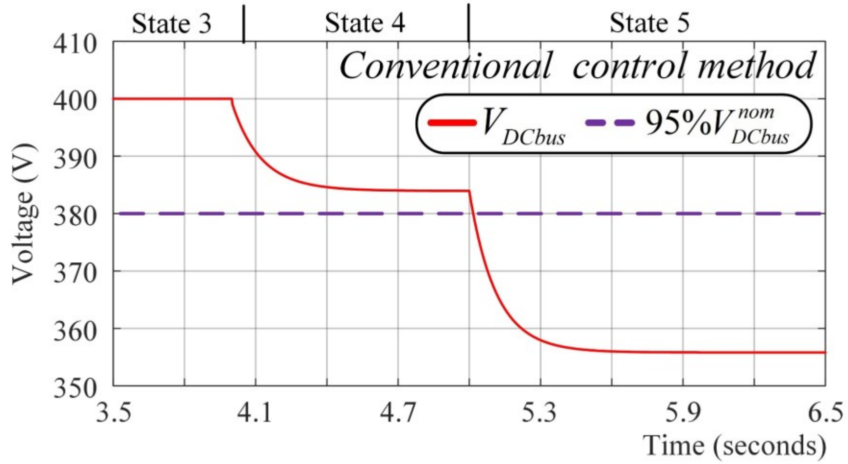
(a) Current sharing performance in states 1, 2, and 3



(b) DC bus voltage in states 1, 2, and 3



(a) Current sharing performance in states 3, 4, and 5

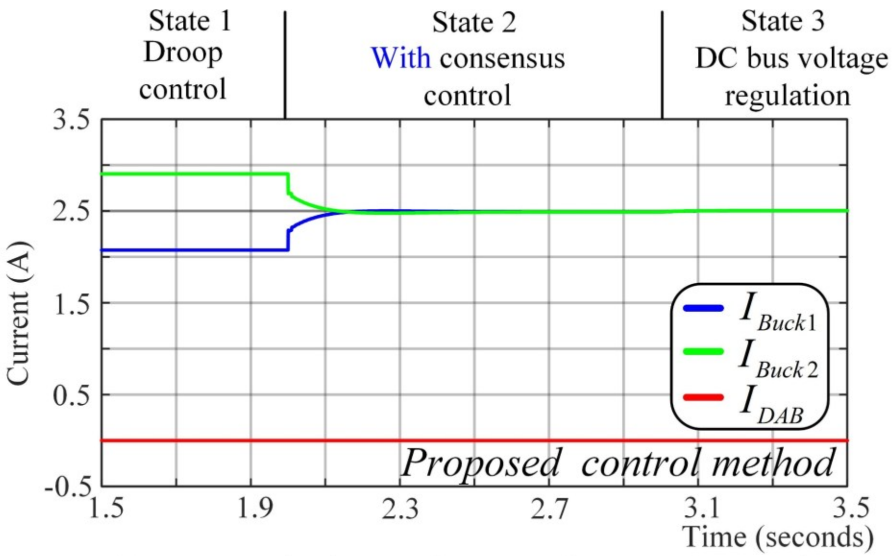


(b) DC bus voltage in states 3, 4, and 5

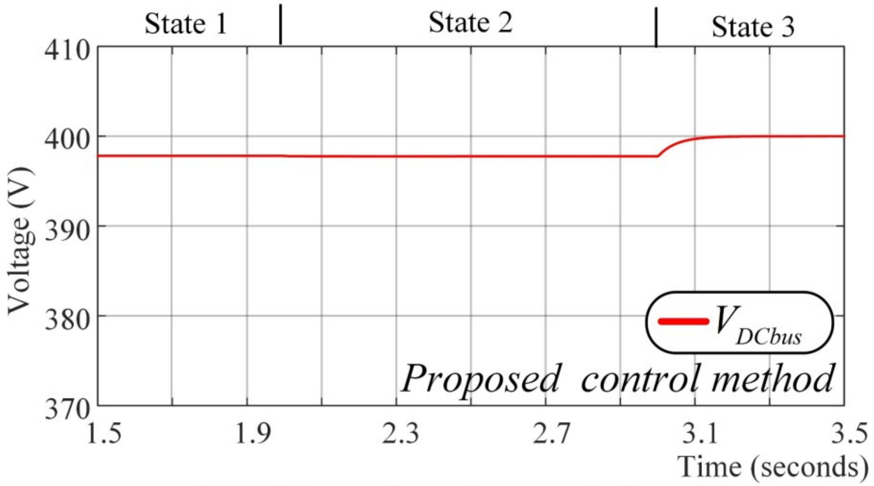
Conventional (1 - 2 – 3)

Conventional (3 - 4 – 5)

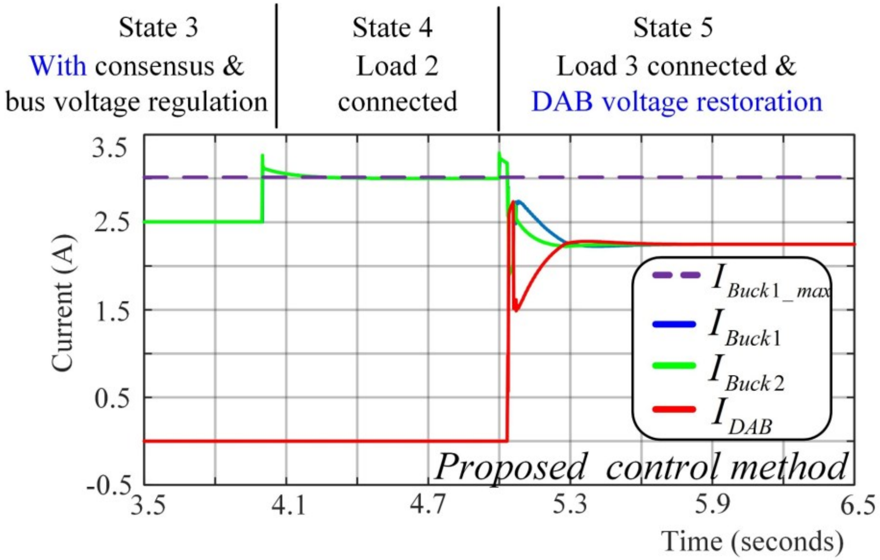
Proposed response in 5 States



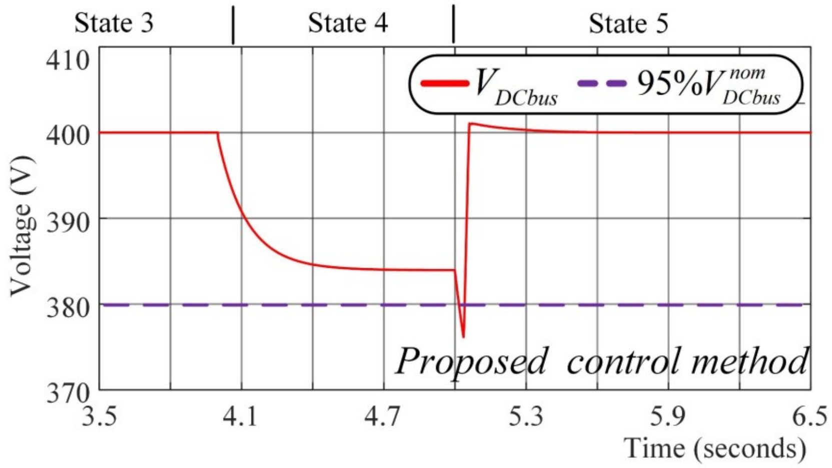
(a) Current sharing performance in states 1, 2, and 3



(b) DC bus voltage in states 1, 2, and 3



(a) Current sharing performance in states 3, 4, and 5

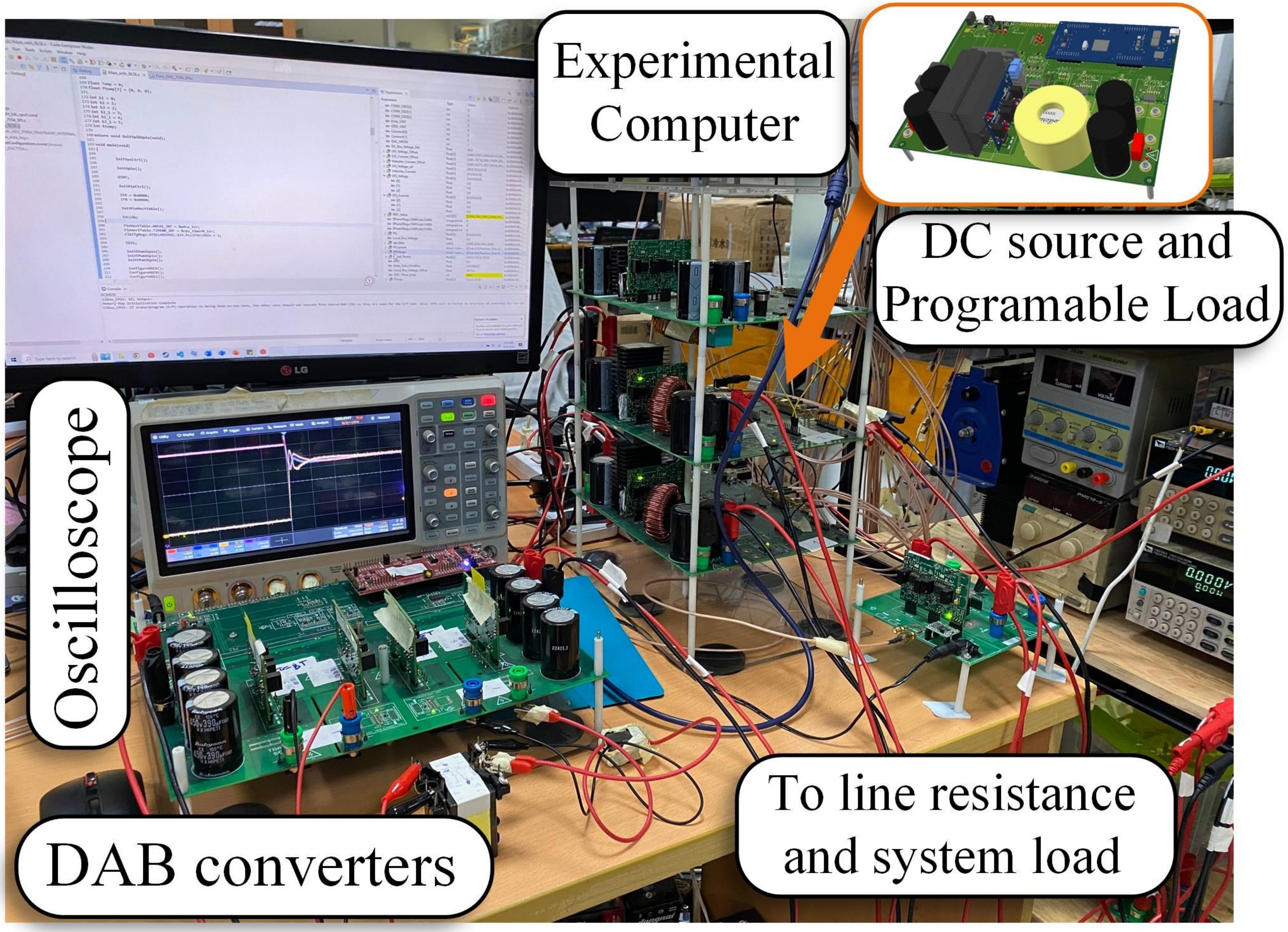


(b) DC bus voltage in states 3, 4, and 5

Proposed (1 - 2 – 3)

Proposed (3 - 4 – 5)

EXPERIMENT SET UP



EXPERIMENT STATES

State 1 – Unequal current sharing: Buck converters share currents unevenly, DC bus voltage drops below nominal.

State 2 – Current balance: Consensus controller compensates mismatches → balanced current sharing.

State 3 – Bus voltage regulation: Consensus + voltage control restores DC bus voltage to nominal while keeping current balance.

State 4 – Load 2 connected: Both Buck converters hit maximum current limit, DC bus voltage drops to ~45.8 V (≈95% of nominal).

State 5 – DAB support: When $V_{dc} < 95\% V_{nom}$, DAB is activated, transfers power from MG2→MG1, shares current with Bucks, avoiding overload.

State 6 – Smooth DAB disconnection: When $V_{dc} \geq 95\% V_{nom}$ & total current < limit, DAB current is reduced to zero, disconnected; Bucks smoothly take over with minimal voltage fluctuation.

EXPERIMENT RESPONSE

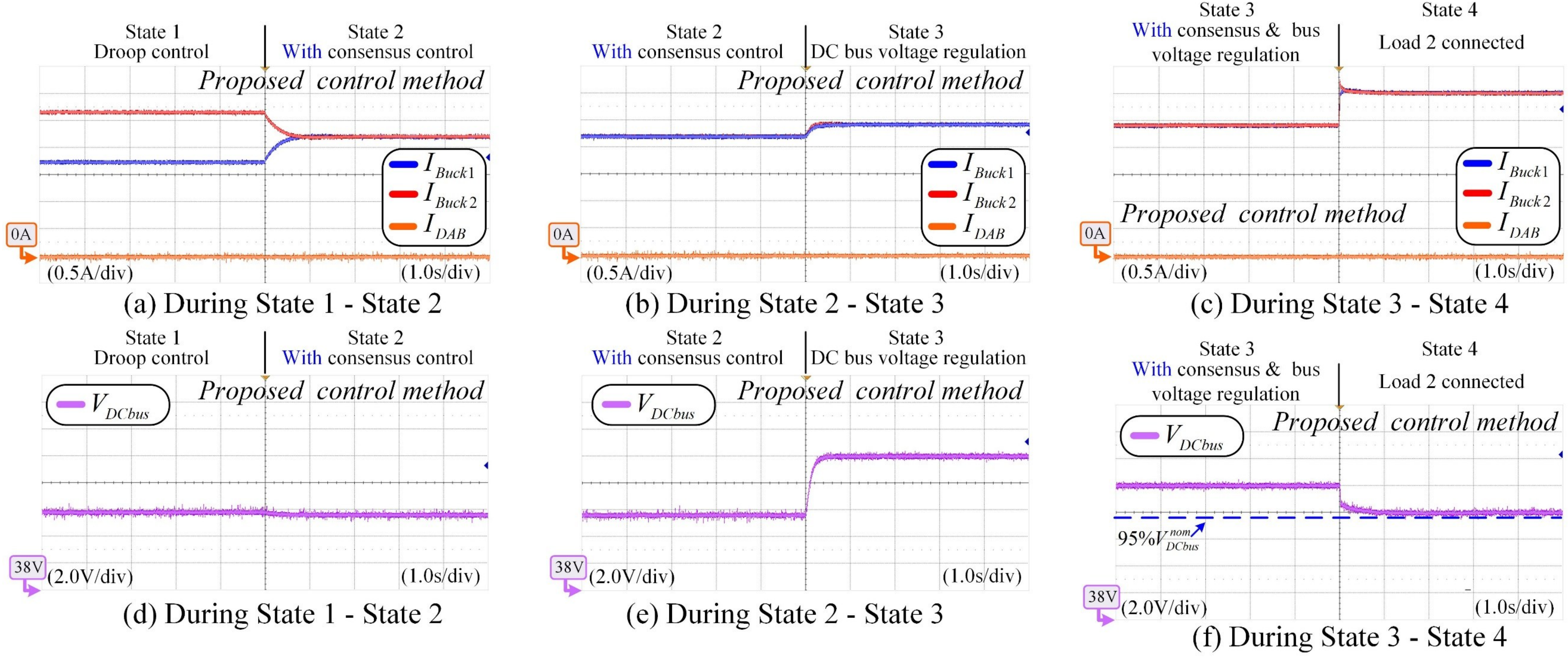


Fig. 12. The experimental results of current and bus voltage during states 1, 2, 3, and 4.

EXPERIMENT RESPONSE

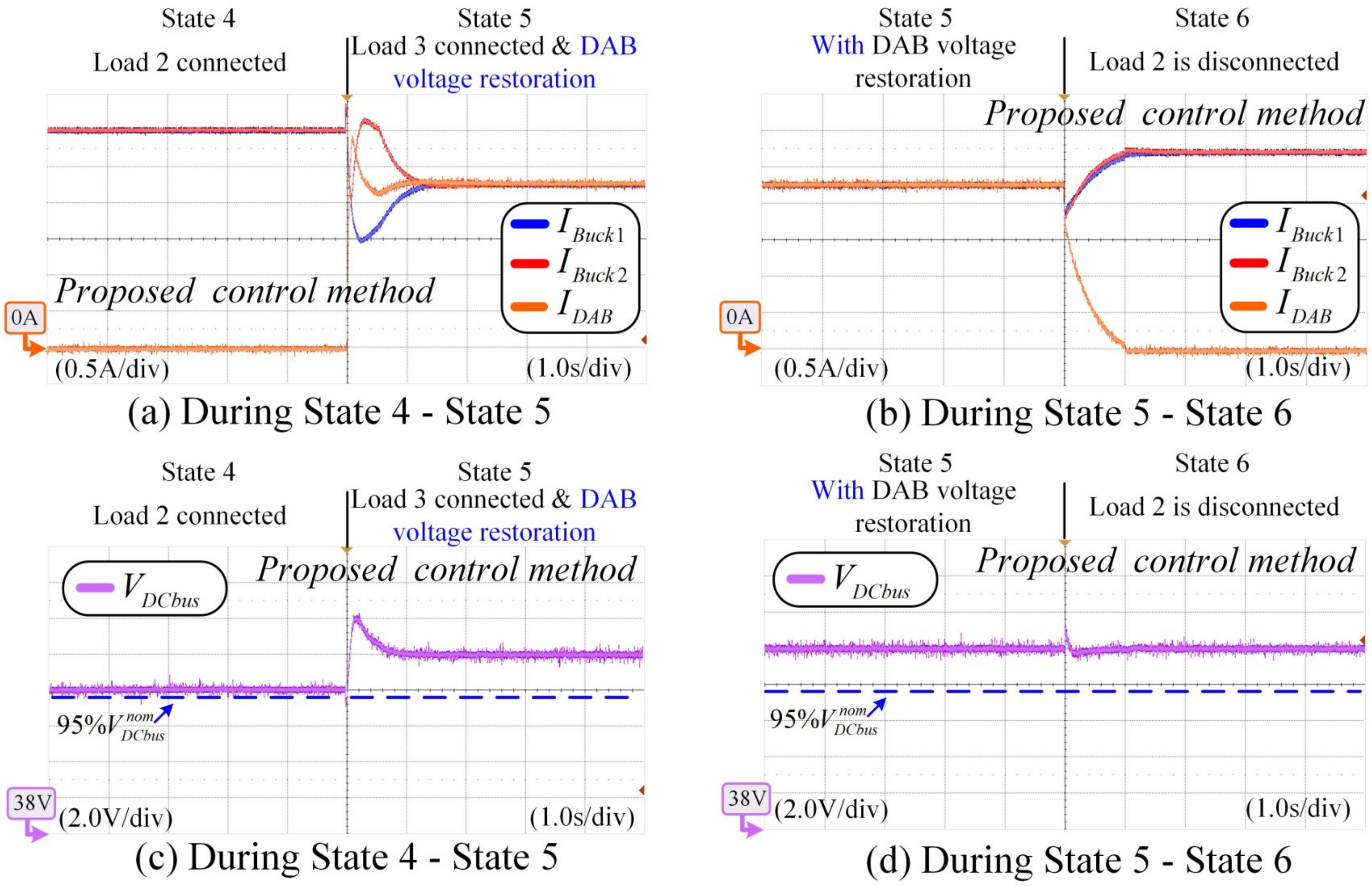


Fig. 13. The experimental results of current and bus voltage during states 4, 5, and 6.