CSCE 616 – Hardware Design Verification

Lab – 10 Regression

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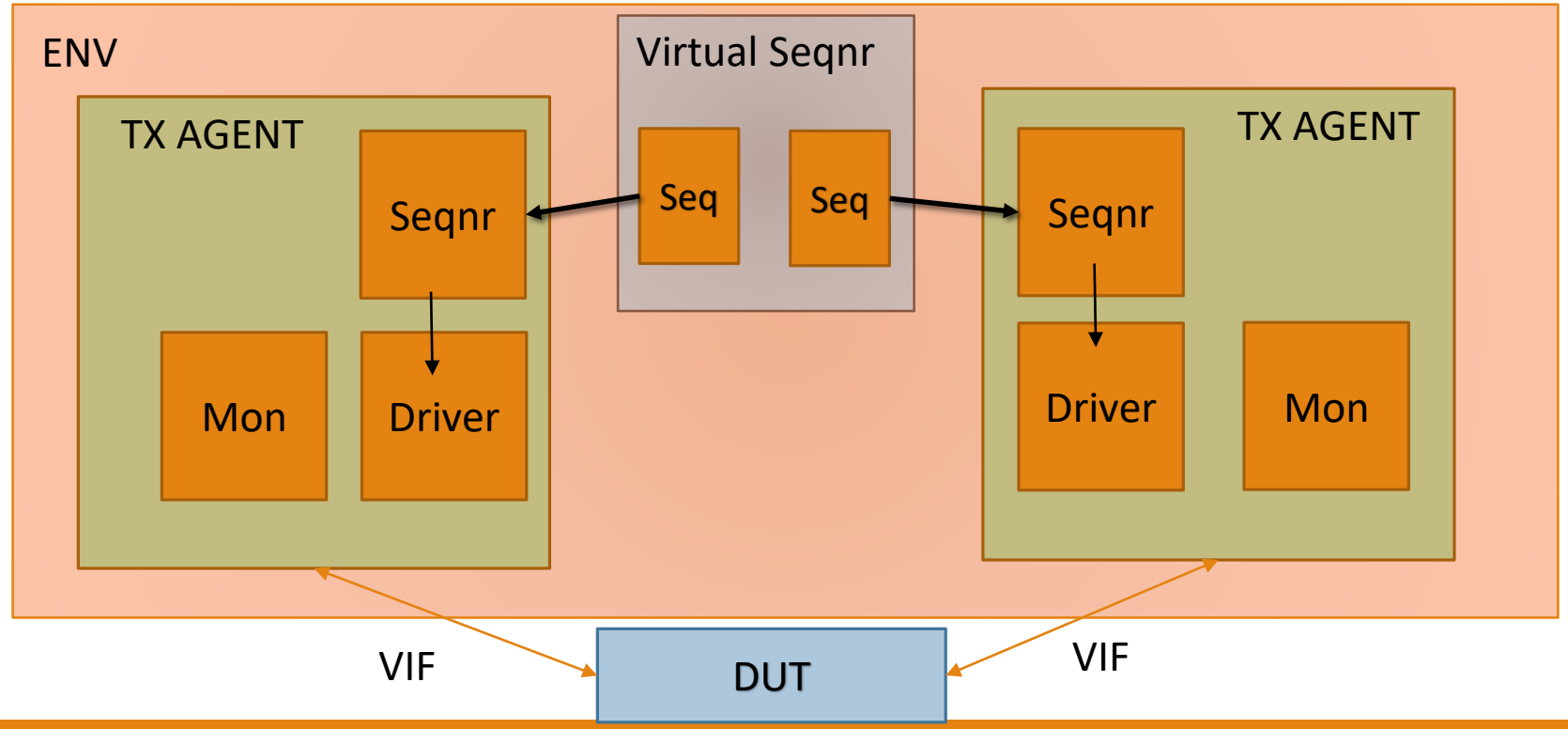
Objective – Write Tests and Run Regression

- Virtual Sequencer
- Virtual Sequence
- UVM Test
- Regression

Virtual Sequencer

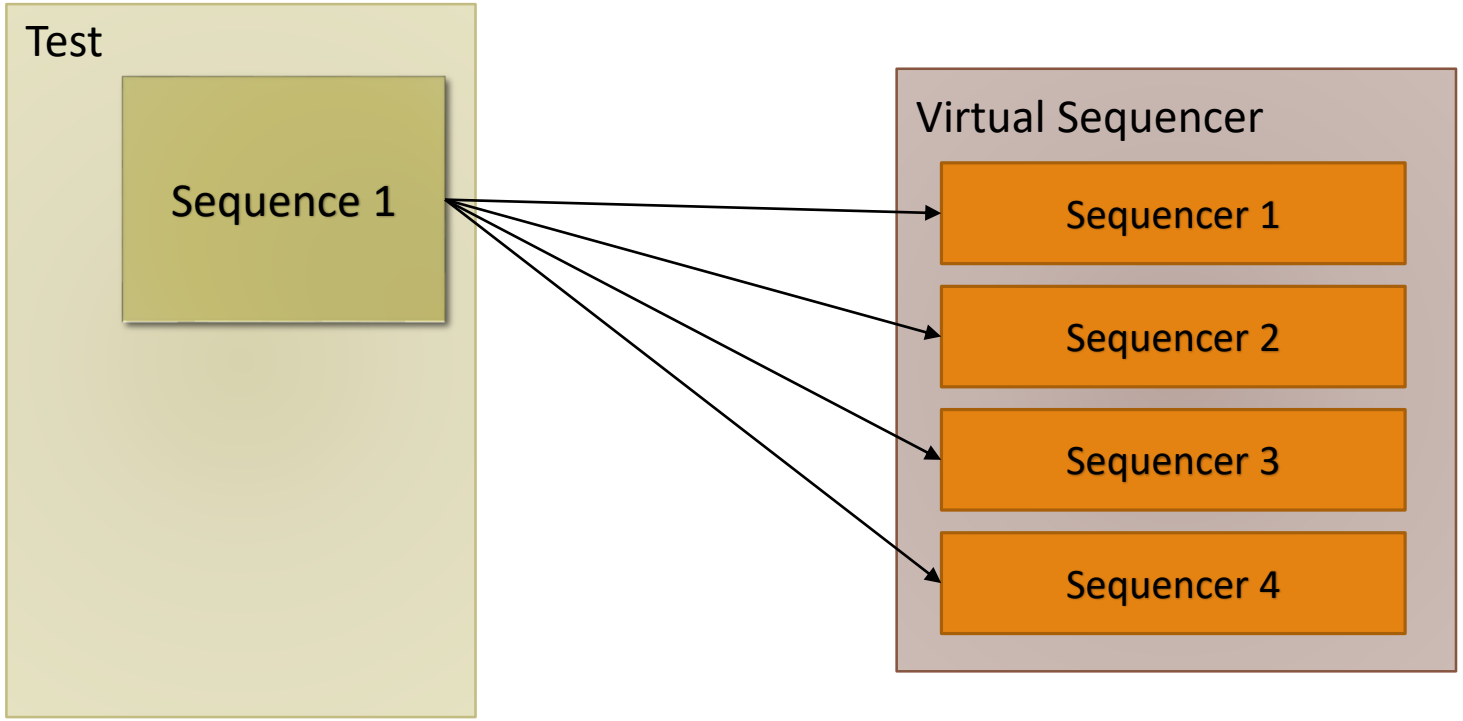
A virtual sequencer is a component in the UVM TB architecture which controls the flow of stimulus or sequence items of more than one sequencer.



Virtual Sequence

A virtual sequence is a container to start multiple sequences on different sequencers.

The virtual sequencer handles the real sequencers in the Agent.



UVM Test

Test class contains the environment, configuration properties, class overrides etc.

A sequence/sequences are created and started in the test.

The UVM TB is activated when run_test() method is called from top.

There are two ways to start any sequence in test:

1. uvm_config_db#(uvm_object_wrapper)::set(this, “*.vsequencer.run_phase", "default_sequence", <v_sequence>::type_id::get());

2. <v_sequence>.start(env.<vsequencer>)

Thank you