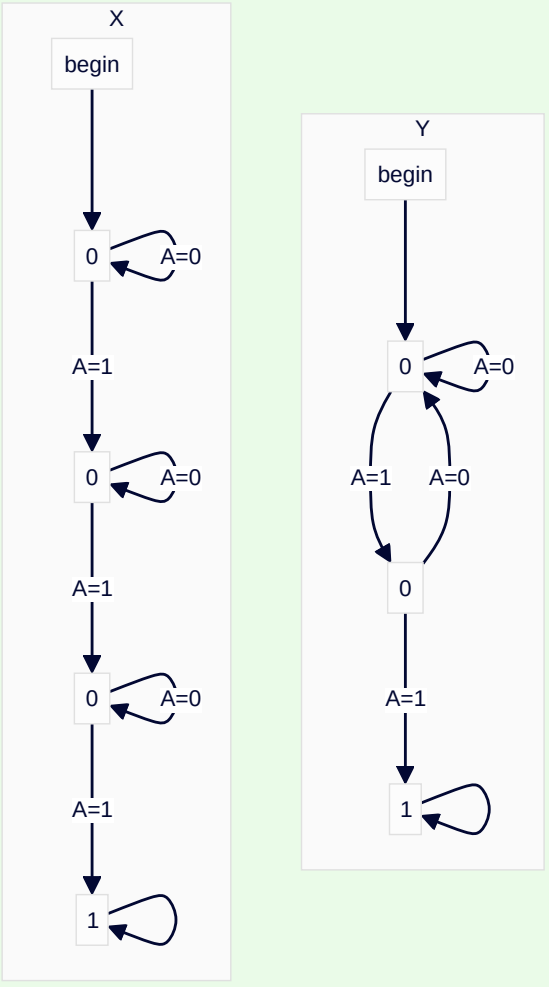
1

Draw the state diagram for the following problem: There is one input A and two outputs X and Y. X becomes 1 if A has been 1 for at least three cycles altogether (not necessarily consecutively). Y becomes 1 if A has been 1 for at least two consecutive cycles.

✓ Answer

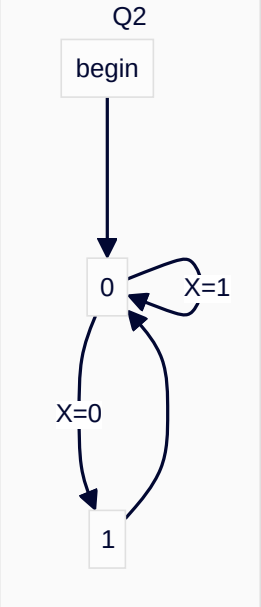


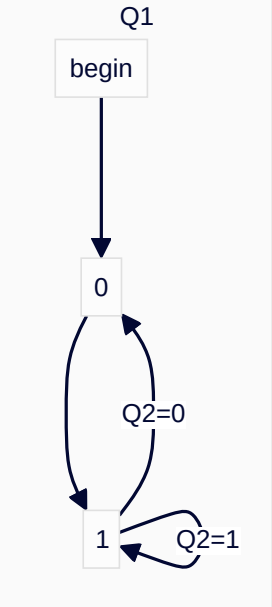
2

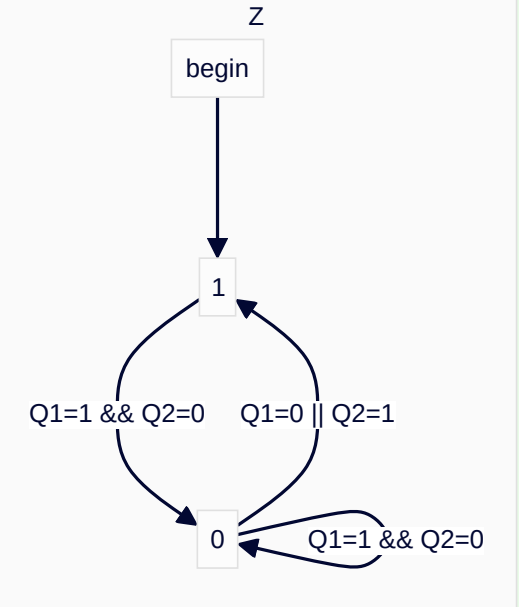
Given the following excitation and output equations, write the state transition and output tables. X is the input, Z is the output. Draw the sequential logic circuit. Please note that state memory is using positive-edge triggered D flip-flops.

$$D1 = Q1' + Q1 \cdot Q2$$
$$D2 = Q2' \cdot X'$$
$$Z = Q1' + Q2$$

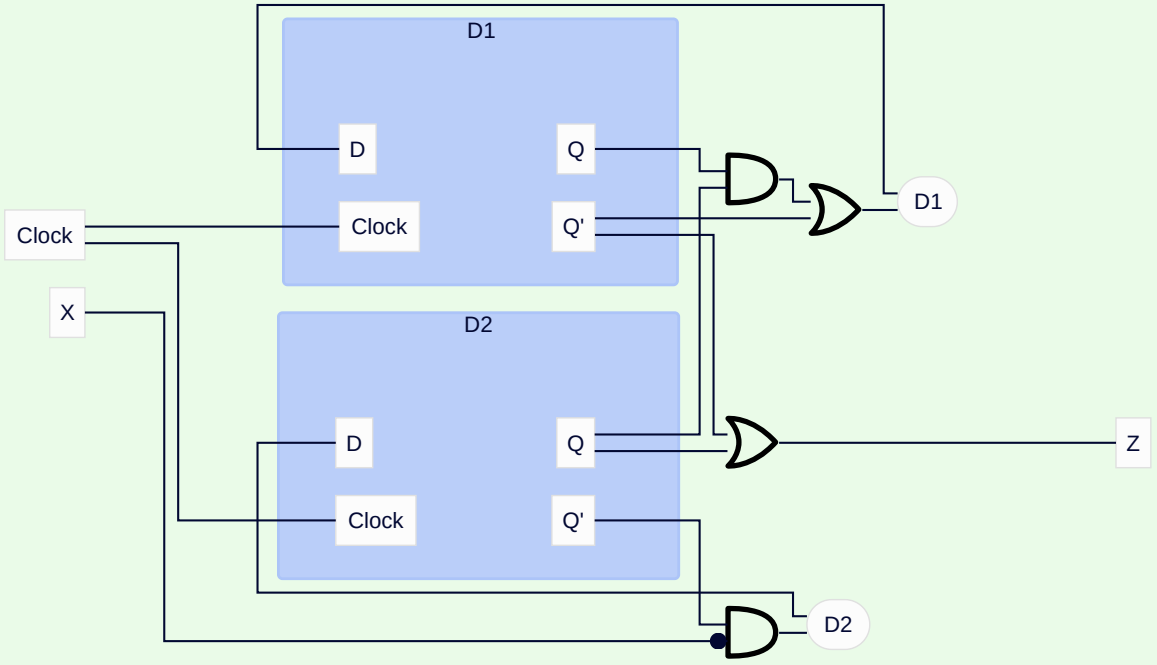
✓ Answer







Q1	Q2	X	D1	D2	Z
0	0	0	1	1	1
0	0	1	1	0	1
0	1	0	1	0	1
0	1	1	1	0	1
1	0	0	0	1	0
1	0	1	0	0	0
1	1	0	1	0	1
1	1	1	1	0	1



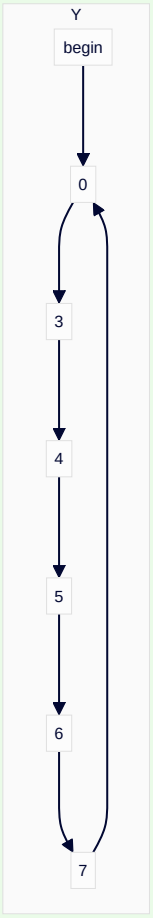
3

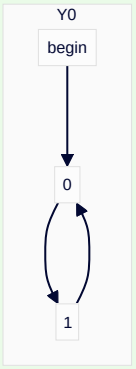
Design a 3-bit binary counter with counting sequence 0, 3, 4, 5, 6, 7, 0, 3, ...
The counter will increment at each clock tick. Use binary state assignments. Use D flip-flops, and combinational logic gates.

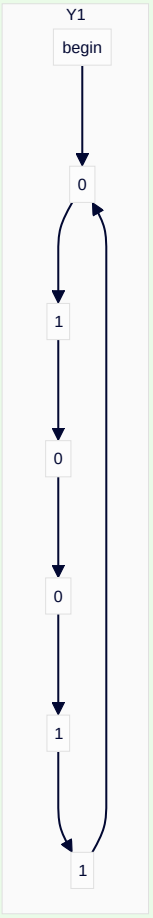
Follow the steps below:

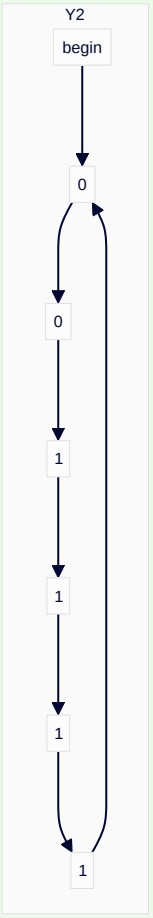
1. Draw a state diagram.
2. Write a state transition table.
3. Write state transition, and excitation equations.
4. Draw the circuit.

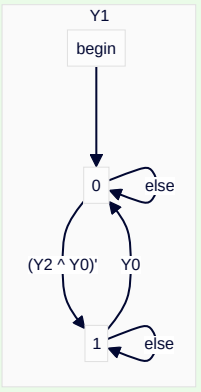
✓ **Answer**

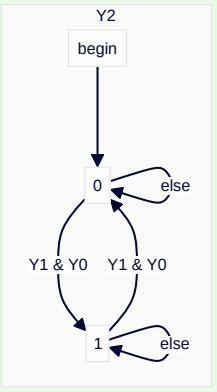






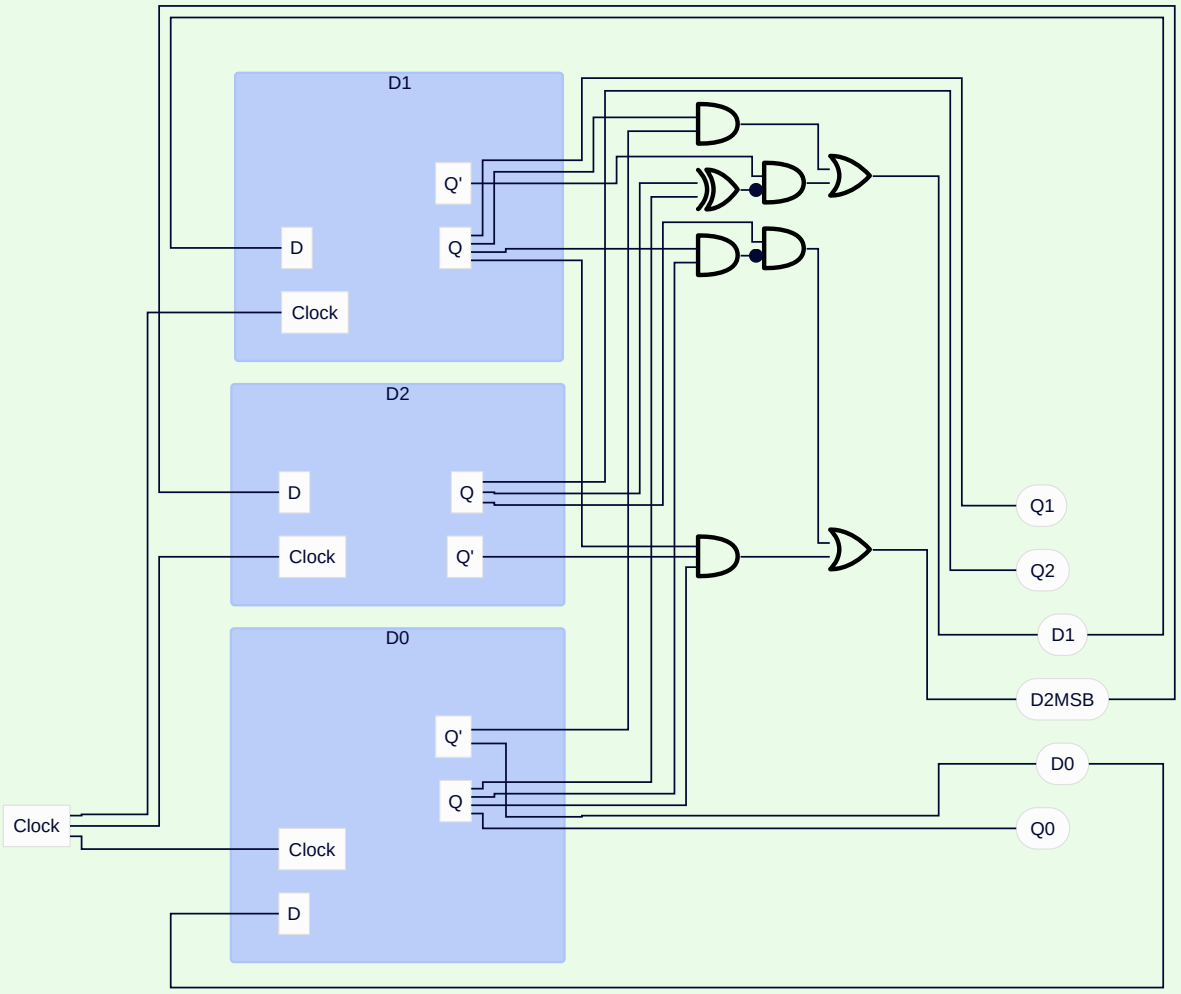






Y2	Y1	Y0	Y2*	Y1*	Y0*
0	0	0	0	1	1
0	1	1	1	0	0
1	0	0	1	0	1
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	0	0	0

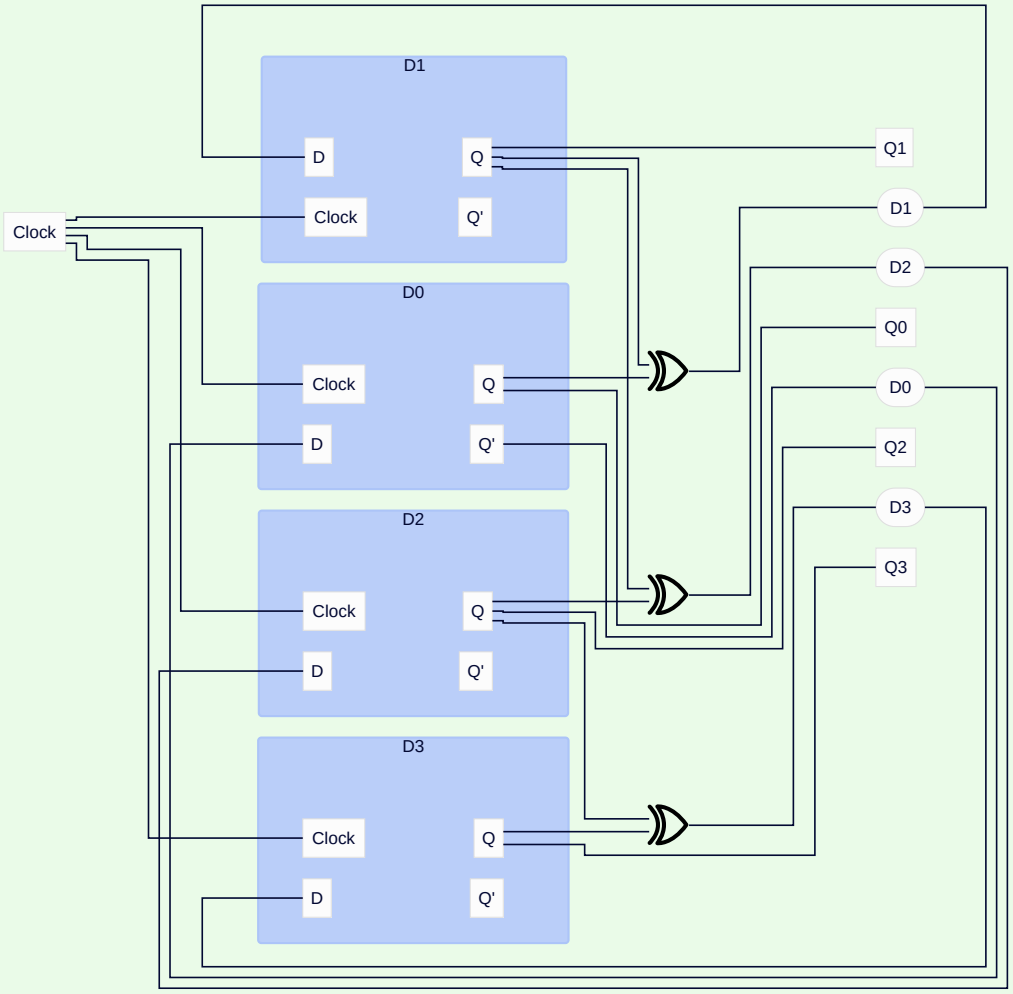
$$D0 = Q0'$$
$$D1 = Q1' \cdot (Q2 \wedge Q0)' + Q1 \cdot Q0'$$
$$D2 = Q2' \cdot Q1 \cdot Q0 + Q2 \cdot (Q1 \cdot Q0)'$$



4

Design a 4-bit ripple up counter using only four D flip-flops.

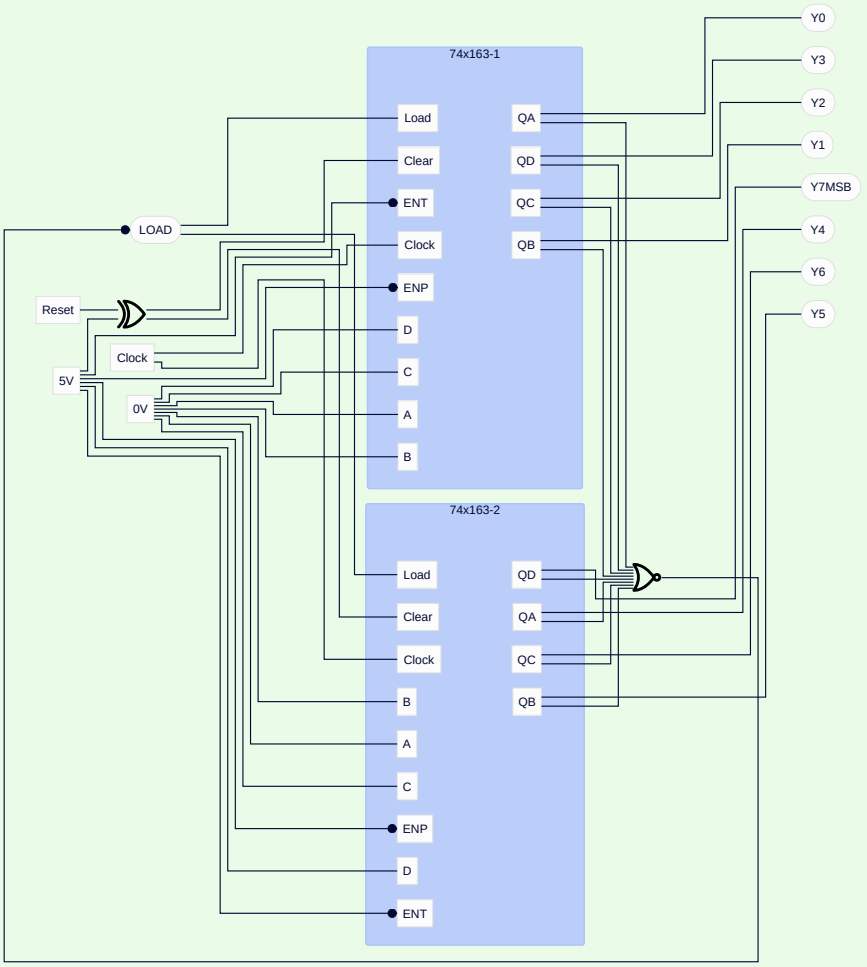
✓ **Answer**



5

Using two 74x163 counters, design a counter with counting sequence 0, 128, 129,..., 254, 255, 0, 128, 129, ... , 254, 255. Logic 0 and 1 are available.

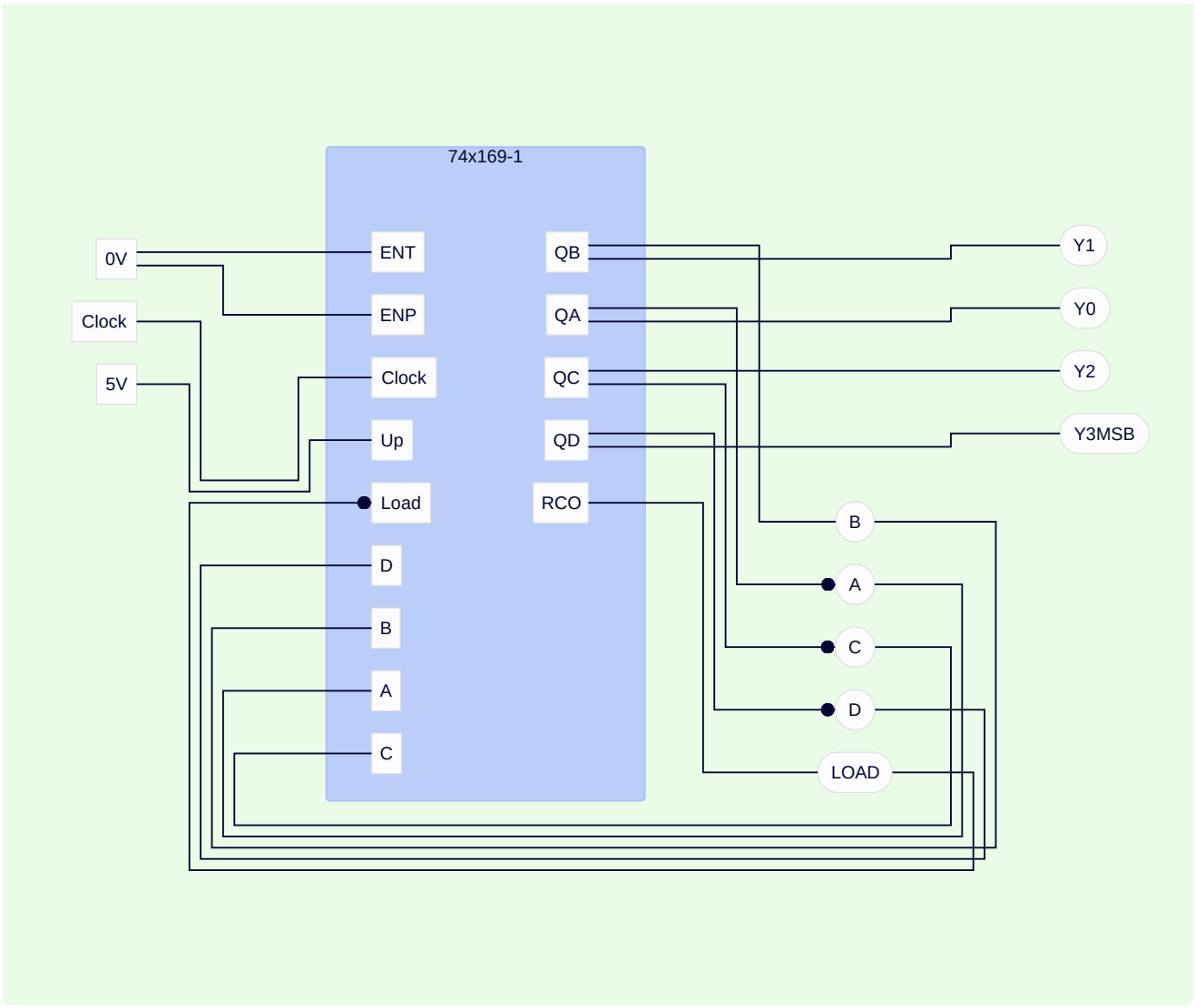
✓ **Answer**



6

Using one 74x169 and three inverters, design a counter with the counting sequence 4, 3, 2, 1, 0, 11, 12, 13, 14, 15, 4, 3 ...

✓ **Answer**


74x169-1
0V
Clock
5V
ENT
ENP
Clock
Up
Load
D
B
A
C
QB
QA
QC
QD
RCO
Y1
Y0
Y2
Y3MSB
B
A
C
D
LOAD