Code

alu_parm.sv

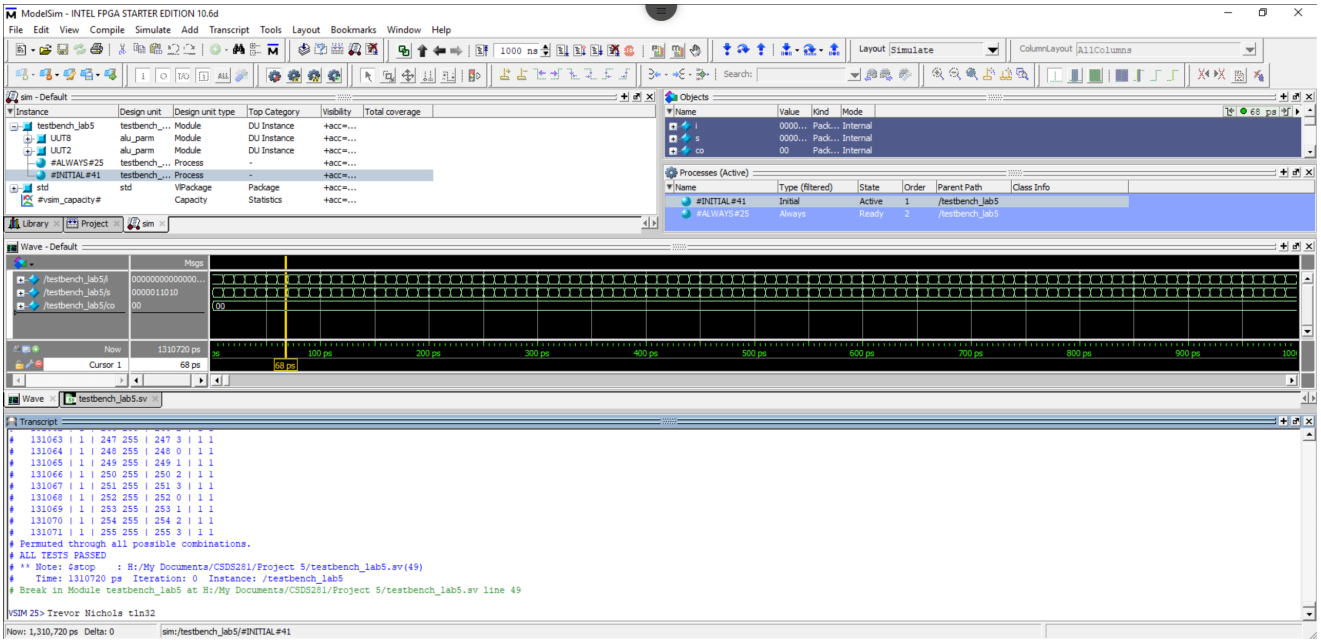
```
module alu_parm #(
    parameter N = 4
) (
    input logic [N-1:0] a, b,
    input logic c_in,
    output logic [N-1:0] s,
    output logic c_out
);
    logic [N-1:0] p, g;
    logic [N:0] c;

    always_comb begin
        p = a ^ b;
        g = a & b;

        c[0] = c_in;
        for (int i = 0 ; i < N; i++) begin
            c[i+1] = g[i] | (p[i] & c[i]);
        end
        s = p ^ c;
        c_out = c[N];
    end
endmodule
```

testbench_lab5.sv

```
`timescale 10ps/1ps

module testbench_lab5 ();

    logic [16:0] i=0;
    logic [9:0] s;
    logic [1:0] co;

    alu_parm #(8) UUT8 (
        i[7:0],
        i[15:8],
        i[16],
        s[9:2],
        co[1]
    );
```

```
    alu_parm #(2) UUT2 (
        i[1:0],
        i[9:8],
        i[16],
        s[1:0],
        co[0]
    );

    always begin
        i = $time % (2 ** 17);

        #0.5
        if (
            (s[9:2] ≠ (i[7:0] + i[15:8] + i[16])) ||
            (s[1:0] ≠ (i[1:0] + i[9:8] + i[16]))
        ) begin
            $display("Failed tests! %2d", $time);
            $display("Values: C_in: %b S: %b I: %b", i[16], s, i[15:0]);
            $display("Got: %b and %b", (i[7:0] + i[1:0] + i[16]),
(i[1:0] + i[9:8] + i[16]));
            $stop();
        end
        #0.5;
    end

    initial begin
        $display("TIME | C_in | A B | S8 S2 | C8 C2");
        $display("———————————————");
        $monitor("  %2d | %d | %d %d | %d %d | %b %b",
            $time, i[16], i[7:0], i[15:8], s[9:2], s[1:0], co[1],
co[0]);
        #131072
        $display("Permuted through all possible combinations.");
        $display("ALL TESTS PASSED");
        $stop();
    end

endmodule
```

Deliverables


ModelSim - INTEL FPGA STARTER EDITION 10.6d
File Edit View Compile Simulate Add Transcript Tools Layout Bookmarks Window Help
sim - Default
Instance
Design unit
Design unit type
Top Category
Visibility
Total coverage
testbench_lab5
UUT8
UUT2
#ALWAYS#25
#INITIAL#41
std
#vsim_capacity#
Objects
Name
Value
Kind
Mode
Processes (Active)
Type (filtered)
State
Order
Parent Path
Class Info
#INITIAL#41
#ALWAYS#25
Wave - Default
/testbench_lab5/i
/testbench_lab5/s
/testbench_lab5/co
Now
Cursor 1
Transcript
131063 | 1 | 247 255 | 247 3 | 1 1 1
131064 | 1 | 248 255 | 248 0 | 1 1 1
131065 | 1 | 249 255 | 249 1 | 1 1 1
131066 | 1 | 250 255 | 250 2 | 1 1 1
131067 | 1 | 251 255 | 251 3 | 1 1 1
131068 | 1 | 252 255 | 252 0 | 1 1 1
131069 | 1 | 253 255 | 253 1 | 1 1 1
131070 | 1 | 254 255 | 254 2 | 1 1 1
131071 | 1 | 255 255 | 255 3 | 1 1 1
Permuted through all possible combinations.
ALL TESTS PASSED
** Note: $stop : H:/My Documents/CSDS281/Project 5/testbench_lab5.sv(49)
Time: 1310720 ps Iteration: 0 Instance: /testbench_lab5
Break in Module testbench_lab5 at H:/My Documents/CSDS281/Project 5/testbench_lab5.sv line 49
VSIM 25> Trevor Nichols tln32
Now: 1,310,720 ps Delta: 0
sim:/testbench_lab5/#INITIAL#41