7

1

What is the benefit of Memory Hierarchy in General Purpose Computers?

✓ **Answer**

It strikes a balance between cost and speed, as faster memory is more expensive, but some applications require large amounts of memory and thus is not cost effective to have that much fast memory.

Having tiers of memory speed/cost allows for frequently used items to be cached at a faster speed, and less frequently used items or larger items to be cached in larger memory, maintaining a wider range of applications while balancing speed.

2

What is the addressable space for 32-bit memory address ?

✓ **Answer**

There will be 2^{32} different possible memory locations, assuming a memory location size of 1 byte, this allows for 2^{32} bytes of memory, or 4GB.

3

Why is DRAM cheaper than SRAM and what is the logic behind using SRAM for cache memory?

✓ **Answer**

DRAM contains fewer components as it utilizes a transistor and a capacitor, while SRAM contains 6 transistors, making SRAM more expensive, but faster.

SRAM is a lower density memory compared to DRAM as well as being more expensive, but faster. This is better suited for low-density high-speed applications like the CPU cache.

4

Redraw the following figure with 4-bit address of 1110 instead of 1101 in the figure (you can hand draw it).

✓ **Answer**

	Tag	Index	Block Offset
Address	1	11	0

Index	Valid	Tag	Data	
00	V_1	T_1	D_1	D_2
01	V_2	T_2	D_3	D_4
10	V_3	T_3	D_5	D_6
11	V_4	T_4	D_7	D_8

$Hit \leftarrow (T_4 = 1) \wedge V_4$
$Data \leftarrow Mux(D_7, D_8, 0) \rightarrow D_7$