1. There is a tremendous variety of products, from single-chip microcomputers costing a few dollars to supercomputers costing tens of millions of dollars that can rightly claim the name "computer".
a. True
b. False

2. The variety of computer products is exhibited only in cost. (Exhibited: trưng bày)
a. True
b. False

3. Computer organization refers to attributes of a system visible to the programmer. (Attributes: thuộc tính)
a. True
b. False

4. Changes in computer technology are finally slowing down.
a. True
b. False

5. The textbook for this course is about the structure and function of computers.
a. True
b. False

6. The number of bits used to represent various data types is an example of an architectural attribute.
a. True
b. False

7. Interfaces between the computer and peripherals is an example of an organizational attribute. (Interfaces: Giao diện) (Peripherals: thiết bị ngoại vi)
a. True
b. False

8. Historically the distinction between architecture and organization has not been an important one. (Distinction: phân biệt)
a. True
b. False

9. A particular architecture may span many years and encompass a number of different computer models, its organization changing with changing technology. (Span: kéo dài) (Encompass: bao gồm)
a. True
b. False

10. A microcomputer architecture and organization relationship is not very close.
a. True
b. False
11. Changes in technology not only influence organization but also result in the introduction of more powerful and more complex architectures.
a. True
b. False

12. The hierarchical nature of complex systems is essential to both their design and their description. (Hierarchical nature: bản chất thứ bậc/ phân cấp)
a. True
b. False

13. Both the structure and functioning of a computer are, in essence, simple. (Essence: bản chất)
a. True
b. False

14. A computer must be able to process, store, move, and control data.
a. True
b. False

15. When data are moved over longer distances, to or from a remote device, the process is known as data transport. (Transport: vận chuyển)
a. True
b. False

16. Computer technology is changing at a _____ pace. (Pace: nhịp độ)
a. slow
b. slow to medium
c. rapid
d. non-existent

17. Computer _____ refers to those attributes that have a direct impact on the logical execution of a program.
a. organization
b. specifics
c. design
d. architecture

18. Architectural attributes include _____ .
a. I/O mechanisms
b. control signals
c. interfaces
d. memory technology used

19. _____ attributes include hardware details transparent to the programmer. (Transparent: minh bạch, rõ ràng)
a. Interface
b. Organizational
c. Memory
d. Architectural
architectural
20. It is a(n) _____ design issue whether a computer will have a multiply instruction. (whether: cho dù)
a. architectural
b. memory
c. elementary
d. organizational

21. It is a(n) _____ issue whether the multiply instruction will be implemented by a special multiply unit or by a mechanism that makes repeated use of the add unit of the system. (Implemented: thực hiện)
a. architectural
b. memory
c. mechanical
d. organizational

22. A _____ system is a set of interrelated subsystems. (interrelated: liên quan)
a. secondary
b. hierarchical
c. complex
d. functional

23. An I/O device is referred to as a _____. (refrerred: được gọi là/ xem như là)
a. CPU
b. control device
c. peripheral
d. register

24. When data are moved over longer distances, to or from a remote device, the process is known as _____.
a. data communications
b. registering
c. structuring
d. data transport

25. The _____ stores data.
a. system bus

b. I/O
c. main memory
d. control unit

26. The _____ moves data between the computer and its external environment.
a. data transport
b. I/O
c. register
d. CPU interconnection

27. A common example of system interconnection is by means of a _____. (Common: phổ biến) (Interconnection: kết nối)
a. register
b. system bus
c. data transport
d. control device

28. A _____ is a mechanism that provides for communication among CPU, main memory, and I/O. (Among: giữa)
a. system interconnection
b. CPU interconnection
c. peripheral
d. processor

29. _____ provide storage internal to the CPU.
a. Control units
b. ALUs
c. Main memory
d. Registers

30. The _____ performs the computer's data processing functions.
a. Register
b. CPU interconnection
c. ALU
d. system bus

31. The world's first general-purpose electronic digital computer was designed and constructed at The Ohio State University. (Construct: thiết kế, xây dựng) - **University of Pennsylvania**
a. True
b. False

32. John Mauchly and John Eckert designed the ENIAC.
a. True
b. False

33. The major drawback of the EDVAC was that it had to be programmed manually by setting switches and plugging and unplugging cables. (Drawback: hạn chế) (Manually: thủ công)
a. True
b. False

34. The IAS is the prototype of all subsequent general-purpose computers. (Prototype: mẫu) (Subsequent: tiếp theo)
a. True
b. False

35. The IAS operates by repetitively performing an instruction cycle. (Intrusction cycle: chu kỳ lệnh)
a. True
b. False

36. Backward compatible means that the programs written for the older machines can be executed on the new machine. (Backward compatible: tương thích ngược)
a. True
b. False

37. A vacuum tube is a solid-state device made from silicon. (Solid-state: chất rắn)
a. True
b. False

38. Computers are classified into generations based on the fundamental hardware technology employed. (Fundamental: cơ bản) (Employed: được sử dụng)
a. True
b. False

39. System software was introduced in the third generation of computers.
a. True
b. False

40. A wafer is made of silicon and is broken up into chips which consists of many gates and/or memory cells plus a number of input and output attachment points. (Attachment: đính kèm)
a. True
b. False

41. IBM's System/360 was the industry's first planned family of computers.
a. True
b. False

42. Intel's 4004 was the first chip to contain all of the components of a CPU on a single chip.

a. True
b. False

43. Designers wrestle with the challenge of balancing processor performance with that of main memory and other computer components. (Wrestle: vật lộn)
a. True
b. False

44. The Intel x86 evolved from RISC design principles and is used in embedded systems.
(Evolved: phát triển) (Principle: nguyên tắc) (Embedded: nhúng)
a. True
b. False

45. A common measure of performance for a processor is the rate at which instructions are executed, expressed as billions of instructions per seconds (BIPS).
(Measure: thước đo) (Expressed: biểu thị)
a. True
b. False

46. The _____ was the world's first general-purpose electronic digital computer.
a. UNIVAC
b. MARK IV
c. ENIAC
d. Hollerith's Counting Machine

47. The Electronic Numerical Integrator and Computer project was a response to U.S. needs during _____.
a. the Civil War
b. the French-American War
c. World War I
d. World War II

48. The ENIAC used _____.
a. vacuum tubes (Bóng đèn điện tử)
b. integrated circuits (Mạch tích hợp)
c. IAS

49. The ENIAC is an example of a _____ generation computer.
a. first
b. second
c. third
d. fourth

50. The _____ interprets the instructions in memory and causes them to be executed. (Interprets: diễn giải)

a. main memory
b. control unit
c. I/O
d. arithmetic and logic unit

51. The memory of the IAS consists of 1000 storage locations called _____.
a. opcodes
b. wafers
c. VLSIs
d. words

52. The _____ contains the 8-bit opcode instruction being executed.
a. memory buffer register
b. instruction buffer register
c. instruction register
d. memory address register

53. During the _____ the opcode of the next instruction is loaded into the IR and the address portion is loaded into the MAR. (Portion: phần)
a. execute cycle
b. fetch cycle (Tìm nạp)
c. instruction cycle
d. clock cycle

54. Second generation computers used _____.
a. integrated circuits
b. Transistors
c. vacuum tubes
d. large-scale integration
integrated circuit
55. The _____ defines the third generation of computers.
a. integrated circuit
b. vacuum tube
c. transistor
d. VLSI

56. The use of multiple processors on the same chip is referred to as _____ and provides the potential to increase performance without increasing the clock rate. (Potential: tiềm năng)
a. multicore
b. GPU
c. data channels
d. MPC

57. With the _____, Intel introduced the use of superscalar techniques that allow multiple instructions to execute in parallel.

a. Core
b. 8080
c. 80486
d. Pentium

58. The _____ measures the ability of a computer to complete a single task.
a. clock speed
b. speed metric (số liệu tốc độ)
c. execute cycle (chu kỳ thực hiện)
d. cycle time (chu kỳ thời gian)

59. ARM processors are designed to meet the needs of _____.
(Meet the needs: đáp ứng nhu cầu)
a. embedded real-time systems (nhúng thời gian thực)
b. application platforms (nền tảng ứng dụng)
c. secure applications (nền tảng an toàn)
d. all of the above

60. One increment, or pulse, of the system clock is referred to as a _____.
(Increment: gia số - tăng) (Pulse: xung)
a. clock tick
b. cycle time
c. clock rate
d. cycle speed

61. At a top level, a computer consists of CPU, memory, and I/O components.
a. True
b. False

62. The basic function of a computer is to execute programs.
a. True
b. False

63. Program execution consists of repeating the process of instruction fetch and instruction execution.
a. True
b. False

64. Interrupts do not improve processing efficiency. (Interrupt: ngắt)
a. True
b. False

65. An I/O module cannot exchange data directly with the processor.
a. True
b. False

66. A key characteristic of a bus is that it is not a shared transmission medium.
a. True
b. False

67. Computer systems contain a number of different buses that provide pathways between components at various levels of the computer system hierarchy.
a. True
b. False

68. In general, the more devices attached to the bus, the greater the bus length and hence the greater the propagation delay.
(Hence: từ đây) (Propagtion: lan truyền) (Attach: gắn)
a. True
b. False

69. It is not possible to connect I/O controllers directly onto the system bus.
a. True
b. False

70. The method of using the same lines for multiple purposes is known as time multiplexing.
a. True
b. False

71. Timing refers to the way in which events are coordinated on the bus.
(Refer: đề cập đến) (Coordinated: phối hợp / điều phối)
a. True
b. False

72. With asynchronous timing the occurrence of events on the bus is determined by a clock. (Asynchronous: không đồng bộ) (Occurrence: tần suất) (Determine: xác định)
a. True
b. False

73. Because all devices on a synchronous bus are tied to a fixed clock rate, the system cannot take advantage of advances in device performance. (Fixed: cố định / bất biến)
a. True
b. False

74. The unit of transfer at the link layer is a phit and the unit transfer at the physical layer is a flit.
a. True
b. False

75. A key requirement for PCIe is high capacity to support the needs of higher data rate I/O devices such as Gigabit Ethernet. (Capacity: dung lượng)

a. True
b. False

76. Virtually all contemporary computer designs are based on concepts developed by _____ at the Institute for Advanced Studies, Princeton.
(Virtually: hầu như) (Contemporary: đương đại/ hiện đại)
A. John Maulchy
B. John von Neumann
C. Herman Hollerith
D. John Eckert

77. The von Neumann architecture is based on which concept?
(Occurs: diễn ra / xảy ra) (Sequential: tuần tự) (Fashion: kiểu)
A. Data and instructions are stored in a single read-write memory
B. The contents of this memory are addressable by location
C. Execution occurs in a sequential fashion
D. All of the above

78. A sequence of codes or instructions is called _____.
A. Software
B. Memory
C. An interconnect
D. A register

79. The processing required for a single instruction is called a(n) _____ cycle.
A. Execute
B. Fetch
C. Instruction
D. Packet

80. A(n) _____ is generated by a failure such as power failure or memory parity error. (Generated: được tạo ra) (Parity: chẵn lẻ)
A. I/O interrupt
B. Hardware failure interrupt
C. Timer interrupt
D. Program interrupt

81. A(n) _____ is generated by some condition that occurs as a result of an instruction execution. (Condition: điều kiện/ tình trạng)
A. Timer interrupt
B. I/O interrupt
C. Program interrupt
D. Hardware failure interrupt

82. The interconnection structure must support which transfer?
A. Memory to processor
B. Processor to memory
C. I/O to or from memory
D. All of the above

83. A bus that connects major computer components (processor, memory, I/O) is called a _____.
A. System bus
B. Address bus
C. Data bus
D. Control bus

84. The _____ are used to designate the source or destination of the data on the data bus. (Designate: chỉ định) (Destination: đích)
A. System lines
B. Data lines
C. Control lines
D. Address lines

85. The data lines provide a path for moving data among system modules and are collectively called the _____.
A. Control bus
B. Address bus
C. Data bus
D. System bus

86. A _____ is the high-level set of rules for exchanging packets of data between devices.
A. Bus
B. Protocol
C. Packet
D. QPI

87. Each data path consists of a pair of wires (referred to as a _____) that transmits data one bit at a time.
A. Lane (làn)
B. Path (đường)
C. Line (hàng)
D. Bus

88. The _____ receives read and write requests from the software above the TL and creates request packets for transmission to a destination via the link layer.
(Above: bên trên) (Via: qua)
A. Transaction layer (lớp giao dịch)
B. Root layer (lớp gốc)
C. Configuration layer (lớp cấu hình)
D. Transport layer (lớp vận chuyển)

89. The TL supports which of the following address spaces?
A. Memory
B. I/O
C. Message
D. All of the above

90. The QPI _____ layer is used to determine the course that a packet will traverse across the available system interconnects.
(Course: quá trình) (Traverse: đi qua) (Across: ngang qua)
A. Link
B. Protocol
C. Routing (định tuyến)
D. Physical

Chap 4:

1. No single technology is optimal in satisfying the memory requirements for a computer system. (Optimal: tối ưu) (Satisfying: đáp ứng/ thỏa mãn)
a. True
b. False

2. A typical computer system is equipped with a hierarchy of memory subsystems, some internal to the system and some external. (Typical: đặc trưng/ điển hình)
a. True
b. False

3. External memory is often equated with main memory. (Equated: ngang nhau)
a. True
b. False

4. The processor requires its own local memory.
a. True
b. False

5. Cache is not a form of internal memory.
a. True
b. False

6. The unit of transfer must equal a word or an addressable unit. (Equal: bằng)
a. True
b. False

7. Both sequential access and direct access involve a shared read-write mechanism. (Involve: liên quan)
a. True
b. False

8. In a volatile memory, information decays naturally or is lost when electrical power is switched off. (Volatile: bay hơi) (decays: sự phân rã)
a. True
b. False

9. To achieve greatest performance the memory must be able to keep up with the processor. (Keep up: theo kịp)
a. True
b. False

10. Secondary memory is used to store program and data files and is usually visible to the programmer only in terms of individual bytes or words.
a. True
b. False

11. The L1 cache is slower than the L3 cache.
a. True
b. False

12. With write back updates are made only in the cache.
a. True
b. False

13. It has become possible to have a cache on the same chip as the processor.
a. True
b. False

14. All of the Pentium processors include two on-chip L1 caches, one for data and one for instructions.
a. True
b. False

15. Cache design for HPC is the same as that for other hardware platforms and applications.
a. True
b. False

16. _____ refers to whether memory is internal or external to the computer.
A. Location
B. Access
C. Hierarchy
D. Tag

17. Internal memory capacity is typically expressed in terms of _____.
A. Hertz
B. Nanos
C. Bytes
D. LOR

18. For internal memory, the _____ is equal to the number of electrical lines into and out of the memory module.
A. Access time
B. Unit of transfer
C. Capacity
D. Memory ratio

19. "Memory is organized into records and access must be made in a specific linear sequence" is a description of _____.
A. Sequential access
B. Direct access
C. Random access
D. Associative

20. individual blocks or records have a unique address based on physical location with _____.
A. Associative
B. Physical access
C. Direct access
D. Sequential access

21. For random-access memory, _____ is the time from the instant that an address is presented to the memory to the instant that data have been stored or made available for use.
A. Memory cycle time
B. Direct access
C. Transfer rate
D. Access time

22. The _____ consists of the access time plus any additional time required before a second access can commence.
A. Latency
B. Memory cycle time
C. Direct access
D. Transfer rate

23. A portion of main memory used as a buffer to hold data temporarily that is to be read out to disk is referred to as a _____.(1 phần bộ nhớ chính)
A. Disk cache
B. Latency
C. Virtual address
D. Miss

24. A line includes a _____ that identifies which particular block is currently being stored.
A. Cache
B. Hit
C. Tag
D. Locality

25. _____ is the simplest mapping technique and maps each block of main memory into only one possible cache line.
A. Direct mapping
B. Associative mapping
C. Set associative mapping
D. None of the above

26. When using the _____ technique all write operations made to main memory are made to the cache as well.
a. write back
b. LRU
c. write through
d. unified cache

27. The key advantage of the _____ design is that it eliminates contention for the cache between the instruction fetch/decode unit and the execution unit.
(loại bỏ sự tranh giành)
a. logical cache
b. split cache
c. unified cache
d. physical cache

28. The Pentium 4 _____ component executes micro-operations, fetching the required data from the L1 data cache and temporarily storing results in registers.
a. fetch/decode unit
b. out-of-order execution logic
c. execution unit
d. memory subsystem

29. In reference to access time to a two-level memory, a _____ occurs if an accessed word is not found in the faster memory.
a. miss
b. hit
c. line
d. tag

30. A logical cache stores data using _____.
a. physical addresses
b. virtual addresses
c. random addresses
d. none of the above

Chap 5:

1. The basic element of a semiconductor memory is the memory cell.
a. True
b. False

2. A characteristic of ROM is that it is volatile.
a. True
b. False

3. RAM must be provided with a constant power supply. (Constant: liên tục)
a. True
b. False

4. The two traditional forms of RAM used in computers are DRAM and SRAM.
a. True
b. False

5. A static RAM will hold its data as long as power is supplied to it.
a. True
b. False

6. Nonvolatile means that power must be continuously supplied to the memory to preserve the bit values. (Preserve: bảo toàn)
a. True
b. False

7. The advantage of RAM is that the data or program is permanently in main memory and need never be loaded from a secondary storage device. (Permanetly: vĩnh viễn)
a. True
b. False

8. Semiconductor memory comes in packaged chips.
a. True
b. False

9. All DRAMs require a refresh operation.
a. True
b. False

10. A number of chips can be grouped together to form a memory bank.
a. True
b. False

11. An error-correcting code enhances the reliability of the memory at the cost of added complexity. (Nâng cao độ tin cậy của bộ nhớ - tăng chi phí độ phức tạp)
a. True
b. False

12. DRAM is much costlier than SRAM. (Đắt hơn)
a. True
b. False

13. RDRAM is limited by the fact that it can only send data to the processor once per bus clock cycle.
a. True
b. False

14. The prefetch buffer is a memory cache located on the RAM chip.
a. True
b. False

15. The SRAM on the CDRAM cannot be used as a buffer to support the serial access of a block of data.
a. True
b. False

16. Which properties do all semiconductor memory cells share?
a. they exhibit two stable states which can be used to represent binary 1 and 0
b. they are capable of being written into to set the state
c. they are capable of being read to sense the state
d. all of the above

17. One distinguishing characteristic of memory that is designated as _____ is that it is possible to both to read data from the memory and to write new data into the memory easily and rapidly.
a. RAM
b. ROM
c. EPROM
d. EEPROM

18. Which of the following memory types are nonvolatile?
a. erasable PROM
b. programmable ROM
c. flash memory
d. all of the above

19. In a _____, binary values are stored using traditional flip-flop logic-gate configurations.
a. ROM
b. SRAM
c. DRAM
d. RAM

20. A _____ contains a permanent pattern of data that cannot be changed, is nonvolatile, and cannot have new data written into it.
a. RAM
b. SRAM
c. ROM
d. flash memory

21. With _____ the microchip is organized so that a section of memory cells are erased in a single action. (tích tắc)
a. flash memory
b. SDRAM
c. DRAM
d. EEPROM

22. _____ can be caused by harsh environmental abuse, manufacturing defects, and wear.
a. SEC errors
b. Hard errors
c. Syndrome errors
d. Soft errors

23. _____ can be caused by power supply problems or alpha particles.
a. Soft errors
b. AGT errors
c. Hard errors
d. SEC errors

24. The _____ exchanges data with the processor synchronized to an external clock signal and running at the full speed of the processor/memory bus without imposing wait states.
a. DDR-DRAM
b. SDRAM
c. CDRAM
d. none of the above

25. _____ can send data to the processor twice per clock cycle.
a. CDRAM
b. SDRAM
c. DDR-DRAM
d. RDRAM

26. _____ increases the data transfer rate by increasing the operational frequency of the RAM chip and by increasing the prefetch buffer from 2 bits to 4 bits per chip. (tăng số hoạt động và từ 2 lên 4 bits)
a. DDR2
b. RDRAM
c. CDRAM
d. DDR3

27. _____ increases the prefetch buffer size to 8 bits.
a. CDRAM
b. RDRAM
c. DDR3
d. all of the above

28. Theoretically, a DDR module can transfer data at a clock rate in the range of _____ MHz.
a. 200 to 600
b. 400 to 1066
c. 600 to 1400
d. 800 to 1600

X * 2 to 200 + (200 – DDR2) + (400 – DDR3) + (600 – DDR4)

29. A DDR3 module transfers data at a clock rate of _____ MHz.
a. 600 to 1200
b. 800 to 1600
c. 1000 to 2000
d. 1500 to 3000

30. The _____ enables the RAM chip to preposition bits to be placed on the data bus as rapidly as possible.
a. flash memory
b. Hamming code
c. RamBus
d. buffer

Chap 6:

1. Magnetic disks are the foundation of external memory on virtually all computer systems.
a. True
b. False

2. During a read or write operation, the head rotates while the platter beneath it stays stationary. (đứng yên)
a. True
b. False

3. The width of a track is double that of the head.
a. True
b. False

4. There are typically hundreds of sectors per track and they may be either fixed or variable lengths.
a. True
b. False

5. A bit near the center of a rotating disk travels past a fixed point slower than a bit on the outside.
a. True
b. False

6. The disadvantage of using CAV is that individual blocks of data can only be directly addressed by track and sector.
a. True
b. False

7. A removable disk can be removed and replaced with another disk.
a. True
b. False

8. The head must generate or sense an electromagnetic field of sufficient magnitude to write and read properly.
a. True
b. False

9. The transfer time to or from the disk does not depend on the rotation speed of the disk.
a. True
b. False

10. RAID is a set of physical disk drives viewed by the operating system as a single logical drive.
a. True
b. False

11. RAID level 0 is not a true member of the RAID family because it does not include redundancy to improve performance.
a. True
b. False

12. Because data are striped in very small strips, RAID 3 cannot achieve very high data transfer rates.
a. True
b. False

13. The SSDs now on the market use a type of semiconductor memory referred to as flash memory.
a. True
b. False

14. SSD performance has a tendency to speed up as the device is used.
a. True
b. False

15. Flash memory becomes unusable after a certain number of writes.
a. True
b. False

16. Greater ability to withstand shock and damage, improvement in the uniformity of the magnet film surface to increase disk reliability, and a significant reduction in overall surface defects to help reduce read-write errors, are all benefits of _____.
a. magnetic read and write mechanisms
b. platters
c. the glass substrate
d. a solid state drive

17. Adjacent tracks are separated by _____. (đường tuyến kết nối với nhau bằng)
a. sectors
b. gaps
c. pits
d. heads

18. Data are transferred to and from the disk in _____.
a. tracks
b. gaps
c. sectors
d. pits

19. In most contemporary systems fixed-length sectors are used, with _____ bytes being the nearly universal sector size.
a. 64
b. 128
c. 256
d. 512

20. Scanning information at the same rate by rotating the disk at a fixed speed is known as the _____.
a. constant angular velocity
b. magnetoresistive
c. rotational delay
d. constant linear velocity

21. The disadvantage of _____ is that the amount of data that can be stored on the long outer tracks is only the same as what can be stored on the short inner tracks.
a. SSD
b. CAV
c. ROM
d. CLV

22. A _____ disk is permanently mounted in the disk drive, such as the hard disk in a personal computer.
a. nonremovable
b. movable-head
c. double sided
d. removable

23. When the magnetizable coating is applied to both sides of the platter the disk is then referred to as _____.
a. multiple sided
b. substrate
c. double sided
d. all of the above

24. The set of all the tracks in the same relative position on the platter is referred to as a _____.
a. floppy disk
b. single-sided disk
c. sector
d. cylinder

25. The sum of the seek time and the rotational delay equals the _____, which is the time it takes to get into position to read or write.
a. access time
b. gap time
c. transfer time
d. constant angular velocity

26. _____ is the standardized scheme for multiple-disk database design.
a. RAID
b. CAV
c. CLV
d. SSD

27. RAID level _____ has the highest disk overhead of all RAID types.
a. 0
b. 1
c. 3
d. 5

28. A _____ is a high-definition video disk that can store 25 Gbytes on a single layer on a single side.
a. DVD
b. DVD-R
c. DVD-RW
d. Blu-ray DVD

29. _____ is when the disk rotates more slowly for accesses near the outer edge than for those near the center.
a. Constant angular velocity (CAV)
b. Magnetoresistive
c. Constant linear velocity (CLV)
d. Seek time

30. The areas between pits are called _____.
a. lands
b. sectors
c. cylinders
d. strips

Chap 7:

1. A set of I/O modules is a key element of a computer system.
a. True
b. False

2. An I/O module must recognize one unique address for each peripheral it controls.
a. True
b. False

3. I/O channels are commonly seen on microcomputers, whereas I/O controllers are used on mainframes.
a. True
b. False

4. It is the responsibility of the processor to periodically check the status of the I/O module until it finds that the operation is complete.
a. True
b. False

5. With isolated I/O there is a single address space for memory locations and I/O devices.
a. True
b. False

6. A disadvantage of memory-mapped I/O is that valuable memory address space is used up.
a. True
b. False

7. The disadvantage of the software poll is that it is time consuming.
a. True
b. False

8. With a daisy chain the processor just picks the interrupt line with the highest priority.
a. True
b. False

9. Bus arbitration makes use of vectored interrupts.
a. True
b. False

10. The rotating interrupt mode allows the processor to inhibit interrupts from certain devices.
a. True
b. False

11. Because the 82C55A is programmable via the control register, it can be used to control a variety of simple peripheral devices.
a. True
b. False

12. When large volumes of data are to be moved, a more efficient technique is direct memory access (DMA).
a. True
b. False

13. An I/O channel has the ability to execute I/O instructions, which gives it complete control over I/O operations.
a. True
b. False

14. A multipoint external interface provides a dedicated line between the I/O module and the external device.
a. True
b. False

15. A Thunderbolt compatible peripheral interface is no more complex than that of a simple USB device.
a. True
b. False

16. The _____ contains logic for performing a communication function between the peripheral and the bus.
a. I/O channel
b. I/O module
c. I/O processor
d. I/O command

17. The most common means of computer/user interaction is a _____.
a. keyboard/monitor
b. mouse/printer
c. modem/printer
d. monitor/printer

18. The I/O function includes a _____ requirement to coordinate the flow of traffic between internal resources and external devices. (điều phối)
a. cycle
b. status reporting
c. control and timing
d. data

19. An I/O module that takes on most of the detailed processing burden, presenting a high-level interface to the processor, is usually referred to as an _____.
a. I/O channel
b. I/O command
c. I/O controller
d. device controller

20. An I/O module that is quite primitive and requires detailed control is usually referred to as an _____.
a. I/O command
b. I/O controller
c. I/O channel
d. I/O processor

21. The _____ command causes the I/O module to take an item of data from the data bus and subsequently transmit that data item to the peripheral.
a. control
b. test
c. read
d. write

22. The _____ command is used to activate a peripheral and tell it what to do.
a. control
b. test
c. read
d. write

23. _____ is when the DMA module must force the processor to suspend operation temporarily.
a. Interrupt
b. Thunderbolt
c. Cycle stealing
d. Lock down

24. The 8237 DMA is known as a _____ DMA controller.
a. command
b. cycle stealing
c. interrupt
d. fly-by

25. _____ is a digital display interface standard now widely adopted for computer monitors, laptop displays, and other graphics and video interfaces.
a. DisplayPort
b. PCI Express
c. Thunderbolt
d. InfiniBand

26. The _____ layer is the key to the operation of Thunderbolt and what makes it attractive as a high-speed peripheral I/O technology.
a. cable
b. application
c. common transport
d. physical

27. The Thunderbolt protocol _____ layer is responsible for link maintenance including hot-plug detection and data encoding to provide highly efficient data transfer.
a. cable
b. application
c. common transport
d. physical

28. The _____ contains I/O protocols that are mapped on to the transport layer.
a. cable
b. application
c. common transport
d. physical

29. A _____ is used to connect storage systems, routers, and other peripheral devices to an InfiniBand switch.
a. target channel adapter
b. InfiniBand switch
c. host channel adapter
d. subnet

30. A _____ connects InfiniBand subnets, or connects an InfiniBand switch to a network such as a local area network, wide area network, or storage area network.
a. memory controller
b. TCA
c. HCA
d. router

Chap 8:
1. Scheduling and memory management are the two OS functions that are most relevant to the study of computer organization and architecture.
a. True
b. False

2. The end user is concerned mainly with the computer's architecture.
a. True
b. False

3. The most important system program is the OS.
a. True
b. False

4. The ABI is the boundary between hardware and software.
a. True
b. False

5. The OS must determine how much processor time is to be devoted to the execution of a particular user program.
a. True
b. False

6. With a batch operating system the user does not have direct access to the processor.
a. True
b. False

7. Privileged instructions are certain instructions that are designated special and can be executed only by the monitor. (hướng dẫn đặc quyền)
a. True
b. False

8. Uniprogramming is the central theme of modern operating systems.
a. True
b. False

9. Both batch multiprogramming and time sharing use multiprogramming.
a. True
b. False

10. An interrupt is a hardware-generated signal to the processor.
a. True
b. False

11. Swapping is an I/O operation.
a. True
b. False

12. With demand paging it is necessary to load an entire process into main memory.
a. True
b. False

13. The Pentium II includes hardware for both segmentation and paging.
a. True
b. False

14. ARM provides a versatile virtual memory system architecture that can be tailored to the needs of the embedded system designer.
a. True
b. False

15. Managers are users of domains that must observe the access permissions of the individual sections and/or pages that make up that domain. (quan sát)
a. True
b. False

16. The _____ is a program that controls the execution of application programs and acts as an interface between applications and the computer hardware.
a. job control language
b. operating system
c. batch system
d. nucleus

17. Facilities and services provided by the OS that assist the programmer in creating programs are in the form of _____ programs that are not actually part of the OS but are accessible through the OS.
a. utility
b. multitasking
c. JCL
d. logical address

18. The _____ defines the repertoire of machine language instructions that a computer can follow.
a. ABI
b. API
c. HLL
d. ISA

19. The _____ defines the system call interface to the operating system and the hardware resources and services available in a system through the user instruction set architecture.
a. HLL
b. API
c. ABI
d. ISA

20. The _____ gives a program access to the hardware resources and services available in a system through the user instruction set architecture supplemented with high-level language library calls.
a. JCL
b. ISA
c. ABI
d. API

21. A _____ system works only one program at a time.
a. batch
b. uniprogramming
c. kernel
d. privileged instruction

22. A _____ is a special type of programming language used to provide instructions to the monitor.
a. job control language
b. multiprogram
c. kernel
d. utility

23. The _____ scheduler determines which programs are admitted to the system for processing.
a. long-term
b. medium-term
c. short-term
d. I/O

24. The _____ scheduler is also known as the dispatcher. (người điều phối)
a. long-term
b. medium-term
c. short-term
d. I/O

25. A _____ is an actual location in main memory. (thực tế)
a. logical address
b. partition address
c. base address
d. physical address

26. _____ is when the processor spends most of its time swapping pages rather than executing instructions.
a. Swapping
b. Thrashing
c. Paging
d. Multitasking

27. Virtual memory schemes make use of a special cache called a _____ for page table entries.
a. TLB
b. HLL
c. VMC
d. SPB

28. With _____ the virtual address is the same as the physical address. (unun)
a. unsegmented unpaged memory
b. unsegmented paged memory
c. segmented unpaged memory
d. segmented paged memory

29. A _____ is a collection of memory regions.
a. APX
b. nucleus
c. domain
d. page table

30. The OS maintains a _____ for each process that shows the frame location for each page of the process.
a. kernel
b. page table
c. TLB
d. logical address

Chap 9:

1. Our primary counting system is based on binary digits to represent numbers.
a. True
b. False

2. The decimal system has a radix of 100.
a. True
b. False

3. Negative powers of 10 are used to represent the positions of the numbers for decimal fractions. (mũ âm)
a. True
b. False

4. A number with both an integer and fractional part has digits raised to both positive and negative powers of 10.
a. True
b. False

5. In any number, the rightmost digit is referred to as the most significant digit. (ngoài cùng bên phải – có nghĩa nhất)
a. True
b. False

6. There are 50 tens in the number 509.
a. True
b. False

7. The decimal system is a special case of a positional number system with radix 10 and with digits in the range 0 through 9. (radix: cơ số)
a. True
b. False

8. A number cannot be converted from binary notation to decimal notation.
a. True
b. False

9. Although convenient for computers, the binary system is exceedingly cumbersome for human beings. (cồng kềnh)
a. True
b. False

10. A nibble is a grouping of four decimal digits.
a. True
b. False

11. Hexadecimal notation is only used for representing integers.
a. True
b. False

12. It is extremely easy to convert between binary and hexadecimal notation.
a. True
b. False

13. Hexadecimal notation is more compact than binary notation. (nhỏ gọn)
a. True
b. False

14. A sequence of hexadecimal digits can be thought of as representing an integer in base 10.
a. True
b. False

15. Because of the inherent binary nature of digital computer components, all forms of data within computers are represented by various binary codes. (bản chất – máy tính hiểu bằng mã nhị phân)
a. True
b. False

16. The decimal system has a base of _____.
a. 0
b. 10
c. 100
d. 1000

17. Which digit represents "hundreds" in the number 8732?
a. 8
b. 7
c. 3

18. Which of the following is correct?
a. 25 = (2 x 102) + (5 x 101)
b. 289 = (2 x 103) + (8 x 101) + (9 x 100)
c. 7523 = (7 x 10^3) + (5 x 10^2) + (2 x 10^1) + (3 x 10^0)
d. 0.628 = (6 x 10-3) + (2 x 10-2) + (8 x 10-1)

19. In the number 3109, the 3 is referred to as the _____.
a. most significant digit
b. least significant digit
c. radix
d. base

20. In the number 3109, the 9 is referred to as the _____.
a. most significant digit
b. least significant digit
c. radix
d. base

21. Numbers in the binary system are represented to the _____.
a. base 0
b. base 1
c. base 2
d. base 10

22. Hexadecimal has a base of _____.
a. 2
b. 8
c. 10
d. 16

23. The binary string 110111100001 is equivalent to _____.
a. DE1 16
b. C78 16
c. FF64 16
d. B8F 16

24. The _____ system uses only the numbers 0 and 1.
a. positional
b. binary
c. hexadecimal
d. decimal

25. Decimal "10" is _____ in binary.
a. 1000
b. 0010
c. 1010
d. 0001

26. Decimal "10" is _____ in hexadecimal.
a. 1
b. A
c. 0
d. FF

27. Four bits is called a _____.
a. radix point
b. byte
c. nibble
d. binary digit

28. Another term for "base" is _____.
a. radix
b. integer
c. position
d. digit

29. In the number 472.156 the 2 is the _____.
a. most significant digit
b. radix point
c. least significant digit
d. none of the above

30. Binary 0101 is hexadecimal _____.
a. 0
b. 5
c. A
d. 10

Chap 10:

1. The operation of the digital computer is based on the storage and processing of binary data.
a. True
b. False

2. Claude Shannon, a research assistant in the Electrical Engineering Department at M.I.T., proposed the basic principles of Boolean algebra. (đề xuất)
a. True
b. False

3. In the absence of parentheses, the AND operation takes precedence over the OR operation. (không có dấu ngoặc – ưu tiên hơn)
a. True
b. False

4. Logical functions are implemented by the interconnection of decoders. (bộ giải mã)
a. True
b. False

5. The delay by the propagation time of signals through the gate is known as the gate delay.
a. True
b. False

6. A combinational circuit consists of n binary inputs and m binary outputs.
a. True
b. False

7. Any Boolean function can be implemented in electronic form as a network of gates.
a. True
b. False

8. A Boolean function can be realized in the sum of products (SOP) form but not in the product of sums (POS) form.
a. True
b. False

9. "Don't care" conditions are when certain combinations of values of variables never occur, and therefore the corresponding output never occurs.
a. True
b. False

10. The value to be loaded into the program counter can come from a binary counter, the instruction register, or the output of the ALU.
a. True
b. False

11. In general, a decoder has n inputs and 2n outputs.
a. True
b. False

12. Combinational circuits are often referred to as "memoryless" circuits because their output depends only on their current input and no history of prior inputs is retained.
a. True
b. False

13. Binary addition is exactly the same as Boolean algebra.
a. True
b. False

14. Events in the digital computer are synchronized to a clock pulse so that changes occur only when a clock pulse occurs.
a. True

15. A register is a digital circuit used within the CPU to store one or more bits of data.
a. True
b. False

16. The operand _____ yields true if and only if both of its operands are true.
a. XOR
b. OR
c. AND
d. NOT

17. The operation _____ yields true if either or both of its operands are true.
a. NOT
b. AND
c. NAND
d. OR

18. The unary operation _____ inverts the value of its operand. (đảo ngược)
a. OR
b. NOT
c. NAND
d. XOR

19. A _____ is an electronic circuit that produces an output signal that is a simple Boolean operation on its input signals.
a. gate
b. decoder
c. counter
d. flip-flop

20. Which of the following is a functionally complete set?
a. AND, NOT
b. NOR
c. AND, OR, NOT
d. all of the above

21. For more than four variables an alternative approach is a tabular technique referred to as the _____ method.
a. DeMorgan
b. Quine-McCluskey
c. Karnaugh map
d. Boole-Shannon

22. _____ are used in digital circuits to control signal and data routing.
a. Multiplexers
b. Program counters
c. Flip-flops
d. Gates

23. _____ is implemented with combinational circuits.
a. Nano memory
b. Random access memory
c. Read only memory
d. No memory

24. The _____ exists in one of two states and, in the absence of input, remains in that state. (không có đầu vào – vẫn ở trạng thái đó)
a. assert
b. complex PLD
c. decoder
d. flip-flop

25. The _____ flip-flop has two inputs and all possible combinations of input values are valid.
a. J-K
b. D
c. S-R
d. clocked S-R

26. A _____ accepts and/or transfers information serially.
a. S-R latch
b. shift register
c. FPGA
d. parallel register

27. Counters can be designated as _____.
a. asynchronous
b. synchronous
c. both asynchronous and synchronous
d. neither asynchronous or synchronous

28. CPUs make use of _____ counters, in which all of the flip-flops of the counter change at the same time.
a. synchronous
b. asynchronous
c. clocked S-R
d. timed ripple

29. The _____ table provides the value of the next output when the inputs and the present output are known, which is exactly the information needed to design the counter or any sequential circuit.
a. excitation
b. Kenough
c. J-K flip-flop
d. FPGA

30. A _____ is a PLD featuring a general structure that allows very high logic capacity and offers more narrow logic resources and a higher ration of flip-flops to logic resources than do CPLDs.
a. SPLD
b. FPGA
c. PAL
d. PLA

Chap 10:

1. One boundary where the computer designer and the computer programmer can view the same machine is the machine instruction set.
a. True
b. False

2. The operation to be performed is specified by a binary code known as the operation code.
a. True
b. False

3. The address of the next instruction to be fetched must be a real address, not a virtual address.
a. True
b. False

4. It has become common practice to use a symbolic representation of machine instructions. (ký hiệu)
a. True
b. False

5. A high-level language expresses operations in a basic form involving the movement of data to or from registers.
a. True
b. False

6. One of the traditional ways of describing processor architecture is in terms of the number of addresses contained in each instruction.
a. True
b. False

7. Memory references are faster than register references.
a. True
b. False

8. The instruction set is the programmer's means of controlling the processor.
a. True
b. False

9. Addresses are a form of data.
a. True
b. False

10. Not all machine languages include numeric data types.
a. True
b. False

11. ARM processors support data types of 8 (byte), 16 (halfword), and 32 (word) bits in length.
a. True
b. False

12. Most machines provide the basic arithmetic operations of add, subtract, multiply, and divide.
a. True
b. False

13. A branch can be either forward or backward. (nhánh)
a. True
b. False

14. Procedures do not allow programming tasks to be subdivided into smaller units.
a. True
b. False

15. The focus of MMX technology is multimedia programming.
a. True
b. False

16. The _____ specifies the operation to be performed.
a. source operand reference
b. opcode
c. next instruction reference
d. processor register

17. A(n) _____ expresses operations in a concise algebraic form using variables. (diễn đạt phép toán dưới dạng đại số ngắn gọn)
a. opcode
b. high-level language
c. machine language
d. register

18. There must be _____ instructions for moving data between memory and the registers.
a. branch
b. logic
c. memory
d. I/O

19. _____ instructions operate on the bits of a word as bits rather than as numbers, providing capabilities for processing any other type of data the user may wish to employ.
a. Logic
b. Arithmetic
c. Memory
d. Test

20. _____ instructions provide computational capabilities for processing number data. (khả năng tính toán)
a. Boolean
b. Logic
c. Memory
d. Arithmetic

21. _____ instructions are needed to transfer programs and data into memory and the results of computations back out to the user.
a. I/O
b. Transfer
c. Control
d. Branch

22. The x86 data type that is a signed binary value contained in a byte, word, or doubleword, using twos complement representation is _____.
a. general
b. ordinal
c. integer
d. packed BCD

23. The most fundamental type of machine instruction is the _____ instruction.
a. conversion
b. data transfer
c. arithmetic
d. logical

24. The _____ instruction includes an implied address. (địa chỉ ngầm định)
a. skip
b. rotate
c. stack
d. push

25. Which of the following is a true statement?
a. a procedure can be called from more than one location
b. a procedure call can appear in a procedure
c. each procedure call is matched by a return in the called program
d. all of the above

26. The entire set of parameters, including return address, which is stored for a procedure invocation is referred to as a _____. (thủ tục gọi)
a. branch
b. stack frame
c. pop
d. push

27. Which ARM operation category includes logical instructions (AND, OR, XOR), add and subtract instructions, and test and compare instructions?
a. data-processing instructions
b. branch instructions
c. load and store instructions
d. extend instructions

28. In the ARM architecture only _____ instructions access memory locations.
a. data processing
b. status register access
c. load and store
d. branch

29. Which data type is defined in MMX?
a. packed byte
b. packed word
c. packed doubleword
d. all of the above

30. A branch instruction in which the branch is always taken is _____.
a. conditional branch
b. unconditional branch
c. jump
d. bi-endian

Chap 11:

1. The value of the mode field determines which addressing mode is to be used. (xác định địa chỉ sử dụng)
a. True
b. False

2. In a system without virtual memory, the effective address is a virtual address or a register.
a. True
b. False

3. The disadvantage of immediate addressing is that the size of the number is restricted to the size of the address field. (định địa chỉ - kích thước bị giới hạn)
a. True
b. False

4. With direct addressing, the length of the address field is usually less than the word length, thus limiting the address range.
a. True
b. False

5. Register addressing is similar to direct addressing with the only difference being that the address field refers to a register rather than a main memory address.
a. True
b. False

6. Register indirect addressing uses the same number of memory references as indirect addressing. (địa chỉ thanh ghi gián tiếp – cùng số - địa chị gián tiếp)
a. True
b. False

7. Three of the most common uses of stack addressing are relative addressing, base-register addressing, and indexing.
a. True
b. False

8. The method of calculating the EA is the same for both base-register addressing and indexing.
a. True
b. False

9. Typically an instruction set will include both preindexing and postindexing.
a. True
b. False

10. The x86 is equipped with a variety of addressing modes intended to allow the efficient execution of high-level languages.
a. True
b. False

11. The base with index and displacement mode sums the contents of the base register, the index register, and a displacement to form the effective address. (dịch chuyển thành địa chỉ hiệu quả)
a. True
b. False

12. The memory transfer rate has not kept up with increases in processor speed.
a. True
b. False

13. For addresses that reference memory the range of addresses that can be referenced is not related to the number of address bits. (địa chỉ tham chiếu ko liên quan bits địa chỉ)
a. True
b. False

14. The principal price to pay for variable-length instructions is an increase in the complexity of the processor.
a. True
b. False

15. One advantage of linking the addressing mode to the operand rather than the opcode is that any addressing mode can be used with any opcode.
a. True
b. False

16. The advantage of _____ is that no memory reference other than the instruction fetch is required to obtain the operand. (không tham chiếu bộ nhớ nào)
a. direct addressing (trực tiếp)
b. immediate addressing (ngay lập tức)
c. register addressing
d. stack addressing

17. The principal advantage of _____ addressing is that it is a very simple form of addressing.
a. displacement
b. register
c. stack
d. direct

18. _____ has the advantage of large address space, however it has the disadvantage of multiple memory references.
a. Indirect addressing
b. Direct addressing
c. Immediate addressing
d. Stack addressing

19. The advantages of _____ addressing are that only a small address field is needed in the instruction and no time-consuming memory references are required.
a. direct
b. indirect
c. register
d. displacement

20. _____ has the advantage of flexibility, but the disadvantage of complexity.
a. Stack addressing
b. Displacement addressing
c. Direct addressing
d. Register addressing

21. For _____, the address field references a main memory address and the referenced register contains a positive displacement from that address. (khoảng cách

địa chỉ)
a. indexing
b. base-register addressing
c. relative addressing
d. all of the above

22. Indexing performed after the indirection is _____. (lập chỉ mục thực hiện sau chuyển hướng)
a. relative addressing
b. autoindexing
c. postindexing
d. preindexing

23. For the _____ mode, the operand is included in the instruction. (toán hạng trong lệnh)
a. immediate
b. base
c. register
d. displacement

24. The only form of addressing for branch instructions is _____ addressing. (lệnh rẽ nhánh)
a. register
b. relative
c. base
d. immediate

25. Which of the following interrelated factors go into determining the use of the addressing bits? (liên quan sử dụng bits địa chỉ)
a. number of operands
b. number of register sets
c. address range
d. all of the above

26. _____ is a principle by which two variables are independent of each other.
a. Opcode
b. Orthogonality (trực giao)
c. Completeness (hoàn chỉnh)
d. Autoindexing (tự động)

27. The _____ was designed to provide a powerful and flexible instruction set within the constraints of a 16-bit minicomputer.
a. PDP-1
b. PDP-8
c. PDP-11
d. PDP-10

28. The _____ byte consists of three fields: the Scale field, the Index field and the Base field.
a. SIB
b. VAX
c. PDP-11
d. ModR/M

29. All instructions in the ARM architecture are _____ bits long and follow a regular format.
a. 8
b. 16
c. 32
d. 64

30. _____ is a design principle employed in designing the PDP-10 instruction set.
a. Orthogonality
b. Completeness
c. Direct addressing
d. All of the above

Chap 12:

1. The processor needs to store instructions and data temporarily while an instruction is being executed.
a. True
b. False

2. The control unit (CU) does the actual computation or processing of data.
a. True
b. False

3. Within the processor there is a set of registers that function as a level of memory above main memory and cache in the hierarchy.
a. True
b. False

4. Condition codes facilitate multiway branches. (tạo điều kiện)
a. True
b. False

5. The allocation of control information between registers and memory are not considered to be a key design issue. (không quan trọng)
a. True
b. False

6. Instruction pipelining is a powerful technique for enhancing performance but requires careful design to achieve optimum results with reasonable complexity.
a. True
b. False

7. The cycle time of an instruction pipeline is the time needed to advance a set of instructions one stage through the pipeline. (cần thiết)
a. True
b. False

8. A control hazard occurs when two or more instructions that are already in the pipeline need the same resource.
a. True
b. False

9. One of the major problems in designing an instruction pipeline is assuring a steady flow of instructions to the initial stages of the pipeline.(đảm bảo ổn định – giai đoạn đầu)
a. True
b. False

10. The predict-never-taken approach is the most popular of all the branch prediction methods.
a. True
b. False

11. It is possible to improve pipeline performance by automatically rearranging instructions within a program so that branch instructions occur later than actually desired. (kiểm soát lệnh rẽ nhánh – muộn hơn so với thực tế)
a. True
b. False

12. Interrupt processing allows an application program to be suspended in order that a variety of interrupt conditions can be serviced and later resumed. (dừng ctr – hoạt động lại sau)
a. True
b. False

13. An interrupt is generated from software and it is provoked by the execution of an instruction.
a. True
b. False

14. While the processor is in user mode the program being executed is unable to access protected system resources or to change mode, other than by causing an exception to occur. (chế độ người dùng – ko truy cập tài nguyên – trừ ngoại lệ)
a. True
b. False

15. The exception modes have full access to system resources and can change modes freely. (chế độ ngoại lệ)
a. True
b. False

16. _____ are a set of storage locations.
A. Processors
B. PSWs
C. Registers
D. Control units

17. The _____ controls the movement of data and instructions into and out of the processor.
A. control unit
B. ALU
C. shifter
D. branch

18. _____ registers may be used only to hold data and cannot be employed in the calculation of an operand address.
A. General purpose
B. Data
C. Address
D. Condition code

19. _____ are bits set by the processor hardware as the result of operations. (kết quả của hoạt động)
A. MIPS
B. Condition codes
C. Stacks
D. PSWs

20. The _____ contains the address of an instruction to be fetched. (chứa địa chỉ của lệnh sẽ được tìm nạp)
A. instruction register
B. memory address register
C. memory buffer register
D. program counter

21. The _____ contains a word of data to be written to memory or the word most recently read. (chứa được ghi vào bộ nhớ - đọc gần nhất)
A. MAR
B. PC
C. MBR
D. IR

22. The _____ determines the opcode and the operand specifiers. (giải)
A. decode instruction
B. fetch operands
C. calculate operands
D. execute instruction

23. _____ is a pipeline hazard.
A. Control
B. Resource
C. Data
D. All of the above

24. A _____ hazard occurs when there is a conflict in the access of an operand location. (rủi ro xung đột khi truy cập toán hạng)
A. resource
B. data
C. structural
D. control

25. A _____ is a small, very-high-speed memory maintained by the instruction fetch stage of the pipeline and containing the n most recently fetched instructions in sequence.
A. loop buffer
B. delayed branch
C. multiple stream
D. branch prediction

26. The _____ is a small cache memory associated with the instruction fetch stage of the pipeline. (liên kết tìm nạp lệnh)
A. dynamic branch
B. loop table
C. branch history table
D. flag

27. The _____ stage includes ALU operations, cache access, and register update.
A. decode
B. execute
C. fetch
D. write back

28. _____ is used for debugging.
A. Direction flag
B. Alignment check
C. Trap flag
D. Identification flag

29. The ARM architecture supports _____ execution modes.
A. 2
B. 8
C. 11
D. 7

30. The OS usually runs in _____.
A. supervisor mode
B. abort mode
C. undefined mode
D. fast interrupt mode

Chap 13:

1. Microprogramming eases the task of designing and implementing the control unit and provides support for the family concept.
a. True
b. False

2. Pipelining is a means of introducing parallelism into the essentially sequential nature of a machine-instruction program. (cơ chế song song vào bản chất tuần tự)
a. True
b. False

3. The major cost in the life cycle of a system is hardware.
a. True
b. False

4. It is common for programs, both system and application, to continue to exhibit new bugs after years of operation. (thường xuất hiện lỗi mới sau nhiều năm hoạt động)
a. True
b. False

5. Procedure calls and returns are not important aspects of HLL programs.
a. True
b. False

6. The register file is on the same chip as the ALU and control unit.
a. True
b. False

7. The register file employs much shorter addresses than addresses for cache and memory.
a. True
b. False

8. To handle any possible pattern of calls and returns the number of register windows would have to be unbounded. (Gọi thủ tục – cửa sổ đkí phải ko bị giới hạn)
a. True
b. False

9. Cache memory is a much faster memory than the register file.
a. True
b. False

10. The cache is capable of handling global as well as local variables.
(capable: khả năng)
a. True
b. False

11. When using graph coloring, nodes that share the same color cannot be assigned to the same register.
a. True
b. False

12. With simple, one cycle instructions, there is little or no need for microcode.
a. True
b. False

13. Almost all RISC instructions use simple register addressing.
a. True
b. False

14. RISC processors are more responsive to interrupts because interrupts are checked between rather elementary operations.
(phản ứng ngắt nhanh – ngắt kiểm tra giữa hoạt động cơ bản)
a. True
b. False

15. Unrolling can improve performance by increasing instruction parallelism by improving pipeline performance. (byby)
a. True
b. False

16. _____ determines the control and pipeline organization.
a. Calculation
b. Execution sequencing
c. Operations performed
d. Operands used

17. The Patterson study examined the dynamic behavior of _____ programs, independent of the underlying architecture. (hành vi động ctr – độc lập ktrúc cơ bản)
a. HLL
b. RISC
c. CISC
d. all of the above

18. _____ is the fastest available storage device.
a. Main memory
b. Cache
c. Register storage
d. HLL

19. The first commercial RISC product was _____. (thương mại đầu tiên)
a. SPARC
b. CISC
c. VAX
d. the Pyramid

20. _____ instructions are used to position quantities in registers temporarily for computational operations. (định vị đại lượng – cho việc tính toán)
a. Load-and-store
b. Window
c. Complex
d. Branch

21. Which stage is required for load and store operations?
a. I
b. E
c. D
d. all of the above

22. A _____ instruction can be used to account for data and branch delays. (dữ liệu và điều kiện delays)
a. SUB
b. NOOP
c. JUMP
d. all of the above

23. The instruction location immediately following the delayed branch is referred to as the _____. (vị trí)
a. delay load
b. delay file
c. delay slot
d. delay register

24. A tactic similar to the delayed branch is the _____, which can be used on LOAD instructions.
a. delayed load
b. delayed program
c. delayed slot
d. delayed register

25. The MIPS R4000 uses _____ bits for all internal and external data paths and for addresses, registers, and the ALU.
a. 16
b. 32
c. 64
d. 128

26. All MIPS R series processor instructions are encoded in a single _____ word format.
a. 4-bit
b. 8-bit
c. 16-bit
d. 32-bit

27. A _____ architecture is one that makes use of more, and more fine-grained pipeline stages. (sử dụng nhiều hơn – nhiều giai đoạn pipeline hơn)
a. parallel
b. superpipelined
c. superscalar
d. hybrid

28. The R4000 can have as many as _____ instructions in the pipeline at the same time.
a. 8
b. 10
c. 5
d. 3

29. SPARC refers to an architecture defined by _____.
a. Microsoft
b. Apple
c. Sun Microsystems
d. IBM

30. The R4000 pipeline stage where the instruction result is written back to the register file is the _____ stage.
a. write back
b. tag check
c. data cache
d. instruction execute