CEA 201 - Full

21 đang học ⭐ 4.8 (71 đánh giá)

Thuật ngữ trong học phần này (600)

D	The _____ enables the RAM chip to preposition bits to be placed on the data bus as rapidly as possible. A. Flash memory B. Hamming code C. RamBus D. Buffer
F	I/O channels are commonly seen on microcomputers, whereas I/O controllers are used on mainframes. (T/F)
F	With isolated I/O there is a single address space for memory locations and I/O devices. (T/F)
C	The _____ layer is the key to the operation of Thunderbolt and what makes it attractive as a high-speed peripheral I/O technology. A. cable B. application C. common transport D. physical

B	A _____ is a PLD featuring a general structure that allows very high logic capacity and offers more narrow logic resources and a higher ration of flip-flops to logic resources than do CPLDs. A. SPLD B. FPGA C. PAL D. PLA
F	A high-level language expresses operations in a basic form involving the movement of data to or from registers. (T/F)
A	_____ instructions are needed to transfer programs and data into memory and the results of computations back out to the user. A. I/O B. Transfer C. Control D. Branch
B	The entire set of parameters, including return address, which is stored for a procedure invocation is referred to as a _____. A. branch B. stack frame C. pop D. push
T	With direct addressing, the length of the address field is usually less than the word length, thus limiting the address range. (T/F)
F	Register indirect addressing uses the same number of memory references as indirect addressing. (T/F)
F	Three of the most common uses of stack addressing are relative addressing, base-register addressing, and indexing. (T/F)
T	The method of calculating the EA is the same for both base-register addressing and indexing. (T/F)
F	Typically an instruction set will include both preindexing and postindexing. (T/F)
T	The base with index and displacement mode sums the contents of the base register, the index register, and a displacement to form the effective address. (T/F)
F	For addresses that reference memory the range of addresses that can be referenced is not related to the number of address bits. (T/F)
B	The advantage of _____ is that no memory reference other than the instruction fetch is required to obtain the operand. A. direct addressing B. immediate addressing C. register addressing D. stack addressing

A	For the _____ mode, the operand is included in the instruction. A. immediate B. base C. register D. displacement
D	The only form of addressing for branch instructions is _____ addressing. A. register B. relative C. base D. immediate
B	_____ is a principle by which two variables are independent of each other. A. Opcode B. Orthogonality C. Completeness D. Autoindexing
C	The _____ was designed to provide a powerful and flexible instruction set within the constraints of a 16-bit minicomputer. A. PDP-1 B. PDP-8 C. PDP-11 D. PDP-10
A	The _____ byte consists of three fields: the Scale field, the Index field and the Base field. A. SIB B. VAX C. PDP-11 D. ModR/M
T	Interrupt processing allows an application program to be suspended in order that a variety of interrupt conditions can be serviced and later resumed. (T/F)
C	The _____ contains a word of data to be written to memory or the word most recently read. A. MAR B. PC C. MBR D. IR
A	The _____ determines the opcode and the operand specifiers. A. decode instruction B. fetch operands C. calculate operands D. execute instruction
A	A _____ is a small, very-high-speed memory maintained by the instruction fetch stage of the pipeline and containing the n most recently fetched instructions in sequence. A. loop buffer B. delayed branch C. multiple stream D. branch prediction

C	The _____ is a small cache memory associated with the instruction fetch stage of the pipeline. A. dynamic branch B. loop table C. branch history table D. flag
A	The OS usually runs in _____. A. supervisor mode B. abort mode C. undefined mode D. fast interrupt mode
F	When using graph coloring, nodes that share the same color cannot be assigned to the same register. (T/F)
A	The Patterson study examined the dynamic behavior of _____ programs, independent of the underlying architecture. A. HLL B. RISC C. CISC D. all of the above
D	The first commercial RISC product was _____. A. SPARC B. CISC C. VAX D. the Pyramid
A	_____ instructions are used to position quantities in registers temporarily for computational operations. A. Load-and-store B. Window C. Complex D. Branch
B	A _____ instruction can be used to account for data and branch delays. A. SUB B. NOOP C. JUMP D. all of the above
C	The instruction location immediately following the delayed branch is referred to as the _____. A. delay load B. delay file C. delay slot D. delay register
F	In the scalar organization there are multiple functional units, each of which is implemented as a pipeline and provides a degree of parallelism by virtue of its pipelined structure. (T/F)
F	Machine parallelism exists when instructions in a sequence are independent and thus can be executed in parallel by overlapping. (T/F)

A	_____ indicates whether this micro-op is scheduled for execution, has been dispatched for execution, or has completed execution and is ready for retirement. A. State B. Memory address C. Micro-op D. Alias register
A	_____ is determined by the number of instructions that can be fetched and executed at the same time and by the speed and sophistication of the mechanisms that the processor uses to find independent instructions. A. Machine parallelism B. Instruction-level parallelism C. Output dependency D. Procedural dependency
C	_____ is used in scalar RISC processors to improve the performance of instructions that require multiple cycles. A. In-order completion B. In-order issue C. Out-of-order completion D. Out-of-order issue
C	Utilizing a branch target buffer (BTB), the _____ uses a dynamic branch prediction strategy based on the history of recent executions of branch instructions. A. 486 B. Pentium C. Pentium 4 D. Pentium Pro
F	The main drawback of the bus organization is reliability.
T	An L1 cache that does not connect directly to the bus cannot engage in a snoopy protocol.
F	With a write-update protocol there can be multiple readers but only one writer at a time.
F	The function of switching applications and data resources over from a failed system to an alternative system in the cluster is referred to as failback.
T	The objective with NUMA is to maintain a transparent system wide memory while permitting multiple multiprocessor nodes, each with its own bus or other internal interconnect system.
F	Snoopy protocols are not suitable for a bus-based multiprocessor.
a	_____ causes results issuing from one functional unit to be fed immediately into another functional unit and so on. a.Chaining b.Rollover c.Passive standby d.Pipelining
a	With _____ instructions are simultaneously issued from multiple threads to the execution units of a superscalar processor. a.SMT b.single-threaded scalar c.coarse-grained multithreading d.chip multiprocessing

c	The _____ contains control fields, such as the vector count, that determine how many elements in the vector registers are to be processed. a.vector-mask register b.vector-activity count c.vector-status register d.vector-instruction register
d	Replicating the entire processor on a single chip with each processor handling separate threads is _____. a.interleaved multithreading b.blocked multithreading c.simultaneous multithreading d.chip multiprocessing
c	A _____ is a dispatchable unit of work within a process that includes a processor context and its own data area for a stack. a.process b.process switch c.thread d.thread switch
b	An operation that switches the processor from one process to another by saving all the process control data, register, and other information for the first and replacing them with the process information for the second is: a.resource ownership switch b.process switch c.thread switch d.cluster switch
c	Hardware-based solutions are generally referred to as cache coherence _____. a.clusters b.streams c.protocols d.vectors
a	A _____ problem arises when multiple copies of the same data can exist in different caches simultaneously, and if processors are allowed to update their own copies freely, an inconsistent view of memory can result. a.cache coherence b.cluster c.failover d.failback
b	With no multithreading, _____ is the simple pipeline found in traditional RISC and CISC machines. a.superscalar b.single-threaded scalar c.blocked multithreaded scalar d.interleaved multithreaded scalar
c	Uniprocessors fall into the _____ category of computer systems. a.MIMD b.SIMD c.SISD d.MISD

a	Vector and array processors fall into the _____ category of computer systems. a.SIMD b.SISD c.MISD d.MIMD
b	A taxonomy first introduced by _____ is still the most common way of categorizing systems with parallel processing capability. a.Randolph b.Flynn c.von Neuman d.Desai
T	Even if an individual application does not scale to take advantage of a large number of threads, it is still possible to gain from multicore architecture by running multiple instances of the application in parallel. (T/F)
F	With hybrid threading each major module is single threaded and the principal coordination involves synchronizing all the threads with a timeline thread. (T/F)
T	The ARM11 MPCore is an example of the L1 cache being divided into instruction and data caches. (T/F)
T	An advantage of using a shared L2 cache on the chip is that data shared by multiple cores is not replicated at the shared cache level. (T/F)
A	With _____, register banks are replicated so that multiple threads can share the use of pipeline resources. A. SMT B. pipelining C. scalar D. superscalar
B	One way to control power density is to use more of the chip area for _____. A. multicore B. cache memory C. silicon D. resistors
A	Lotus Domino or Siebel CRM are examples of _____ applications. A. threaded B. multi-process C. Java D. multi-instance
D	Oracle database, SAP, and PeopleSoft are examples of _____ applications. A. Java B. multithreaded native C. multi-instance D. multi-process

C	_____ applications that can benefit directly from multicore resources include application servers such as Sun's Java Application Server, BEA's Weblogic, IBM's Websphere, and the open-source Tomcat application server. A. Multi-instance B. Multi-process C. Java D. Threaded
A	Putting rendering on one processor, AI on another, and physics on another is an example of _____ threading. A. coarse B. multi-instance C. fine-grained D. hybrid
B	A loop that iterates over an array of data can be split up into a number of smaller parallel loops in individual threads that can be scheduled in parallel when using _____ threading. A. multi-process B. fine-grained C. hybrid D. coarse
D	The _____ is an example of splitting off a separate, shared L3 cache, with dedicated L1 and L2 caches for each core processor. A. IBM 370 B. ARM11 MPCore C. AMD Opteron D. Intel Core i7
C	The _____ connects to the external bus, known as the Front Side Bus, which connects to main memory, I/O controllers, and other processor chips. A. L2 B. APIC C. bus interface D. all of the above
B	The Intel Core i7-990X, introduced in 2008, implements ____ x86 SMT processors, each with a dedicated L2 cache, and with a shared L3 cache. A. 2 B. 4 C. 6 D. 8
B	Processors are called _____. A. dies B. cores C. QPI D. interconnects
A	The _____ feature enables moving dirty data from one CPU to another without writing to L2 and reading the data back in from external memory. A. migratory lines B. DDI C. VFP unit D. IPIs
F	A microprogrammed control unit is a relatively complex logic circuit.

F	The advantage of horizontal microinstructions is that they are more compact than vertical microinstructions, at the expense of a small additional amount of logic and time delay.
T	The degree of packing relates to the degree of identification between a given control task and specific microinstruction bits.
F	The PDP-11 is the first member of the LSI-11 family that was offered as a single board processor.
T	The TI 8800 Software Development Board is a microprogrammable 32-bit computer card that fits into an IBM PC-compatible host computer.
A	QN=1 The term microprogram was first coined by _____ in the early 1950s. a. M.V. Wilkes b. D. Siewiorek c. M. Sebern d. S. Tucker
A	QN=8 The terms _____ microprogramming are used to suggest the degree of closeness to the underlying control signals and hardware layout. a. hard/soft b. horizontal/vertical c. direct/indirect d. packed/unpacked
B	QN=9 With _____ encoding one field is used to determine the interpretation of another field. a. resource b. indirect c. direct d. functional
C	QN=11 The standard IBM 3033 control memory consists of _____ words. a. 2K b. 8K c. 4K d. 16K
F	Knowing the machine instruction set does not play a part in knowing the functions that the processor must perform.
F	The sequence of instruction cycles are always the same as the written sequence of instructions that make up the program.
T	All of the Pentium processors include two on-chip L1 caches, one for data and one for instructions. (T/F)
C	The Pentium 4 _____ component executes micro-operations, fetching the required data from the L1 data cache and temporarily storing results in registers. A. Fetch/decode unit B. Out-of-order execution logic C. Execution unit D. Memory subsystem
T	All DRAMs require a refresh operation. (T/F)

B	In a _____, binary values are stored using traditional flip-flop logic-gate configurations. A. ROM B. SRAM C. DRAM D. RAM
A	With _____ the microchip is organized so that a section of memory cells are erased in a single action. A. Flash memory B. SDRAM C. DRAM D. EEPROM
B	The _____ exchanges data with the processor synchronized to an external clock signal and running at the full speed of the processor/memory bus without imposing wait states. A. DDR-DRAM B. SDRAM C. CDRAM D. None of the above
A	_____ increases the data transfer rate by increasing the operational frequency of the RAM chip and by increasing the prefetch buffer from 2 bits to 4 bits per chip. A. DDR2 B. RDRAM C. CDRAM D. DDR3
A	Theoretically, a DDR module can transfer data at a clock rate in the range of _____ MHz. A. 200 to 600 B. 400 to 1066 C. 600 to 1400 D. 800 to 1600
B	A DDR3 module transfers data at a clock rate of _____ MHz. A. 600 to 1200 B. 800 to 1600 C. 1000 to 2000 D. 1500 to 3000
F	During a read or write operation, the head rotates while the platter beneath it stays stationary. (T/F)
F	The width of a track is double that of the head. (T/F)
T	There are typically hundreds of sectors per track and they may be either fixed or variable lengths. (T/F)
T	A bit near the center of a rotating disk travels past a fixed point slower than a bit on the outside. (T/F)
F	The disadvantage of using CAV is that individual blocks of data can only be directly addressed by track and sector. (T/F)

C	Greater ability to withstand shock and damage, improvement in the uniformity of the magnet film surface to increase disk reliability, and a significant reduction in overall surface defects to help reduce read-write errors, are all benefits of _____. a. magnetic read and write mechanisms b. platters c. the glass substrate d. a solid state drive
B	The disadvantage of _____ is that the amount of data that can be stored on the long outer tracks is only the same as what can be stored on the short inner tracks. a. SSD b. CAV c. ROM d. CLV
A	The sum of the seek time and the rotational delay equals the _____, which is the time it takes to get into position to read or write. a. access time b. gap time c. transfer time d. constant angular velocity
C	_____ is when the disk rotates more slowly for accesses near the outer edge than for those near the center. a. Constant angular velocity (CAV) b. Magnetoresistive c. Constant linear velocity (CLV) d. Seek time
T	The disadvantage of the software poll is that it is time consuming. (T/F)
F	With a daisy chain the processor just picks the interrupt line with the highest priority. (T/F)
F	The rotating interrupt mode allows the processor to inhibit interrupts from certain devices. (T/F)
F	A multipoint external interface provides a dedicated line between the I/O module and the external device. (T/F)
B	The _____ contains logic for performing a communication function between the peripheral and the bus. A. I/O channel B. I/O module C. I/O processor D. I/O command
C	The I/O function includes a _____ requirement to coordinate the flow of traffic between internal resources and external devices. A. cycle B. status reporting C. control and timing D. data

A	An I/O module that takes on most of the detailed processing burden, presenting a high-level interface to the processor, is usually referred to as an _____. A. I/O channel B. I/O command C. I/O controller D. device controller
D	The Thunderbolt protocol _____ layer is responsible for link maintenance including hot-plug detection and data encoding to provide highly efficient data transfer. A. cable B. application C. common transport D. physical
B	The _____ contains I/O protocols that are mapped on to the transport layer. A. cable B. application C. common transport D. physical
A	A _____ is used to connect storage systems, routers, and other peripheral devices to an InfiniBand switch. A. target channel adapter B. InfiniBand switch C. host channel adapter D. subnet
D	A _____ connects InfiniBand subnets, or connects an InfiniBand switch to a network such as a local area network, wide area network, or storage area network. A. memory controller B. TCA C. HCA D. router
T	Privileged instructions are certain instructions that are designated special and can be executed only by the monitor. (T/F)
F	With demand paging it is necessary to load an entire process into main memory. (T/F)
C	A _____ is a collection of memory regions. A. APX B. nucleus C. domain D. page table
B	The OS maintains a _____ for each process that shows the frame location for each page of the process. A. kernel B. page table C. TLB D. logical address
T	One drawback of sign-magnitude representation is that there are two representations of 0.
F	For base 2 representation, a normal number is one in which the most significant bit of the significand is zero.
F	Overflow is a less serious problem because the result can generally be satisfactorily approximated by 0.

sign extension	Moving the sign bit to the new leftmost position and filling in with copies of the sign bit is called _____. a. sign extension b. range extension c. bit extension d. partial extension
Subnormal numbers	_____ are included in IEEE 754 to handle cases of exponent underflow. a. Subnormal numbers b. Guard bits c. Normal numbers d. Radix points
F	Claude Shannon, a research assistant in the Electrical Engineering Department at M.I.T., proposed the basic principles of Boolean algebra. (T/F)
F	Logical functions are implemented by the interconnection of decoders. (T/F)
A	A _____ is an electronic circuit that produces an output signal that is a simple Boolean operation on its input signals. A. gate B. decoder C. counter D. flip-flop
D	Which of the following is a functionally complete set? A. AND, NOT B. NOR C. AND, OR, NOT D. all of the above
B	For more than four variables an alternative approach is a tabular technique referred to as the _____ method. A. DeMorgan B. Quine-McCluskey C. Karnaugh map D. Boole-Shannon
A	_____ are used in digital circuits to control signal and data routing. A. Multiplexers B. Program counters C. Flip-flops D. Gates
C	_____ is implemented with combinational circuits. A. Nano memory B. Random access memory C. Read only memory D. No memory
B	A _____ accepts and/or transfers information serially. A. S-R latch B. shift register C. FPGA D. parallel register

C	Counters can be designated as _____. A. asynchronous B. synchronous C. both asynchronous and synchronous D. neither asynchronous or synchronous
A	The _____ table provides the value of the next output when the inputs and the present output are known, which is exactly the information needed to design the counter or any sequential circuit. A. excitation B. Kenough C. J-K flip-flop D. FPGA
T	The operation to be performed is specified by a binary code known as the operation code. (T/F)
T	The instruction set is the programmer's means of controlling the processor. (T/F)
F	Not all machine languages include numeric data types. (T/F)
B	A(n) _____ expresses operations in a concise algebraic form using variables. A. opcode B. high-level language C. machine language D. register
D	_____ instructions provide computational capabilities for processing number data. A. Boolean B. Logic C. Memory D. Arithmetic
C	The x86 data type that is a signed binary value contained in a byte, word, or doubleword, using twos complement representation is _____. A. general B. ordinal C. integer D. packed BCD
A	The _____ instruction includes an implied address. A. skip B. rotate C. stack D. push
D	Which of the following is a true statement? A. a procedure can be called from more than one location B. a procedure call can appear in a procedure C. each procedure call is matched by a return in the called program D. all of the above
A	Which ARM operation category includes logical instructions (AND, OR, XOR), add and subtract instructions, and test and compare instructions? A. data-processing instructions B. branch instructions C. load and store instructions D. extend instructions

C	In the ARM architecture only _____ instructions access memory locations. A. data processing B. status register access C. load and store D. branch
D	Which data type is defined in MMX? A. packed byte B. packed word C. packed doubleword D. all of the above
B	A branch instruction in which the branch is always taken is _____. A. conditional branch B. unconditional branch C. jump D. bi-endian
T	The value of the mode field determines which addressing mode is to be used. (T/F)
F	In a system without virtual memory, the effective address is a virtual address or a register. (T/F)
T	The disadvantage of immediate addressing is that the size of the number is restricted to the size of the address field. (T/F)
T	Register addressing is similar to direct addressing with the only difference being that the address field refers to a register rather than a main memory address. (T/F)
T	The x86 is equipped with a variety of addressing modes intended to allow the efficient execution of high-level languages. (T/F)
T	The memory transfer rate has not kept up with increases in processor speed. (T/F)
T	The principal price to pay for variable-length instructions is an increase in the complexity of the processor. (T/F)
T	One advantage of linking the addressing mode to the operand rather than the opcode is that any addressing mode can be used with any opcode. (T/F)
D	The principal advantage of _____ addressing is that it is a very simple form of addressing. A. displacement B. register C. stack D. direct
A	_____ has the advantage of large address space, however it has the disadvantage of multiple memory references. A. Indirect addressing B. Direct addressing C. Immediate addressing D. Stack addressing

C	The advantages of _____ addressing are that only a small address field is needed in the instruction and no time-consuming memory references are required. A. direct B. indirect C. register D. displacement
B	_____ has the advantage of flexibility, but the disadvantage of complexity. A. Stack addressing B. Displacement addressing C. Direct addressing D. Register addressing
A	For _____, the address field references a main memory address and the referenced register contains a positive displacement from that address. A. indexing B. base-register addressing C. relative addressing D. all of the above
C	Indexing performed after the indirection is _____. A. relative addressing B. autoindexing C. postindexing D. preindexing
D	Which of the following interrelated factors go into determining the use of the addressing bits? A. number of operands B. number of register sets C. address range D. all of the above
C	All instructions in the ARM architecture are _____ bits long and follow a regular format. A. 8 B. 16 C. 32 D. 64
D	_____ is a design principle employed in designing the PDP-10 instruction set. A. Orthogonality B. Completeness C. Direct addressing D. All of the above
T	The processor needs to store instructions and data temporarily while an instruction is being executed. (T/F)
F	The control unit (CU) does the actual computation or processing of data. (T/F)
T	Within the processor there is a set of registers that function as a level of memory above main memory and cache in the hierarchy. (T/F)
T	Condition codes facilitate multiway branches. (T/F)

F	The allocation of control information between registers and memory are not considered to be a key design issue. (T/F)
T	Instruction pipelining is a powerful technique for enhancing performance but requires careful design to achieve optimum results with reasonable complexity. (T/F)
T	The cycle time of an instruction pipeline is the time needed to advance a set of instructions one stage through the pipeline. (T/F)
F	A control hazard occurs when two or more instructions that are already in the pipeline need the same resource. (T/F)
T	One of the major problems in designing an instruction pipeline is assuring a steady flow of instructions to the initial stages of the pipeline. (T/F)
T	The predict-never-taken approach is the most popular of all the branch prediction methods. (T/F)
T	It is possible to improve pipeline performance by automatically rearranging instructions within a program so that branch instructions occur later than actually desired. (T/F)
F	An interrupt is generated from software and it is provoked by the execution of an instruction. (T/F)
T	While the processor is in user mode the program being executed is unable to access protected system resources or to change mode, other than by causing an exception to occur. (T/F)
T	The exception modes have full access to system resources and can change modes freely. (T/F)
C	_____ are a set of storage locations. A. Processors B. PSWs C. Registers D. Control units
A	The _____ controls the movement of data and instructions into and out of the processor. A. control unit B. ALU C. shifter D. branch
B	_____ registers may be used only to hold data and cannot be employed in the calculation of an operand address. A. General purpose B. Data C. Address D. Condition code

B	_____ are bits set by the processor hardware as the result of operations. A. MIPS B. Condition codes C. Stacks D. PSWs
D	The _____ contains the address of an instruction to be fetched. A. instruction register B. memory address register C. memory buffer register D. program counter
D	_____ is a pipeline hazard. A. Control B. Resource C. Data D. All of the above
B	A _____ hazard occurs when there is a conflict in the access of an operand location. A. resource B. data C. structural D. control
B	The _____ stage includes ALU operations, cache access, and register update. A. decode B. execute C. fetch D. write back
C	_____ is used for debugging. A. Direction flag B. Alignment check C. Trap flag D. Identification flag
D	The ARM architecture supports _____ execution modes. A. 2 B. 8 C. 11 D. 7
T	Microprogramming eases the task of designing and implementing the control unit and provides support for the family concept. (T/F)
T	Pipelining is a means of introducing parallelism into the essentially sequential nature of a machine-instruction program. (T/F)
F	The major cost in the life cycle of a system is hardware. (T/F)
T	It is common for programs, both system and application, to continue to exhibit new bugs after years of operation. (T/F)
F	Procedure calls and returns are not important aspects of HLL programs. (T/F)

T	The register file employs much shorter addresses than addresses for cache and memory. (T/F)
T	To handle any possible pattern of calls and returns the number of register windows would have to be unbounded. (T/F)
F	Cache memory is a much faster memory than the register file. (T/F)
T	The cache is capable of handling global as well as local variables. (T/F)
T	With simple, one cycle instructions, there is little or no need for microcode. (T/F)
T	Almost all RISC instructions use simple register addressing. (T/F)
T	RISC processors are more responsive to interrupts because interrupts are checked between rather elementary operations. (T/F)
T	Unrolling can improve performance by increasing instruction parallelism by improving pipeline performance. (T/F)
B	_____ determines the control and pipeline organization. A. Calculation B. Execution sequencing C. Operations performed D. Operands used
C	_____ is the fastest available storage device. A. Main memory B. Cache C. Register storage D. HLL
D	Which stage is required for load and store operations? A. I B. E C. D D. all of the above
A	A tactic similar to the delayed branch is the _____, which can be used on LOAD instructions. A. delayed load B. delayed program C. delayed slot D. delayed register
D	All MIPS R series processor instructions are encoded in a single _____ word format. A. 4-bit B. 8-bit C. 16-bit D. 32-bit

B	A _____ architecture is one that makes use of more, and more fine-grained pipeline stages. A. parallel B. superpipelined C. superscalar D. hybrid
A	The R4000 can have as many as _____ instructions in the pipeline at the same time. A. 8 B. 10 C. 5 D. 3
C	SPARC refers to an architecture defined by _____. A. Microsoft B. Apple C. Sun Microsystems D. IBM
A	The R4000 pipeline stage where the instruction result is written back to the register file is the _____ stage. A. write back B. tag check C. data cache D. instruction execute
T	The superscalar approach has now become the standard method for implementing high-performance microprocessors. (T/F)
T	In a traditional scalar organization there is a single pipelined functional unit for integer operations and one for floating-point operations. (T/F)
T	The superscalar approach depends on the ability to execute multiple instructions in parallel. (T/F)
T	True data dependency is also called flow dependency or read after write (RAW) dependency. (T/F)
T	Resources include: memories, caches, buses, and register-file ports. (T/F)
T	The simplest instruction issue policy is to issue instructions in the exact order that would be achieved by sequential execution (in-order issue) and to write results in that same order (in-order completion). (T/F)
T	In-order completion requires more complex instruction issue logic than out-of-order completion. (T/F)
T	The reorder buffer is temporary storage for results completed out of order that are then committed to the register file in program order. (T/F)
T	Register renaming eliminates antidependencies and output dependencies. (T/F)

T	In effect, the Pentium 4 architecture implements a CISC instruction set architecture on a RISC microarchitecture. (T/F)
T	The schedulers are responsible for retrieving micro-ops from the micro-op queues and dispatching these for execution. (T/F)
F	ARM architecture has yet to implement superscalar techniques in the instruction pipeline. (T/F)
T	The Cortex-A8 targets a wide variety of mobile and consumer applications including mobile phones, set-top boxes, gaming consoles and automotives navigation/entertainment systems. (T/F)
D	The superscalar approach can be used on _____ architecture. A. RISC B. CISC C. neither RISC nor CISC D. both RISC and CISC
C	The essence of the _____ approach is the ability to execute instructions independently and concurrently in different pipelines. A. scalar B. branch C. superscalar D. flow dependency
D	Which of the following is a fundamental limitation to parallelism with which the system must cope? A. procedural dependency B. resource conflicts C. antidependency D. all of the above
A	The situation where the second instruction needs data produced by the first instruction to execute is referred to as _____. A. true data dependency B. output dependency C. procedural dependency D. antidependency
B	The instructions following a branch have a _____ on the branch and cannot be executed until the branch is executed. A. resource dependency B. procedural dependency C. output dependency D. true data dependency
A	_____ refers to the process of initiating instruction execution in the processor's functional units. A. Instruction issue B. In-order issue C. Out-of-order issue D. Procedural issue

C	Instead of the first instruction producing a value that the second instruction uses, with _____ the second instruction destroys a value that the first instruction uses. A. in-order issue B. resource conflict C. antidependency D. out-of-order completion
B	_____ exists when instructions in a sequence are independent and thus can be executed in parallel by overlapping. A. Flow dependency B. Instruction-level parallelism C. Machine parallelism D. Instruction issue
D	_____ is a protocol used to issue instructions. A. Micro-ops B. Scalar C. SIMD D. Instruction issue policy
D	Which of the following is a hardware technique that can be used in a superscalar processor to enhance performance? A. duplication of resources B. out-of-order issue C. renaming D. all of the above
T	Symmetric multiprocessors (SMPs) are one of the earliest, and still the most common, example of parallel organization.
T	The key to the design of a supercomputer or array processor is to recognize that the main task is to perform arithmetic operations on arrays or vectors of floating-point numbers.
T	The term SMP refers to a computer hardware architecture and also to the operating system behavior that reflects that architecture.
T	With multithreading the instruction stream is divided into several smaller streams, known as threads, such that the threads can be executed in parallel.
T	An attractive feature of an SMP is that the existence of multiple processors is transparent to the user.
T	The most important measure of performance for a processor is the rate at which it executes instructions.
T	An SMP operating system manages processor and other computer resources so that the user perceives a single operating system controlling system resources.
T	Software cache coherence schemes attempt to avoid the need for additional hardware circuitry and logic by relying on the compiler and operating system to deal with the problem.
T	Both clusters and symmetric multiprocessors provide a configuration with multiple processors to support high-demand applications.
a	A _____ is an instance of a program running on a computer. a.process b.process switch c.thread d.thread switch

b	SMPs, clusters, and NUMA systems fit into the _____ category of computer systems. a.SISD b.MIMD c.SIMD d.MISD
d	Which of the following is an approach to vector computation? a.pipelined ALU b.parallel ALU's c.parallel processors d.all of the above
T	The organizational changes in processor design have primarily been focused on increasing instruction-level parallelism so that more work could be done in each clock cycle. (T/F)
T	With superscalar organization increased performance can be achieved by increasing the number of parallel pipelines. (T/F)
T	The increasingly difficult engineering challenge related to processor logic is one of the reasons that an increasing fraction of the processor chip is devote to the simpler memory logic. (T/F)
F	The demand on power requirements has not grown as chip density and clock frequency have risen. (T/F)
F	As chip transistor density has increased, the percentage of chip area devoted to memory has decreased. (T/F)
T	The potential performance benefits of a multicore organization depend on the ability to effectively exploit the parallel resources available to the application. (T/F)
T	Database management systems and database applications are one area in which multicore systems can be used effectively. (T/F)
T	A potential advantage to having only dedicate L2 caches on the chip is that each core enjoys more rapid access to its private L2 cache. (T/F)
T	The thermal management unit monitors digital sensors for high-accuracy die temperature measurements. (T/F)
F	The Advanced Programmable Interrupt controller (APIC) monitors thermal conditions and CPU activity and adjusts voltage levels and power consumption appropriately. (T/F)
T	A multicore computer combines two or more processors on a single piece of silicon. (T/F)

D	_____ is where individual instructions are executed through a pipeline of stages so that while one instruction is executing in one stage of the pipeline, another instruction is executing in another stage of the pipeline. A. Superscalar B. Scalar C. Pipelining D. Simultaneous multithreading
B	_____ is when multiple pipelines are constructed by replicating execution resources, enabling parallel execution of instructions in parallel pipelines so long as hazards are avoided. A. Vectoring B. Superscalar C. Hybrid multithreading D. Pipelining
C	The _____ is responsible for maintaining coherency among L1 data caches. A. VFP unit B. distributed interrupt controller C. snoop control unit (SCU) D. watchdog
T	A microprogram consists of a sequence of instructions in a microprogramming language.
T	Microprogramming became a popular technique for implementing the control unit of CISC processors.
F	To implement a control unit as an interconnection of basic logic elements is a very simple task.
T	A microprogram is midway between hardware and software.
F	It is easier to design in hardware than in firmware.
T	It is more difficult to write a firmware program than a software program.
T	Reading a microinstruction from the control memory is the same as executing that microinstruction.
T	The principal advantage of the use of microprogramming to implement a control unit is that it simplifies the design of the control unit.
T	The principal disadvantage of a microprogrammed unit is that it will be somewhat slower than a hardwired unit of comparable technology.
T	It is important to design compact, time-efficient techniques for microinstruction branching.
B	QN=3 The _____ contains the address of the next microinstruction to be read. a. control memory b. control address register c. control word d. control buffer register
A	QN=4 When a microinstruction is read from the control memory it is transferred to a _____. a. control buffer register b. control memory c. control address register d. control unit

D	QN=5 Which of the following is a control unit input? a. IR b. ALU flags c. clock d. all of the above
C	QN=7 The terms _____ relate to the relative width of microinstructions. a. packed/unpacked b. hard/soft c. horizontal/vertical d. direct/indirect
D	QN=10 Which of the following is a LSI-11 microinstruction? a. add word b. test word c. Jump d. all of the above
A	QN=12 The _____ allows multiple levels of nested calls or interrupts and it can be used to support branching and looping. a. stack b. register c. counter d. firmware
B	QN=13 The _____ is a 32-bit ALU with 64 registers that can be configured to operate as four 8-bit ALUs, two 16-bit ALUs, or a single 32-bit ALU. a. PDP-11 b. 8832 c. 3033 d. 8818
A	QN=14 _____ is a subfield that is used to indicate a conditional branch. a. ZERION b. S2-S0 c. SELDR d. OSEL
C	QN=15 A _____ is a combinatorial circuit that generates an address based on the microinstruction, the machine instruction, the microinstruction program counter, and an interrupt register. a. microsequencer b. vertical microinstruction c. translation array d. control word
T	A cycle is made up of a sequence of micro-operations.
T	One technique for implementing a control unit is referred to as hardwired implementation, in which the control unit is a combinatorial circuit.
T	The control unit controls the operation of the processor.
T	The execution of a program consists of the sequential execution of instructions.
T	There is a tremendous variety of products, from single-chip microcomputers costing a few dollars to supercomputers costing tens of millions of dollars that can rightly claim the name "computer". (T/F)
F	The variety of computer products is exhibited only in cost. (T/F)

F	Computer organization refers to attributes of a system visible to the programmer. (T/F)
F	Changes in computer technology are finally slowing down. (T/F)
T	The textbook for this course is about the structure and function of computers. (T/F)
T	The number of bits used to represent various data types is an example of an architectural attribute. (T/F)
T	Interfaces between the computer and peripherals is an example of an organizational attribute. (T/F)
F	Historically the distinction between architecture and organization has not been an important one. (T/F)
T	A particular architecture may span many years and encompass a number of different computer models, its organization changing with changing technology. (T/F)
F	A microcomputer architecture and organization relationship is not very close. (T/F)
T	Changes in technology not only influence organization but also result in the introduction of more powerful and more complex architectures. (T/F)
T	The hierarchical nature of complex systems is essential to both their design and their description. (T/F)
T	Both the structure and functioning of a computer are, in essence, simple. (T/F)
T	A computer must be able to process, store, move, and control data. (T/F)
F	When data are moved over longer distances, to or from a remote device, the process is known as data transport. (T/F)
C	Computer technology is changing at a _____ pace. A. Slow B. Slow to medium C. Rapid D. Non-existent
D	Computer _____ refers to those attributes that have a direct impact on the logical execution of a program. A. Organization B. Specifics C. Design D. Architecture
A	Architectural attributes include _____ . A. I/O mechanisms B. Control signals C. Interfaces D. Memory technology used

B	_____ attributes include hardware details transparent to the programmer. A. Interface B. Organizational C. Memory D. Architectural
A	It is a(n) _____ design issue whether a computer will have a multiply instruction. A. Architectural B. Memory C. Elementary D. Organizational
D	It is a(n) _____ issue whether the multiply instruction will be implemented by a special multiply unit or by a mechanism that makes repeated use of the add unit of the system. A. Architectural B. Memory C. Mechanical D. Organizational
B	A _____ system is a set of interrelated subsystems. A. Secondary B. Hierarchical C. Complex D. Functional
C	An I/O device is referred to as a _____. A. CPU B. Control device C. Peripheral D. Register
A	When data are moved over longer distances, to or from a remote device, the process is known as _____. A. Data communications B. Registering C. Structuring D. Data transport
C	The _____ stores data. A. System bus B. I/O C. Main memory D. Control unit
B	The _____ moves data between the computer and its external environment. A. Data transport B. I/O C. Register D. CPU interconnection
B	A common example of system interconnection is by means of a _____. A. Register B. System bus C. Data transport D. Control device

A	A _____ is a mechanism that provides for communication among CPU, main memory, and I/O. A. System interconnection B. CPU interconnection C. Peripheral D. Processor
D	_____ provide storage internal to the CPU. A. Control units B. ALUs C. Main memory D. Registers
C	The _____ performs the computer's data processing functions. A. Register B. CPU interconnection C. ALU D. System bus
F	The world's first general-purpose electronic digital computer was designed and constructed at The Ohio State University. (T/F)
T	John Mauchly and John Eckert designed the ENIAC. (T/F)
F	The major drawback of the EDVAC was that it had to be programmed manually by setting switches and plugging and unplugging cables. (T/F)
T	The IAS is the prototype of all subsequent general-purpose computers. (T/F)
T	The IAS operates by repetitively performing an instruction cycle. (T/F)
T	Backward compatible means that the programs written for the older machines can be executed on the new machine. (T/F)
F	A vacuum tube is a solid-state device made from silicon. (T/F)
T	Computers are classified into generations based on the fundamental hardware technology employed. (T/F)
F	System software was introduced in the third generation of computers. (T/F)
T	A wafer is made of silicon and is broken up into chips which consists of many gates and/or memory cells plus a number of input and output attachment points. (T/F)
T	IBM's System/360 was the industry's first planned family of computers. (T/F)
T	Intel's 4004 was the first chip to contain all of the components of a CPU on a single chip. (T/F)
T	Designers wrestle with the challenge of balancing processor performance with that of main memory and other computer components. (T/F)

F	The Intel x86 evolved from RISC design principles and is used in embedded systems. (T/F)
F	A common measure of performance for a processor is the rate at which instructions are executed, expressed as billions of instructions per seconds (BIPS). (T/F)
C	The _____ was the world's first general-purpose electronic digital computer. A. UNIVAC B. MARK IV C. ENIAC D. Hollerith's Counting Machine
D	The Electronic Numerical Integrator and Computer project was a response to U.S. needs during _____. A. The Civil War B. The French-American War C. World War I D. World War II
A	The ENIAC used _____. A. Vacuum tubes B. Integrated circuits C. IAS D. Transistors
A	The ENIAC is an example of a _____ generation computer. A. First B. Second C. Third D. Fourth
B	The _____ interprets the instructions in memory and causes them to be executed. A. Main memory B. Control unit C. I/O D. Arithmetic and logic unit
D	The memory of the IAS consists of 1000 storage locations called _____. A. Opcodes B. Wafers C. VLSIs D. Words
C	The _____ contains the 8-bit opcode instruction being executed. A. Memory buffer register B. Instruction buffer register C. Instruction register D. Memory address register
B	During the _____ the opcode of the next instruction is loaded into the IR and the address portion is loaded into the MAR. A. Execute cycle B. Fetch cycle C. Instruction cycle D. Clock cycle

B	Second generation computers used _____. A. Integrated circuits B. Transistors C. Vacuum tubes D. Large-scale integration
A	The _____ defines the third generation of computers. A. Integrated circuit B. Vacuum tube C. Transistor D. VLSI
A	The use of multiple processors on the same chip is referred to as _____ and provides the potential to increase performance without increasing the clock rate. A. Multicore B. GPU C. Data channels D. MPC
D	With the _____, Intel introduced the use of superscalar techniques that allow multiple instructions to execute in parallel. A. Core B. 8080 C. 80486 D. Pentium
B	The _____ measures the ability of a computer to complete a single task. A. Clock speed B. Speed metric C. Execute cycle D. Cycle time
D	ARM processors are designed to meet the needs of _____. A. Embedded real-time systems B. Application platforms C. Secure applications D. All of the above
A	One increment, or pulse, of the system clock is referred to as a _____. A. Clock tick B. Cycle time C. Clock rate D. Cycle speed
T	At a top level, a computer consists of CPU, memory, and I/O components. (T/F)
T	The basic function of a computer is to execute programs. (T/F)
T	Program execution consists of repeating the process of instruction fetch and instruction execution. (T/F)
F	Interrupts do not improve processing efficiency. (T/F)
F	An I/O module cannot exchange data directly with the processor. (T/F)
F	A key characteristic of a bus is that it is not a shared transmission medium. (T/F)

T	Computer systems contain a number of different buses that provide pathways between components at various levels of the computer system hierarchy. (T/F)
T	In general, the more devices attached to the bus, the greater the bus length and hence the greater the propagation delay. (T/F)
F	It is not possible to connect I/O controllers directly onto the system bus. (T/F)
T	The method of using the same lines for multiple purposes is known as time multiplexing. (T/F)
T	Timing refers to the way in which events are coordinated on the bus. (T/F)
F	With asynchronous timing the occurrence of events on the bus is determined by a clock. (T/F)
T	Because all devices on a synchronous bus are tied to a fixed clock rate, the system cannot take advantage of advances in device performance. (T/F)
F	The unit of transfer at the link layer is a phit and the unit transfer at the physical layer is a flit. (T/F)
T	A key requirement for PCIe is high capacity to support the needs of higher data rate I/O devices such as Gigabit Ethernet. (T/F)
B	Virtually all contemporary computer designs are based on concepts developed by _____ at the Institute for Advanced Studies, Princeton. A. John Maulchy B. John von Neumann C. Herman Hollerith D. John Eckert
D	The von Neumann architecture is based on which concept? A. Data and instructions are stored in a single read-write memory B. The contents of this memory are addressable by location C. Execution occurs in a sequential fashion D. All of the above
A	A sequence of codes or instructions is called _____. A. Software B. Memory C. An interconnect D. A register
C	The processing required for a single instruction is called a(n) _____ cycle. A. Execute B. Fetch C. Instruction D. Packet
B	A(n) _____ is generated by a failure such as power failure or memory parity error. A. I/O interrupt B. Hardware failure interrupt C. Timer interrupt D. Program interrupt

C	A(n) _____ is generated by some condition that occurs as a result of an instruction execution. A. Timer interrupt B. I/O interrupt C. Program interrupt D. Hardware failure interrupt
D	The interconnection structure must support which transfer? A. Memory to processor B. Processor to memory C. I/O to or from memory D. All of the above
A	A bus that connects major computer components (processor, memory, I/O) is called a _____. A. System bus B. Address bus C. Data bus D. Control bus
D	The _____ are used to designate the source or destination of the data on the data bus. A. System lines B. Data lines C. Control lines D. Address lines
C	The data lines provide a path for moving data among system modules and are collectively called the _____. A. Control bus B. Address bus C. Data bus D. System bus
B	A _____ is the high-level set of rules for exchanging packets of data between devices. A. Bus B. Protocol C. Packet D. QPI
A	Each data path consists of a pair of wires (referred to as a _____) that transmits data one bit at a time. A. Lane B. Path C. Line D. Bus
A	The _____ receives read and write requests from the software above the TL and creates request packets for transmission to a destination via the link layer. A. Transaction layer B. Root layer C. Configuration layer D. Transport layer
D	The TL supports which of the following address spaces? A. Memory B. I/O C. Message D. All of the above

C	The QPI _____ layer is used to determine the course that a packet will traverse across the available system interconnects. A. Link B. Protocol C. Routing D. Physical
T	No single technology is optimal in satisfying the memory requirements for a computer system. (T/F)
T	A typical computer system is equipped with a hierarchy of memory subsystems, some internal to the system and some external. (T/F)
F	External memory is often equated with main memory. (T/F)
T	The processor requires its own local memory. (T/F)
F	Cache is not a form of internal memory. (T/F)
F	The unit of transfer must equal a word or an addressable unit. (T/F)
T	Both sequential access and direct access involve a shared read-write mechanism. (T/F)
T	In a volatile memory, information decays naturally or is lost when electrical power is switched off. (T/F)
T	To achieve greatest performance the memory must be able to keep up with the processor. (T/F)
F	Secondary memory is used to store program and data files and is usually visible to the programmer only in terms of individual bytes or words. (T/F)
F	The L1 cache is slower than the L3 cache. (T/F)
T	With write back updates are made only in the cache. (T/F)
T	It has become possible to have a cache on the same chip as the processor. (T/F)
F	Cache design for HPC is the same as that for other hardware platforms and applications. (T/F)
A	_____ refers to whether memory is internal or external to the computer. A. Location B. Access C. Hierarchy D. Tag

C	Internal memory capacity is typically expressed in terms of _____. A. Hertz B. Nanos C. Bytes D. LOR
B	For internal memory, the _____ is equal to the number of electrical lines into and out of the memory module. A. Access time B. Unit of transfer C. Capacity D. Memory ratio
A	"Memory is organized into records and access must be made in a specific linear sequence" is a description of _____. A. Sequential access B. Direct access C. Random access D. Associative
C	individual blocks or records have a unique address based on physical location with _____. A. Associative B. Physical access C. Direct access D. Sequential access
D	For random-access memory, _____ is the time from the instant that an address is presented to the memory to the instant that data have been stored or made available for use. A. Memory cycle time B. Direct access C. Transfer rate D. Access time
B	The _____ consists of the access time plus any additional time required before a second access can commence. A. Latency B. Memory cycle time C. Direct access D. Transfer rate
A	A portion of main memory used as a buffer to hold data temporarily that is to be read out to disk is referred to as a _____. A. Disk cache B. Latency C. Virtual address D. Miss
C	A line includes a _____ that identifies which particular block is currently being stored. A. Cache B. Hit C. Tag D. Locality

A	_____ is the simplest mapping technique and maps each block of main memory into only one possible cache line. A. Direct mapping B. Associative mapping C. Set associative mapping D. None of the above
C	When using the _____ technique all write operations made to main memory are made to the cache as well. A. Write back B. LRU C. Write through D. Unified cache
B	The key advantage of the _____ design is that it eliminates contention for the cache between the instruction fetch/decode unit and the execution unit. A. Logical cache B. Split cache C. Unified cache D. Physical cache
A	In reference to access time to a two-level memory, a _____ occurs if an accessed word is not found in the faster memory. A. Miss B. Hit C. Line D. Tag
B	A logical cache stores data using _____. A. Physical addresses B. Virtual addresses C. Random addresses D. None of the above
T	The basic element of a semiconductor memory is the memory cell. (T/F)
F	A characteristic of ROM is that it is volatile. (T/F)
T	RAM must be provided with a constant power supply. (T/F)
T	The two traditional forms of RAM used in computers are DRAM and SRAM. (T/F)
T	A static RAM will hold its data as long as power is supplied to it. (T/F)
F	Nonvolatile means that power must be continuously supplied to the memory to preserve the bit values. (T/F)
F	The advantage of RAM is that the data or program is permanently in main memory and need never be loaded from a secondary storage device. (T/F)
T	Semiconductor memory comes in packaged chips. (T/F)
T	A number of chips can be grouped together to form a memory bank. (T/F)

T	An error-correcting code enhances the reliability of the memory at the cost of added complexity. (T/F)
F	DRAM is much costlier than SRAM. (T/F)
F	RDRAM is limited by the fact that it can only send data to the processor once per bus clock cycle. (T/F)
T	The prefetch buffer is a memory cache located on the RAM chip. (T/F)
F	The SRAM on the CDRAM cannot be used as a buffer to support the serial access of a block of data. (T/F)
D	Which properties do all semiconductor memory cells share? A. They exhibit two stable states which can be used to represent binary 1 and 0 B. They are capable of being written into to set the state C. They are capable of being read to sense the state D. All of the above
A	One distinguishing characteristic of memory that is designated as _____ is that it is possible to both to read data from the memory and to write new data into the memory easily and rapidly. A. RAM B. ROM C. EPROM D. EEPROM
D	Which of the following memory types are nonvolatile? A. Erasable PROM B. Programmable ROM C. Flash memory D. All of the above
C	A _____ contains a permanent pattern of data that cannot be changed, is nonvolatile, and cannot have new data written into it. A. RAM B. SRAM C. ROM D. Flash memory
B	_____ can be caused by harsh environmental abuse, manufacturing defects, and wear. A. SEC errors B. Hard errors C. Syndrome errors D. Soft errors
A	_____ can be caused by power supply problems or alpha particles. A. Soft errors B. AGT errors C. Hard errors D. SEC errors
C	_____ can send data to the processor twice per clock cycle. A. CDRAM B. SDRAM C. DDR-DRAM D. RDRAM

C	_____ increases the prefetch buffer size to 8 bits. A. CDRAM B. RDRAM C. DDR3 D. All of the above
T	Magnetic disks are the foundation of external memory on virtually all computer systems. (T/F)
T	A removable disk can be removed and replaced with another disk. (T/F)
T	The head must generate or sense an electromagnetic field of sufficient magnitude to write and read properly. (T/F)
F	The transfer time to or from the disk does not depend on the rotation speed of the disk. (T/F)
T	RAID is a set of physical disk drives viewed by the operating system as a single logical drive. (T/F)
T	RAID level 0 is not a true member of the RAID family because it does not include redundancy to improve performance. (T/F)
F	Because data are striped in very small strips, RAID 3 cannot achieve very high data transfer rates. (T/F)
T	The SSDs now on the market use a type of semiconductor memory referred to as flash memory. (T/F)
F	SSD performance has a tendency to speed up as the device is used. (T/F)
T	Flash memory becomes unusable after a certain number of writes. (T/F)
B	Adjacent tracks are separated by _____. a. sectors b. gaps c. pits d. heads
C	Data are transferred to and from the disk in _____. a. tracks b. gaps c. sectors d. pits
D	In most contemporary systems fixed-length sectors are used, with _____ bytes being the nearly universal sector size. a. 64 b. 128 c. 256 d. 512

A	Scanning information at the same rate by rotating the disk at a fixed speed is known as the _____. a. constant angular velocity b. magnetoresistive c. rotational delay d. constant linear velocity
A	A _____ disk is permanently mounted in the disk drive, such as the hard disk in a personal computer. a. nonremovable b. movable-head c. double sided d. removable
C	When the magnetizable coating is applied to both sides of the platter the disk is then referred to as _____. a. multiple sided b. substrate c. double sided d. all of the above
D	The set of all the tracks in the same relative position on the platter is referred to as a _____. a. floppy disk b. single-sided disk c. sector d. cylinder
A	_____ is the standardized scheme for multiple-disk database design. a. RAID b. CAV c. CLV d. SSD
B	RAID level _____ has the highest disk overhead of all RAID types. a. 0 b. 1 c. 3 d. 5
D	A _____ is a high-definition video disk that can store 25 Gbytes on a single layer on a single side. a. DVD b. DVD-R c. DVD-RW d. Blu-ray DVD
A	The areas between pits are called _____. a. lands b. sectors c. cylinders d. strips
T	A set of I/O modules is a key element of a computer system. (T/F)
T	An I/O module must recognize one unique address for each peripheral it controls. (T/F)

T	It is the responsibility of the processor to periodically check the status of the I/O module until it finds that the operation is complete. (T/F)
T	A disadvantage of memory-mapped I/O is that valuable memory address space is used up. (T/F)
T	Bus arbitration makes use of vectored interrupts. (T/F)
T	Because the 82C55A is programmable via the control register, it can be used to control a variety of simple peripheral devices. (T/F)
T	When large volumes of data are to be moved, a more efficient technique is direct memory access (DMA). (T/F)
T	An I/O channel has the ability to execute I/O instructions, which gives it complete control over I/O operations. (T/F)
F	A Thunderbolt compatible peripheral interface is no more complex than that of a simple USB device. (T/F)
A	The most common means of computer/user interaction is a _____. A. keyboard/monitor B. mouse/printer C. modem/printer D. monitor/printer
B	An I/O module that is quite primitive and requires detailed control is usually referred to as an _____. A. I/O command B. I/O controller C. I/O channel D. I/O processor
D	The _____ command causes the I/O module to take an item of data from the data bus and subsequently transmit that data item to the peripheral. A. control B. test C. read D. write
A	The _____ command is used to activate a peripheral and tell it what to do. A. control B. test C. read D. write
C	_____ is when the DMA module must force the processor to suspend operation temporarily. A. Interrupt B. Thunderbolt C. Cycle stealing D. Lock down

D	The 8237 DMA is known as a _____ DMA controller. A. command B. cycle stealing C. interrupt D. fly-by
A	_____ is a digital display interface standard now widely adopted for computer monitors, laptop displays, and other graphics and video interfaces. A. DisplayPort B. PCI Express C. Thunderbolt D. InfiniBand
T	Scheduling and memory management are the two OS functions that are most relevant to the study of computer organization and architecture. (T/F)
F	The end user is concerned mainly with the computer's architecture. (T/F)
T	The most important system program is the OS. (T/F)
F	The ABI is the boundary between hardware and software. (T/F)
T	The OS must determine how much processor time is to be devoted to the execution of a particular user program. (T/F)
T	With a batch operating system the user does not have direct access to the processor. (T/F)
F	Uniprogramming is the central theme of modern operating systems. (T/F)
T	Both batch multiprogramming and time sharing use multiprogramming. (T/F)
T	An interrupt is a hardware-generated signal to the processor. (T/F)
T	Swapping is an I/O operation. (T/F)
T	The Pentium II includes hardware for both segmentation and paging. (T/F)
T	ARM provides a versatile virtual memory system architecture that can be tailored to the needs of the embedded system designer. (T/F)
F	Managers are users of domains that must observe the access permissions of the individual sections and/or pages that make up that domain. (T/F)
B	The _____ is a program that controls the execution of application programs and acts as an interface between applications and the computer hardware. A. job control language B. operating system C. batch system D. nucleus

A	Facilities and services provided by the OS that assist the programmer in creating programs are in the form of _____ programs that are not actually part of the OS but are accessible through the OS. A. utility B. multitasking C. JCL D. logical address
D	The _____ defines the repertoire of machine language instructions that a computer can follow. A. ABI B. API C. HLL D. ISA
C	The _____ defines the system call interface to the operating system and the hardware resources and services available in a system through the user instruction set architecture. A. HLL B. API C. ABI D. ISA
D	The _____ gives a program access to the hardware resources and services available in a system through the user instruction set architecture supplemented with high-level language library calls. A. JCL B. ISA C. ABI D. API
B	A _____ system works only one program at a time. A. batch B. uniprogramming C. kernel D. privileged instruction
A	A _____ is a special type of programming language used to provide instructions to the monitor. A. job control language B. multiprogram C. kernel D. utility
A	The _____ scheduler determines which programs are admitted to the system for processing. A. long-term B. medium-term C. short-term D. I/O
C	The _____ scheduler is also known as the dispatcher. A. long-term B. medium-term C. short-term D. I/O

D	A _____ is an actual location in main memory. A. logical address B. partition address C. base address D. physical address
B	_____ is when the processor spends most of its time swapping pages rather than executing instructions. A. Swapping B. Thrashing C. Paging D. Multitasking
A	Virtual memory schemes make use of a special cache called a _____ for page table entries. A. TLB B. HLL C. VMC D. SPB
A	With _____ the virtual address is the same as the physical address. A. unsegmented unpaged memory B. unsegmented paged memory C. segmented unpaged memory D. segmented paged memory
F	Our primary counting system is based on binary digits to represent numbers. (T/F)
F	The decimal system has a radix of 100. (T/F)
T	Negative powers of 10 are used to represent the positions of the numbers for decimal fractions. (T/F)
T	A number with both an integer and fractional part has digits raised to both positive and negative powers of 10. (T/F)
F	In any number, the rightmost digit is referred to as the most significant digit. (T/F)
F	A number cannot be converted from binary notation to decimal notation. (T/F)
T	There are 50 tens in the number 509. (T/F)
T	The decimal system is a special case of a positional number system with radix 10 and with digits in the range 0 through 9. (T/F)
T	Although convenient for computers, the binary system is exceedingly cumbersome for human beings. (T/F)
F	A nibble is a grouping of four decimal digits. (T/F)
F	Hexadecimal notation is only used for representing integers. (T/F)

T	It is extremely easy to convert between binary and hexadecimal notation. (T/F)
T	Hexadecimal notation is more compact than binary notation. (T/F)
F	A sequence of hexadecimal digits can be thought of as representing an integer in base 10. (T/F)
T	Because of the inherent binary nature of digital computer components, all forms of data within computers are represented by various binary codes. (T/F)
B	The decimal system has a base of _____. A. 0 B. 10 C. 100 D. 1000
B	Which digit represents "hundreds" in the number 8732? A. 8 B. 7 C. 3 D. 2
C	Which of the following is correct? A. 25 = (2 x 10^2) + (5 x 10^1) B. 289 = (2 x 10^3) + (8 x 10^1) + (9 x 10^0) C. 7523 = (7 x 10^3) + (5 x 10^2) + (2 x 10^1) + (3 x 10^0) D. 0.628 = (6 x 10^-3) + (2 x 10^-2) + (8 x 10^-1)
A	In the number 3109, the 3 is referred to as the _____. A. most significant digit B. least significant digit C. radix D. base
B	In the number 3109, the 9 is referred to as the _____. A. most significant digit B. least significant digit C. radix D. base
C	Numbers in the binary system are represented to the _____. A. base 0 B. base 1 C. base 2 D. base 10
D	Hexadecimal has a base of _____. A. 2 B. 8 C. 10 D. 16
A	The binary string 110111100001 is equivalent to _____. A. DE1 (16) B. C78 (16) C. FF64 (16) D. B8F (16)

B	The _____ system uses only the numbers 0 and 1. A. positional B. binary C. hexadecimal D. decimal
C	Decimal "10" is _____ in binary. A. 1000 B. 0010 C. 1010 D. 0001
B	Decimal "10" is _____ in hexadecimal. A. 1 B. A C. 0 D. FF
C	Four bits is called a _____. A. radix point B. byte C. nibble D. binary digit
A	Another term for "base" is _____. A. radix B. integer C. position D. digit
D	In the number 472.156 the 2 is the _____. A. most significant digit B. radix point C. least significant digit D. none of the above
B	Binary 0101 is hexadecimal _____. A. 0 B. 5 C. A D. 10
T	Both sign-magnitude representation and twos complement representation use the most significant bit as a sign bit.
F	It is not necessary for the ALU to signal when overflow occurs.
F	Overflow can only occur if there is a carry.
T	Compared with addition and subtraction, multiplication is a complex operation, whether performed in hardware of software.
T	For each 1 on the multiplier, an add and a shift operation are required; but for each 0 only a shift is required.
T	Addition and subtraction can be performed on numbers in twos complement notation by treating them as unsigned integers.
F	Booth's algorithm performs more additions and subtractions than a straightforward algorithm.
T	With a fixed-point notation it is possible to represent a range of positive and negative integers centered on or near 0.

T	An advantage of biased representation is that nonnegative floating-point numbers can be treated as integers for comparison purposes.
T	Actual floating-point representations include a special bit pattern to designate zero.
T	The numbers represented in floating-point notation are not spaced evenly along the number line, as are fixed-point numbers.
T	One of the trade-offs of floating-point math is that many calculations produce results that are not exact and have to be rounded to the nearest value that the notation can represent.
twos complement representation	The most common scheme in implementing the integer portion of the ALU is: a. sign-magnitude representation b. biased representation c. twos complement representation d. ones complement representation
Twos compliment	_____ representation is almost universally used as the processor representation for integers. a. Biased b. Twos compliment c. Sign-magnitude d. Decimal
sign-magnitude	In _____ representation the rule for forming the negation of an integer is to invert the sign bit. a. ones complement b. twos complement c. biased d. sign-magnitude
Overflow	_____ is when the result may be larger than can be held in the word size being used. a.Overflow b. Arithmetic shift c. Underflow d. Partial product
Multiplication	_____ involves the generation of partial products, one for each digit in the multiplier, which are then summed to produce the final product. a. Addition b. Subtraction c. Multiplication d. Division
mantissa	Although considered obsolete, the term _____ is sometimes used instead of significand. a. minuend b. mantissa c. base d. subtrahend
negative overflow	Negative numbers less than -(2 - 2^-23) x 2 128 are called _____. a. positive underflow b. positive overflow c. negative underflow d. negative overflow

negative underflow	Negative numbers greater than 2^-127 are called _____. a. negative overflow b. negative underflow c. positive overflow d. positive underflow
positive underflow	Positive numbers less than 2^-127 are called _____. a. positive underflow b. positive overflow c. negative underflow d. negative overflow
positive overflow	Positive numbers greater than (2 - 2^-23) x 2^-128 are called _____. a. negative underflow b. positive overflow c. positive underflow d. negative overflow
Extended precision	_____ formats extend a supported basic format by providing additional bits in the exponent and in the significand. a. Arithmetic b. Basic c. Extended precision d. Interchange
Exponent overflow	_____ is when a positive exponent exceeds the maximum possible exponent value. a. Significand underflow b. Significand overflow c. Exponent overflow d. Exponent underflow
Exponent underflow	_____ means that the number is too small to be represented and it may be reported as 0. a. Negative underflow b. Exponent underflow c. Positive underflow d. Significand underflow
T	The operation of the digital computer is based on the storage and processing of binary data. (T/F)
T	In the absence of parentheses, the AND operation takes precedence over the OR operation. (T/F)
T	The delay by the propagation time of signals through the gate is known as the gate delay. (T/F)
T	A combinational circuit consists of n binary inputs and m binary outputs. (T/F)
T	Any Boolean function can be implemented in electronic form as a network of gates. (T/F)
F	A Boolean function can be realized in the sum of products (SOP) form but not in the product of sums (POS) form. (T/F)

T	"Don't care" conditions are when certain combinations of values of variables never occur, and therefore the corresponding output never occurs. (T/F)
T	The value to be loaded into the program counter can come from a binary counter, the instruction register, or the output of the ALU. (T/F)
T	In general, a decoder has n inputs and 2^n outputs. (T/F)
T	Combinational circuits are often referred to as "memoryless" circuits because their output depends only on their current input and no history of prior inputs is retained. (T/F)
F	Binary addition is exactly the same as Boolean algebra. (T/F)
T	Events in the digital computer are synchronized to a clock pulse so that changes occur only when a clock pulse occurs. (T/F)
T	A register is a digital circuit used within the CPU to store one or more bits of data. (T/F)
C	The operand _____ yields true if and only if both of its operands are true. A. XOR B. OR C. AND D. NOT
D	The operation _____ yields true if either or both of its operands are true. A. NOT B. AND C. NAND D. OR
B	The unary operation _____ inverts the value of its operand. A. OR B. NOT C. NAND D. XOR
D	The _____ exists in one of two states and, in the absence of input, remains in that state. A. assert B. complex PLD C. decoder D. flip-flop
A	The _____ flip-flop has two inputs and all possible combinations of input values are valid. A. J-K B. D C. S-R D. clocked S-R
A	CPUs make use of _____ counters, in which all of the flip-flops of the counter change at the same time. A. synchronous B. asynchronous C. clocked S-R D. timed ripple

T	One boundary where the computer designer and the computer programmer can view the same machine is the machine instruction set. (T/F)
F	The address of the next instruction to be fetched must be a real address, not a virtual address. (T/F)
T	It has become common practice to use a symbolic representation of machine instructions. (T/F)
T	One of the traditional ways of describing processor architecture is in terms of the number of addresses contained in each instruction. (T/F)
F	Memory references are faster than register references. (T/F)
T	Addresses are a form of data. (T/F)
T	ARM processors support data types of 8 (byte), 16 (halfword), and 32 (word) bits in length. (T/F)
T	Most machines provide the basic arithmetic operations of add, subtract, multiply, and divide. (T/F)
T	A branch can be either forward or backward. (T/F)
F	Procedures do not allow programming tasks to be subdivided into smaller units. (T/F)
T	The focus of MMX technology is multimedia programming. (T/F)
B	The _____ specifies the operation to be performed. A. source operand reference B. opcode C. next instruction reference D. processor register
C	There must be _____ instructions for moving data between memory and the registers. A. branch B. logic C. memory D. I/O
A	_____ instructions operate on the bits of a word as bits rather than as numbers, providing capabilities for processing any other type of data the user may wish to employ. A. Logic B. Arithmetic C. Memory D. Test

B	The most fundamental type of machine instruction is the _____ instruction. A. conversion B. data transfer C. arithmetic D. logical
T	The register file is on the same chip as the ALU and control unit. (T/F)
C	The MIPS R4000 uses _____ bits for all internal and external data paths and for addresses, registers, and the ALU. A. 16 B. 32 C. 64 D. 128
B	The _____ introduced a full-blown superscalar design with out-of-order execution. A. Pentium B. Pentium Pro C. 386 D. 486
C	QN=2 The set of microinstructions is stored in the _____. a. control address register b. control buffer register c. control memory d. control word
D	QN=6 In executing a microprogram the address of the next microinstruction to be executed is in which of the following categories? a. determined by instruction register b. branch c. next sequential address d. all of the above

F	The "read word from memory" and "increment PC" actions cannot be used simultaneously because they will interfere with each other.
T	Each micro-operation of the fetch cycle involves the movement of data into or out of a register.
T	At the completion of the execute cycle a test is made to determine whether any enabled interrupts have occurred, and if they have, the interrupt cycle occurs.
F	The execute cycle is simple and predictable.
T	Each phase of the instruction cycle can be decomposed into a sequence of elementary micro-operations.
T	For the control unit to perform its function it must have inputs that allow it to determine the state of the system and outputs that allow it to control the behavior of the system.
T	The control unit is the engine that runs the entire computer.
T	The use of common data paths simplifies the interconnection layout and the control of the processor.
F	The number of machine cycles for an instruction depends on the number of times the processor must communicate with internal devices.

D	QN=1 A single micro-operation generally involves which of the following? a. a transfer between registers b. a transfer between a register and an external bus c. a simple ALU operation d. all of the above
B	QN=2 Each instruction executed during an instruction cycle is made up of shorter ____. a. executions b. subcycles c. steps d. none of the above
A	QN=3 _____ are the functional, or atomic, operations of a processor. a. Micro-operations b. Interrupts c. Subcycles d. All of the above
C	QN=4 The _____ cycle occurs at the beginning of each instruction cycle and causes an instruction to be fetched from memory. a. execute b. indirect c. fetch d. interrupt
B	QN=5 The _____ is connected to the address lines of the system bus. a. MBR b. MAR c. PC d. IR
C	QN=6 The _____ is connected to the data lines of the system bus. a. MAR b. PC c. MBR d. IR
B	QN=7 The _____ holds the address of the next instruction to be fetched. a. IR b. PC c. MAR d. MBR
D	QN=8 The _____ holds the last instruction fetched. a. PC b. MBR c. MAR d. IR
C	QN=9 The groupings of micro-operations must follow which rule? a. a sequence of events does not need to be followed b. use read to and write from the same register in one time unit c. conflicts must be avoided d. all of the above

A	QN=10 The _____ designates the state of the processor in terms of which portion of the cycle it is in. a. ICC b. BSA c. ALE d. ISC
B	QN=11 Machine cycles are defined to be equivalent to _____ accesses. a. flag b. bus c. clock d. path
D	QN=12 The _____ portion of the control unit issues a repetitive sequence of pulses. a. instruction register b. flag c. control bus signals d. clock
C	QN=13 The _____ pulse signals the start of each machine cycle from the control unit and alerts external circuits. a. AC b. INSTR c. ALE d. OUT
D	QN=14 Which of the following is an Intel 8085 external signal? a. CLK(OUT) b. read control c. HOLDA d. all of the above
A	QN=15 The _____ module handles multiple levels of interrupt signals. a. interrupt control b. incrementer address latch c. serial I/O control d. decrementer address latch