QSPI Controller – Design Summary

Overview

This QSPI (Quad Serial Peripheral Interface) controller IP is designed for integration into an SoC system. It supports: - Two mutually exclusive modes: 1. Command Mode (with or without DMA) 2. XIP Mode (Execute In Place, via AXI4-Lite slave) - FIFO buffering for data transfers between CPU/AXI and QSPI flash - APB interface for CSR access (CPU configuration) - AXI4-Lite Master interface for memory transfer via DMA - AXI4-Lite Slave interface for memory-mapped XIP - Handles clock domain differences between QSPI and AXI via FIFO or CDC Target flash device: Macronix MX25L6436F (64Mb SPI NOR Flash)

Mode 1: Command Mode

CPU programs a command via APB CSRs and optionally enables DMA. Manual (non-DMA) Flow: CPU → CSR → Command Engine → QSPI FSM → Flash Flash → FIFO_RX → CSR → CPU reads back With DMA Flow: CPU → CSR (CMD_TRIGGER + DMA_EN = 1) QSPI FSM → Flash → FIFO_RX → DMA → AXI memory - Commands like READ, WRITE, ERASE, READ STATUS supported - DMA is optional: offload data transfer to memory - CMD_DONE and DMA_DONE status bits indicate completion

Mode 2: XIP Mode (Execute-In-Place)

CPU or AXI master reads flash like memory through AXI4-Lite slave. Flow: AXI Read → XIP Engine → QSPI FSM → Flash → FIFO_RX → AXI Response - XIP is enabled via CSR (XIP_CFG) - No CMD_TRIGGER or DMA needed - QSPI FSM is triggered by AXI read - Designed for instruction or data fetch from flash - Write is not supported in XIP for this lab

Key Components

- CSR: APB interface, control/status registers - QSPI FSM: Generates flash protocol sequences (opcodes, addr, dummy, data) - FIFO_RX/TX: Buffers between QSPI and CPU/DMA/XIP - Command Engine: Parses CMD_* registers, starts FSM and/or DMA - DMA Engine: AXI master, transfers FIFO_RX to memory - XIP Engine: AXI slave, handles AXI reads and triggers QSPI FSM

Mode Exclusivity

- Only one mode active at a time - Controlled by: - CMD_TRIGGER (for Command Mode) - XIP_EN bit in CTRL register (for XIP Mode)

Clock Domains

- AXI clock is 4× faster than QSPI clock - FIFO-based CDC (Clock Domain Crossing) is used - FSM runs on QSPI clock; AXI/DMA run on system clock

Testbench & Verification Notes

- Use Lab 5 APB master BFM to test APB CSRs and Command Mode - Simulate QSPI FSM waveform (CMD, ADDR, DUMMY, READ/WRITE) - XIP: connect AXI-Lite master to xip_engine and simulate burst reads - FIFO full/empty flags must be verified via FIFO_STAT register