Roll: 1703057

ISA Instructions of a 5-bit CPU with a 10x17 RAM along with a 5-bit register set containing 5 registers:

Register Mode: Opcode (2-bit + 1-bit) + Register RA (3-bit) + Register RB (3-bit) + Unused (8-bit).

Opcode 1st 2 bit = 00 + Opcode last 1 bit = OR (0), SHR (1)

Example:

OR = 000 100 011 00000000

SHR = 001 000 001 00000000

Immediate Mode: Opcode (2-bit + 1-bit) + Register RA (3-bit) + Immediate Value (5-bit) + Unused (6-bit).

Opcode 1st 2 bit = 01 + Opcode last 1 bit = OR (0), SHR (1)

Example:

OR = 010 100 11000 000000

SHR = 011 000 10011 000000

Branching Mode: Opcode (2-bit + 1-bit) + Address (4-bit) + Unused (10-bit).

Opcode 1st 2 bit = 10 + Opcode last 1 bit = JC (0)

Example:

JC = 100 0010 0000000000