Ho Chi Minh University of Technology

Faculty of Computer Science and Engineering
Course: Logic Design with HDL (CO1025)

Logic Design Lab:

Weekly report - 1

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Ho Chi Minh, April 2022

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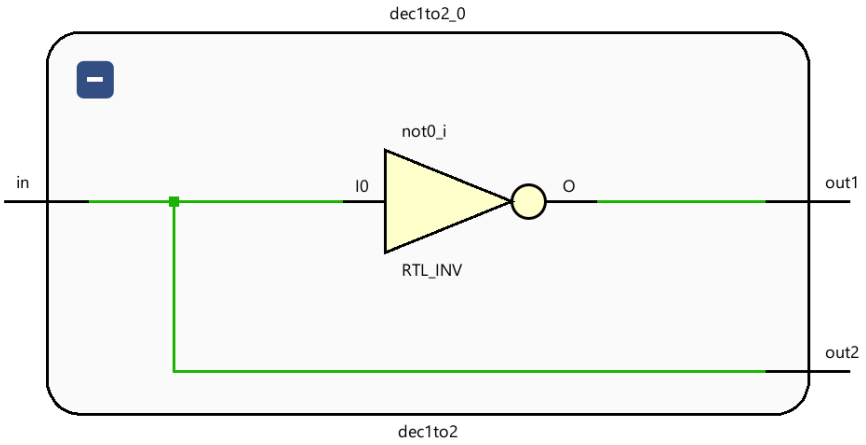

Figure 1: Decoder 1 to 2 RTL Module

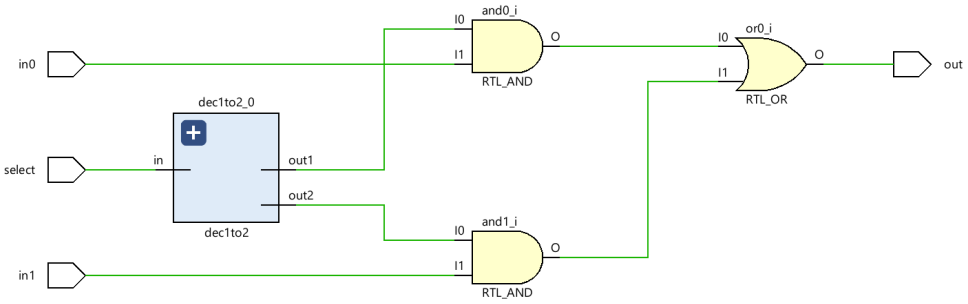

Figure 2: Multiplexer 2 to 1 RTL Module

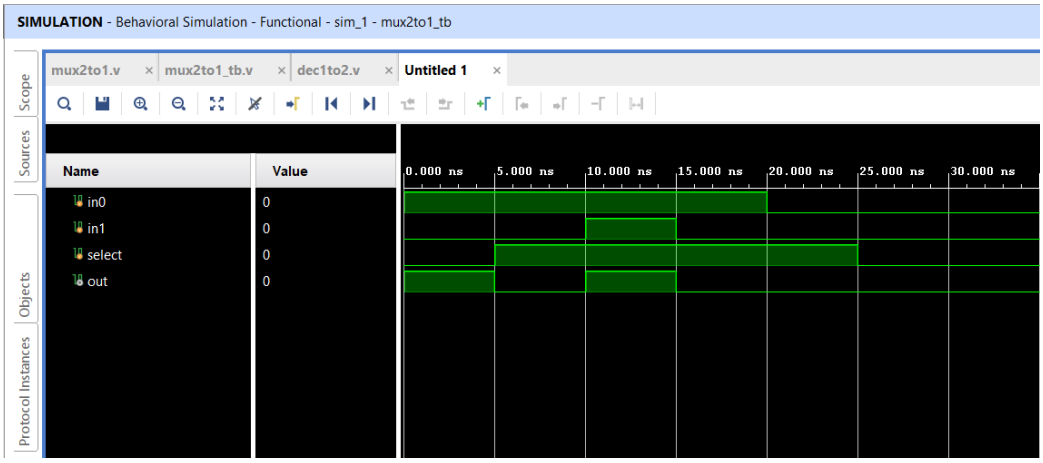

Figure 3: Multiplexer 2 to 1 Testbench Waveform

2 Exercise 2

Full Adder Module will be constructed by 2 Half Adder Module.

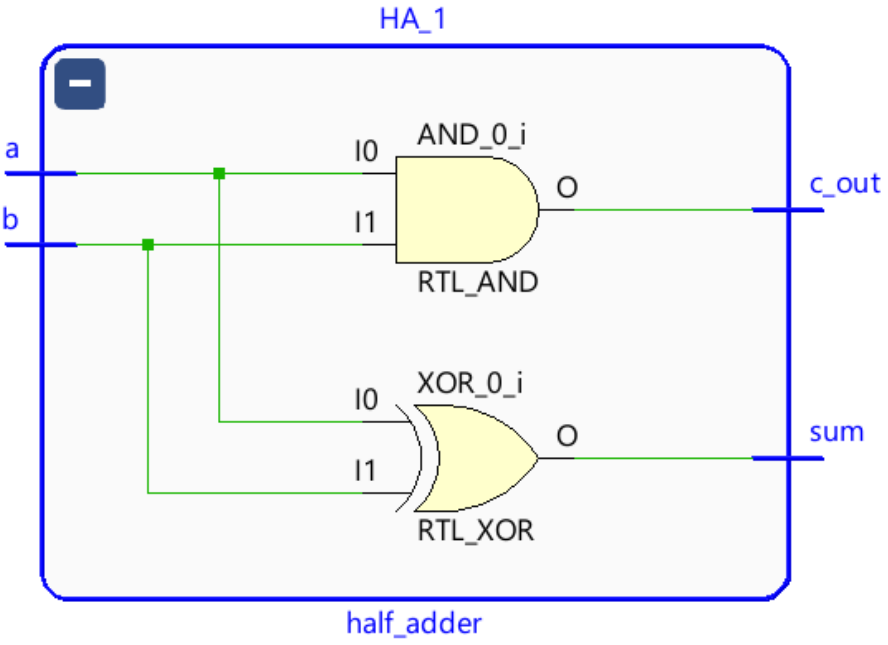

Figure 4: Half Adder RTL Module

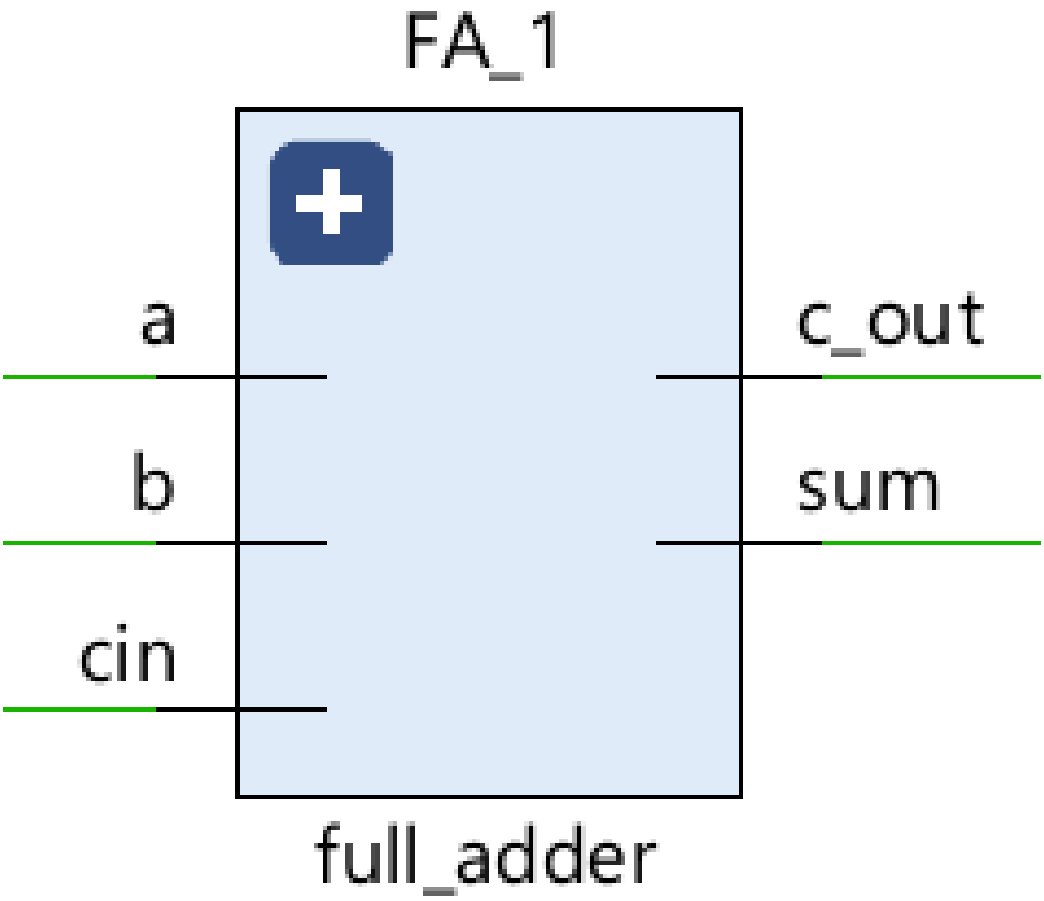

Figure 5: Full Adder Block

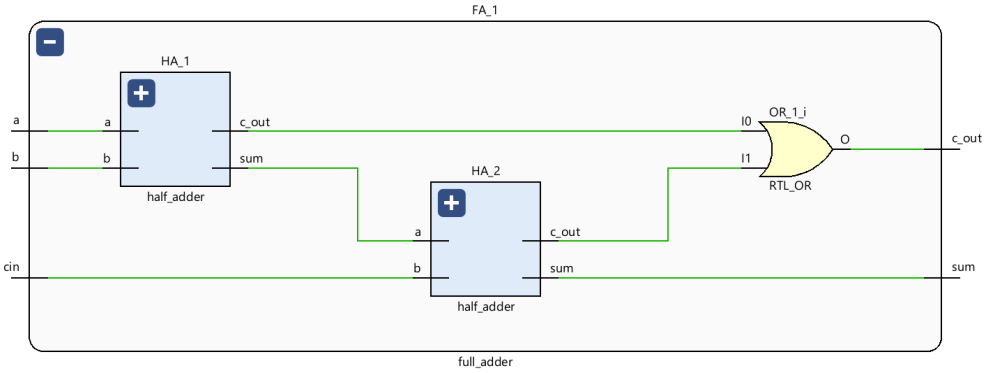

Figure 6: Full Adder RTL Module

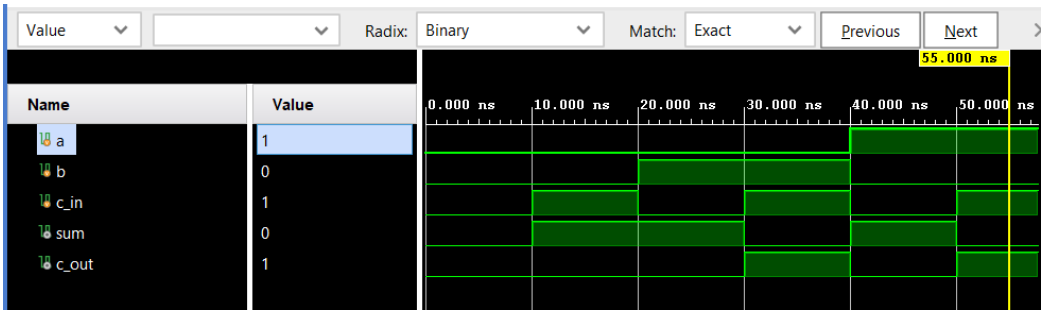

Figure 7: Full Adder Testbench Waveform

3 Exercise 3

The idea behind design a 4-bit Ripple Carry Adder is to have 4 1-bit full adders for the addition of each bit of 2 inputs orderly. Each bit of the sum will be the addition between bits of 2 inputs orderly.

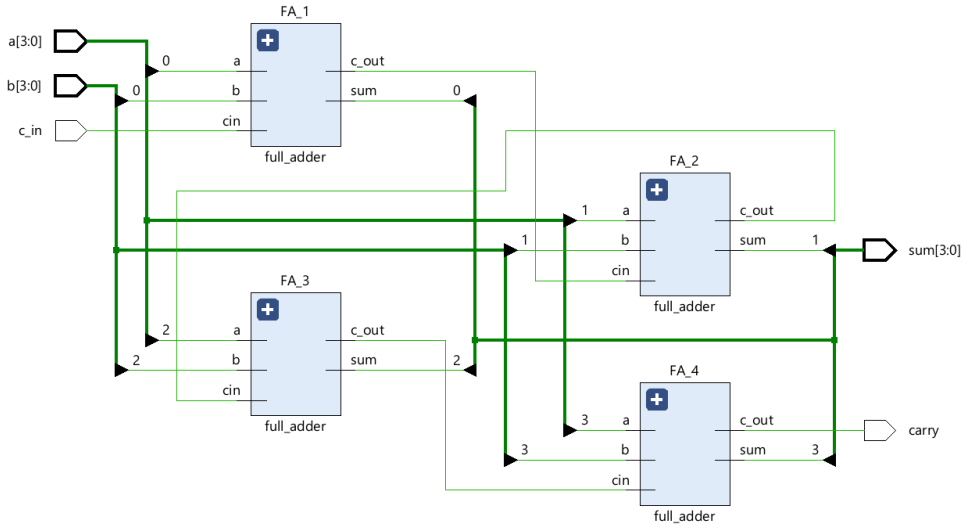

Figure 8: 4 Bit Ripple Carry Adder RTL Module

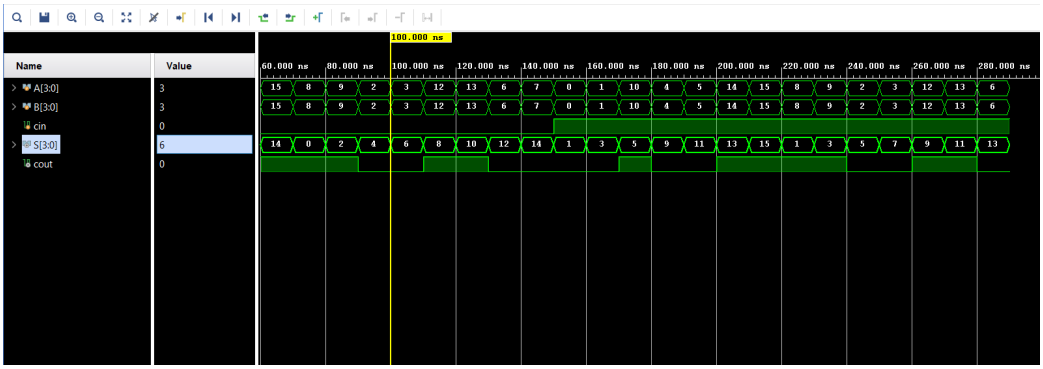

Figure 9: 4 Bit Ripple Carry Adder RTL Module Testbench Waveform

4 Exercise 4

In the 2-bit Comparator Module, it will take 2 2-bit inputs to give out the value of greater, less than and equal between 2 inputs. If 1 in 3 outputs is active, the other two will be assigned to bit 0.

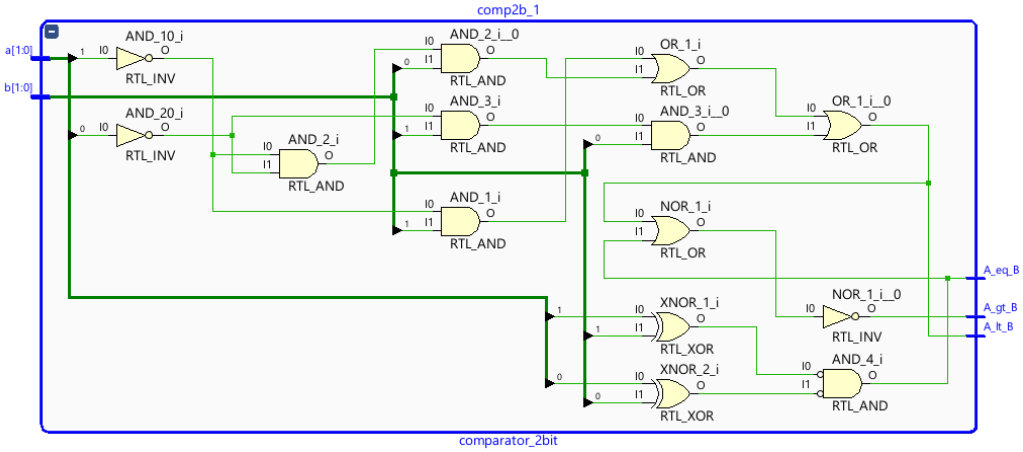

Figure 10: 2 Bit Comparator RTL

In the 4-bit Comparator Module, 2 2-bit Comparators will be used to compare the first 2 bits and the last 2 bits between 2 inputs. The Module will continue to process the output of the 2 sub modules to give out the final comparison of a 4 bit Comparator.

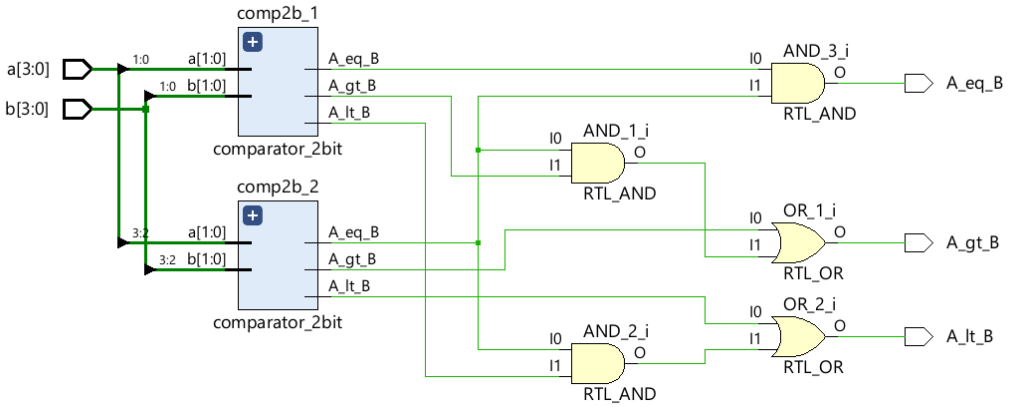

Figure 11: 4 Bit Comparator RTL

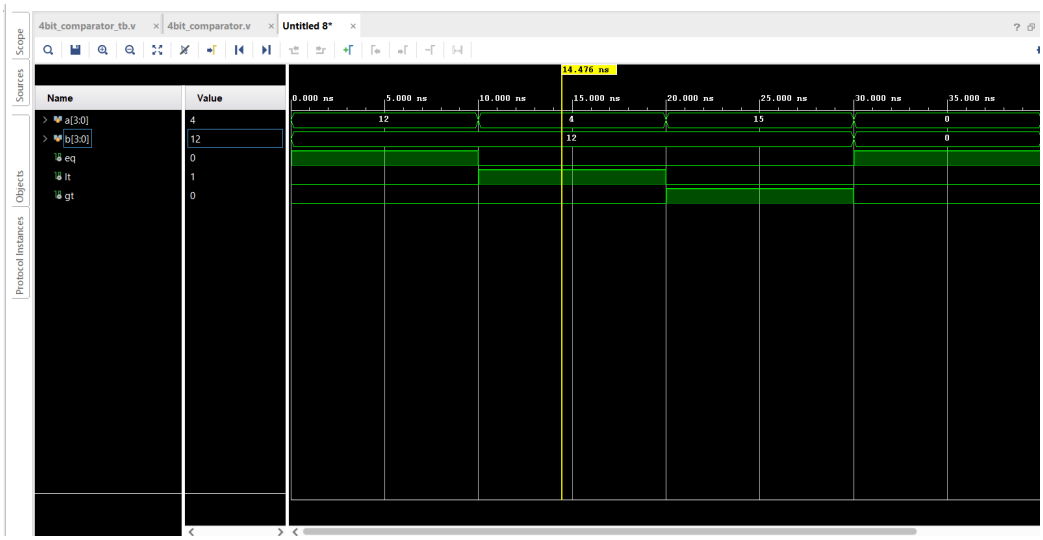

Figure 12: 4 Bit Comparator Testbench Waveform