

# 1. Description

## 1.1. Project

Project Name	STCubeGenerated
Board Name	custom
Generated with:	STM32CubeMX 6.11.1
Date	06/20/2024

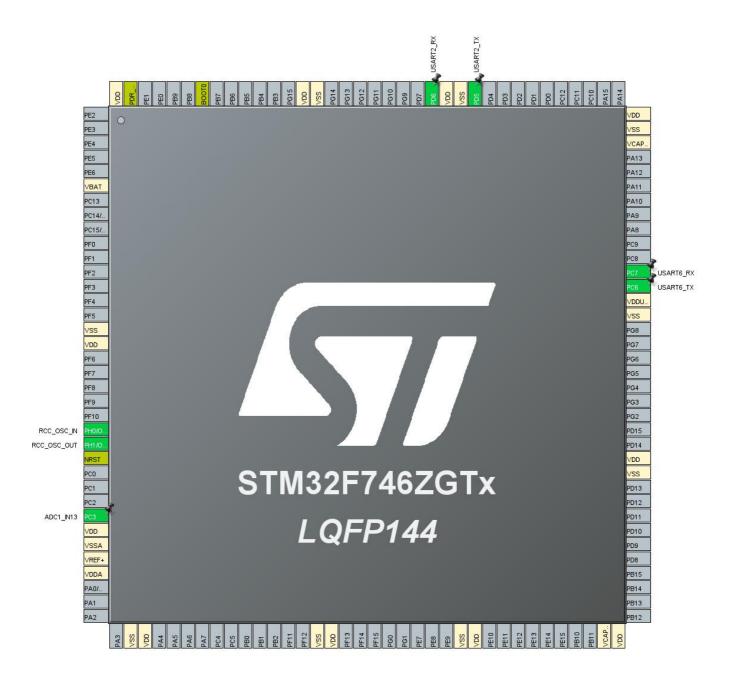
### 1.2. MCU

MCU Series	STM32F7
MCU Line	STM32F7x6
MCU name	STM32F746ZGTx
MCU Package	LQFP144
MCU Pin number	144

## 1.3. Core(s) information

Core(s)	Arm Cortex-M7

## 2. Pinout Configuration

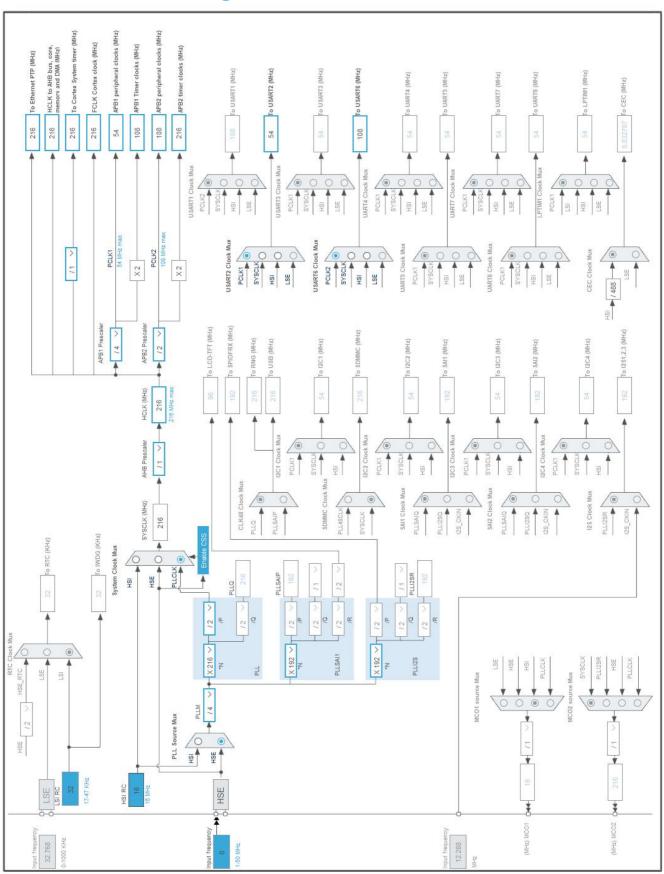


# 3. Pins Configuration

Pin Number	Pin Name	Pin Type	Alternate	Label
LQFP144	(function after		Function(s)	
	reset)			
6	VBAT	Power		
16	VSS	Power		
17	VDD	Power		
23	PH0/OSC_IN	I/O	RCC_OSC_IN	
24	PH1/OSC_OUT	I/O	RCC_OSC_OUT	
25	NRST	Reset		
29	PC3	I/O	ADC1_IN13	
30	VDD	Power		
31	VSSA	Power		
32	VREF+	Power		
33	VDDA	Power		
38	VSS	Power		
39	VDD	Power		
51	VSS	Power		
52	VDD	Power		
61	VSS	Power		
62	VDD	Power		
71	VCAP_1	Power		
72	VDD	Power		
83	VSS	Power		
84	VDD	Power		
94	VSS	Power		
95	VDDUSB	Power		
96	PC6	I/O	USART6_TX	
97	PC7	I/O	USART6_RX	
106	VCAP_2	Power		
107	VSS	Power		
108	VDD	Power		
119	PD5	I/O	USART2_TX	
120	VSS	Power		
121	VDD	Power		
122	PD6	I/O	USART2_RX	
130	VSS	Power		
131	VDD	Power		
138	воото	Boot		
143	PDR_ON	Reset		

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
144	VDD	Power		

# 4. Clock Tree Configuration



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# 5. Software Project

## 5.1. Project Settings

Name	Value
Project Name	STCubeGenerated
Project Folder	C:\Users\Tobias
Toolchain / IDE	Makefile
Firmware Package Name and Version	STM32Cube FW_F7 V1.17.1
Application Structure	Basic
Generate Under Root	No
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

## 5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Add necessary library files as reference in the toolchain project configuration file
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power	No
consumption)	
Enable Full Assert	No

### 5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_DMA_Init	DMA
4	MX_USART6_UART_Init	USART6
5	MX_USART2_UART_Init	USART2
6	MX_ADC1_Init	ADC1
7	MX_CRC_Init	CRC

## 1. Power Consumption Calculator report

### 1.1. Microcontroller Selection

Series	STM32F7
Line	STM32F7x6
мси	STM32F746ZGTx
Datasheet	DS10916_Rev4

### 1.2. Parameter Selection

Temperature	25
Vdd	3.3

### 1.3. Battery Selection

Battery	Alkaline(9V)	
Capacity	625.0 mAh	
Self Discharge	0.3 %/month	
Nominal Voltage	9.0 V	
Max Cont Current	200.0 mA	
Max Pulse Current	0.0 mA	
Cells in series	1	
Cells in parallel	1	

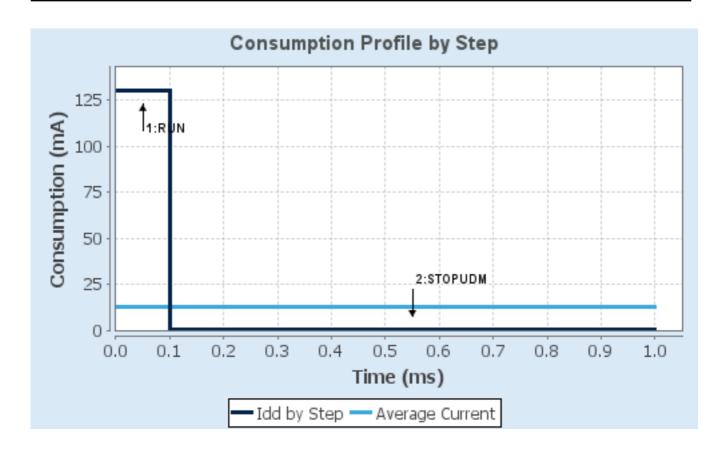
## 1.4. Sequence

Ston	Cton4	Ston 2
Step	Step1	Step2
Mode	RUN	STOP UDM (Under Drive)
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	Scale1-High	No Scale
Fetch Type	ITCM/FLASH/REGON	n/a
CPU Frequency	216 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator LP Flash-PwrDwn
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	130 mA	100 μΑ
Duration	0.1 ms	0.9 ms
DMIPS	462.0	0.0
Ta Max	87.84	104.99
Category	In DS Table	In DS Table

### 1.5. Results

Sequence Time	1 ms	Average Current	13.09 mA
Battery Life	1 day, 23 hours	Average DMIPS	462.24005
			DMIPS

### 1.6. Chart



## 2. Peripherals and Middlewares Configuration

2.1. ADC1 mode: IN13

#### 2.1.1. Parameter Settings:

ADCs\_Common\_Settings:

Mode Independent mode

ADC\_Settings:

Clock Prescaler PCLK2 divided by 4

Resolution 12 bits (15 ADC Clock cycles)

Data Alignment Right alignment

Scan Conversion Mode Disabled
Continuous Conversion Mode Disabled
Discontinuous Conversion Mode Disabled
DMA Continuous Requests Disabled

End Of Conversion Selection EOC flag at the end of all conversions \*

ADC\_Regular\_ConversionMode:

Number Of Conversion 1

External Trigger Conversion Source Regular Conversion launched by software

External Trigger Conversion Edge None Rank 1

Channel 13
Sampling Time 56 Cycles \*

ADC\_Injected\_ConversionMode:

Number Of Conversions 0

WatchDog:

Enable Analog WatchDog Mode false

#### **2.2. CORTEX M7**

#### 2.2.1. Parameter Settings:

#### Speculation default mode Settings:

Speculation default mode Disabled

**Cortex Interface Settings:** 

Flash Interface AXI Interface
ART ACCELERATOR Disabled
Instruction Prefetch Enabled \*

CPU ICache Enabled \*

CPU DCache Enabled \*

**Cortex Memory Protection Unit Control Settings:** 

MPU Control Mode Background Region Privileged accesses only + MPU Disabled

during hard fault, NMI and FAULTMASK handlers \*

**Cortex Memory Protection Unit Region 0 Settings:** 

MPU Region Enabled \*

MPU Region Base Address

MPU Region Size

MPU SubRegion Disable

MPU TEX field level

MPU TEX field level

MPU Access Permission ALL ACCESS NOT PERMITTED

MPU Instruction Access

MPU Shareability Permission

MPU Cacheable Permission

MPU Bufferable Permission

DISABLE

DISABLE

Cortex Memory Protection Unit Region 1 Settings:

MPU Region

Disabled

Cortex Memory Protection Unit Region 2 Settings:

MPU Region

Disabled

Cortex Memory Protection Unit Region 3 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 4 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 5 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 6 Settings:

MPU Region Disabled

**Cortex Memory Protection Unit Region 7 Settings:** 

MPU Region Disabled

2.3. CRC

mode: Activated

2.3.1. Parameter Settings:

**Basic Parameters:** 

Default Polynomial State Enable

Default Init Value State Enable

**Advanced Parameters:** 

Input Data Inversion Mode None
Output Data Inversion Mode Disable
Input Data Format Bytes

#### 2.4. RCC

#### High Speed Clock (HSE): BYPASS Clock Source

#### 2.4.1. Parameter Settings:

#### **System Parameters:**

VDD voltage (V) 3.3

Flash Latency(WS) 7 WS (8 CPU cycle)

**RCC Parameters:** 

HSI Calibration Value 16

TIM Prescaler Selection Disabled
HSE Startup Timout Value (ms) 100
LSE Startup Timout Value (ms) 5000

**Power Parameters:** 

Power Over Drive Enabled

Power Regulator Voltage Scale Power Regulator Voltage Scale 1

#### 2.5. SYS

**Timebase Source: TIM6** 

#### 2.6. USART2

**Mode: Asynchronous** 

#### 2.6.1. Parameter Settings:

#### **Basic Parameters:**

Baud Rate 115200

Word Length 8 Bits (including Parity)

Parity None Stop Bits 1

**Advanced Parameters:** 

Data Direction Receive and Transmit

Over Sampling 16 Samples

Single Sample Disable

**Advanced Features:** 

Auto Baudrate Disable TX Pin Active Level Inversion Disable RX Pin Active Level Inversion Disable Disable **Data Inversion** Disable TX and RX Pins Swapping Enable Overrun DMA on RX Error Enable MSB First Disable

#### 2.7. **USART6**

#### **Mode: Asynchronous**

#### 2.7.1. Parameter Settings:

#### **Basic Parameters:**

Baud Rate 115200

Word Length 8 Bits (including Parity)

Parity None Stop Bits 1

#### **Advanced Parameters:**

Data Direction Receive and Transmit

Over Sampling 16 Samples
Single Sample Disable

#### **Advanced Features:**

Auto Baudrate Disable TX Pin Active Level Inversion Disable **RX Pin Active Level Inversion** Disable Disable Data Inversion TX and RX Pins Swapping Disable Overrun Enable DMA on RX Error Enable MSB First Disable

#### \* User modified value

# 3. System Configuration

## 3.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PC3	ADC1_IN13	Analog mode	No pull-up and no pull-down	n/a	
RCC	PH0/OSC_I	RCC_OSC_IN	n/a	n/a	n/a	
	PH1/OSC_O UT	RCC_OSC_OUT	n/a	n/a	n/a	
USART2	PD5	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD6	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
USART6	PC6	USART6_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC7	USART6_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	

### 3.2. DMA configuration

DMA request	Stream	Direction	Priority
USART6_RX	DMA2_Stream1	Peripheral To Memory	Medium *
USART6_TX	DMA2_Stream6	Memory To Peripheral	Medium *
USART2_RX	DMA1_Stream5	Peripheral To Memory	Low
USART2_TX	DMA1_Stream6	Memory To Peripheral	Low

#### USART6\_RX: DMA2\_Stream1 DMA request Settings:

Mode: Circular \*

Use fifo: Enable \*

FIFO Threshold: Full
Peripheral Increment: Disable
Memory Increment: Enable \*

Peripheral Data Width: Byte
Memory Data Width: Byte
Peripheral Burst Size: Single
Memory Burst Size: Single

### USART6\_TX: DMA2\_Stream6 DMA request Settings:

Mode: Normal
Use fifo: Enable \*
FIFO Threshold: Full

Peripheral Increment: Disable

Memory Increment: Enable \*

Peripheral Data Width: Byte
Memory Data Width: Byte
Peripheral Burst Size: Single
Memory Burst Size: Single

#### USART2\_RX: DMA1\_Stream5 DMA request Settings:

Mode: Circular \*

Use fifo: Disable
Peripheral Increment: Disable
Memory Increment: Enable \*

Peripheral Data Width: Byte

Memory Data Width: Byte

### USART2\_TX: DMA1\_Stream6 DMA request Settings:

Mode: Normal
Use fifo: Disable
Peripheral Increment: Disable
Memory Increment: Enable \*

Peripheral Data Width: Byte
Memory Data Width: Byte

## 3.3. NVIC configuration

## 3.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority	
Non maskable interrupt	true	0	0	
Hard fault interrupt	true	0	0	
Memory management fault	true	0	0	
Pre-fetch fault, memory access fault	true	0	0	
Undefined instruction or illegal state	true	0	0	
System service call via SWI instruction	true	0	0	
Debug monitor	true	0	0	
Pendable request for system service	true	0	0	
System tick timer	true	15	0	
DMA1 stream5 global interrupt	true	0	0	
DMA1 stream6 global interrupt	true	0	0	
USART2 global interrupt	true	0	0	
TIM6 global interrupt, DAC1 and DAC2 underrun error interrupts	true	15	0	
DMA2 stream1 global interrupt	true	0	0	
DMA2 stream6 global interrupt	true	0	0	
USART6 global interrupt	true	0	0	
PVD interrupt through EXTI line 16		unused		
Flash global interrupt	unused			
RCC global interrupt	unused			
ADC1, ADC2 and ADC3 global interrupts	unused			
FPU global interrupt	unused			

## 3.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	false	false
Hard fault interrupt	false	false	false
Memory management fault	false	false	false
Pre-fetch fault, memory access fault	false	false	false
Undefined instruction or illegal state	false	false	false
System service call via SWI instruction	false	false	false
Debug monitor	false	false	false
Pendable request for system service	false	false	false
System tick timer	false	false	true
DMA1 stream5 global interrupt	false	true	true
DMA1 stream6 global interrupt	false	true	true

Enabled interrupt Table	Select for init	Generate IRQ	Call HAL handler
	sequence ordering	handler	
USART2 global interrupt	false	true	true
TIM6 global interrupt, DAC1 and DAC2 underrun error interrupts	false	true	true
DMA2 stream1 global interrupt	false	true	true
DMA2 stream6 global interrupt	false	true	true
USART6 global interrupt	false	true	true

<sup>\*</sup> User modified value

# 4. System Views

- 4.1. Category view
- 4.1.1. Current



## 5. Docs & Resources

Type Link

BSDL files https://www.st.com/resource/en/bsdl\_model/stm32f7\_bsdl.zip

IBIS models https://www.st.com/resource/en/ibis\_model/stm32f7\_ibis.zip

System View https://www.st.com/resource/en/svd/stm32f7-svd.zip

Description

Presentations https://www.st.com/resource/en/product\_presentation/stm32-

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**User Manuals**