Application Note AN-1162

Compensator Design Procedure for Buck Converter with Voltage-Mode Error-Amplifier

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Synchronous buck converters have received great attention in low voltage DC/DC converter applications because they can offer high efficiency; provide more precise output voltage and also meet the size requirement constraints. International Rectifier Inc. has developed a series of integrated buck regulators (***SupIRBuck***™) to accommodate all the above. These regulators combine IR's latest MOSFET technology with high performance process technology for IC controller. These regulators use a PWM voltage mode control scheme with external loop compensation to provide good noise immunity and maximum flexibility in selecting inductor values and capacitor types. The switching frequency can be programmed from 250kHz to above 1.5MHz to provide the capability of optimizing the design in terms of size and performance.

In this application note stabilizing the buck converter with voltage-mode error amplifier is discussed. The goal is to highlight the advantage of this control scheme and illustrate how a high performance feedback loop that allows fast load transient response and accurate steady state output can be achieved.

1. Introduction to Synchronous Buck Converter with Voltage-Mode Error-Amplifier

A buck converter with voltage-mode control and voltage-mode error amplifier can be stabilized with a proportional-integral (PI) type of compensator. However, to have high performance a more sophisticated compensation network is required, especially when MLCC (Multi Layer Ceramic Capacitor) capacitors are used. MLCC capacitors are widely used at the output of low voltage DC/DC converters because of their low equivalent series resistance (ESR) and low equivalent series inductance (ESL). Low ESL, which results in high resonance frequency, makes the MLCC capacitors desirable at high switching frequencies. Besides, low ESL and low ESR make the output voltage switching ripple smaller which is very desirable. On the other hand, stabilizing a DC/DC converter

with MLCC output capacitors requires more attention as compared to stabilizing a converter with electrolytic output capacitors. Depending on the type/size of the components of output filter which are used and the design parameters (switching frequency, bandwidth, etc), different compensation networks might be required. In addition, to achieve the desired performance, the parameters of the compensation network must be adjusted properly. This document provides guidelines to design appropriate compensation network in various conditions. In addition, the procedure of compensator design has been explained with examples.

Figure 1 shows a typical synchronous buck converter with voltage-mode control and voltage-mode error-amplifier.

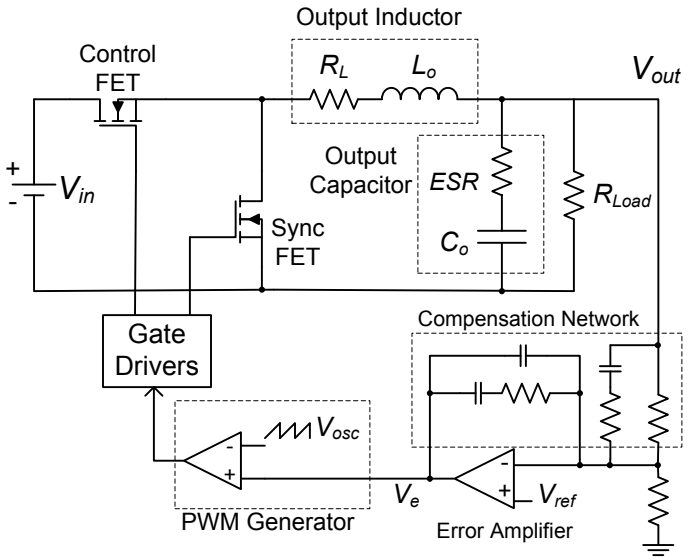

Figure 1 - Simplified circuit diagram of a synchronous buck converter with a voltage-mode error-amplifier

In Figure 1, R_L is the inherent resistance of the output inductor and *ESR* is the equivalent series resistance of the output capacitor. To make the analysis simpler, the *ESL* of the output capacitors is neglected. The circuit shown in Figure 1 can be modeled with three blocks as presented in Figure 2. The power stage ($G_p(s)$) includes the switches, the drivers and the output inductor and capacitor. The model of the PWM generator is simply $1/V_{osc}$ [2], where V_{osc} is the peak to peak amplitude of the oscillator voltage (saw-tooth)

listed in the datasheet. The compensator block (H(s)) represents the error-amplifier with the compensation network.

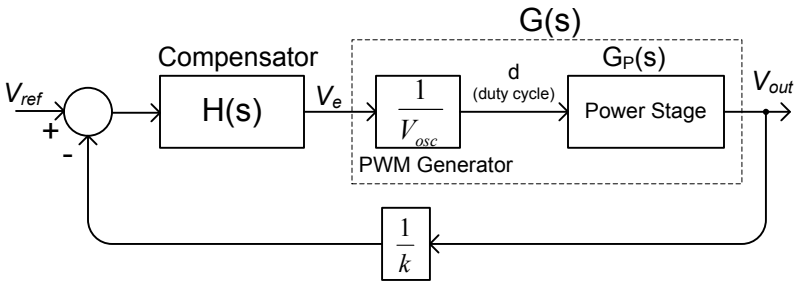

Figure 2 - The block diagram model of the synchronous buck converter

The transfer function of the power stage can be simplified as follows:

$$G_P(s) = \frac{V_{out}}{d}(s) = \frac{R_{Load}(C_o \cdot ESR \cdot s + 1)}{L_o C_o \cdot s^2 (R_{Load} + ESR) + s \cdot (L_o + R_{Load} \cdot C_o \cdot ESR) + R_{Load}} \times V_{in} \quad (1)$$

The 's' indicates that the transfer function varies as a function of the frequency. For simplicity the transfer functions of the PWM generator and the power stage can be combined:

$$G(s) = G_P(s) \cdot \frac{1}{V_{osc}} \quad (2)$$

Therefore, *G(s)* is usually referred to as the transfer function of the power stage. The roots of the polynomial in the denominator of (1) are called the poles of the transfer function of the power stage. Similarly the roots of the numerator of (1) are the zeros of the transfer function of the power stage. The transfer function of the power stage is a second order system with a double pole at the resonance frequency (of the LC filter) and a zero produced by the *ESR* of the output capacitor. The resonance frequency and the zero frequency associated with the ESR are given by (3) and (4). The approximate Bode plot of the power stage is sketched in Figure 3. The double pole causes the gain to fall with a slope of -40dB/dec up to the zero frequency (F_{ESR}) which compensates one of the poles. The zero frequency is a characteristic parameter of the output capacitor and is dependant on the type of the capacitor used. This frequency can be as low as a few kHz

for an electrolytic capacitor to as high as a few MHz for a ceramic capacitor. More information about designing the power stage is provided in Appendix A.

$$F_{LC} = \frac{1}{2 \cdot \pi \cdot \sqrt{L_o \cdot C_o}} \quad \text{(frequency of the double poles)} \tag{3}$$

$$F_{ESR} = \frac{1}{2 \cdot \pi \cdot ESR \cdot C_o} \quad \text{(frequency of the zero)} \tag{4}$$

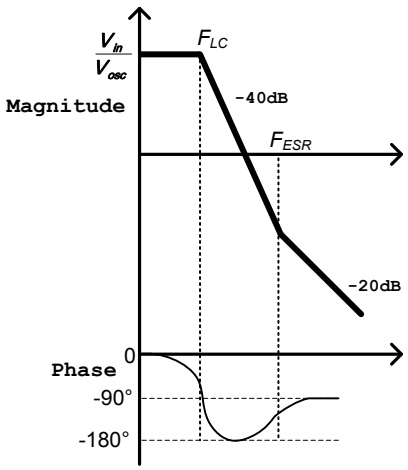

Figure 3 - The bode plot of the power stage of the buck converter

2. Loop Gain of the system

The loop gain of system is defined as the product of transfer functions along the closed control loop. Using Figure 2, the loop gain is defined as:

$$M(s) = \frac{1}{k} \times H(s) \times \frac{1}{V_{osc}} \times G_P(s) = \frac{1}{k} \times H(s) \times G(s) \tag{5}$$

Where $1/k$ represents the gain of the resistor divider which is used in the feedback loop when $V_{out} > V_{ref}$. For some configurations of compensation network, as the ones discussed in the next sections, this term $(1/k)$ is canceled out and does not appear in the loop-gain equation.

The bode plots of power stage and desired loop gain is shown in Figure 4, where F_0 is the zero crossover frequency defined as the frequency when loop gain equals unity. F_0 is also called “the bandwidth of the loop” or “the bandwidth of the system”.

Typically, F_0 can be set to 1/10~1/5 of the switching frequency. The speed of the system response to load transients is determined by F_0. In other words, the higher the crossover frequency, the faster the load transient response would be. However, the crossover frequency should be low enough to allow attenuation of switching noise. The slope of the loop gain at F_0 should be about –20dB in order to ensure a stable system. The phase margin should be greater than 45º for overall stability.

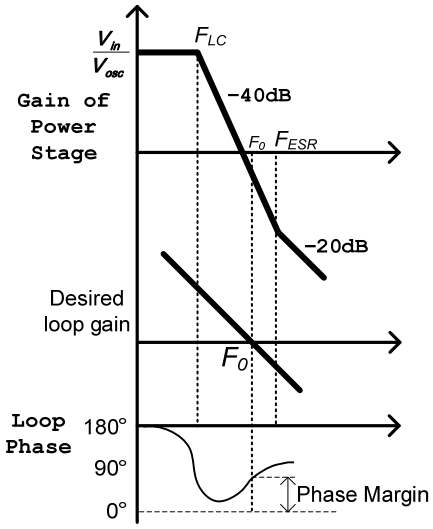

Figure 4 - Bode plot of the power stage, desired loop gain, and loop phase

3. Step by step compensator design procedure

As mentioned in the Introduction, to have a stable closed loop buck converter with appropriate performance, a properly designed compensator is required. The typical procedure of compensator design is as follows:

Step 1 - Collect system parameters such as input voltage, output voltage, maximum load/output current, switching frequency, input and output capacitance, and output inductance.

Step 2 - Using (3) and (4) determine the power stage poles and zero

Step 3 - Determine the zero crossover frequency of the loop, F_0. Usually this frequency is chosen equal to 1/10 to 1/5 of the switching frequency.

$$F_0 = (1/10 \sim 1/5) \cdot F_S \quad (6)$$

Step 4 - Determine the compensation type. The compensation type is determined by the location of zero crossover frequency and characteristics of the output capacitor as shown in Table 1.

Step 5 - Determine the desired location of the poles and zeros of the selected compensator (this will be explained for each type of compensator).

Step 6 - Calculate the real parameters (resistors and capacitors) for the selected compensator so that the desired poles/zeros are achieved. Choose the standard values for resistors and capacitors such that they are as close to the calculated values as possible.

Table 1 - The compensation type and location of zero crossover frequency.

Compensator Type	Relative location of the crossover and power-stage frequencies	Typical Output Capacitor
Type II (PI)	$F_{LC} < F_{ESR} < F_0 < F_S/2$	Electrolytic, POS-Cap, SP-Cap
Type III-A (PID)	$F_{LC} < F_0 < F_{ESR} < F_S/2$	POS-Cap, SP-Cap
Type III-B (PID)	$F_{LC} < F_0 < F_S/2 < F_{ESR}$	Ceramic

4. Type II Compensator Design

Type II compensation is used for applications where the frequency of the zero caused by output capacitor and its ESR (F_{ESR}) is smaller than the closed loop bandwidth (F_0) as shown below:

$$F_{LC} < F_{ESR} < F_0 < F_S/2 \quad (7)$$

This condition is usually met when the output capacitor is of electrolytic type. The F_{ESR} (refer to (4)) for this type of capacitor is in the range of a few kHz.

The schematic of the type II compensator is depicted in Figure 5.

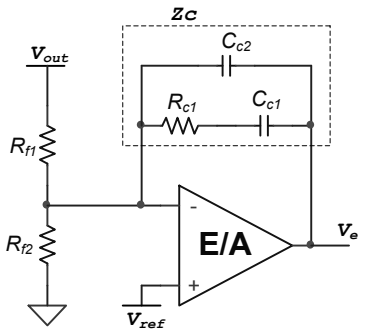

Figure 5 - Type II compensator

Assuming the gain/band-width of the error-amplifier (E/A) is very high, the transfer function of this compensator is given by:

$$H(s)=\frac{V_e}{V_{out}}(s)=-\frac{1+R_{C1}\cdot C_{C1}\cdot s}{R_{f1}\cdot s\cdot(C_{C1}+C_{C2})\cdot(R_{C1}\cdot\frac{C_{C1}\cdot C_{C2}}{C_{C1}+C_{C2}}\cdot s+1)} \quad (8)$$

The capacitor C_{C2} is chosen so that $C_{C2} << C_{C1}$. Therefore:

$$H(s)\approx-\frac{1+R_{C1}\cdot C_{C1}\cdot s}{R_{f1}\cdot s\cdot C_{C1}\cdot(R_{C1}\cdot C_{C2}\cdot s+1)} \quad (9)$$

The root of the numerator in (8) is the zero of compensator and the roots of the denominator are the poles of the compensator. Therefore, the compensator has a pole at the origin (an integrator) and another pole and one zero as given below:

$$F_{Z1}=\frac{1}{2\pi\cdot R_{C1}\cdot C_{C1}} \quad (10)$$

$$F_{P2}=\frac{1}{2\pi\cdot R_{C1}\cdot C_{C2}} \quad (11)$$

The approximate bode-plot of the power stage, the Type II compensator, and the desired loop gain has been drawn in Figure 6.

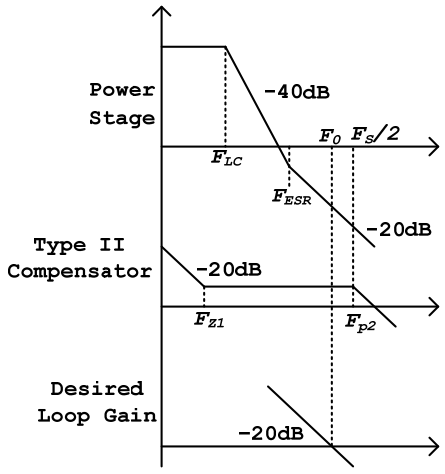

Figure 6 - Bode plot of the buck converter power stage, desired loop gain, and Type II compensator

Each pole makes the phase of the loop drop by 90º and each zero makes the phase rise by 90º. The phase change of a zero/pole starts at about 1 decade below the frequency of the zero/pole and ends about 1 decade above it. It should be noted that due to negative feedback (minus sign of *H(s)*) initially there is 180º phase-shift in the compensator. The phase change due to poles and zeros are added to this 180º. Hence, to have a stable system, the overall phase of the loop should never become 360º/0º (or close to it) when the gain is greater than 1 (0dB). Especially, at crossover frequency (F_0), the phase should be at least 45º (45º phase margin).

Since the compensator has a pole at the origin, the zero of the compensator should be placed at a frequency lower than the double poles of the LC filter to make sure the phase of the loop does not drop close to 0º around F_{LC}. Usually the following equation is used:

$$F_{Z1} \approx 0.75 \times F_{LC} \quad (12)$$

The second pole of the compensator should be placed higher than the cross-over frequency so that its lagging phase (phase drop) does not decrease the phase margin of the loop. On the other hand, it should be placed lower than the switching frequency, so that enough attenuation at the switching ripple is obtained. The following equation gives a reasonable compromise:

$$F_{P2} \approx F_S / 2 \quad (13)$$

After F_{Z1} and F_{p2} are selected the values of the components of the compensator can be calculated.

There is one degree of freedom in calculating the values of the parameters of the compensator. The procedure can be started by selecting a reasonable value for R_{f1}. A value of a few kΩ should be a good starting point. Since R_{f1} and R_{f2} are used to set the output voltage (Figure 5), R_{f2} can be calculated using the following equation:

$$R_{f2} = \frac{R_{f1} \cdot V_{ref}}{(V_{out} - V_{ref})} \tag{14}$$

The transfer function from the output of the error amplifier to the output voltage is:

$$G(s) = \frac{V_{out}}{V_e}(s) = \frac{V_{in}}{V_{osc}} \cdot \frac{R_{Load}(C_o \cdot ESR \cdot s + 1)}{L_o C_o \cdot s^2 (R_{Load} + ESR) + s \cdot (L_o + R_{Load} \cdot C_o \cdot ESR) + R_{Load}} \tag{15}$$

In the above equation, V_{osc} is the amplitude of the saw-tooth/triangular modulator signal

The amplitude of the loop-gain at crossover frequency is equal to one. Therefore,

$$\left| H(s) \times G(s) \right|_{f=F_0} = 1 \tag{16}$$

Using the (9), (15), and (16) R_{C1} is calculated:

$$R_{C1} = \frac{R_{f1} \cdot F_{ESR} \cdot V_{osc} \cdot F_0}{V_{in} \cdot F_{LC}^2} \tag{17}$$

Since F_{Z1} was chosen and R_{C1} was calculated, C_{C1} can be calculated:

$$C_{C1} = \frac{1}{2\pi \cdot R_{C1} \cdot F_{Z1}} = \frac{1}{1.5\pi \cdot R_{C1} \cdot F_{LC}} \tag{18}$$

Similarly, C_{C2} can be calculated:

$$C_{C2} = \frac{1}{2\pi \cdot R_{C1} \cdot F_{P2}} = \frac{1}{\pi \cdot R_{C1} \cdot F_S} \tag{19}$$

4.1 Design example of Type II compensator

For this design an IR3840 regulator is used. The schematic of the design is given in Figure 7.

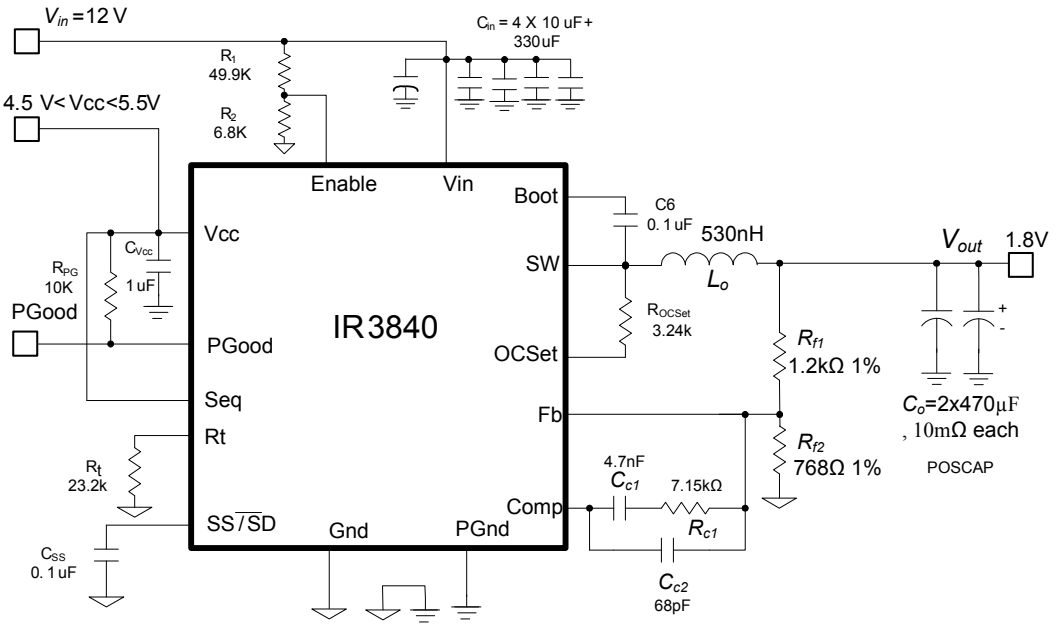

Figure 7 - Application of IR3840 with type II compensator for a 12A, 1.8V regulator

Step 1 - Collect the system information such as input and output voltage and the switching frequency:

$V_{in} = 12V$

$V_{out} = 1.8V$

$V_{ref} = 0.7V$

$V_{osc} = 1.8V$

$L_o = 530nH$

$C_o = 2 \times 470\mu F$

$ESR(C_o) = 10m\Omega \ each$

$F_S = 600KHz$

$I_o(max) = 12A$

Step 2 - Calculate the poles and zero of the power stage. Using (3), the double pole of the power stage is at:

$$F_{LC} = \frac{1}{2\pi \times \sqrt{L_o \cdot C_o}} = \frac{1}{2\pi \times \sqrt{530nH \times 940\mu F}} = 7.1KHz$$

The zero caused by the *ESR* of the output capacitor can be calculated using (4):

$$F_{ESR} = \frac{1}{2\pi \cdot ESR \cdot C_o} = \frac{1}{2\pi \cdot 10m\Omega \times 470\mu F} = 33.8kHz$$

Step 3 - Select crossover frequency to be 1/10 of the switching frequency:

$F_0 = 60KHz$

Step 4 - Select the type of compensator. Since $F_{LC} < F_{ESR} < F_0 < F_S / 2$, Type II compensator is suitable for this application.

Step 5 - Select the pole and zero of the compensator. Using (13) and (12):

$$F_{Z1} = 0.75 \times F_{LC} = 0.75 \times 7.1kHz = 5.33kHz$$
$$F_{P2} = F_S / 2 = 600kHz / 2 = 300kHz$$

Step 6 - Calculate the parameters (resistors and capacitors) of the compensator. Select $R_{f1} = 1.2K\Omega$. R_{f2} is calculated using (14):

$$R_{f2} = \frac{1.2k\Omega \times 0.7V}{(1.8V - 0.7V)} = 764\Omega$$

Select $R_{f2} = 768\Omega$. Calculate R_{C1} using (17):

$$R_{C1} = \frac{1.2k\Omega \times 33.8kHz \times 1.8V \times 60kHz}{12V \times (7.1kHz)^2} = 7.24k\Omega$$

Choose $R_{C1} = 7.15k\Omega$. Calculate C_{C1} using (18):

$$C_{C1} = \frac{1}{2\pi \times 7.15k\Omega \times 5.33kHz} = 4.2nF$$

Choose $C_{C1} = 4.7nF$. Calculate C_{C2} using (19):

$$C_{C2} = \frac{1}{2\pi \times 7.15k\Omega \times 300kHz} = 74pF$$

Choose $C_{C2} = 68pF$. The experimentally measured Bode plot of the loop for this design is shown in Figure 8. The resulting crossover frequency is about *61kHz* and the phase margin is about *54°*.

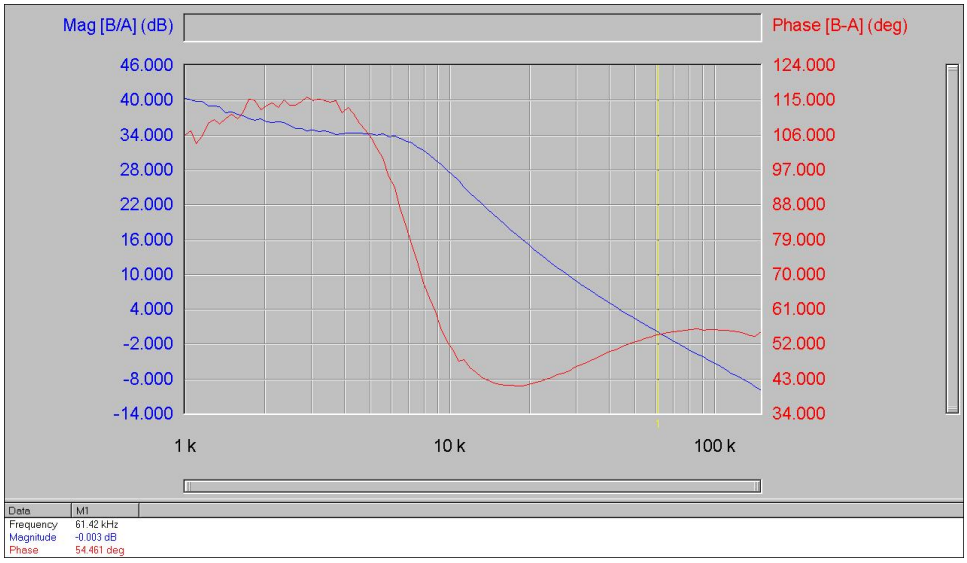

Figure 8 - The bode plot of the loop for the example with Type II compensator

5. Type III Compensator

For a general solution for unconditional stability for any type of output capacitors, and a wide range of ESR values, local feedback should be implemented with a type III compensation network. Specially, when $F_0 < F_{ESR}$ type II compensator is not useful and type III compensator must be used. The typically type III compensation network which is used for a voltage-mode PWM converter is shown in figure 9.

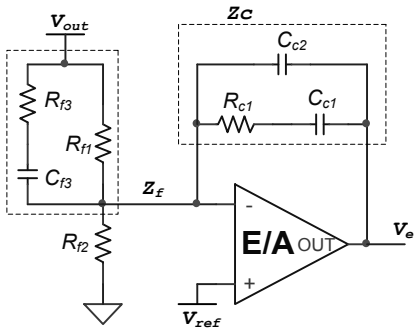

Figure 9 - Type III compensator

The transfer function of type III compensator is given by:

$$H(s) = \frac{V_e}{V_{out}} = -\frac{Z_C}{Z_f} \tag{20}$$

$$H(s) = -\frac{(1+s\cdot R_{C1}\cdot C_{C1})\cdot[1+s\cdot C_{f3}\cdot(R_{f1}+R_{f3})]}{s\cdot R_{f1}\cdot(C_{C1}+C_{C2})\cdot[1+s\cdot R_{C1}\cdot(\frac{C_{C1}\cdot C_{C2}}{C_{C1}+C_{C2}})]\cdot(1+s\cdot R_{f3}\cdot C_{f3})} \quad (21)$$

The pole which is generated by C_{C2} and R_{C1} is usually set at a much higher frequency as compared with the frequency of the zero generated by C_{C1} and R_{C1}. This means: $C_{C2} << C_{C1}$. Therefore:

$$H(s) \approx -\frac{(1+R_{C1}\cdot C_{C1}\cdot s)\cdot[1+s\cdot C_{f3}\cdot(R_{f1}+R_{f3})]}{s\cdot R_{f1}\cdot C_{C1}\cdot(R_{C1}\cdot C_{C2}\cdot s+1)\cdot(1+s\cdot R_{f3}\cdot C_{f3})} \quad (22)$$

The compensator has two zeros and three poles as given below:

$$F_{Z1} = \frac{1}{2\pi\cdot R_{C1}\cdot C_{C1}} \quad (23)$$

$$F_{Z2} = \frac{1}{2\pi\cdot C_{f3}\cdot(R_{f1}+R_{f3})} \quad (24)$$

$$F_{p1} = 0 \quad (25)$$

$$F_{p2} = \frac{1}{2\pi\cdot C_{f3}\cdot R_{f3}} \quad (26)$$

$$F_{p3} = \frac{1}{2\pi\cdot R_{C1}\cdot C_{C2}} \quad (27)$$

Depending upon the relative location of F_{ESR}, type III compensator design is divided into two categories: Type III-A and Type III-B compensators.

5.1 Type III- A Compensator

If the zero cased by the ESR is below half of the switching frequency, that is if (28) is valid, Type III-A compensation method is used.

$$F_{LC} < F_0 < F_{ESR} < F_S/2 \quad (28)$$

Condition (28) might happen when OSCON, POS-cap or SP-Cap types of capacitors are used at the output of the DC/DC converter. If this happens, the poles and zeros of the compensator will be placed as follows:

$$F_{Z2} = F_{LC} \tag{29}$$

$$F_{Z1} = 0.75 \times F_{Z2} = 0.75 \times F_{LC} \tag{30}$$

$$F_{p2} = F_{ESR} \tag{31}$$

$$F_{p3} = F_S / 2 \tag{32}$$

The approximate bode-plot of the power stage for the Type III-A compensator and the desired loop gain has been drawn in Figure 10.

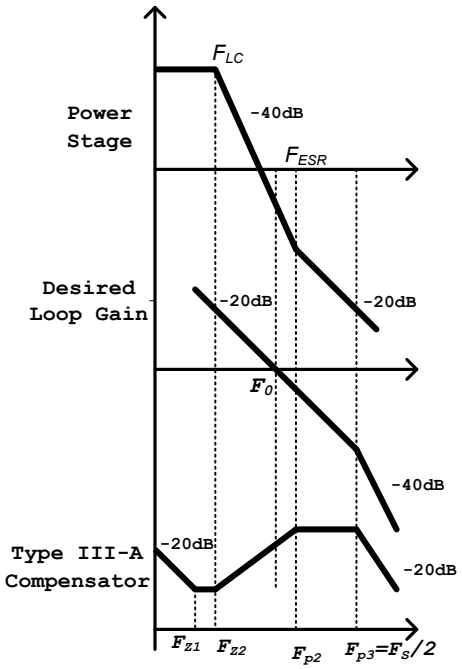

Figure 10 - Bode plot of the buck converter power stage, desired loop gain, and Type III-A compensator

The first zero of the compensator (F_{Z1}) compensates the phase lag of the pole which is at the origin. The second zero (F_{Z2}) is to compensate for one of the poles of the LC filter so that at F_0 the slope of the bode plot of the loop is about -20dB/dec. The second pole of the compensator (F_{p2}) and the zero of the ESR of the capacitor (F_{ESR}) cancel each other and the third pole (F_{p3}) is to provide more attenuation for frequencies above $F_S / 2$.

The parameters of the compensator can be calculated as follows. First a value for C_{f3} is selected (2.2nF can be a good start). Using (26) R_{f3} is calculated:

$$R_{f3} = \frac{1}{2\pi \cdot C_{f3} \cdot F_{p2}} \tag{33}$$

Using (24) R_{f1} is calculated:

$$R_{f1} = \frac{1}{2\pi \cdot C_{f3} \cdot F_{Z2}} - R_{f3} \tag{34}$$

Using (14), R_{f2} is calculated and R_{C1} is calculated using the following equation:

$$R_{C1} = \frac{2\pi \cdot F_0 \cdot L_o \cdot C_o \cdot V_{osc}}{V_{in} \cdot C_{f3}} \tag{35}$$

Using (23) calculate C_{C1}:

$$C_{C1} = \frac{1}{2\pi \cdot R_{C1} \cdot F_{Z1}} \tag{36}$$

Using (27) calculate C_{C2}:

$$C_{C2} = \frac{1}{2\pi \cdot R_{C1} \cdot F_{p3}} \tag{37}$$

5.2 Design example of Type III-A compensator

For this design, as shown in Figure 11, IR3840 regulator is used.

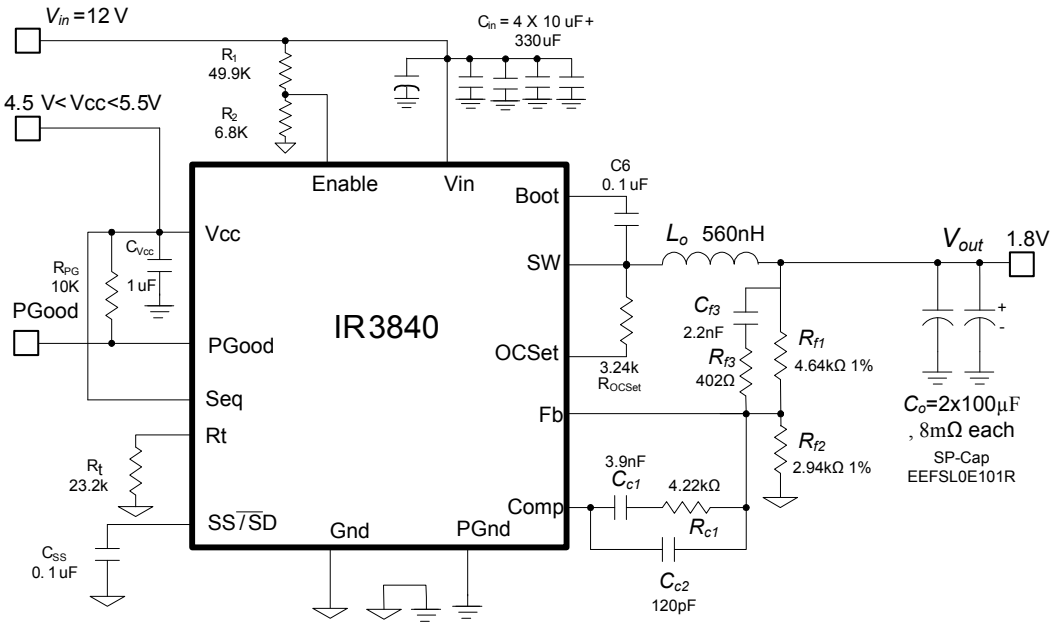

Figure 11 - Application of IR3840 with type III-A compensator for a 12A, 1.8V regulator

Step 1 - Collect the system information such as input and output voltage and the switching frequency:

$V_{in} = 12V$
$V_{Out} = 1.8V$
$V_{ref} = 0.7V$
$V_{osc} = 1.8V$
$L_o = 560nH$
$C_o = 2 \times 110\mu F$
$ESR(C_o) = 8m\Omega \ each$
$F_S = 600KHz$
$I_o(max) = 12A$

Step 2 - Using (3) and (4) calculate the poles and zero of the power stage:

$$F_{LC} = \frac{1}{2\pi \times \sqrt{560nH \times 220\mu F}} = 14.34KHz$$

$$F_{ESR} = \frac{1}{2\pi \times (8m\Omega / 2) \times 220\mu F} = 180kHz$$

Step 3 - Selected crossover frequency to be about 1/8 of the switching frequency:

$F_0 = 80KHz$

Step 4 - Select the type of compensator. Since $F_{LC} < F_0 < F_{ESR} < F_S / 2$, Type III-A compensator is suitable for this application.

Step 5 - Calculate the poles and zeros of the compensator. Using (29) to (32) the poles and zeros can be calculated:

$F_{Z2} = F_{LC} = 14.34kHz$

$F_{Z1} = 0.75 \times 14.34kHz = 10.8kHz$

$F_{p2} = F_{ESR} = 180kHz$

$F_{p3} = 600kHz / 2 = 300kHz$

Step 6 - Calculate the values of the parameters of the compensator. Choose $C_{f3} = 2.2nF$. Using (33):

$$R_{f3} = \frac{1}{2\pi \times 2.2nF \times 180kHz} = 401.9\Omega$$

Choose $R_{f3} = 402\Omega$. Use (34) to calculate R_{f1}:

$$R_{f1} = \frac{1}{2\pi \times 2.2nF \times 14.34kHz} - 402 = 4.64\Omega$$

Select $R_{f1} = 4.64k\Omega$. Using (14), R_{f2} can be calculated:

$$R_{f2} = \frac{4.64k\Omega \times 0.7V}{(1.8V - 0.7V)} = 2.95k\Omega$$

Select $R_{f2} = 2.94k\Omega$. Use (35) to calculate R_{C1}:

$$R_{C1} = \frac{2\pi \times 80k\Omega \times 560nH \times 220\mu F \times 1.8V}{12V \times 2.2nF} = 4.22k\Omega$$

Choose $R_{C1} = 4.22k\Omega$. Use (36) to calculate C_{C1}:

$$C_{C1} = \frac{1}{2\pi \times 4.22k \times 10.8k} = 3.49nF$$

Choose $C_{C1} = 3.9nF$. Use (37) to calculate C_{C2}:

$$C_{C2} = \frac{1}{2\pi \times 4.22k \times 300k} = 125pF$$

Choose $C_{C2} = 120pF$. The experimentally measured bode plot of the loop for this design is shown in Figure 12 which shows the loop crossover frequency is $F_0 \approx 77kHz$ and a phase-margin is about 53º.

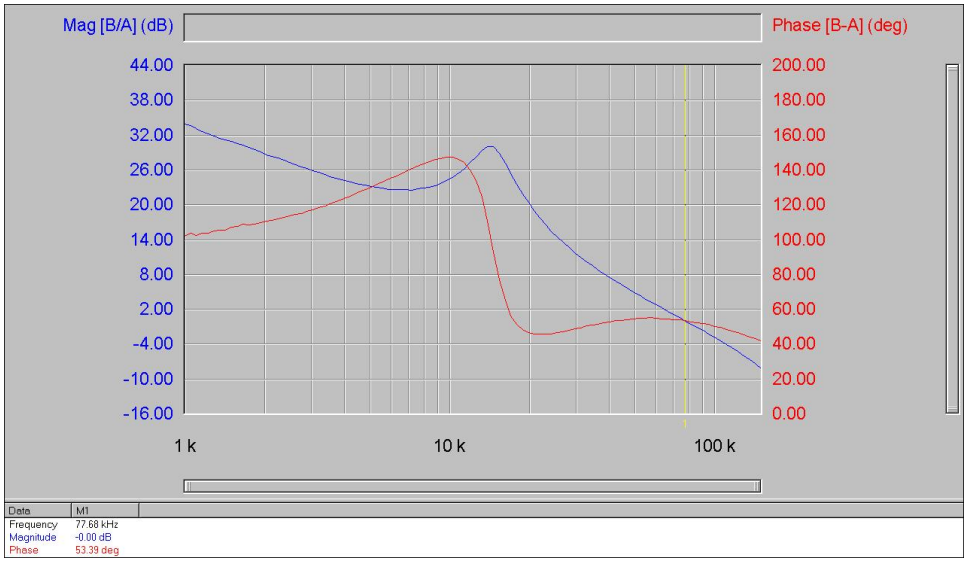

Figure 12 - The bode plot of the loop for the example with Type III-A compensator

5.3 Type III- B compensator

If the zero cased by the ESR is above half of the switching frequency, that is if (38) is valid, Type III-B compensation method is used.

$$F_{LC} < F_0 < F_S/2 < F_{ESR} \tag{38}$$

Condition (38) happens when MLCC capacitors are used at the output side of the converter. Sometimes, using POS-Cap or SP-Cap types of capacitors results in a type III-B system as well. If this happens, the poles and zeros of the compensator will be placed as follows:

$$F_{p3} = F_S/2 \tag{39}$$

F_{Z2} and F_{p2} pair (second pole and second zero of the compensator) are considered as a lead-compensator and are located so that the maximum phase lead of this pair results at crossover frequency (F_0). The following formulas can be used to locate F_{Z2} and F_{p2} in order to get a maximum phase lead of θ at crossover frequency [3]:

$$F_{Z2} = F_0 \cdot \sqrt{\frac{1-Sin\theta}{1+Sin\theta}} \tag{40}$$

$$F_{p2} = F_0 \cdot \sqrt{\frac{1+Sin\theta}{1-Sin\theta}} \tag{41}$$

θ is usually chosen to be 70º and this is about the maximum practical phase-lead obtainable from a lead compensator. The other zero of the compensator is chosen using the following formula:

$$F_{Z1} = 0.5 \times F_{Z2} \tag{42}$$

The approximate bode-plot of the power stage, the desired loop gain and the type III-B compensator has been drawn in Figure 13. Sometimes, the value of F_{p2} calculated by (41) falls above F_{p3}. The order of the poles is not important, however, the important fact is that there are always two compensator poles above F_0 as shown in Figure 13. F_{Z1} compensates the phase lag of the pole which is at origin. F_{Z2} and F_{p2} form a lead-compensator and provide their maximum leading phase at crossover frequency and F_{p3} provides further attenuation for frequencies above $F_S/2$.

Similar to the calculation for type III-A compensator, the parameters of the compensator can be calculated. That is, a value for C_{f3} is selected and then using (33) to (37) the parameters of the compensator are calculated.

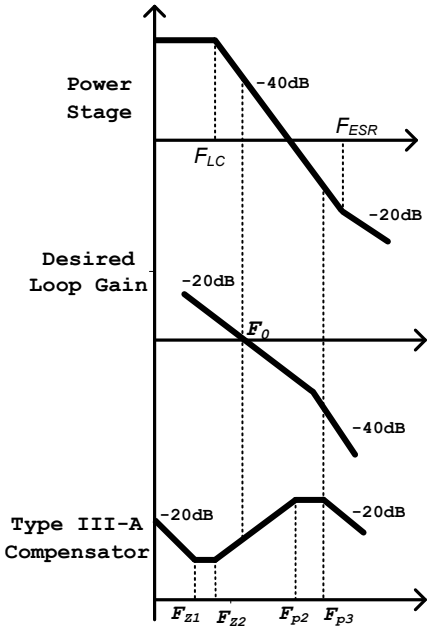

Figure 13 - Bode plot of the buck converter power stage, desired loop gain, and Type III-B compensator

5.4 Design example of Type III-B compensator

For this design, as shown in Figure 14, IR3842 regulator is used.

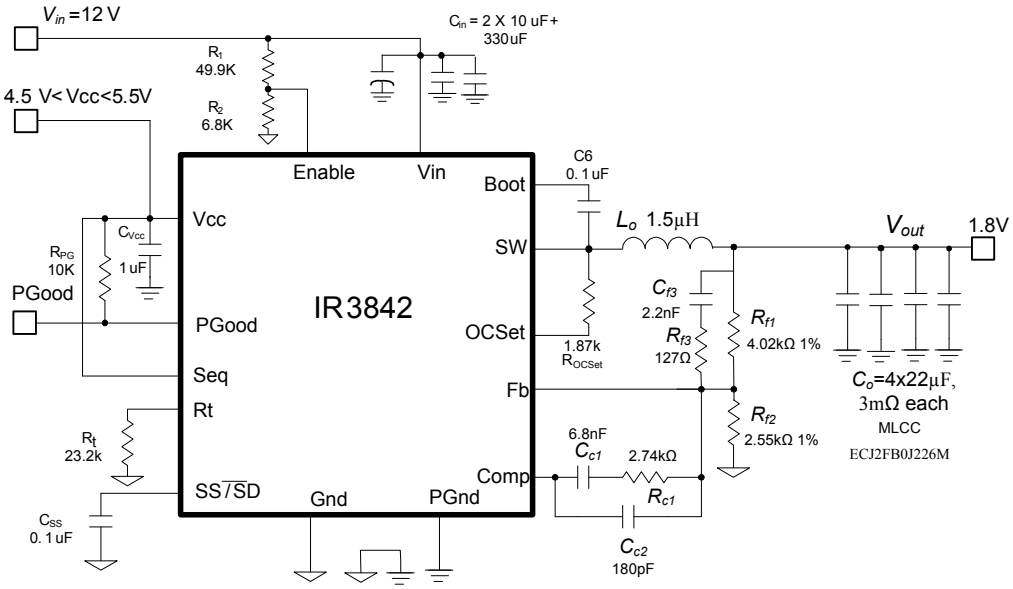

Figure 14 - Application of IR3842 with type III-B compensator for a 4A, 1.8V regulator

Step 1 - Collect the system information such as input and output voltage and the switching frequency:

$V_{in} = 12V$
$V_{Out} = 1.8V$
$V_{ref} = 0.7V$
$V_{osc} = 1.8V$
$L_o = 1.5\mu H$
$C_o = 4 \times 10.8\mu F$
$ESR(C_o) = 3m\Omega \ each$
$F_S = 600kHz$
$I_o(max) = 4A$

It should be noted here that the value of the capacitance used in the compensator design must be the small signal value. Ceramic capacitors lose some portion of their capacitance as their biasing voltage increases. The MLCC capacitors which are used in this example have 22µF nominal capacitance. However, at the biasing voltage and 600kHz their capacitance drops to about 10.8µF. It is this value that must be used for all computations related to the compensation. The small signal value may be obtained from the manufacturer's datasheets, design tools or SPICE models [4]. Alternatively, they may also be inferred from measuring the power stage transfer function of the converter and measuring the double pole frequency (F_{LC}) and using equation (3) to compute the small signal value (refer to Appendix C).

Step 2 - Using (3) and (4) calculate the poles and zero of the power stage:

$$F_{LC} = \frac{1}{2\pi \times \sqrt{43.2\mu F \times 1.5\mu H}} = 19.7kHz$$

$$F_{ESR} = \frac{1}{2\pi \times 3m\Omega \times 10.8\mu F} = 4.9MHz$$

Step 3 - Selected crossover frequency to be 1/6 of the switching frequency:

$F_0 = 100kHz$

Step 4 - Select the type of compensator. Since $F_{LC} < F_0 < F_S/2 < F_{ESR}$, type III-B compensator is suitable for this application.

Step 5 - Calculate the poles and zeros of the compensator. Using (40) and (41):

$$F_{Z2} = 100kHz \cdot \sqrt{\frac{1-Sin70°}{1+Sin70°}} = 17.6kHz$$

$$F_{p2} = 100kHz \cdot \sqrt{\frac{1+Sin70°}{1-Sin70°}} = 567kHz$$

Using (42):

$$F_{Z1} = 0.5 \times 17.6kHz = 8.8kHz$$

Using (39):

$$F_{p3} = 600kHz / 2 = 300kHz$$

Step 6 - Calculate the values of the parameters of the compensator. Choose $C_{f3} = 2.2nF$.

Using (33):

$$R_{f3} = \frac{1}{2\pi \cdot 2.2nF \cdot 567k} = 127.6\Omega$$

Choose $R_{f3} = 127\Omega$. Use (34) to calculate R_{f1}:

$$R_{f1} = \frac{1}{2\pi \cdot 2.2n \cdot 17.6k} - 127 = 3.98k\Omega$$

Select $R_{f1} = 4.02k\Omega$. Using (14), R_{f2} can be calculated:

$$R_{f2} = \frac{4.02k\Omega \times 0.7V}{(1.8V - 0.7V)} = 2.56k\Omega$$

Choose $R_{f2} = 2.55k\Omega$. Use (35) to calculate R_{C1}:

$$R_{C1} = \frac{2\pi \cdot 100k \cdot 1.5\mu \cdot 43.2\mu \cdot 1.8}{12 \cdot 2.2n} = 2.77k\Omega$$

Choose $R_{C1} = 2.74k\Omega$. Use (36) to calculate C_{C1}:

$$C_{C1} = \frac{1}{2\pi \cdot 2.74k \cdot 8.8k} = 6.6nF$$

Choose $C_{C1} = 6.8nF$. Use (37) to calculate C_{C2}:

$$C_{C2} = \frac{1}{2\pi \cdot 2.74k \cdot 300k} = 193pF$$

Choose $C_{C2} = 180pF$. The bode plot of the loop has been sketched in Figure 8 which shows the closed loop system has a crossover frequency of $F_0 \approx 105kHz$ and the phase-margin of about 51º.

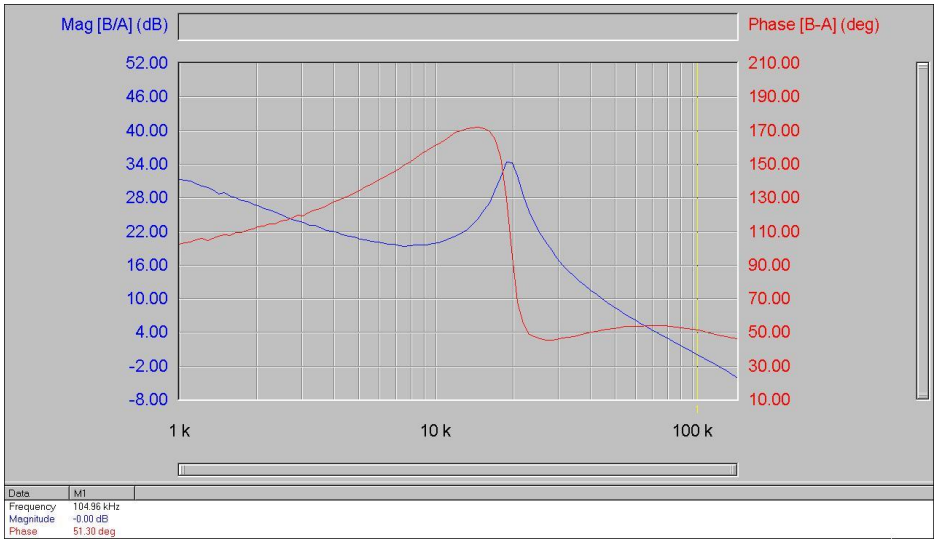

Figure 8 - The bode plot of the loop for the example with Type III-B compensator

6. Conclusion

The control loop design based on regular voltage-mode error-amplifier was discussed for synchronous buck converter. When electrolytic capacitor or low performance tantalum capacitors are used a simple type II compensator can be employed. For ceramic, or high performance POS-cap or SP-Cap output capacitors, a type III compensator is usually required. Although IR3840 and IR3842 regulators were taken as examples in this application note, the proposed design method also applies to applications using other types of buck regulator/control ICs which utilize a voltage-mode error-amplifier.

References

[1] M. Qiao, P. Parto, and R. Amirani, "Stabilize the Buck Converter with Transconductance Amplifier," *IR-application note AN-1043*, 2002.

[2] Ned Mohan, Tore M. Undeland, and William P. Robbins, *Power Electronics: Converters, Applications, and Design*, New York: John Wiley & Sons, ISBN: 0-471-22693-9, 2003.

[3] R. W. Erickson, D. Maksimovic, *Fundamentals of Power Electronics*, New York: Springer Science + Business Media, ISBN: 978-0-7923-7270-7, 2001.

[4] P. Asadi, Y. Chen, P. Parto, "Optimal Utilization of Multi Layer Ceramic Capacitors for Synchronous Buck Converters in Point of Load Applications", *PCIM China*, Shanghai, China, June 2010, pp. 233-237.

Appendix A: Designing the Power Stage of the Synchronous Buck Converter

The first step in designing a switching DC/DC converter is designing the power stage. The power stage includes the output LC filter of the converter as well as the switches and their drivers. Many factors are involved in designing the power stage including, efficiency, cost, space, EMI, acceptable output voltage ripple, transient response requirement, etc. The design requirements usually compete with each other. For example, to decrease the output voltage ripple the designer might increase the value of the inductor and/or capacitor. Increasing the value of the capacitor increases the cost and increasing the value of the inductor can decrease the efficiency and can make the transient response slower. On the other hand, the output voltage ripple can be decreased by increasing the switching frequency. However, higher switching frequency may result in less efficiency due to increased switching losses. Therefore, the designer has to find a trade off between different design requirements by going through a few design iterations.

Switching frequency is usually the first parameter which is selected. In selecting the switching frequency different factors including efficiency, EMI requirements, required closed-loop bandwidth, etc are involved. The switching frequency might even be dictated by the system that the converter is going to be a part of.

In this appendix the procedure of designing the power stage is briefly discussed with an example.

Suppose that the switching frequency as well as the maximum output current and the input and output voltages are given. Depending on the maximum output current the appropriate switching regulator is selected. The list of IR's integrated switching regulators and their specifications can be found on IR's website. Among the design requirements, usually the inductor ripple current is given. If not, starting with a 40% current ripple is reasonable:

$$I_{Lripple} = 40\% \times I_{Load\_Max} \tag{A1}$$

The inductor value can be calculated using the following equation:

$$L_o = \frac{V_{in} - V_{out}}{I_{Lripple}} \cdot \frac{V_{out}}{V_{in}} \cdot \frac{1}{F_S} \tag{A2}$$

The amplitude of the overshoot/undershoot of the transient response of the converter as well as the output voltage ripple determine the value of the output capacitor. The amplitude of the switching ripple is usually much smaller than the permissible value if an appropriate output capacitor combination is utilized. The minimum required amount of output capacitor is given by the following equation:

$$C_{o\_Min} = \frac{L_o \times I_{Load\_Step}^{\ 2}}{2 \cdot V_{out} \times \Delta V_{out\_Max}} \qquad \text{(A3)}$$

where I_{Load_Step} is the maximum step load in Amps and ΔV_{out_Max} is the maximum permissible output voltage change due to transients/switching. Equation (A3) is based on having ideal output capacitors (no ESR) and infinite control-loop band-width. The required amount of output capacitance is usually higher than the value given by (A3) especially when the output capacitors have a considerable amount of ESR. However, the value calculated by (A3) is a good starting point to choose the output capacitor. Suppose the designer intends to use a type of capacitor with the value of C_E. If the ESR of the capacitor could be neglected, the number of capacitors which is required would have been:

$$N_{Min}(ESR = 0) = C_{o\_Min} / C_E \qquad \text{(A4)}$$

However, if each capacitor has an ESR equal to ESR_E, the minimum number of required capacitors to have a satisfactory transient response is:

$$N_{Min} = \frac{ESR_E}{\Delta V_{out\_Max}} \times I_{Load\_Step} + \frac{V_{out}}{2 \cdot C_E \times L_o \times \Delta V_{out\_Max}} \cdot \left(\frac{L_o \times I_{Load\_Step}}{V_{out}} - ESR_E \times C_E\right)^2 \qquad \text{(A5)}$$

Usually the first integer which is greater than the value given by (A5) should be considered. For more information about (A5) refer to [A1].

The input capacitor of the converter should be able to handle the input current ripple:

$$I_{in\_ripple} = I_{Load\_Max} \cdot \sqrt{D \cdot (1 - D)} \qquad \text{(A6)}$$

where D is the duty cycle of the converter. If the input capacitor is comprised of multiple capacitors connected in parallel, we have:

$$C_{in} = N_{in} \times C_{E\_in} \qquad \text{(A7)}$$

If the current ripple that each of the capacitors can handle is given by $I_{C\_ripple\_max}$, then the number of capacitors which should be parallel to form C_{in} are:

$$N_{in} = \frac{I_{in\_ripple}}{I_{C\_ripple\_max}} \tag{A8}$$

It is worth mentioning that values of capacitors change as temperature, bias voltage, and operating frequency change. For example MLCC capacitors lose a considerable portion of their capacitance as their bias voltage is increased. Therefore, in all calculations throughout this document the effective value of the capacitors at the given operating condition should be considered.

Design example of power stage

Consider the following data is given:

$$\begin{aligned} V_{in} &= 12V \\ V_{out} &= 1.8V \\ F_S &= 600KHz \\ I_{Load\_Max} &= 12A \\ I_{Load\_Step} &= 6A \\ \Delta V_{out\_Max} &= 54mV \\ I_{Lripple} &= 4.55A \end{aligned} \tag{A9}$$

Using (A2) the value of the inductor is calculated:

$$L_o = \frac{12-1.8}{4.55} \cdot \frac{1.8}{12} \cdot \frac{1}{600K} = 560nH \tag{A10}$$

Using (A3) the minimum required output capacitance is calculated:

$$C_{o\_Min} = \frac{560n \times 6^2}{2 \cdot 1.8 \times 54m} = 103\mu F \tag{A11}$$

Suppose the following capacitors are going to be used:

$$\begin{aligned} C_E &= 330\mu F \\ ESR_E &= 12m\Omega \end{aligned} \tag{A12}$$

Since $C_E > C_{o\_Min}$, it seems that one capacitor should be enough, however using (A5) suggests:

$$N_{Min} = \frac{12m}{54m} \times 6 + \frac{1.8}{2 \cdot 330\mu \times 560n \times 54m} \cdot (\frac{560n \times 6}{1.8} - 12m \times 330\mu)^2 = 1.7 \quad \text{(A13)}$$

Therefore, 2 capacitors with the specifications given in (A12) should be used:

$$C_o = 2 \times 330\mu F = 660\mu F$$
$$ESR = \frac{12m\Omega}{2} = 6m\Omega \quad \text{(A14)}$$

Suppose the capacitors which are going to be used in input side are 3.3µF capacitors which can handle a maximum of 1.3A. The input current ripple is:

$$I_{in\_ripple} = 12 \cdot \sqrt{1.8/12 \cdot (1 - 1.8/12)} = 4.28Arms \quad \text{(A15)}$$

$$N_{in} = 4.28/1.4 = 3.3 \quad \text{(A16)}$$

Therefore, the minimum numbers of capacitors which should be paralleled at the input are 4 capacitors.

References:

[A1] C. Qiao, J. Zhang, P. Parto, and D. Jauregui, "Output Capacitor Comparison for Low Voltage High Current Applications," in *Proc. IEEE 35th Power Electronics Specialists Conference*, Aachen, Germany, June 2004, pp. 622-628.

Appendix B: Some Special Cases of Compensator Design

The guidelines provided earlier in this document on compensator design are general guidelines which result in appropriate values for the compensator parameters in most cases. However, sometimes fine tuning might be desirable. That is, the designer might want to adjust the locations of the zeros and poles of the compensator (by a few design iterations) to get better/optimized results. There might be extreme conditions where fine tuning is necessary. In this appendix, one extreme condition in which the designer must adjust the compensation is discussed by an example.

In some extreme conditions, the values of inductor and capacitor in the power stage may become too large so that the resonance frequency, F_{LC}, becomes too low compared to the cross over frequency (F_0). In such conditions, if the compensator type III-B is used, the resulting bode-plot of the loop might not be appropriate. Therefore, some modifications in the design procedure are required. Such cases are demonstrated by an example.

Consider a synchronous buck converter with the parameters given by (B1). The designer has been conservative in keeping the inductor current ripple and output voltage ripple/transient very low.

$$
\begin{aligned}
&V_{in} = 16V \\
&V_{out} = 2.5V \\
&V_{ref} = 0.7V \\
&V_{osc} = 1.8V \\
&L_o = 4.7\mu H \\
&R_{Lo} = 13m\Omega \\
&C_o = 9 \times 47\mu F \\
&ESR(C_o) = 3m\Omega \ each \\
&F_S = 600KHz \\
&I_{O\_Max} = 2A \\
&F_0 = 100kHz
\end{aligned}
\qquad \text{(B1)}
$$

At the specified output voltage, the effective value of each output capacitor is about 16µF. Therefore:

$$F_{LC} = \frac{1}{2\pi \cdot \sqrt{4.7\mu H \cdot 9 \times 16\mu F}} = 6.12kHz \quad \text{(B2)}$$

$$F_{ESR} = \frac{1}{2\pi \cdot 16\mu F \cdot 3m\Omega} = 3.3M\Omega \quad \text{(B3)}$$

Since $F_{LC} < F_0 < F_S / 2 < F_{ESR}$, type III-B compensator is used.

Using (39)-(42) the poles and zeros of the compensator are calculated as follows:

$$F_{Z2} = 100kHz \cdot \sqrt{\frac{1 - Sin70°}{1 + Sin70°}} = 17.6kHz \quad \text{(B4)}$$

$$F_{p2} = 100kHz \cdot \sqrt{\frac{1 + Sin70°}{1 - Sin70°}} = 567kHz \quad \text{(B5)}$$

$$F_{Z1} = 0.5 \times 17.6kHz = 8.8kHz \quad \text{(B6)}$$

$$F_{p3} = 600kHz / 2 = 300kHz \quad \text{(B7)}$$

Now the values of the parameters of the compensator are calculated. If the value of $2.2nF$ is selected for C_{f3}, the following values are resulted:

$$R_{f3} = \frac{1}{2\pi \cdot 2.2nF \cdot 567k} \approx 127\Omega \quad \text{(B8)}$$

$$R_{f1} = \frac{1}{2\pi \cdot 2.2n \cdot 17.6k} - 127 \approx 4.02k\Omega \quad \text{(B9)}$$

$$R_{C1} = \frac{2\pi \cdot 100k \cdot 4.7\mu \cdot 144\mu \cdot 1.8}{16 \cdot 2.2n} \approx 21.5k\Omega \quad \text{(B10)}$$

$$C_{C1} = \frac{1}{2\pi \cdot 8.8k \cdot 21.5k} \approx 0.82nF \quad \text{(B11)}$$

$$C_{C2} = \frac{1}{2\pi \cdot 21.5k \cdot 300k} \approx 24pF \quad \text{(B12)}$$

It is noticed that the value of R_{C1} is relatively large (>20kΩ) whereas C_{C1} and C_{C2} are relatively small. If a larger value for C_{f3} had been chosen, more reasonable values for R_{C1}, C_{C1}, and C_{C2} would have been resulted. Apart from this, considering the bode plot of the loop, which is obtained by simulation and is presented in Figure B1, it is clear that the behavior of the phase of the loop is not appropriate. The phase drops to below 0º at about 9kHz which makes the system conditionally stable.

It should be noted that the bode-plot sketched in Figure B1 is based on the average model for the buck converter. Therefore, it is valid only up to half of the switching frequency.

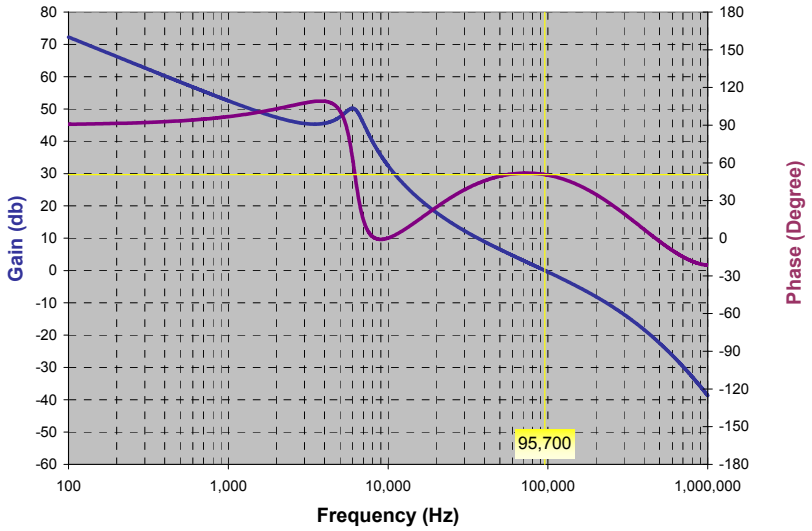

Figure B1 - The bode plot of the loop for the example with Type III-B compensator shows a bandwidth of 95.7kHz and a phase margin of 50º

The reason for the phase drop at about 9kHz is that the pole and zero selection has been done to secure enough phase-margin at the loop cross-over frequency. The cross-over frequency is much higher than the resonance frequency (F_{LC} or double-pole frequency). Consequently, both zeros of the compensator are above the resonance frequency where the double pole causes 180 degrees phase-drop. Technically, it is required to have the zeros at about F_{LC} or even at lower frequencies. Therefore, when the procedure of type III-B compensator design is followed, if the calculated zeros of the compensator are both above F_{LC}, modifications in the procedure are required as follows:

- Design for lower loop Bandwidth (1/10 of the switching frequency).

- Place the zeros of the compensator according to type III-A compensator design procedure.

There are two reasons to design for lower loop bandwidth. First, due to relatively large value of the selected output capacitors, usually there is no need to design for a high loop

bandwidth to achieve satisfactory transient response. Second, when the resonance frequency of the regulator is much lower than the designed loop bandwidth, a relatively high gain-bandwidth is demanded from the error amplifier. Therefore, to avoid running into the gain-bandwidth-product limitation of the error amplifier, it is recommended to design for a lower loop bandwidth. In this case, we design the loop for a BW of 60kHz.

Placing the zeros of the compensator according to the type III-A compensator design procedure, moves the zeros to lower frequencies. This, in turn, reduces the gain at low frequencies. However, according to Figure B1, the low-frequency gain is relatively large (G(100Hz)>60dB), therefore, reducing the low-frequency gain is acceptable. Equations (B5) or (41) can still be used to calculate the location of the second pole of the compensator. The poles and zeros of the compensator which is going to be designed are:

$$F_{Z2} = 6.2kHz \tag{B13}$$

$$F_{p2} = 340kHz \tag{B14}$$

$$F_{Z1} = 0.75 \times 6.2kHz = 4.65kHz \tag{B15}$$

$$F_{p3} = 600kHz / 2 = 300kHz \tag{B16}$$

The design procedure is started with $C_{f3} = 2.2nF$. Now, the values of the components can be calculated:

$$\begin{aligned} C_{f3} &= 2.2nF \\ R_{f3} &= 215\Omega \\ R_{f1} &= 11.5k\Omega \\ R_{f2} &= 4.42k\Omega \\ R_{C1} &= 12.4k\Omega \\ C_{C1} &= 2.7nF \\ C_{C2} &= 43pF \end{aligned} \tag{B17}$$

With the above component values for the compensator, the bode plot of the loop is measured and presented in Figure B2. The bode plot shows that the phase-dip around 9kHz does not go below 45º and the phase margin has increased by 9º.

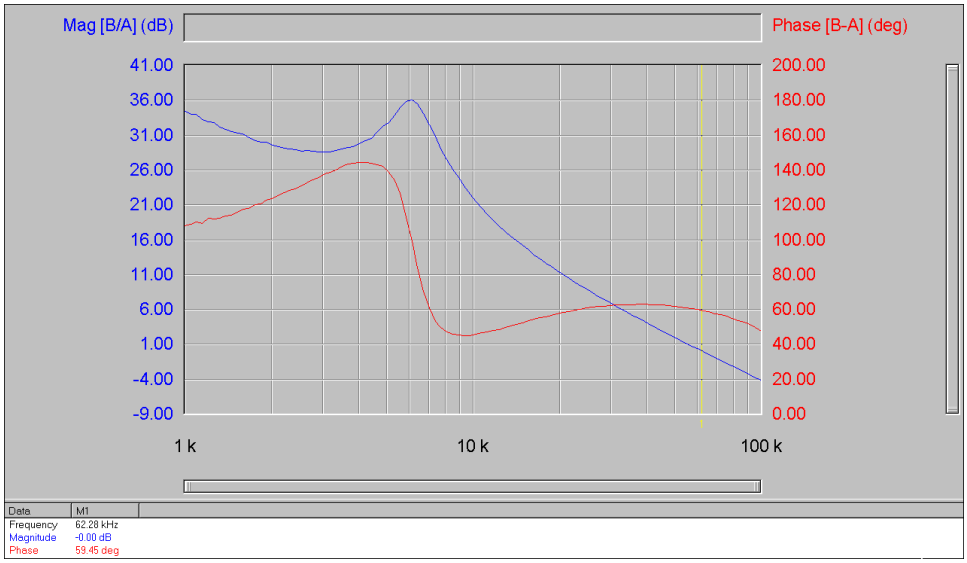

Figure B2 - The bode plot of the loop for the example with modified Type III compensator shows a bandwidth of 62kHz and a phase margin of 59º

Appendix C: Loop Response Measurement

A properly measured loop response will allow measurement of control bandwidth and phase margin. In addition, it allows estimation of actual or effective output capacitance in a circuit. Control bandwidth indicates the speed of the system in responding to load transients and phase margin is a very important indication of robustness of stability of the closed loop system.

A PWM DC-DC converter exhibits time-varying effects above half of the switching frequency and any measurements at such frequencies have no basis for comparison with averaged model designs and predictions which do not account for the time-varying effects. This implies that it does not serve any purpose to measure the loop response at frequencies approaching or exceeding half of the switching frequency.

At very low frequencies and at very high frequencies, the measurement is susceptible to noise, because of the very high and very low loop gains respectively. For typical values of L and C used in POL designs, the LC resonant poles lie between 1 kHz and 30 kHz, and any loop measurement must clearly show this region. For a switching frequency of 600 kHz, used in IR's integrated buck regulator designs (***SupIRBuck***™) for most POL applications, loop response measurement in the range of 1kHz -150 kHz is sufficient.

Figure C1 shows the general schematic for a family of ***SupIRBucks***. This schematic is used to show how the loop response in measured. The measurement technique can similarly be used for any other IR's ***SupIRBucks***. The three test points (A, B, and C) which are used for loop-response measurement have been indicated by solid circles. To measure the loop response the following steps should be taken:

- Using a network analyzer, apply a 15mV-30mV perturbation signal between test points A and B.
- Set up the network analyzer to measure v(B)/v(A).
- Set the frequency range of measurement between 1 kHz and 150 kHz.
- Measure the control bandwidth as the frequency at which the loop gain response crosses 0 dB.

- Measure the phase margin as the loop phase response at the loop gain crossover frequency.

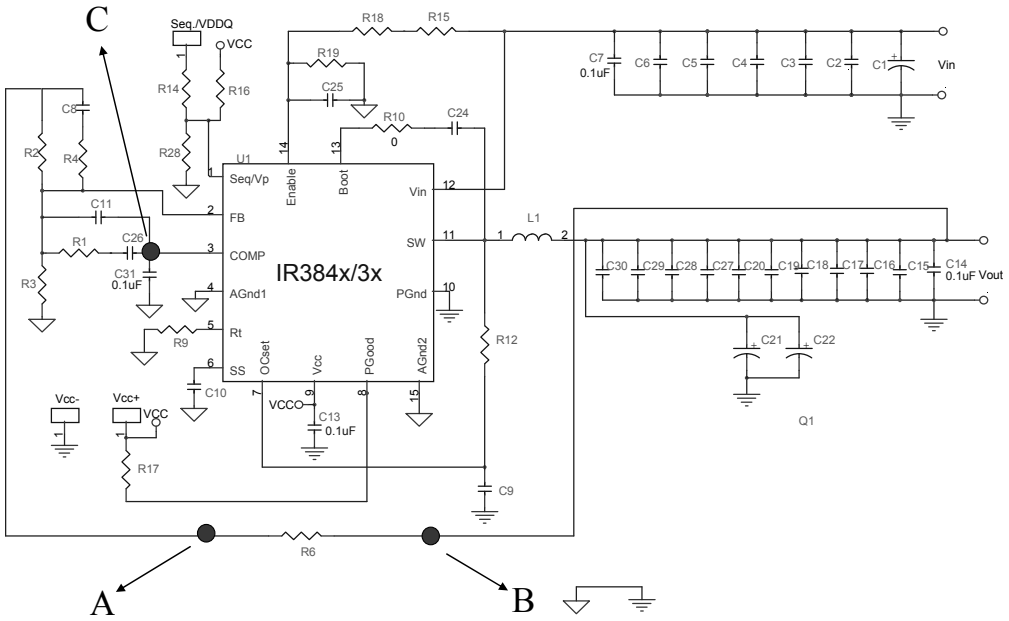

Figure C1 - The typical schematic of a family of IR's ***SupIRBucks*** and the associated test points which are used for frequency response measurements.

Figure C2 shows the result of a typical frequency response measurement. The figure shows that the control loop bandwidth is 100.98kHz and the phase-margin is 47.975º.

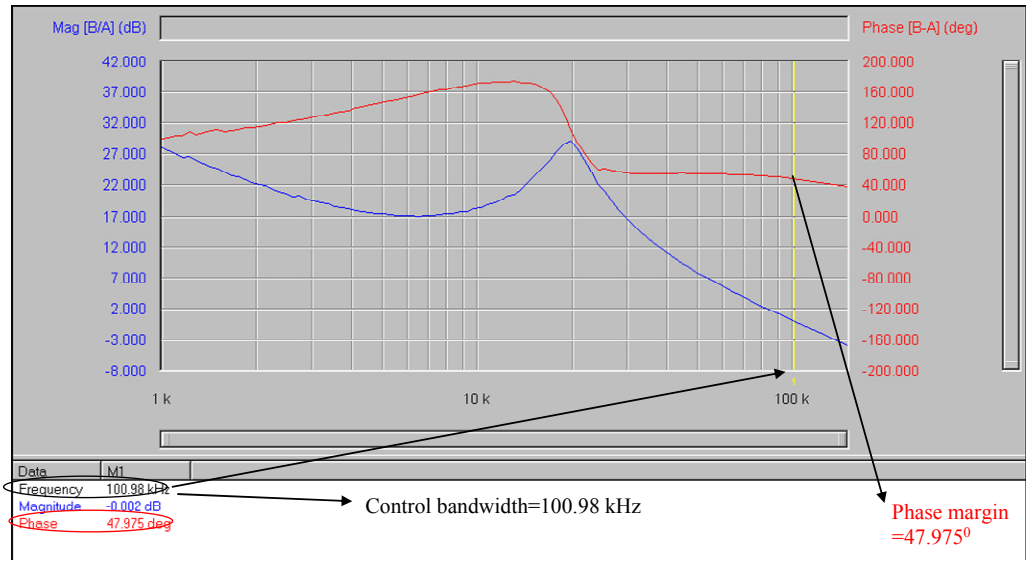

Figure C2 - The result of loop frequency-response measurement for a typical POL application which is the amplitude and phase of v(B)/v(A) versus frequency

Ideally the loop frequency response should not depend on the output current of the rail. However, due to the dead-times of the switches and some other factors, the frequency response changes with load current to some extent. Usually the loop response should be measured at nominal current of the rail. In addition, at the current that the loop response is measured the converter must operate without jitter.

Another frequency response which provides useful information is the power stage frequency response. To measure the frequency response of the power stage the following procedure should be followed:

- Using a network analyzer, apply a 15mV-30mV perturbation signal between test points A and B.
- Set up the network analyzer to measure v(B)/v(C).
- Set the frequency range of measurement between 1 kHz and 150 kHz.
- Measure the resonant frequency f_{LC} of the LC output filter.
- Measure the amplitude of the frequency response at low frequencies (G_Power_Stage_DC). This value is measured in dB scale.
- With L known, compute the effective value of output capacitance using (C1).
- Use (C2) to estimate the amplitude of the ramp signal in the modulator.

$$C_o = \frac{1}{4\pi^2 f_{LC}{}^2 L} \tag{C1}$$

$$V_{osc} = \frac{Vin}{10^{\left(\frac{G\_Power\_Stage\_DC}{20}\right)}} \tag{C2}$$

Using (C1) the effective / small-signal value of the output capacitance is obtained. This value should be used in all computations related to compensator design. Obtaining the effective value of the output capacitance is especially important when ceramic capacitors are used, since ceramic capacitors considerably loose their capacitance as bias voltage is increased. The small signal value of the output capacitors may also be obtained from the manufacturer's datasheets and design tools. The amplitude of the ramp signal, V_{osc}, is also required in the process of compensator design. This value can be obtained from the datasheet as well. Figure C3 shows the frequency response of a typical power stage.

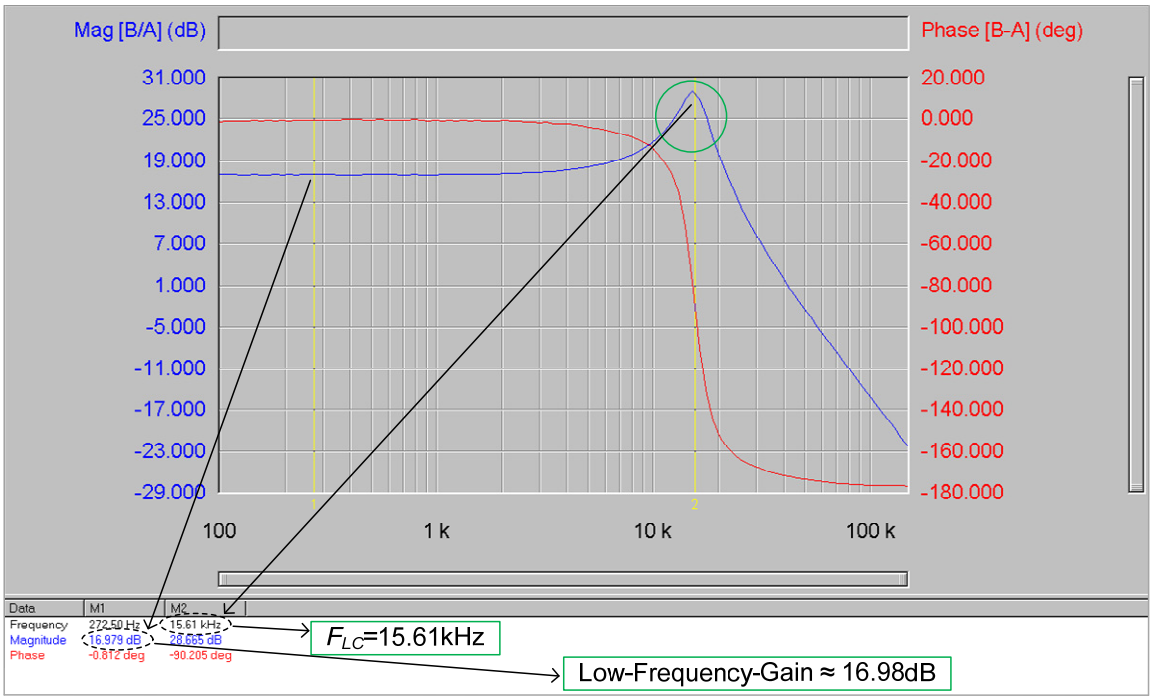

Figure C3 - The frequency response of a typical power stage showing the resonance frequency

If, for instance, a 1µH inductor is used, the effective value of the output capacitance is:

$$C_o = \frac{1}{4\pi^2 (15.61\text{kHz})^2 1\mu\text{H}} = 104\mu\text{F} \qquad \text{(C3)}$$

Figure C3 shows that at low frequencies the gain of the power stage is about 16.98dB. Therefore, assuming the input voltage is 12V, the amplitude of the ramp signal will be:

$$V_{osc} = \frac{12}{10^{(\frac{16.98}{20})}} \approx 1.7V \qquad \text{(C4)}$$