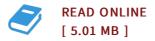




Chip Design for Submicron VLSI: CMOS Layout and Simulation

By Uyemura, John P.

Cengage Learning, 2005. Book Condition: New. Brand New, Unread Copy in Perfect Condition. A+ Customer Service! Summary: Chapter 1. Installing the Microwind Software 1.1 Getting Started 1.2 Exploring Microwind 1.3 Installing Dsch 1.4 Plan of the Book 1.5 Some Important Details 1.6 References Chapter 2. Views of a Chip 2.1 The Design Hierarchy 2.2 Integrated Circuit Layers 2.3 Photolithography and Patter Transfer 2.4 Planarization 2.5 Electrical Characteristics 2.6 Silicon Characteristics 2.7 Overview of Layout Design 2.8 References 2.9 Exercises Chapter 3. CMOS Technology 3.1 Meet the MOSFETs 3.2 CMOS Fabrication 3.3 Submicron CMOS Processes 3.4 Process Technologies in Microwind 3.5 Masks and Layout 3.6 The Microwind MOS Generator 3.7 Chapter Summary and Roadmap 3.8 References 3.9 Exercises Chapter 4. Using a Layout Editor 4.1 Lambda-Based Layout 4.2 Rectangles and Polygons 4.3 The MOS Generator Revisited 4.4 Summary 4.5 Exercises Chapter 5. CMOS Design Rules 5.1 Types of Rules 5.2 The SCMOS Design Rule Set 5.3 FET Layout 5.4 References 5.5 Exercises Chapter 6. MOSFETs 6.1 MOSFET Operation 6.2 MOSFET Switch Models 6.3 The Square Law Model 6.4 MOSFET Parasitics 6.5 Comments on Devise Layout 6.6 References 6.7 Exercises Chapter 7. MOSFET Modeling with SPICE 7.1 SPICE Levels 7.2 MOSFET Modeling...



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