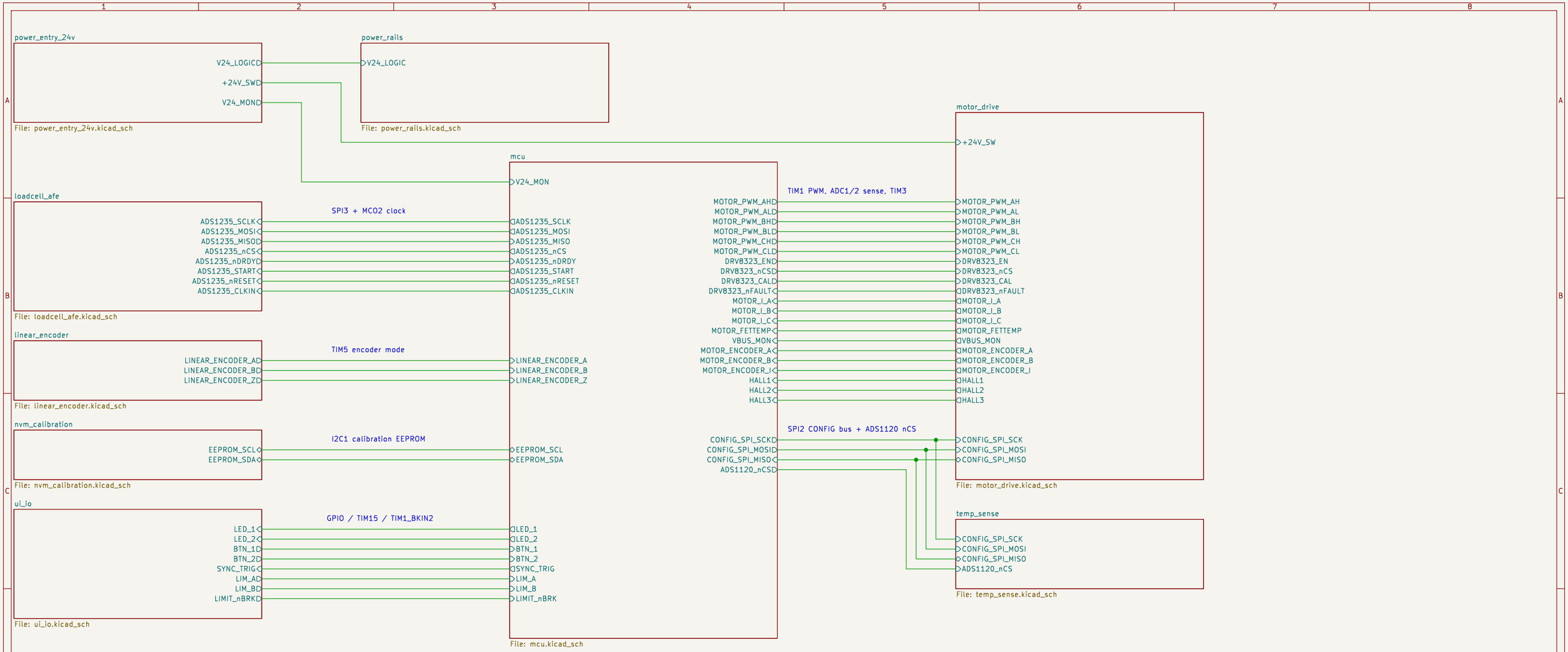


ROOT SHEET — THE BLOCK MAP, WIRED. DEC-0009 is closed.

Every net that crosses a block boundary is drawn: one sheet pin for each hierarchical label a child sheet declares, each one on a wire. Nothing on this sheet connects by name.

NINE BLOCKS, NOT TEN. test_debug was dissolved into the sheets its circuits serve: the SWD + USART3 header, the rail probe header and the GND hooks all moved onto mcu, so SWDIO, SWCLK, SWO, MCU_nRESET, DBG_TX and DBG_RX are sheet-local there and no longer cross a boundary. Test coverage lives on the circuit page it covers — docs/decisions/actuator-rev-testdebug.md.

GLOBAL POWER NETS CARRY NO SHEET PIN. GND, +5V, +5VA, +3V3 and +3V3A are Amodo power symbols and connect across the hierarchy on their own. power_rails produces all four and owns their PWR_FLAGs; power_entry_24v owns the flags for GND and +24V_SW. Only +24V_SW, V24_LOGIC and V24_MON leave power_entry_24v as ordinary nets, and they are drawn along the top of the sheet.

LAYOUT follows docs/FAFF-2-Electronics-Full.svg left to right: 24 V in at the top left, sensing and user I/O down the left column, the STM32H723VET6 in the middle, motor drive on the right. temp_sense sits under motor_drive rather than in the sensor column because it hangs off the same shared SPI2 CONFIG bus as the DRV8323 (ARCHITECTURE 5.1); the three bus wires are tapped once each, at the junctions between the two blocks. Its two probe channels stay inside its own sheet.

REFERENCE DESIGNATORS are allocated per sheet, 100 apart, from a fixed table — NOT from the page number, which changed when test_debug went: 2xx power_entry_24v, 3xx power_rails, 5xx loadcell_afe, 6xx linear_encoder, 7xx temp_sense, 8xx nvm_calibration, 9xx ui_io, 10xx mcu, 11xx motor_drive. 4xx is retired. Power symbols follow the same ranges (#PWR5xx, #PWR7xx, ...) so that no two sheets merge into one part at netlist time.

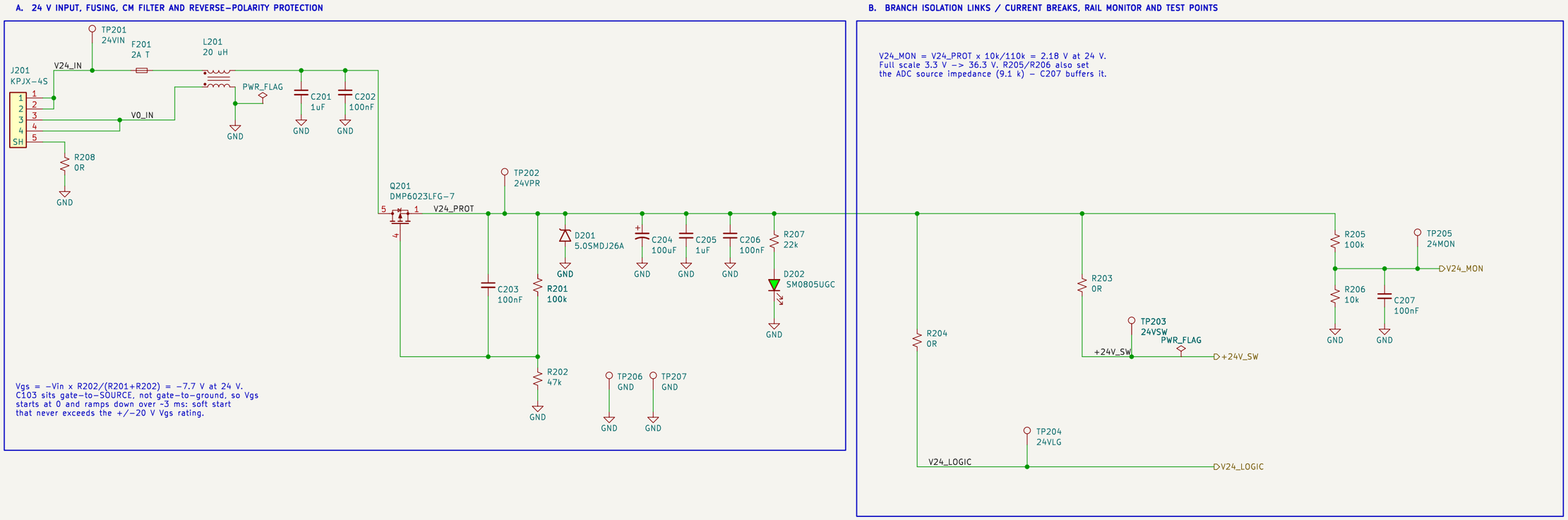
Requirements docs/REQUIREMENTS.md — architecture docs/ARCHITECTURE.md — decisions docs/DECISIONS.md and docs/decisions/actuator-sch-integrate.md — bring-up docs/TEST_PLAN.md

Decisions: docs/DECISIONS.md
Requirements: docs/REQUIREMENTS.md
Hierarchical block map, wired; see docs/ARCHITECTURE.md
Proof-of-concept control board — development-board form factor
Amodo Design

Sheet: /
File: faff2_cbs1.kicad_sch

Title: ARIA_SRB_FAFF_2 CBs_1 — Root

Size: A3	Date: 2026-09-03	**Rev: 0.2**
KiCad E.D.A. 9.0.8		Id: 1/10



BLOCK: power_entry_24v — 24 V DC input and protection (REQ-EL-01..04)

CHAIN J201 KPJX-4S (contacts doubled: 1,2 = +24 V, 3,4 = 0 V, 5 = shell)
-> F201 2 A time-lag (25 W peak = 1.04 A at 24 V; 2 A T holds 1.5 A)
-> L201 common-mode choke, both lines; board GND is defined on its load side
-> Q201 P-channel reverse-polarity series switch (drain = supply, source = load,
so the body diode blocks a reversed supply and nothing downstream conducts)
-> D201 TVS + C204..C206 bulk/HF -> V24_PROT, the protected 24 V bus.

BRANCHES (docs/TEST_PLAN.md 3.3 - each an isolation link AND a current break)
R203 -> +24V_SW : motor_drive only. Open R203 and the whole board can be
exercised with no possibility of the actuator moving.
R204 -> V24_LOGIC: power_rails only. Independent of R203.
One 0R link per branch serves as both the isolation link and the current
break; a second series part would add joints and no capability.

GROUND One GND net board-wide. AGND / DGND / PGND in the block stub notes are
layout partitions of it, not separate nets - see the decisions file.
This sheet owns the single GND PWR_FLAG; no other sheet may add one.

INTERFACES exported (hierarchical labels, wired to root sheet pins - DEC-0009)
OUT +24V_SW -> motor_drive OUT V24_LOGIC -> power_rails
OUT V24_MON -> mcu PC1 / ADC1_INP11
Global power nets used here: GND.

Reasoning, part sizing and residual ERC: docs/decisions/actuator-sch-power.md

Design reasoning: docs/decisions/actuator-sch-power.md
Requirements: REQ-EL-01..04 - docs/REQUIREMENTS.md
Independent motor / logic branch links (TEST_PLAN 3.3)
24 V in on KPJX-4S: fuse, CM choke, reverse polarity, TVS

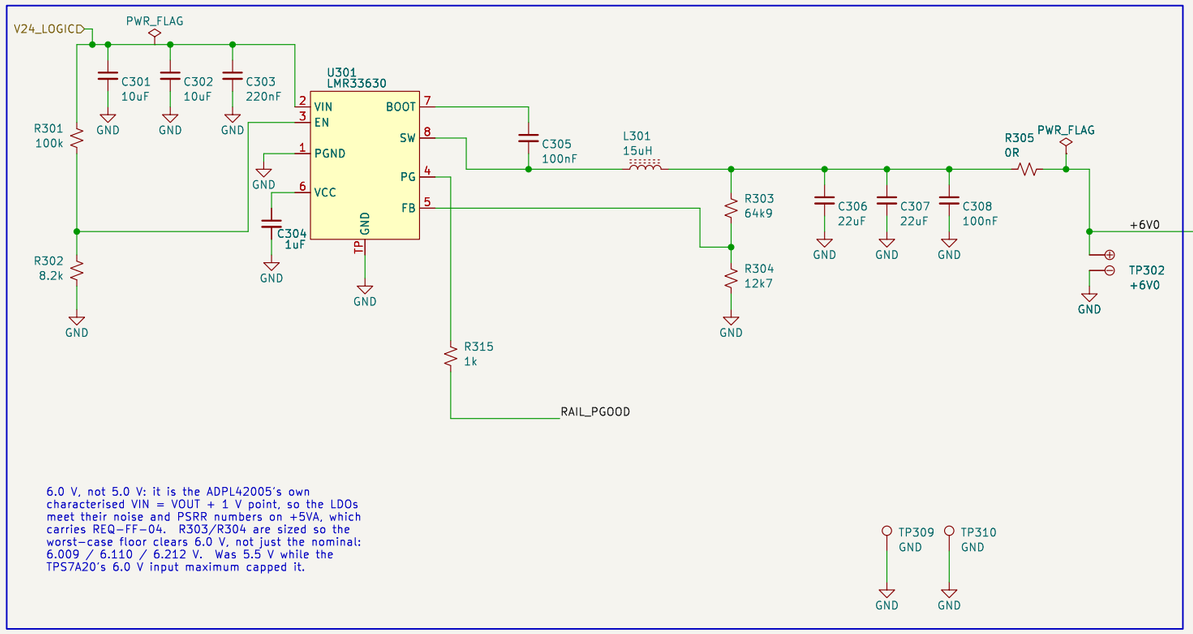
Amodo Design

Sheet: /power_entry_24v/
File: power_entry_24v.kicad_sch

Title: CBs_1 - Power Entry 24 V

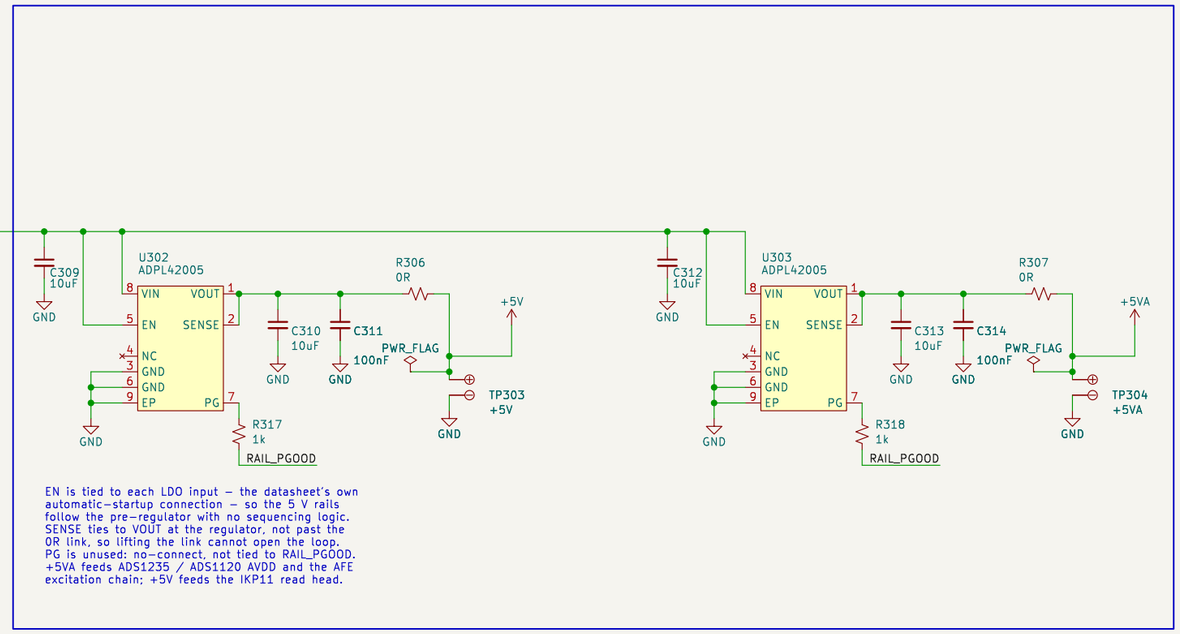
Size: A3	Date: 2026-09-02	Rev: 0.2
KiCad E.D.A. 9.0.8		Id: 2/10

A. PRE-REGULATOR V24_LOGIC -> 6.0 V (LMR33630, 400 kHz)



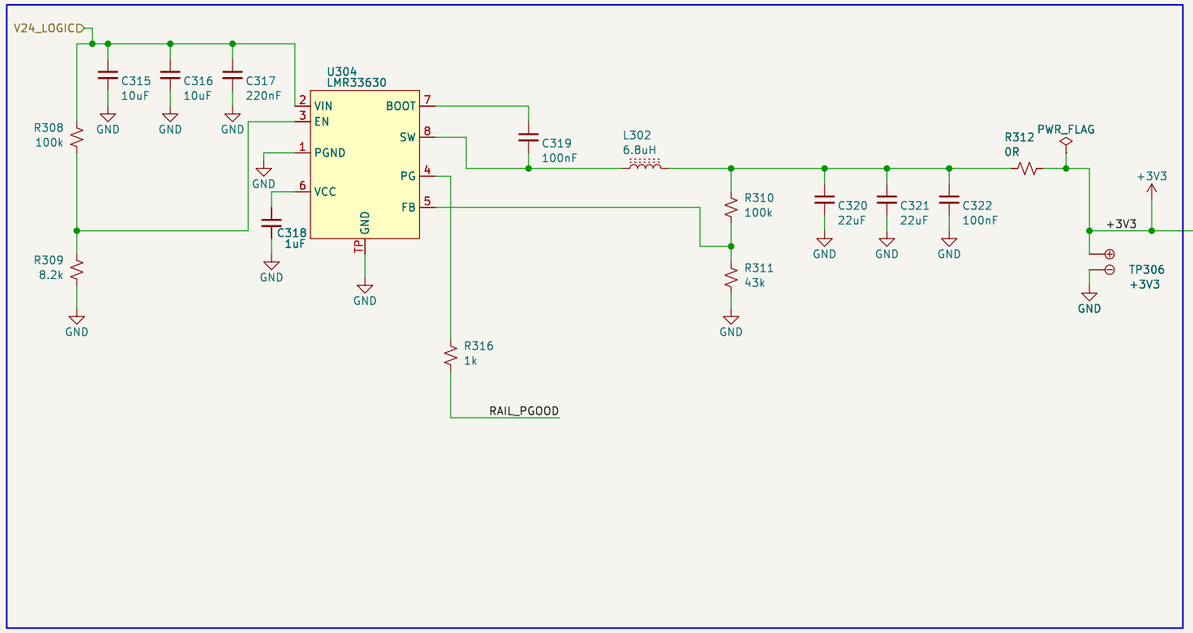
6.0 V, not 5.0 V: it is the ADPL42005's own characterised VIN = VOUT + 1 V point, so the LDOs meet their noise and PSRR numbers on +5VA, which carries REQ-FF-04. R303/R304 are sized so the worst-case floor clears 6.0 V, not just the nominal: 6.009 / 6.110 / 6.212 V. Was 5.5 V while the TPS7A20's 6.0 V input maximum capped it.

B. POST-REGULATED 5 V RAILS (ADPL42005: +5V digital, +5VA analog)

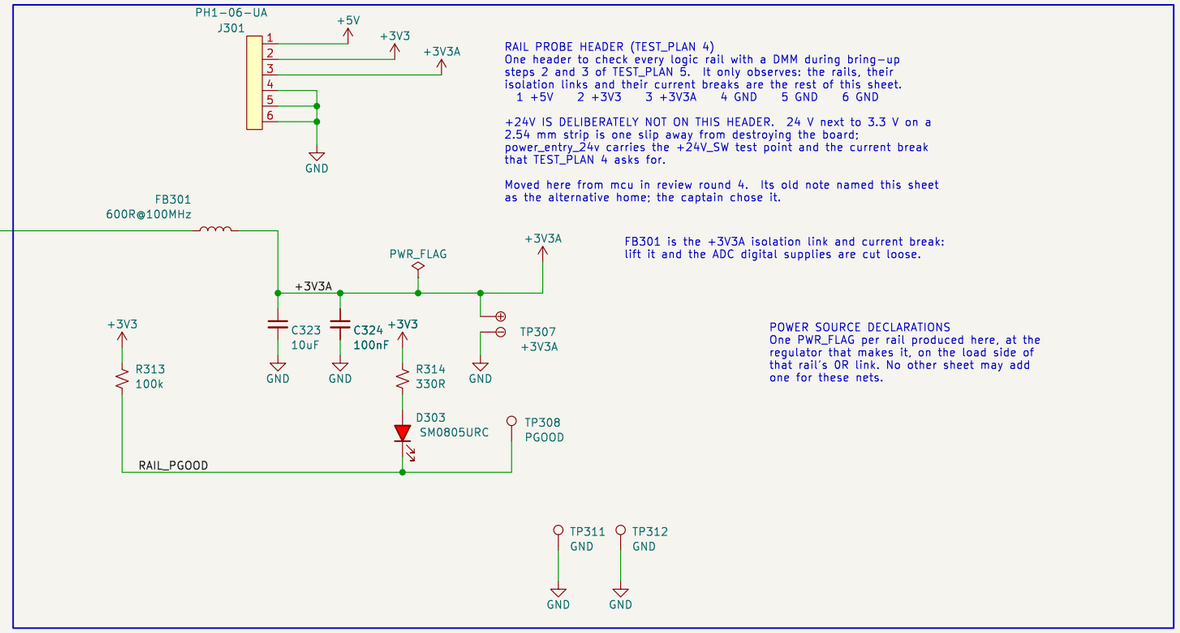


EN is tied to each LDO input — the datasheet's own automatic-startup connection — so the 5 V rails follow the pre-regulator with no sequencing logic. SENSE ties to VOUT at the regulator, not past the OR link, so lifting the link cannot open the loop. PG is unused: no-connect, not tied to RAIL_PGOOD. +5VA feeds ADS1235 / ADS1120 AVDD and the AFE excitation chain; +5V feeds the IKP11 read head.

C. 3V3 REGULATOR V24_LOGIC -> 3.3 V (LMR33630, 400 kHz)



D. ANALOG 3V3, RAIL POWER-GOOD, AND THE RAIL PROBE HEADER



RAIL PROBE HEADER (TEST_PLAN 4)
One header to check every logic rail with a DMM during bring-up steps 2 and 3 of TEST_PLAN 5. It only observes: the rails, their isolation links and their current breaks are the rest of this sheet.
1 +5V 2 +3V3 3 +3V3A 4 GND 5 GND 6 GND

+24V IS DELIBERATELY NOT ON THIS HEADER. 24 V next to 3.3 V on a 2.54 mm strip is one slip away from destroying the board; power_entry_24v carries the +24V_SW test point and the current break that TEST_PLAN 4 asks for.

Moved here from mcu in review round 4. Its old note named this sheet as the alternative home; the captain chose it.

FB301 is the +3V3A isolation link and current break: lift it and the ADC digital supplies are cut loose.

POWER SOURCE DECLARATIONS
One PWR_FLAG per rail produced here, at the regulator that makes it, on the load side of that rail's OR link. No other sheet may add one for these nets.

BLOCK: power_rails — rail set and topology; answers OQ-02 and OQ-07

RAILS +6V0 LMR33630 buck from V24_LOGIC. Pre-regulator only, local to this sheet.
+5V ADPL42005 LDO from +5V5. IKP11 read head (<65 mA plus RS-422 drive) and spare.
+5VA ADPL42005 LDO from +5V5. ADS1235 / ADS1120 AVDD and the AFE 5 V excitation and reference chain, which lives in loadcell_afe — take it from +5VA, not +5V.
+3V3 LMR33630 buck from V24_LOGIC. STM32, USB3320, DRV8323 logic, QSPI, EEPROM, RS-422 receiver, rotary encoder. ~1.1 A worst case against a 3 A part.
+3V3A ferrite-isolated from +3V3 for the ADC digital supplies.

WHY A PRE-REGULATOR The analog 5 V must be regulated separately from the digital 5 V or the read head switching current lands on the ADC supply, and an LDO needs headroom above 5 V to do it. One buck at 6.0 V feeding two LDOs costs one converter and post-regulates both 5 V rails. 400 kHz on both bucks: 3.3 V at 1.4 MHz would need a ~98 ns on-time, too close to the minimum.

PER RAIL (docs/TEST_PLAN.md 3.1) one OR link that is BOTH the isolation link and the current-measurement break, a test point downstream of it, on a dual pad so a scope ground clips beside the probe. No test point sits on a feedback node: R305 +5V5, R306 +5V, R307 +5VA, R312 +3V3, FB301 +3V3A. Per-CONSUMER links are not here: every block takes the same global rail net, so per-block breaks would need per-block rail names and would break the frozen block contracts. A block that wants one fits a OR at its own supply entry, inside its sheet.

SEQUENCING None required. The shared EN divider (16.2 V rising) holds both converters off until the 24 V input is real; the LDOs follow +5V5 and +3V3A follows +3V3.

INTERFACES IN V24_LOGIC <- power_entry_24v (owns its PWR_FLAG). RAIL_PGOOD is open drain, the wired-AND of all four regulators through R315 / R316 / R317 / R318. SHEET-LOCAL: LED D303, TP308 are its only consumers until OQ-07 allocates an MCU GPIO. Global power nets produced here: +5V, +5VA, +3V3, +3V3A. GND is board-wide, one net; power_entry_24v owns its PWR_FLAG.

Reasoning, part sizing and residual ERC: docs/decisions/actuator-sch-power.md

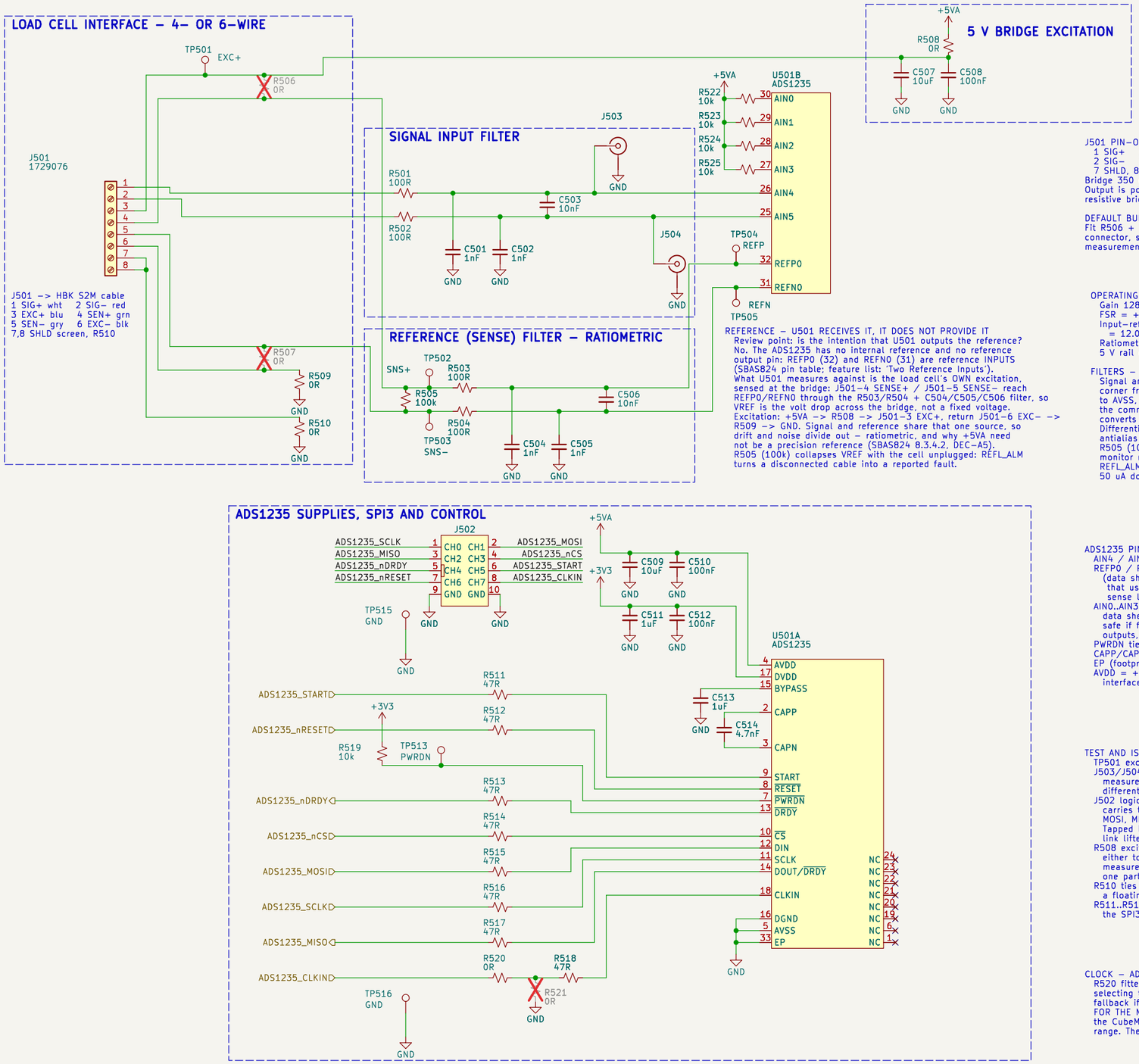
Design reasoning: docs/decisions/actuator-sch-power.md
Rail set and topology answer OQ-02 / OQ-07
Per-rail isolation link / current break and test point
24 V -> 5V5 pre-reg -> +5V and +5VA; 24 V -> +3V3 -> +3V3A

Amodo Design

Sheet: /power_rails/
File: power_rails.kicad_sch

Title: CBs_1 — Power Rails

Size: A3	Date: 2026-09-02	Rev: 0.2
KiCad E.D.A. 9.0.8		Id: 3/10



REFERENCE – U501 RECEIVES IT, IT DOES NOT PROVIDE IT
Review point: is the intention that U501 outputs the reference?
No. The ADS1235 has no internal reference and no reference output pin: REFP0 (32) and REFN0 (31) are reference INPUTS (SBAS824 pin table; feature list: 'Two Reference Inputs').
What U501 measures against is the load cell's OWN excitation, sensed at the bridge: J501–4 SENSE+ / J501–5 SENSE– reach REFP0/REFN0 through the R503/R504 + C504/C505/C506 filter, so VREF is the volt drop across the bridge, not a fixed voltage.
Excitation: +5VA –> R508 –> J501–3 EXC+, return J501–6 EXC– –> R509 –> GND. Signal and reference share that one source, so drift and noise divide out – ratiometric, and why +5VA need not be a precision reference (SBAS824 8.3.4.2, DEC–A5).
R505 (100k) collapses VREF with the cell unplugged: REFL_ALM turns a disconnected cable into a reported fault.

J501 PIN–OUT – HBK S2M SIX–WIRE CABLE (data sheet B03594, 2025–02–28)
1 SIG+ (white) 3 EXC+ (blue) 5 SENSE– (gray)
2 SIG– (red) 4 SENSE+ (green) 6 EXC– (black)
7 SHLD, 8 SHLD – cable screen / drain, tied to GND through R510
Bridge 350 ohm nominal, 2 mV/V, 5 V excitation –> +/–10 mV FS, -14.5 mA.
Output is positive in compression. The same terminal block accepts a resistive bridge simulator for bring–up step 6 of TEST_PLAN.md.

DEFAULT BUILD IS 6–WIRE (DEC–0014): R506 and R507 are DNP.
Fit R506 + R507 for a 4–wire cell. That ties SENSE+/– to EXC+/– at the connector, so the reference stops tracking the lead drop and the measurement loses Kelvin sensing – it is the lower–accuracy option.

OPERATING POINT (prelim calc Force sheet; ADS1235 SBAS824)
Gain 128, 4800 SPS, Sinc2, VREF = bridge excitation (ratiometric)
FSR = +/–VREF/128 = +/–39.06 mV (78.125 mV span) vs +/–10 mV signal
Input–referred noise 0.29 uVrms / 2.4 uVpp (data sheet table 1)
= 12.0 mNpp (V50N) / 2.4 mNpp (V10N) vs REQ–FF–04 20 / 5 mNpp
Ratiometric operation cancels excitation drift and noise, so the 5 V rail does not need to be a precision reference.

FILTERS – the ADS1235 data sheet figure 84 reference design.
Signal and reference filters are deliberately identical so their corner frequencies match: 100R series per leg, 1 nF C0G common mode to AVSS, 10 nF C0G differential. The differential capacitor is 10x the common–mode capacitors, so common–mode capacitor mismatch converts little common–mode noise into differential noise.
Differential corner ~76 kHz, common mode ~1.6 MHz; the ADC PGA antialias filter (C514, 4.7 nF C0G) is at 60 kHz.
R505 (100k) across the sense pair is the data sheet reference monitor resistor; it collapses VREF if the cable is unplugged so REFL_ALM asserts. It sits on the bridge side of R503/R504 so its 50 uA does not develop an error across the reference filter.

ADS1235 PIN USE
AIN4 / AIN5 = SIG+ / SIG– (bridge output, PGA gain 128)
REFP0 / REFN0 = SENSE+ / SENSE–, external reference, ratiometric (data sheet 8.3.4.2: "for 6–wire strain–gauge bridge applications that use excitation–sense connections, connect the excitation sense lines to the reference input pins")
AIN0..AIN3 unused – biased to AVDD through 10k (R522..R525) per data sheet 9.1.3. Resistors rather than a hard tie keep the pins safe if firmware ever configures them as GPIO or AC–excitation outputs, which are referenced to AVDD/AVSS.
PWRDN tied high through R519; reset by command or by ADS1235_nRESET.
CAPP/CAPN 4.7 nF C0G and BYPASS 1 uF to DGND are both mandatory.
EP (footprint pad 33) to AVSS.
AVDD = +5VA (also the excitation rail), DVDD = +3V3 so the serial interface sits at STM32 logic level.

TEST AND ISOLATION PROVISIONS (TEST_PLAN.md section 4)
TP501 excitation+ TP502/TP503 sense+/– TP504/TP505 ADC reference
J503/J504 U.FL on the ADC–side SIG+/SIG– nodes – the noise–floor measurement that decides REQ–FF–04. Placed symmetrically so the differential pair stays balanced (TEST_PLAN section 2.3).
J502 logic–analyser header (Amodo keyed 0.1in socket, 8510–4500PL) carries the whole digital interface on one plug: CH0..CH7 = SCLK, MOSI, MISO, nCS, nDRDY, START, nRESET, CLKIN; GND on 9 and 10. Tapped MCU–side of R511..R518, so it still sees the bus with a link lifted. TP513 (PWRDN) and TP515/TP516 GND hooks stay.
R508 excitation feed link and R509 excitation return link: open either to isolate the bridge, or replace one with a meter to measure excitation current (isolation link and current break in one part – see docs/decisions/actuator–sch–afe.md).
R510 ties the cable screen to GND at the connector; lift it to test a floating screen.
R511..R518 (47R) are the ADS1235 data sheet series terminators AND the SPI3 isolation links: remove one to take the ADC off the bus.

CLOCK – ADS1235_CLKIN COMES FROM STM32 MCO2 (REQ–AR–09)
R520 fitted = MCO2 drives CLKIN. R521 (DNP) instead grounds CLKIN, selecting the ADC internal 7.3728 MHz oscillator – a bring–up fallback if the MCO2 clock tree is not ready. Fit one, never both.
FOR THE MCU / FIRMWARE TASK: the .ioc leaves MCO2PinFreq_Value at the CubeMX default 64 MHz, outside the ADS1235 1..8 MHz CLKIN range. The clock tree must deliver 7.3728 MHz nominal on PC9.

Reasoning + root–sheet needs: docs/decisions/actuator–sch–afe.md
Requirements: REQ–FF–01..13, REQ–AR–08/09
HBK S2M 2 mV/V, +/–10 mV FS – one design serves V50N and V10N (DEC–0010)
ADS1235 gain 128, 4800 SPS Sinc2, 5 V ratiometric bridge excitation

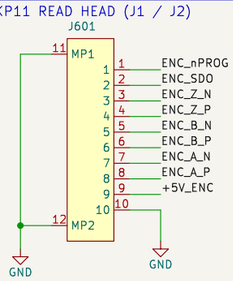
Amodo Design

Sheet: /loadcell_afe/
File: loadcell_afe.kicad_sch

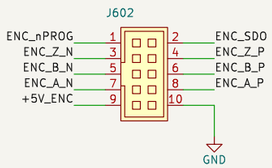
Title: CBs_1 – Load Cell AFE (ADS1235)

Size: A3	Date: 2026–09–02	**Rev: 0.1**
KiCad E.D.A. 9.0.8		Id: 4/10

IKP11 READ HEAD (J1 / J2)

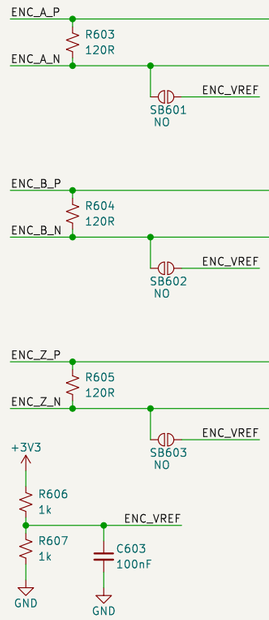


J1 – 10-way 0.5 mm FFC, the primary head connection. Mates the stock Bogen cable KABL-FFC-P0.5x10-L100 / -L300.

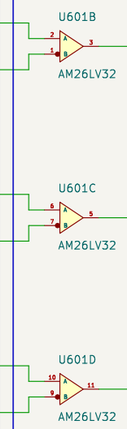


J2 – 2x5 1.27 mm shrouded header (REQ-PS-09). The same ten signals in parallel with J1, pin n = head pin n. Alternate head connection and the injection point of TEST_PLAN 4.

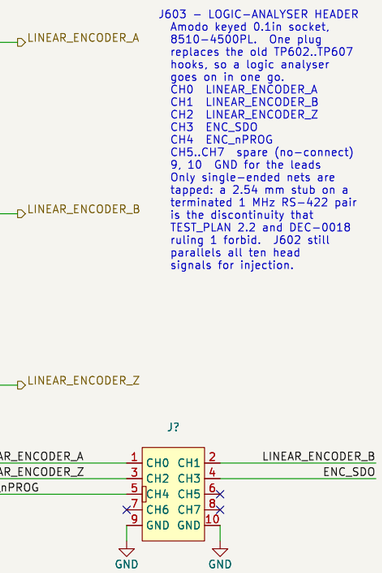
TERMINATION + MODE SELECT



RECEIVERS (U1)

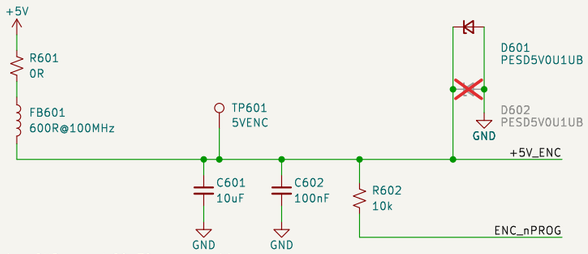


TO MCU – TIM5 (PA0/PA1/PA2)



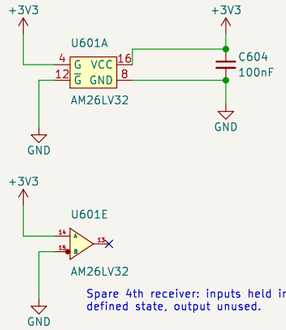
J603 – LOGIC-ANALYSER HEADER
Amodo keyed 0.1in socket, 8510-4500PL. One plug replaces the old TP602..TP607 hooks, so a logic analyser goes on in one go.
CH0 LINEAR_ENCODER_A
CH1 LINEAR_ENCODER_B
CH2 LINEAR_ENCODER_Z
CH3 ENC_SDO
CH4 ENC_nPROG
CH5..CH7 spare (no-connect)
9, 10 GND for the leads
Only single-ended nets are tapped: a 2.54 mm stub on a terminated 1 MHz RS-422 pair is the discontinuity that TEST_PLAN 2.2 and DEC-0018 ruling 1 forbid. J602 still parallels all ten head signals for injection.

5 V READ-HEAD SUPPLY + HEAD CONFIG



D602 is a DNP second SC-79 clamp position on D601 – a different clamp voltage, or a bidirectional part, without reworking D601's pads. Not fitted by default.
To meter head current, replace R601 with a shunt. To bypass the bead, lift FB601.
R601 is this block's current break (TEST_PLAN 3.1): lift it to meter the read head against the 200 mA the CALC power budget allows it – the head draws < 65 mA.
R602 holds !PROG inactive so the head can never fall into programming mode.

RECEIVER SUPPLY + SPARE CHANNEL



+3V3 / +5V / GND are generated in power_rails and enter this block through the hierarchy. Nothing here drives them, so ERC reports power_pin_not_driven until that sheet lands – see docs/decisions/actuator-sch-periph.md.

Spare 4th receiver: inputs held in a defined state, output unused.

BLOCK NOTES – linear_encoder

Ordered head: Bogen IKP11-Z1.4-P1-V5-D1-R0.5-F1000-C1 (DEC-0003, REQ-PS-05)
- Z1.4 periodic index from the pole pitch, 4 counts
- V5 5 V supply, < 65 mA
- R0.5 0.5 um resolution, post-quadrature
- C1 15.8 x 15.4 PCB: a 10-way 0.5 mm FFC connector AND a 1.27 mm pad row
- P1 1 mm pole pitch
- D1 RS-422 A/B/Z
- F1000 1 MHz per channel

HEAD PIN ORDER (datasheet rev 3.7 p.6 – same order on the FFC and the pads)
1 !PROG 2 SDO 3 /Z 4 Z 5 /B 6 B 7 /A 8 A 9 V+ 10 V-
Check the FFC cable contact side (type A / type D) against J1 before ordering – J1 is a bottom-contact receptacle. J2 needs no such check and is the fallback.

MODES
- RS-422, the ordered D1 build (default): R603/R604/R605 fitted, SB601/SB602/SB603 open. 120 R across each pair, as the head datasheet asks (Z0 = 120 R at the receiving end). No external fail-safe bias is needed: the AM26LV32 has open-circuit, shorted AND 100 R-terminated fail-safe, so an unplugged or dead head drives a static high – a stalled count, never phantom motion.
- Single-ended TTL / bench injection: remove R603/R604/R605, close SB601/SB602/SB603. Each inverting input then sits on ENC_VREF (1.65 V), so a 0-3.3 V or 0-5 V single-ended source on ENC_x_P decodes correctly. This covers a TTL head variant (order code D3) and injection through J2 with no read head fitted.

U1 runs from 3V3, so its outputs are native 3V3 logic (REQ-PS-06); its -0.3 V to +5.5 V input common-mode range accepts the 5 V head directly, and it switches to 32 MHz against the 1 MHz per channel of REQ-PS-07. Both enables are tied active: G (pin 4) high, /G (pin 12) low.

No test points sit on the differential pairs: a probe stub on a terminated 1 MHz RS-422 line is a discontinuity (TEST_PLAN 2.2), and the receiver outputs carry the same information single-ended. J603, the keyed logic-analyser socket, replaces the old TP602..TP607 hooks: CH0..CH4 = LINEAR_ENCODER_A / _B / _Z, ENC_SDO, ENC_nPROG, with GND on 9 and 10 for the ground leads. TP601 stays, a 1.0 mm SMT pad for a DMM on the 5 V head supply.

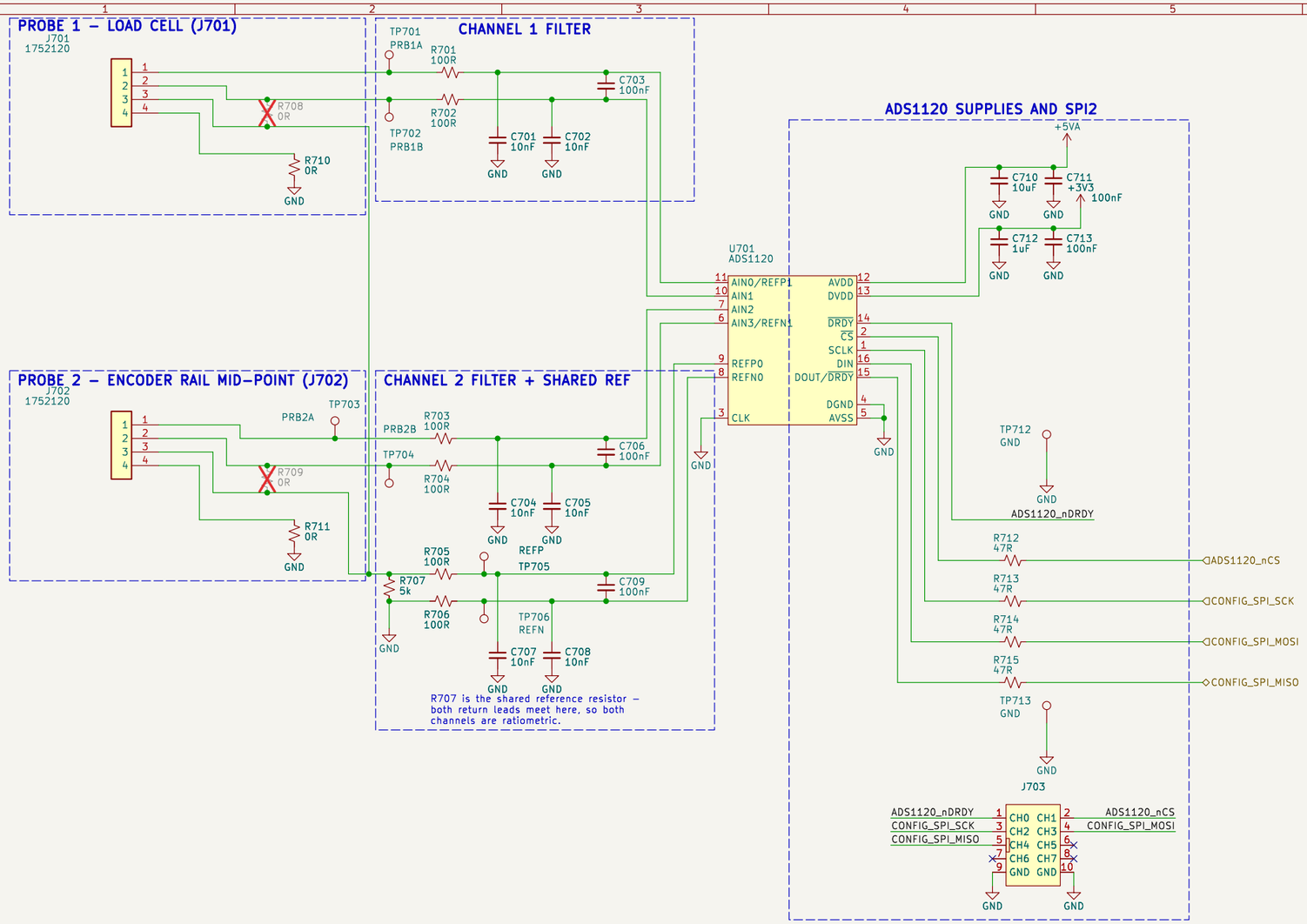
Test strategy: docs/TEST_PLAN.md
REQ-PS-01..10, REQ-AR-07, DEC-0003
RS-422 A/B/Z -> 3V3 into TIM5 (encoder mode TI12 + CH3 capture)
Bogen IKP11-Z1.4-P1-V5-D1-R0.5-F1000-C1 read head interface

Amodo Design

Sheet: /linear_encoder/
File: linear_encoder.kicad_sch

Title: CBs_1 – Linear Encoder (IKP11)

Size: A3	Date: 2026-09-02	Rev: 0.2
KiCad E.D.A. 9.0.8		Id: 5/10



OQ-04 RESOLVED: RTD, NOT NTC – Pt1000, 3-wire, class A (IEC 60751)
Chosen over an NTC because the ADS1120 exists to do exactly this: two matched IDACs give ratiometric excitation with automatic lead compensation, and a class-A RTD is accurate to +/-(0.15 + 0.002|t|) degC interchangeably – no per-part beta calibration, which an NTC would need to reach REQ-EL-07 1 degC. Pt1000 rather than Pt100 because every ohm of error in the signal path costs 10x less in degC; the house-stocked RTD_PT100_3W_D6X50_3M probe is a Pt100 and still works here – see the build options below.
A 2-wire probe (Pt1000, Pt100 or an NTC) is accommodated by fitting R708 / R709, which tie the sense lead to the return at the connector. Lead compensation is then lost; that is the lower-accuracy option.

RATIOMETRIC 3-WIRE MEASUREMENT (ADS1120 SBAS535D section 9.2.2)
IDAC1 -> the AIN carrying the A lead, IDAC2 -> the AIN carrying the B lead. Both currents return through the shared reference resistor R707, so VREF = (IDAC1 + IDAC2) x R707 and the conversion result is Code ~ R(RTD) x Gain / (2 x R707): independent of the IDAC value. Because IDAC1 and IDAC2 are matched, the drop in lead A cancels the drop in lead B and the lead resistance falls out.
This is the datasheet variant that routes the IDACs to the same pins used for measurement, which is what lets ONE ADS1120 and ONE reference resistor serve BOTH 3-wire RTDs (SBAS535D section 9.2.2: "even two 3-wire RTDs sharing the same reference resistor can be measured with a single device"). It requires the filter resistors R701..R704 to be small and well matched, hence 100R 0.1%.

DEFAULT BUILD – Pt1000	ALTERNATE BUILD – Pt100
IDAC1 = IDAC2 = 250 uA	IDAC1 = IDAC2 = 250 uA
R707 = 5k (fitted)	R707 = 5k (unchanged)
VREF = 2.5 V	VREF = 2.5 V
Gain 4, FSR +/-625 mV	Gain 32, FSR +/-78.1 mV
1039..1155 ohm over 10..40 C	103.9..115.5 ohm over 10..40 C
260..289 mV at the PGA	26..29 mV at the PGA

Only the ADS1120 register settings differ – no BOM or layout change.
Gain 4 (not 8) is deliberate: it keeps the input inside FSR up to +200 degC, so a probe on warm structure cannot silently over-range.
Resolution is still 0.02 degC, 50x better than REQ-EL-07 needs.

ERROR BUDGET AGAINST REQ-EL-07 (1 degC), Pt1000 build

Pt1000 class A at 40 degC	+/-0.23 degC
R707 tolerance 0.05%	+/-0.14 degC
R707 drift, 5 ppm/degC over +/-15 C	+/-0.02 degC
R701..R704 mismatch, 0.2 ohm worst	+/-0.05 degC
ADS1120 INL 20 ppm FSR	+/-0.02 degC
RSS total	+/-0.28 degC
Worst-case sum	+/-0.46 degC

ADC gain error (0.1% max) and IDAC mismatch (0.3% max) are gain terms: they are removed either by a one-point calibration into the nvm_calibration EEPROM, or in firmware by IDAC rotation – swapping which IDAC drives which AIN between readings and averaging, which this topology supports directly. Without either, IDAC mismatch alone would add up to +/-0.41 degC, still inside 1 degC.
Self-heating at 250 uA in 1000 ohm is 63 uW, under 0.02 degC.

INTERFACE AND TEST NOTES
SPI2 is shared with motor_drive (DRV8323) – see ARCHITECTURE.md section 5. R712..R715 (47R) are both the series terminators and the SPI2 isolation links for this peripheral (TEST_PLAN 3.3).
ADS1120 DRDY has NO pin in the .ioc, so it is brought out to J703 CH0 only; firmware polls DOUT/DRDY instead. If an interrupt is wanted later, allocate a spare GPIO in the .ioc and wire it here.
CLK is tied to DGND: the ADS1120 runs on its internal oscillator.
Firmware must leave the low-side power switch (PSW) off – it sits between AIN3/REFN1 and AVSS, and AIN3 is a live input here.
TP701..TP704 probe leads, TP705/TP706 the ADC reference, TP712/TP713 GND hooks.
J703 is the logic-analyser socket (Amodo keyed 0.1in, B510-4500PL): one plug for the whole SPI2 interface, in place of the TP707..TP711 hooks, as on J502 and J603. CH0 ADS1120_nDRDY, CH1 ADS1120_nCS, CH2 CONFIG_SPI_SCK, CH3 CONFIG_SPI_MOSI, CH4 CONFIG_SPI_MISO, CH5..CH7 spare, 9 and 10 GND for the leads. Tapped MCU-side of R712..R715, so the bus is still visible with an isolation link out.
Substituting a fixed resistor for a probe (TEST_PLAN section 4) is a push-in terminal operation – no soldering.
+5VA and +3V3 PWR_FLAGs live in loadcell_afe; both sheets consume the same global rails from power_rails (OQ-02).

Reasoning + root-sheet needs: docs/decisions/actuator-sch-afe.md
ADS1120 on the shared SPI2 config bus (REQ-AR-10); OQ-04 resolved to RTD
Load cell probe and linear-encoder rail mid-point – REQ-EL-07, 1 degC
Two 3-wire Pt1000 RTD channels, ratiometric, sharing one reference resistor

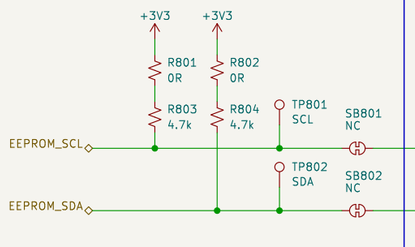
Amodo Design

Sheet: /temp_sense/
File: temp_sense.kicad_sch

Title: CBs_1 – Temperature Sense (ADS1120)

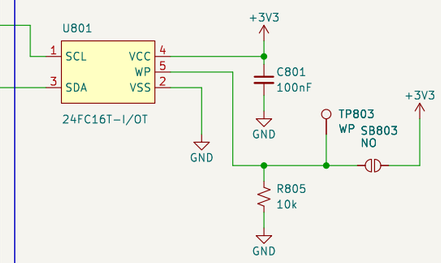
Size: A3	Date: 2026-09-02	**Rev: 0.1**
KiCad E.D.A. 9.0.8		Id: 6/10

I2C1 BUS, PULL-UPS, ISOLATION



R801/R802 are the removable links of TEST_PLAN 4: lift either to drop its pull-up. SB801/SB802 are cut to take the EEPROM off I2C1 while the bus stays pulled up – this block owns that break, so mcu must not duplicate it. The SDA pull-up crosses the SCL run, no junction.

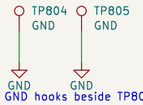
EEPROM, DECOUPLING, WRITE PROTECT



WP is ACTIVE HIGH. R805 holds it low, so the part is writable and firmware can store calibration at any time; solder SB803 to lock the device permanently. TP3 lets a jig drive WP either way. This resolves OQ-06 – no MCU pin is spent on write protect.

GROUND HOOKS

+3V3 and GND are generated in power_rails and enter this block through the hierarchy; nothing here drives them, so ERC reports power_pin_not_driven until that sheet lands. See docs/decisions/actuator-sch-periph.md.



GND hooks beside TP801/TP802 for the scope or analyser clips.

BLOCK NOTES – nvm_calibration

U1 = Microchip 24FC16T-I/OT, 16 kbit (2048 x 8) I2C EEPROM in SOT-23-5.
Pin map verified against the datasheet package drawing (DS20001703R p.1):
1 SCL 2 VSS 3 SDA 4 VCC 5 WP.
1.7–5.5 V and 1 MHz capable, so it keeps up with I2C1 at either 400 kHz or Fast-mode Plus, and 4 million erase/write cycles covers repeated calibration.

2 KB is sized for coefficients, not tables: force and temperature calibration constants, the variant (V50N / V10N – see DEC-0010, where the variants differ only by a calibration constant), board serial number and build state. Bulk force profiles live in the OCTOSPI1 RAM on the mcu sheet (DEC-0006), not here.

ADDRESSING CAVEAT. The 24xx16 uses all three block-select bits internally, so it answers to the WHOLE 1010xxx address space and A0/A1/A2 do not exist on the part. No second 1010-family device can share I2C1. It is the only device on the bus today; if another is ever added, swap to a smaller 24xx02/04 first.

4k7 pull-ups suit 400 kHz on a short board-level bus with one load. They are the only pull-ups on I2C1: the mcu block must not add its own.

Test strategy: docs/TEST_PLAN.md
REQ-EL-08, REQ-AR-11; resolves OQ-06 (write protect)
I2C1: EEPROM_SCL PB8, EEPROM_SDA PB9
16 kbit I2C EEPROM for calibration and compensation data

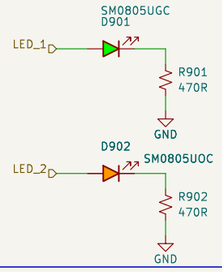
Amodo Design

Sheet: /nvm_calibration/
File: nvm_calibration.kicad_sch

Title: CBs_1 – NVM / Calibration Store

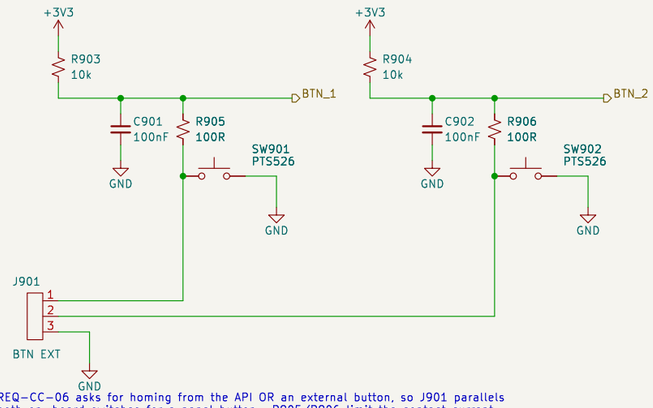
Size: A3	Date: 2026-09-02	**Rev: 0.2**
KiCad E.D.A. 9.0.8		Id: 7/10

STATUS LEDS



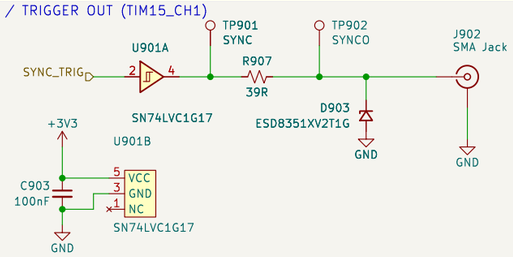
Active high, about 2.8 mA each. LED_1 green is the heartbeat of TEST_PLAN bring-up step 3; LED_2 orange is the fault / status lamp.

USER BUTTONS (BTN_1 = HOME)



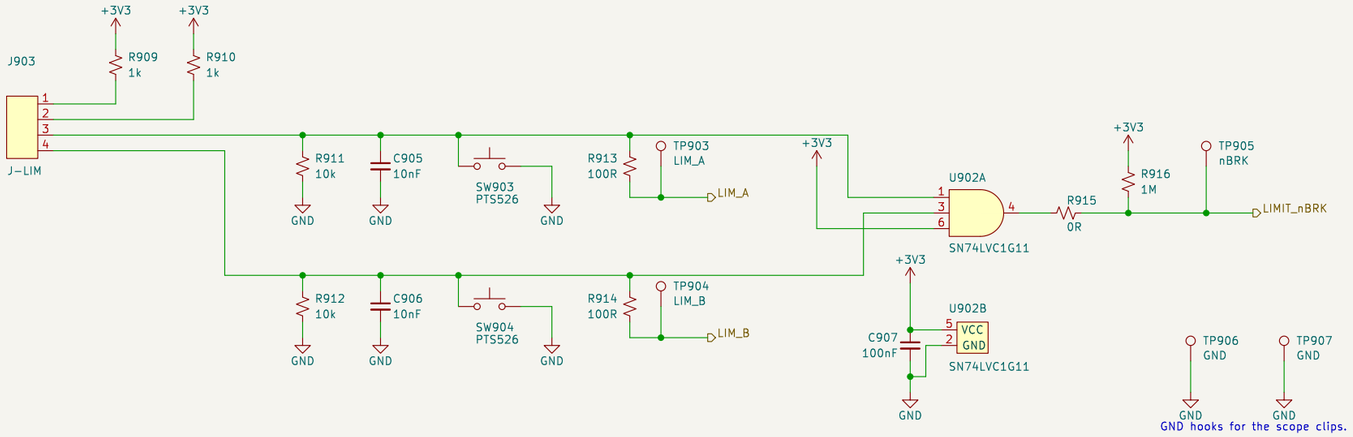
REQ-CC-06 asks for homing from the API OR an external button, so J901 parallels both on-board switches for a panel button. R905/R906 limit the contact current and set the debounce with C901/C902 - about 1 ms rise, 10 us fall. Which of BTN_1 / BTN_2 is HOME is OQ-05: firmware and silkscreen only, the two channels are electrically identical.

SYNC / TRIGGER OUT (TIM15_CH1)



REQ-EL-05 / REQ-EL-06: 3.3 V push-pull, 50 ohm source terminated, SMA jack. U901 buffers PE5 so the MCU pin never sees the cable and the source impedance is repeatable: R907 39 R plus the LVC output impedance (10-15 ohm typical) is about 50 ohm. TP901 is pre-termination, TP902 post; the SMA itself is the coaxial access of TEST_PLAN 2.3. D903 is 0.55 pF and does not soften the edge.

END-OF-STROKE LIMIT SWITCHES + TIM1 BREAK



J-LIM pinout: 1 LIM_A feed 2 LIM_B feed 3 LIM_A return 4 LIM_B return. Both switches are NORMALLY CLOSED, so a closed switch pulls its node HIGH (3.0 V) and an open switch - or a broken wire, or an unplugged connector - lets the 10 k pull-down take it LOW. LOW therefore means 'at that end of stroke, or the wiring has failed', which is the safe direction to fail in.

BLOCK NOTES - ui_io

SAFETY. SPEC 9.1 asks only for a firmware kill on limit actuation (REQ-SF-02). The block diagram and the .ioc both carry a second, independent hardware path (REQ-SF-05, DEC-0012): U902 ANDs the two healthy-limit nodes, so LIMIT_nBRK is HIGH only while both switches are closed and both harness legs are intact. Any limit reached, any broken wire, an unplugged J-LIM or a dead 3V3 rail drives it LOW into TIM1_BKIN2, and the PWM outputs go inactive with firmware taking no part. LIM_A / LIM_B reach the MCU on their own EXTI pins for the firmware kill and for telling the two ends apart. The AND gate's third input is tied high.

R915 is the TEST_PLAN 3.3 link that lets the two TIM1 BREAK sources be exercised alone. It is fitted by default and must be marked on the silkscreen. With it lifted, R916 (1 M) holds LIMIT_nBRK high so the DRV8323_nFAULT path can be tested on its own; the firmware kill through LIM_A / LIM_B is unaffected either way. 1 M is weak enough that a tripped chain still pulls the net down to about 30 mV.

SW903 / SW904 are the 'assert each limit without the mechanics' means of TEST_PLAN 4: pressing one pulls its node low through the 1 k feed (3.3 mA), which is exactly the state that end of stroke produces. They act independently because the two switch loops are independent - a series safety chain could not be stimulated one end at a time.

C905 / C906 (10 nF) with the ~0.9 k source give about 9 us of rise filtering and 100 us of fall; at the 20 mm/s of REQ-ME-03 that is 2 um of extra travel before the break asserts, against millimetres of switch overtravel. R913 / R914 protect the MCU pins. No discrete TVS is fitted on the limit lines: the harness stays inside the instrument and the RC plus the series resistor already bound the current into the MCU clamps. The SMA is the one externally exposed pin here, and it does get a clamp (D903).

+3V3 and GND are generated in power_rails and enter this block through the hierarchy; nothing here drives them, and power_rails owns their PWR_FLAGs, so project ERC is clean at severity-all.

Test strategy: docs/TEST_PLAN.md
REQ-EL-05/06/09, REQ-CC-06, REQ-SF-01/02/05
LIMIT_nBRK PE6 -> TIM1_BKIN2: hardware motor kill (DEC-0012)
Status LEDs, user buttons, SMA SYNC output, end-of-stroke limits

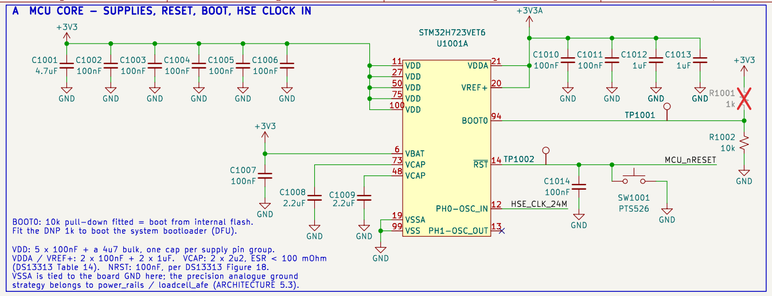
Amodo Design

Sheet: /ui_io/
File: ui_io.kicad_sch

Title: CBs_1 - User I/O, SYNC, Limit Switches

Size: A3	Date: 2026-09-02	**Rev: 0.2**
KiCad E.D.A. 9.0.8		Id: 8/10

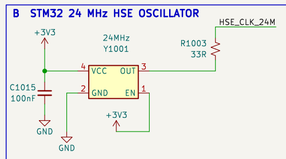
A MCU CORE — SUPPLIES, RESET, BOOT, HSE CLOCK IN



BOOT0: 10k pull-down fitted = boot from internal flash.
Fit the DNP 1k to boot the system bootloader (DFU).

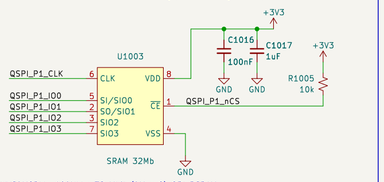
VDD: 5 x 100nF + a 4u7 bulk, one cap per supply pin group.
VDDA / VREF+: 2 x 100nF + 2 x 1uF. VCAP: 2 x 2u2, ESR < 100 mOhm (DS13313 Table 14). NRST: 100nF, per DS13313 Figure 18.
VSSA is tied to the board GND here; the precision analogue ground strategy belongs to power_rails / loadcell_afe (ARCHITECTURE 5.3).

B STM32 24 MHz HSE OSCILLATOR



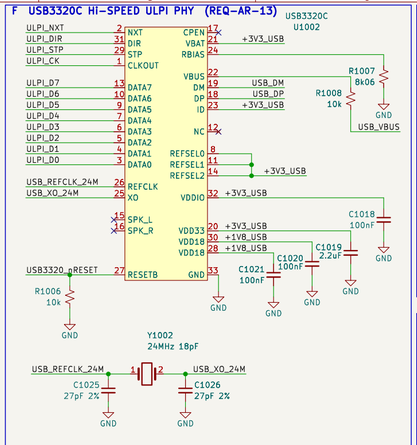
24 MHz LVCMOS MEMS oscillator, 10 ppm, driving the STM32 HSE ONLY — the USB3320 now has its own crystal (block C), so the two clock domains share nothing. STM32 HSE is an EXTERNAL CLOCK on PH0 (PH1-OSC_OUT unallocated in the .ioc, REQ-AR-16), so no bare crystal here. 33R source-terminates the one trace.

D OCTOSPI1 FORCE-PROFILE RAM (QPI PSRAM) REQ-AR-12



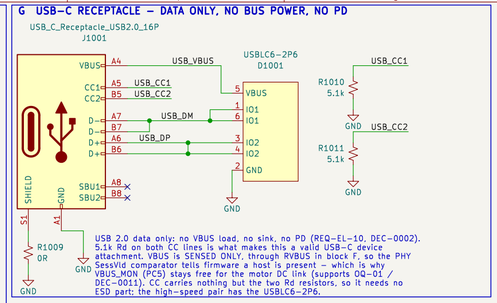
IS66WVS4M8BLL-104NLI : 32 Mbit (4M x 8) QPI PSRAM.
ALL = 1.8 V part, BLL = 3.0 V part — BLL is the 3V3-compatible one.
104 MHz. 50 ohm output drive: point to point, no series termination.
CE# pull-up keeps the device deselected while the MCU pins are hi-Z.
NO TEST POINTS ON THIS BUS — DEC-0018 ruling 1.

F USB3320C HI-SPEED ULPI PHY (REQ-AR-13)



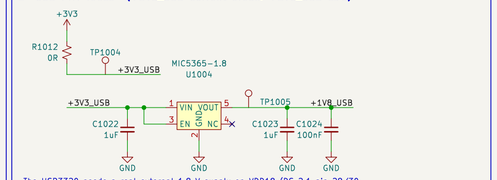
USB3320C-EZK-TR. ULPI OUTPUT CLOCK mode: the PHY generates the 60 MHz ULPI clock on CLKOUT —> STM32 ULPI_CK (PA5). Its 24 MHz reference is its OWN crystal on REFCLK / XO (block C) — no clock is shared with the STM32. REFSEL[2:0]=111 still selects 24 MHz (DS Table 5-10). RBIAS 8.06k 1% and RVBUS 10k (device-only) are datasheet-mandated values (DS 2.1, Table 5-7). ID tied to VDD33 = device-only operation (DS 5.6.1). CPEN / SPK_L / SPK_R / N-C are unused: no OTG VBUS switch, no audio. RESETB has no internal pull-down — the 10k holds the PHY in reset while the STM32 pins are hi-Z, which also covers the VDD18-before-VDDIO sequence note.
NO TEST POINTS ON THE ULPI BUS — DEC-0018 ruling 1.

G USB-C RECEPTACLE — DATA ONLY, NO BUS POWER, NO PD



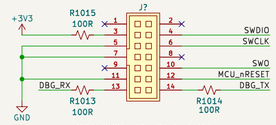
USB 2.0 data only: no VBUS load, no sink, no PD (REQ-EL-10, DEC-0002).
5.1k Rd on both CC lines is what makes this a valid USB-C device attachment. VBUS is SENSED ONLY, through RVBUS in block F, so the PHY SessVld comparator tells firmware a host is present — which is why VBUS_MON (PC5) stays free for the motor DC link (supports OQ-01 / DEC-0011). CC carries nothing but the two Rd resistors, so it needs no ESD part: the high-speed pair has the USBLC6-2P6.

E USB PHY RAILS (+3V3_USB current break, +1V8_USB LDO)



The USB3320 needs a real external 1.8 V supply on VDD18 (DS 2.1 pin 28/30 and DS 5.5.3) as well as 3.3 V on VBAT/VDD33/VDDIO. 1.8 V is generated here rather than requested from power_rails, so no new cross-block rail is invented mid-wave; the mcu block therefore owns its test point and current break (producer-owns-the-break, DEC-0007 / TEST_PLAN 3).
VBAT and VDD33 are tied together per USB3320 DS Figure 5-7 (3.3 V supply).

H SWD + USART3 DEBUG HEADER (REQ-AR-15)

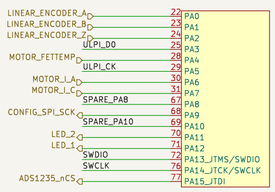


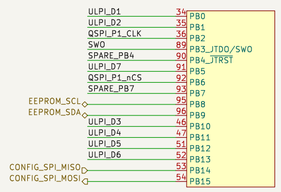
PINOUT — the STM32 14-way 1.27 mm IDC order, copied pin for pin from ARIA_EITSYS_CBs_1 (Microcontroller.kicad_sch, J11) so one debug cable serves both boards:
1 NC 2 NC 3 VDD (+3V3 via R1015 100R)
4 SWDIO 5 GND 6 SWCLK 7 GND
8 NC 9 NC 10 SWO 11 GND
12 nRESET 13 DBG_RX 14 DBG_TX

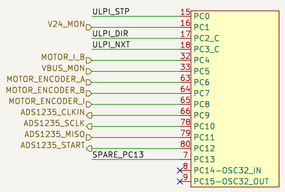
SWO on pin 10 is this board's ONE addition: pin 10 is NC on the reference board, this design has SWO (REQ-AR-15), and a cable wired for that board just leaves it open.
USART3 shares the header, as REQ-AR-15 and the block diagram both ask. It is SWD-safe: a probe drives 4, 6 and 12 and reads 10, and the .ioc sets Trace_Asynchronous_SW so PB4 / PB3 are not JTAG.
R1013 / R1014 / R1015, 100R each, make a mis-plugged probe or a shorted console pin a nuisance rather than damage.

DBG_TX / DBG_RX keep the .ioc net names: DBG_TX is the STM32 OUTPUT (USART3_TX, PD8), DBG_RX the STM32 INPUT (USART3_RX, PD9). MCU_nRESET comes from block A, which owns its 100 nF, its push button and its test point. All six debug nets are sheet-local now that the header sits on the page it serves.

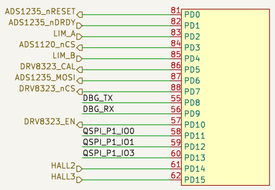
MCU PORTS — PIN ASSIGNMENT IS THE .ioc (DEC-0013); ULPI / QSPI / USB3320_nRESET / SPARE_* stay on this sheet

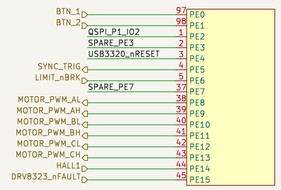




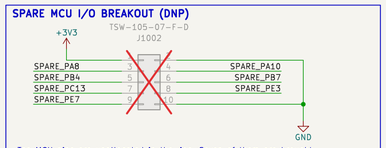


MCU PORTS (cont.)





SPARE MCU I/O BREAKOUT (DNP)



Ten MCU pins are unallocated in the .ioc. Seven of them are brought out here so a wire mod can serve OQ-06 (EEPROM nWP) and OQ-07 (rail PGOOD / enable) without a board spin. DNP by default — fit only if needed. PC14/PC15 (OSC32) and PH1-OSC_OUT are left unconnected so a 32.768 kHz LSE remains possible on a later revision.

SHEET NOTES

STM32H723VET6 + USB3320 ULPI PHY + USB-C (data only) + OCTOSPI1 PSRAM, with the board's debug and bring-up access alongside it (blocks H, J, K).
Pin map authority: hardware/cubemx/ARIA_SRB_FAFF_2_POC_CBs_1.ioc (DEC-0013) — nothing here re-pins it.

Local labels stay on this sheet: ULPI_*, QSPI_P1_*, USB_*, HSE_CLK_24M, USB_REFCLK_24M, USB_XO_24M, USB3320_nRESET, SPARE_*, +3V3_USB, +1V8_USB — and now SWDIO, SWCLK, SWO, MCU_nRESET, DBG_TX and DBG_RX as well, because the header that consumes them is on this sheet and they no longer leave it. Hierarchical labels leave it: the full list and every direction is in docs/decisions/actuator-sch-mcu.md.

PC2_C / PC3_C carry ULPI_DIR and ULPI_NXT; firmware MUST close the SYSCFG_PMCR analog switch (PC2SO / PC3SO) before the ULPI link will run — the pins are otherwise isolated from the digital I/O. DS13313 6.3.16 Tbl 56.

TEST ACCESS (TEST_PLAN 4). The whole test_debug sheet lives here now: block H is the SWD + USART3 debug header, J the rail probe header, K the GND hooks. Test coverage belongs on the page it covers, not on a sheet of its own — docs/decisions/actuator-rev-testdebug.md.
Other TPs: NRST (hook), BOOT0, HSE clock (dual TP, block B), +3V3_USB and +1V8_USB (block E). MCO2 leaves the sheet as ADS1235_CLKIN and is probed in loadcell_afe, which owns that net's break. Supply-pin groups are reachable at the decoupling banks in blocks A, D, E and F.
DELIBERATELY NO test points on ULPI or OCTOSPI (DEC-0018 ruling 1 / TP 2.2).

ROOT SHEET. Every hierarchical label on this sheet is a sheet pin on the mcu block of the root. SWDIO, SWCLK, SWO, MCU_nRESET, DBG_TX and DBG_RX are no longer among them — they became sheet-local when test_debug was dissolved, and their sheet pins came off the root with it.

K GND HOOKS FOR SCOPE CLIPS

Six through-hole GND loops, spread across the board at layout so an oscilloscope ground clip is never far from the signal hook being probed. The house standard asks for these wherever TestPointHook is used, and the block sheets use hooks on I2C1, SPI2, SPI3 and the fault lines.

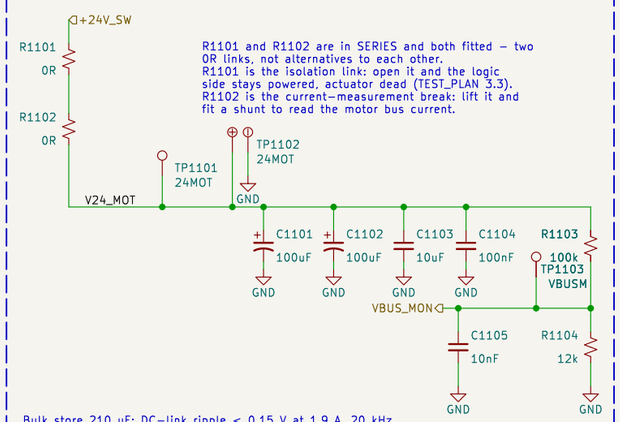
Reasoning: docs/decisions/actuator-sch-mcu.md
No test points on the ULPI or OCTOSPI buses (DEC-0018)
USB-C is DATA ONLY — no USB-PD, no bus power (DEC-0002)
Pin map authority: hardware/cubemx (.ioc) — DEC-0013

Amodo Design
Sheet: /mcu/
File: mcu.kicad_sch

Title: CBs_1 — MCU (STM32H723VET6) + USB + QSPI

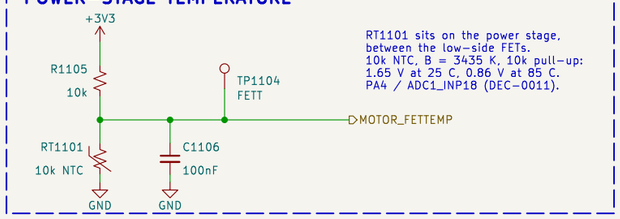
Size: A2	Date: 2026-09-02	Rev: 0.2
KiCad E.D.A. 9.0.8		Id: 9/10

24 V MOTOR BUS, BULK STORE AND DC-LINK SENSE



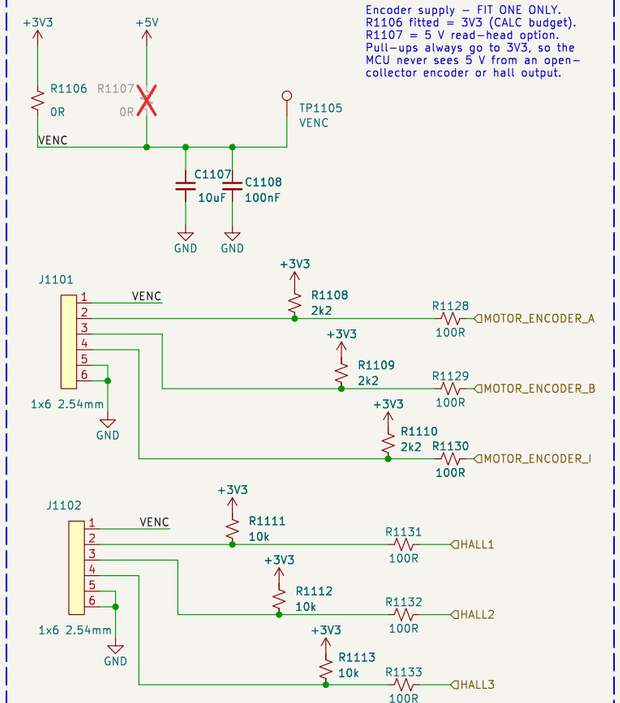
Bulk store 210 uF: DC-link ripple < 0.15 V at 1.9 A, 20 kHz. VBUS_MON 100k/12k: 3.30 V full scale = 30.8 V bus; 24.0 V reads 2.571 V. PC5 / ADC2_INP8 (DEC-0011, OQ-01).

POWER-STAGE TEMPERATURE



RT1101 sits on the power stage, between the low-side FETs. 10k NTC, B = 3435 K, 10k pull-up: 1.65 V at 25 C, 0.86 V at 85 C. PA4 / ADC1_INP18 (DEC-0011).

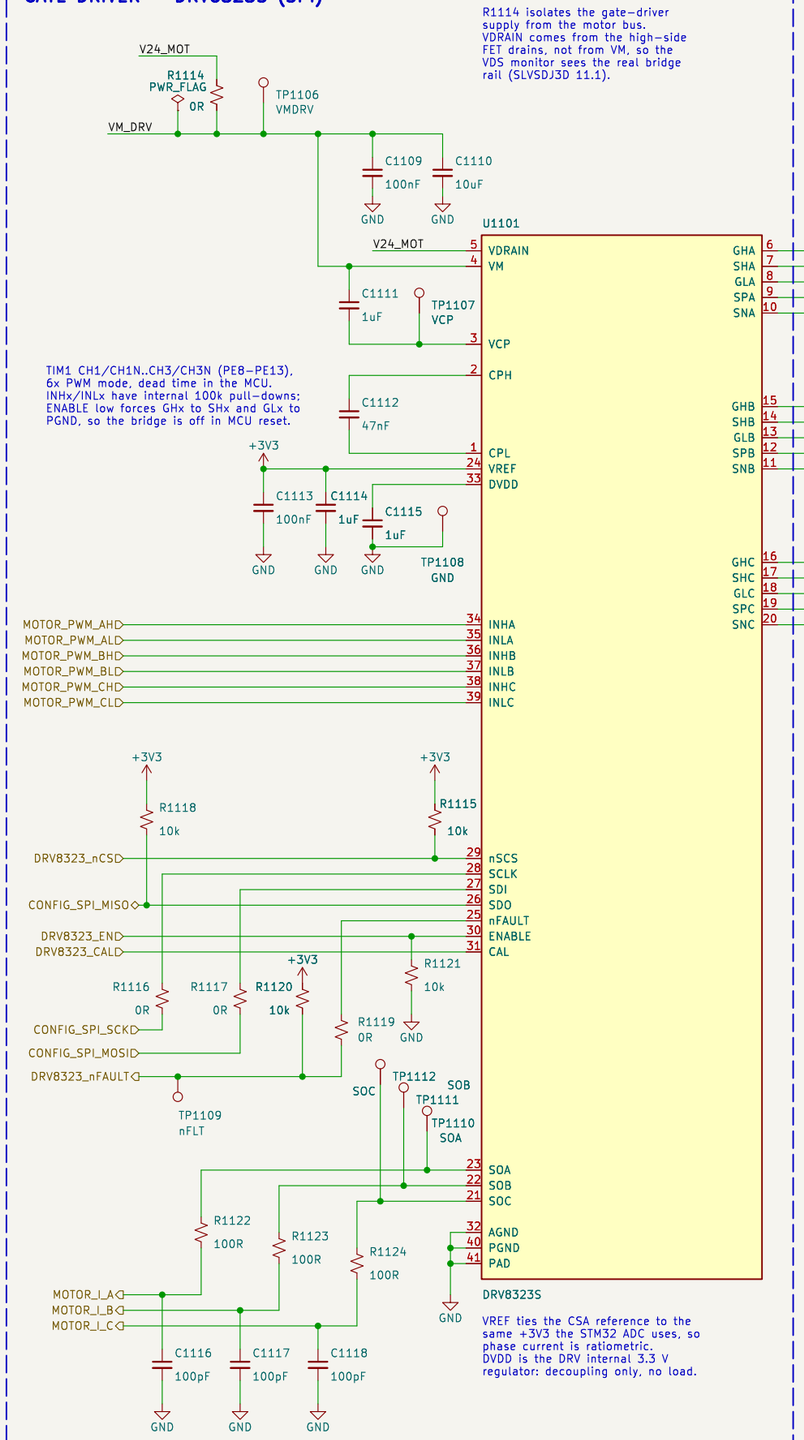
MOTOR ROTARY ENCODER AND HALL SENSORS



Encoder supply — FIT ONE ONLY. R1106 fitted = 3V3 (CALC budget). R1107 = 5 V read-head option. Pull-ups always go to 3V3, so the MCU never sees 5 V from an open-collector encoder or hall output.

J102 A/B/Z -> TIM3 CH1/CH2/CH3 (PC6/PC7/PC8). J103 halls -> PE14/PD14/PD15 (GPIO). Motor not fixed (DEC-0004): this pinout suits every candidate BLDC in the design log. R1128..R1133 100R bound the current into the six MCU pins, the same treatment the limit and button harnesses get. The cable is internal, so no TVS array — see the ESD audit in docs/decisions/actuator-sch-review-r1.md.

GATE DRIVER — DRV8323S (SPI)

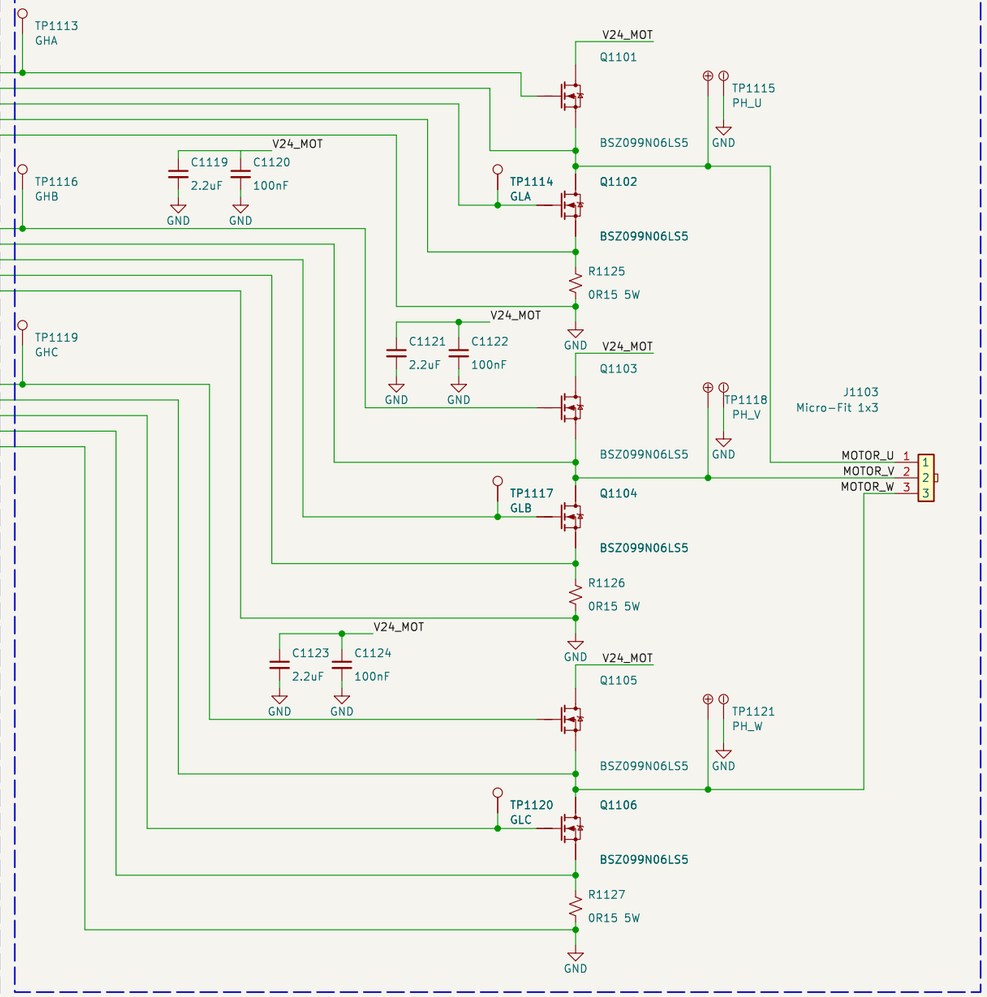


R1114 isolates the gate-driver supply from the motor bus. VDRAIN comes from the high-side FET drains, not from VM, so the VDS monitor sees the real bridge rail (SLVSDJ3D 11.1).

TIM1 CH1/CH1N..CH3/CH3N (PE8-PE13), 6x PWM mode, dead time in the MCU. INHx/INLx have internal 100k pull-downs; ENABLE low forces GHx to SHx and GLx to PGND, so the bridge is off in MCU reset.

VREF ties the CSA reference to the same +3V3 the STM32 ADC uses, so phase current is ratiometric. DVDD is the DRV internal 3.3 V regulator: decoupling only, no load.

3-PHASE POWER STAGE AND PHASE-CURRENT SHUNTS



BRIDGE DECOUPLING one 2.2 uF + 100 nF pair per half-bridge: C1119/C1120 phase U, C1121/C1122 phase V, C1123/C1124 phase W. The 210 uF bulk at the bus entry is too far round the loop to serve commutation; each pair goes hard against its own leg, across the high-side drain and the shunt return. Not per FET — a capacitor across one FET is a snubber, not decoupling, and is a bring-up decision (SLVSDJ3D 10, 11.1).

DESIGN NOTES

SAFETY-CRITICAL BREAK PATH. R1119 is FITTED by default and marked on the silkscreen. DRV8323_nFAULT (open drain) drives TIM1_BKIN on PE15; opening R1119 exercises the LIMIT_nBRK path alone (TEST_PLAN.md 3.3, bring-up step 8). R1120 holds PE15 high while R1119 is out. R1116/R1117 are the SPI2 stub links — remove both to lift U1101 off the shared bus; SDO is open drain and Hi-Z while nSCS is high, so MISO needs no link. R1121 keeps ENABLE — and the bridge — off until PD10 drives high.

PEAK CURRENT LIMIT (REQ-SF-03, closes OQ-08). One shunt value serves both variants; the limit is an SPI setting plus a firmware threshold, not a board change. 0R15 with CSA gain 5 V/V gives +/-1.87 A full scale on V50N, so the 75 N (1.843 A) limit lands on the last ADC code; gain 20 V/V gives +/-0.467 A on V10N, 15 N at 79 % of scale. SEN_LVL 00b trips the hardware comparator at 1.667 A = 67.8 N, below the V50N cell limit. A V10N build wanting that trip at 15 N fits 0R68.

POWER STAGE. No series gate resistors and no G-S pull-downs — slew rate is set by IDRIVE/TDRIVE over SPI, and external gate parts degrade the VDS and gate-fault monitors. SPx is the VDS monitor return as well as the CSA input, so keep it Kelvin to the FET source. LAYOUT: shunt -> PGND -> bulk-cap negative is ONE tight loop, joined to system ground at a single point at the bulk capacitors.

Root sheet wired by the integration pass (DEC-0009)
Requirements: docs/REQUIREMENTS.md Tests: docs/TEST_PLAN.md
Reasoning: docs/decisions/actuator-sch-motor.md
3-phase inverter, phase-current sense, motor and rotary-encoder interface

Amodo Design

Sheet: /motor_drive/
File: motor_drive.kicad_sch

Title: CBs_1 — Motor Drive (DRV8323S)		
Size: A3	Date: 2026-09-03	**Rev: 0.2**
KiCad E.D.A. 9.0.8		Id: 10/10