

# Microcontroladores

## Semana 6

Semestre 2021-0

Profesor: Kalun Lau

1

### Preguntas previas

- ¿Problemas para acceder a la carpeta compartida de TF?

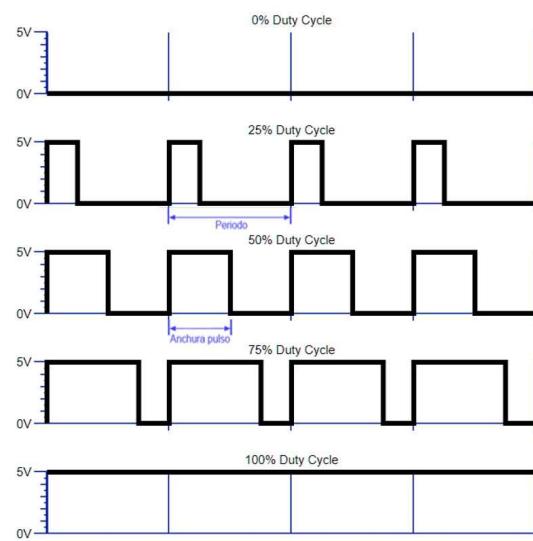
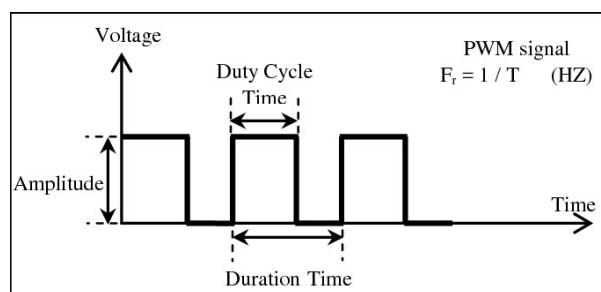
2

## Agenda

- PWM con CCP
- Comunicación serial
  - I2C
  - Serial síncrona
  - Serial asíncrona
  - Otros protocolos e interfaces

3

## PWM : Modulación de ancho de pulso



- Aumento de eficiencia en diferentes aplicaciones de circuitos electrónicos.
- Aplicaciones:
  - Arranque y control de velocidad de motores eléctricos
  - Comunicaciones digitales
  - Amplificadores de audio!
  - Control de intensidad luminosa en lámparas LED
  - Cargadores de celular y demás fuentes de energía conmutadas
  - Largo etc

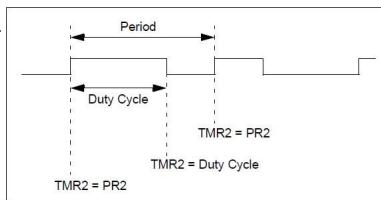
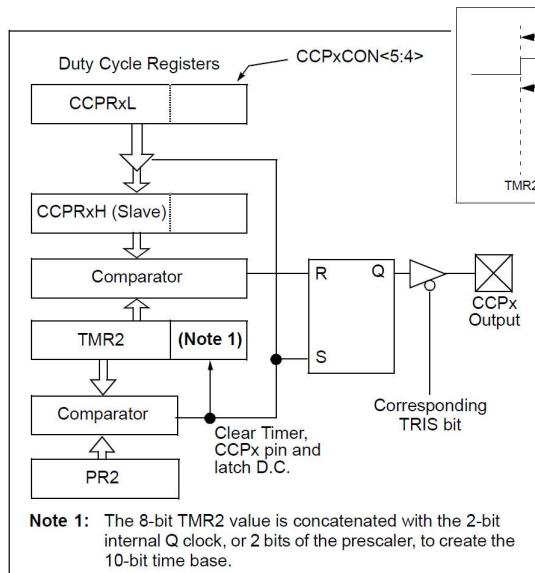
4

## Fuente lineal vs fuente conmutada



5

## PWM con el CCP



1. Set the PWM period by writing to the PR2 register.
2. Set the PWM duty cycle by writing to the CCPRxL register and CCPxCON<5:4> bits.
3. Make the CCPx pin an output by clearing the appropriate TRIS bit.
4. Set the TMR2 prescale value, then enable Timer2 by writing to T2CON.
5. Configure the CCPx module for PWM operation.

$$\text{PWM Period} = [(PR2 + 1) \cdot 4 \cdot Tosc \cdot (TMR2 \text{ Prescale Value})]$$

$$\text{PWM Duty Cycle} = (CCPRxL; CCPxCON<5:4>) \cdot Tosc \cdot (TMR2 \text{ Prescale Value})$$

$$\text{PWM Resolution (max)} = \frac{\log(\frac{Fosc}{FPWM})}{\log(2)} \text{ bits}$$

6

## Generar 1KHz 50% con el CCP en modo PWM

$$\text{PWM Period} = [(PR2) + 1] \cdot 4 \cdot TOSC \cdot \\ (\text{TMR2 Prescale Value})$$

- ~~1~~ • ¿PR2 si Fosc=48MHz?
  - PR2=749 => inválido
- ~~1~~ • ¿PR2 si Fosc=16MHz?
  - PR2=249 => válido
- ~~2~~ • Valor de CCPR2L para 50% DC?
  - 125
- ~~3~~ • TRISCbits.RC1 = 0; //poner el puerto de PWM como salida
- ~~4~~ • T2CON = 0x06
- ~~5~~ • CCP2CON = 0x0C

$$\frac{1}{1\text{KHz}} = [(PR2)+1] \cdot 4 \cdot \left(\frac{1}{48\text{MHz}}\right) \cdot (16)$$

PR2 = 749     

7

## T2CON:

REGISTER 13-1: T2CON: TIMER2 CONTROL REGISTER

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	T2OUTPS3	T2OUTPS2	T2OUTPS1	T2OUTPS0	TMR2ON	T2CKPS1	T2CKPS0

## Legend:

R = Readable bit  
-n = Value at PORW = Writable bit  
'1' = Bit is setU = Unimplemented bit, read as '0'  
'0' = Bit is cleared

x = Bit is unknown

bit 7      **Unimplemented:** Read as '0'bit 6-3      **T2OUTPS3:T2OUTPS0:** Timer2 Output Postscale Select bits

0000 = 1:1 Postscale

0001 = 1:2 Postscale

.

.

1111 = 1:16 Postscale

bit 2      **TMR2ON:** Timer2 On bit

1 = Timer2 is on

0 = Timer2 is off

bit 1-0      **T2CKPS1:T2CKPS0:** Timer2 Clock Prescale Select bits

00 = Prescaler is 1

01 = Prescaler is 4

1x = Prescaler is 16

$$T2CON = \emptyset \times \emptyset 6$$

8

## CCP2CON:

REGISTER 15-1: CCP <sub>x</sub> CON: STANDARD CCP <sub>x</sub> CONTROL REGISTER							
U-0 —(1)	U-0 —(1)	R/W-0 DCxB1	R/W-0 DCx00	R/W-0 CCPxM3	R/W-0 CCPxM2	R/W-0 CCPxM1	R/W-0 CCPxM0 bit 7

**Legend:**

- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as '0'
- n = Value at POR
- '1' = Bit is set
- '0' = Bit is cleared
- x = Bit is unknown

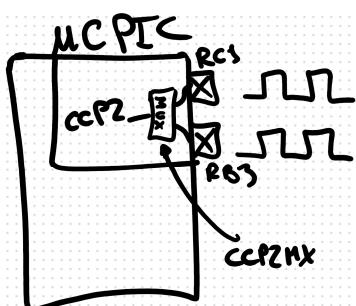
bit 7-6      Unimplemented: Read as '0'(1)  
 bit 5-4      DCxB1:DCx00: PWM Duty Cycle Bit 1 and Bit 0 for CCP<sub>x</sub> Module  
 Capture mode:  
 Unused.  
 Compare mode:  
 Unused.  
 PWM mode:  
 These bits are the two LSbs (bit 1 and bit 0) of the 10-bit PWM duty cycle. The eight MSbs of the duty cycle are found in CCPR1L.

bit 3-0      CCPxM3:CCPxM0: CCP<sub>x</sub> Module Mode Select Bits  
 0000 = Capture/Compare/PWM disabled (resets CCP<sub>x</sub> module)  
 0001 = Reserved  
 0010 = Compare mode: toggle output on match (CCPxIF bit is set)  
 0011 = Reserved  
 0100 = Capture mode: every falling edge  
 0101 = Capture mode: every rising edge  
 0110 = Capture mode: every 4th rising edge  
 0111 = Capture mode: every 16th rising edge  
 1000 = Compare mode: initialize CCP<sub>x</sub> pin low; on compare match, force CCP<sub>x</sub> pin high (CCPxIF bit is set)  
 1001 = Compare mode: initialize CCP<sub>x</sub> pin high; on compare match, force CCP<sub>x</sub> pin low (CCPxIF bit is set)  
 1010 = Compare mode: generate software interrupt on compare match (CCPxIF bit is set, CCP<sub>x</sub> pin reflects I/O state)  
 1011 = Compare mode: trigger special event, reset timer, start A/D conversion on CCP<sub>x</sub> match (CCPxIF bit is set)  
 11xx = PWM mode

Note 1: These bits are not implemented on 28-pin devices and are read as '0'.

9

## Código en XC8:

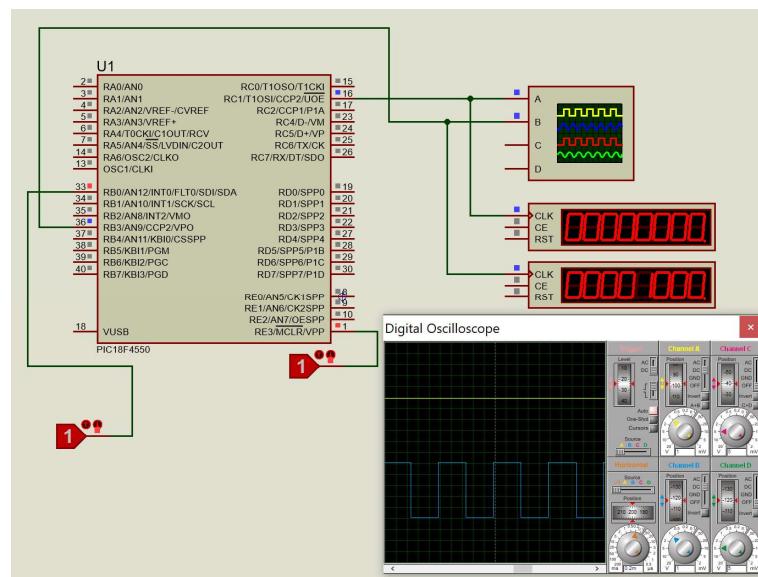


```

1  #pragma config PLLDIV = 1           // PLL
2  #pragma config CPUDIV = OSC4_PLL6// Syst
3  #pragma config FOSC = XTPLL_XT // Oscil
4  #pragma config FWRT = ON          // Power
5  #pragma config BOR = OFF          // Brown
6  #pragma config WDT = OFF          // Watch
7  #pragma config CCP2MX = OFF        // CCP2
8  #pragma config PBADEN = OFF        // PORTE
9  #pragma config MCLRE = ON          // MCLR
10 #pragma config LVP = OFF          // Singl
11
12 #include <xc.h>
13 #define _XTAL_FREQ 16000000UL      //fx
14
15 void init_config(void){
16     PR2 = 249;                  //PWMrreq=1kHz
17     CCPR2L = 125;                //PWMrdc=50%
18     //TRISBbits.RC1 = 0; //CCP2MX = ON
19     TRISBbits.RB3 = 0; //CCP2MX = OFF
20     T2CON = 0x06;               //FSC1:16
21     CCP2CON = 0x0C;             //PWM mode
22 }
23
24 void main(void){
25     init_config();
26     while(1){
27         if(PORTBbits.RB0 == 1){
28             CCP2CON = 0x0C; //CCP2 PWM
29         }
30         else{
31             CCP2CON = 0x00; //CCP2 OFF
32         }
33     };
34 }
```

10

## Simulación



11

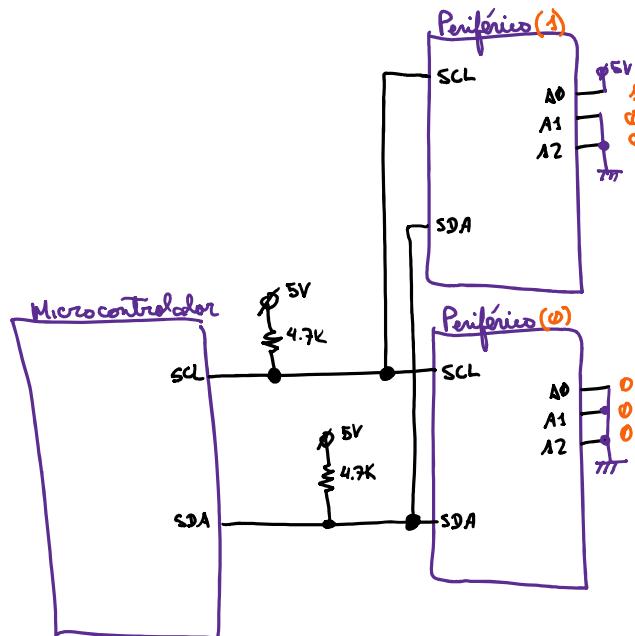
## Comunicaciones seriales

- ¿Por qué necesitamos comunicarnos serialmente con el microcontrolador?
  - Hay periféricos especializados no incluídos dentro del microcontrolador
  - Para conectar dichos periféricos hay que saber qué protocolo e interfaz utiliza.
  - I<sup>2</sup>C, SPI, 1-wire, UART, I<sup>2</sup>S, etc

12

## Comunicación I<sup>2</sup>C

- Inter-Integrated Circuit
- Serial síncrono
- Dos líneas para la comunicación (SCL y SDA)
- Direcciones de 7 bits
- Topología tipo bus
- Diferentes tipos de periféricos:
  - Memorias EEPROM (24Cxx)
  - Expansores de puertos (PCF8574)
  - Drivers de motores de paso
  - Conversores A/D
  - RTC (DS1307)
  - Sensores de temperatura (MCP9808)
  - etc



13

## I<sup>2</sup>C:

- Tipo de periféricos I<sup>2</sup>C que encontramos:
  - DS1307 – RTC
  - PCF8574 – Expansor de 8 I/Os
  - 24C01 hasta 24C1024 – Memorias EEPROM
  - AD7997 – A/D 8ch 12bit
  - MCP9808 - Sensor de temperatura de precisión
  - PCA9685 – Servo controller up to 16 units
  - Devantech SRF08 – Sensor de ultrasonido
  - SH1106 – OLED interface display
  - HTU21D – Sensor de temperatura/humedad
  - MPU6050 – Acelerómetro
  - PCF8591 – A/D 4ch & D/A 1ch 8bit converter
  - HT16K33 – LED driver
  - DS3231 – RTC
  - DS1621 – Thermometer and Thermostat
  - SHT31 – Temperature & Humidity Sensor
  - MCP23016 - 16 I/O port expander

14

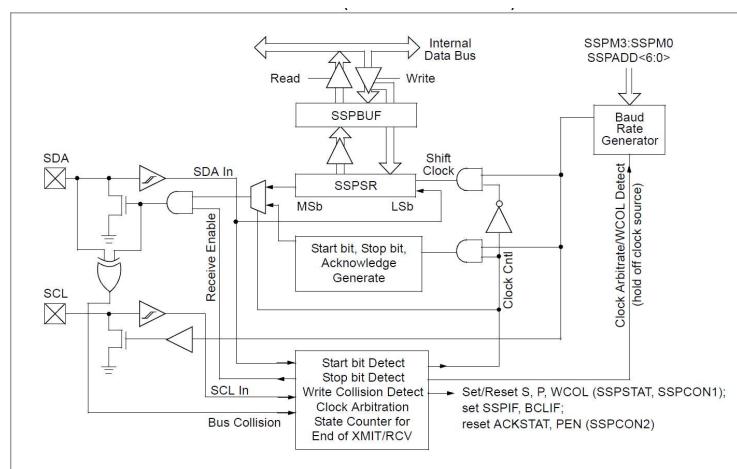
## Interface I2C en el Microcontrolador PIC

- Dos opciones:
  - Hardware (módulo periférico MSSP)
  - Software (implementar una librería)

15

## El MSSP en modo I2C Maestro

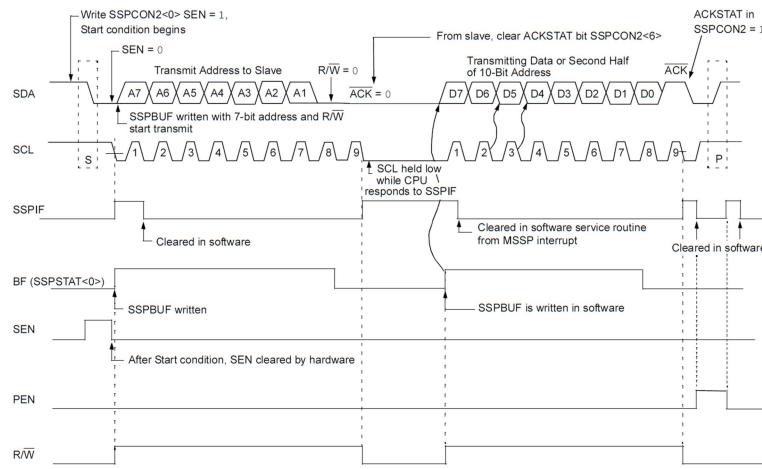
- Referencia: capítulo 19.4.6 de la hoja técnica del PIC18F4550



16

# El MSSP en modo I2C Maestro

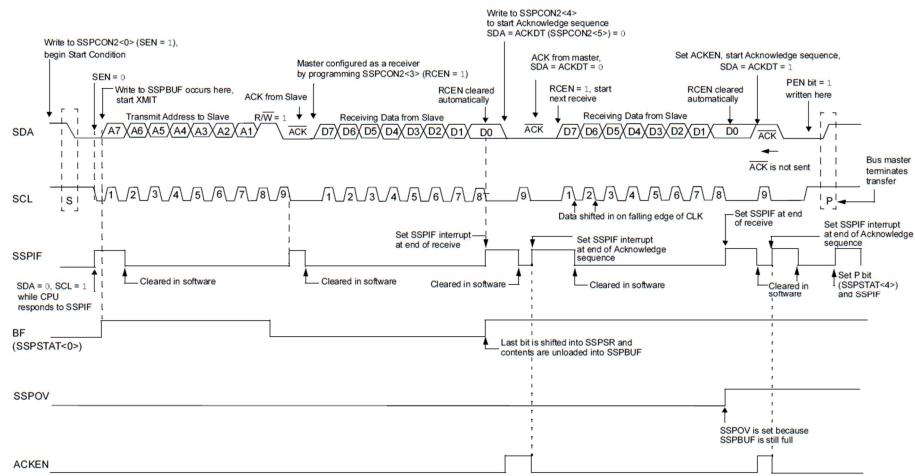
- Evento de transmisión:



17

# El MSSP en modo I2C Maestro

- Evento de recepción:



18

# El MSSP en modo I<sup>2</sup>C Maestro

- Registros relacionados: El SSPSTAT

REGISTER 19-3: SSPSTAT: MSSP STATUS REGISTER (I <sup>2</sup> C™ MODE)							
R/W-0	R/W-0	R-0	R-0	R-0	R-0	R-0	R-0
SMP	CKE	D/A	P(1)	S(1)	R/W(2,3)	UA	BF
bit 7							
<b>Legend:</b> R = Readable bit W = Writable bit -n = Value at POR							
U = Unimplemented bit, read as '0' '1' = Bit is set '0' = Bit is cleared x = Bit is unknown							
bit 7 <b>SMP:</b> Slave Rate Control bit  In Master or Slave mode: 1 = Slave rate control disabled for Standard Speed mode (100 kHz and 1 MHz) 0 = Slave rate control enabled for High-Speed mode (400 kHz)							
bit 6 <b>CKE:</b> SMBus Select bit  In Master or Slave mode: 1 = Enables SMBus specific inputs 0 = Disables SMBus specific inputs							
bit 5 <b>D/A:</b> Data Address bit  In Master mode: Reserved In Slave mode: 1 = Indicates that the last byte received or transmitted was data 0 = Indicates that the last byte received or transmitted was address							
bit 4 <b>P:</b> Stop bit(1) 1 = Indicates that a Stop bit has been detected last 0 = Stop bit was not detected last							
bit 3 <b>S:</b> Start bit(1) 1 = Indicates that a Start bit has been detected last 0 = Start bit was not detected last							
bit 2 <b>R/W:</b> Read/Write Information bit(2,3)  In Slave mode: 1 = Read 0 = Write  In Master mode: 1 = Transmitter is in progress 0 = Transistor is not in progress							
bit 1 <b>UA:</b> Update Address bit (10-Bit Slave mode only) 1 = Indicates that the user needs to update the address in the SSPADD register 0 = Address does not need to be updated							
bit 0 <b>BF:</b> Buffer Full Status bit  In Transmit mode: 1 = SSPBUF is full 0 = SSPBUF is empty  In Receive mode: 1 = SSPBUF is full (does not include the ACK and Stop bits) 0 = SSPBUF is empty (does not include the ACK and Stop bits)							

Note 1: This bit is cleared on Reset and when SSPEN is cleared.  
 2: This bit holds the R/W bit information following the last address match. This bit is only valid from the address match to the next Start bit, Stop bit or not ACK bit.

3: ORing this bit with SEN, RSEN, PEN, RCEN or ACKEN will indicate if the MSSP is in Active mode.

19

# El MSSP en modo I<sup>2</sup>C Maestro

- Registros relacionados: El SSPCON1

REGISTER 19-4: SSPCON1: MSSP CONTROL REGISTER 1 (I <sup>2</sup> C™ MODE)							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0
bit 7							
<b>Legend:</b> R = Readable bit W = Writable bit -n = Value at POR							
U = Unimplemented bit, read as '0' '1' = Bit is set '0' = Bit is cleared x = Bit is unknown							
bit 7 <b>WCOL:</b> Write Collision Detect bit  In Master Transmit mode: 1 = When the SSPBUF register was attempted while the I <sup>2</sup> C conditions were not valid for a transmission to be started (must be cleared in software) 0 = No collision  In Slave Transmit mode: 1 = The SSPBUF register is written while it is still transmitting the previous word (must be cleared in software) 0 = No collision  In Receive mode (Master or Slave modes): This is a 'don't care' bit. <b>SSPOV:</b> Receive Overflow Indicator bit  In Receive mode: 1 = A byte is received while the SSPBUF register is still holding the previous byte (must be cleared in software) 0 = No overflow  In Transmit mode: This is a 'don't care' bit in Transmit mode. <b>SSPEN:</b> Master Synchronous Serial Port Enable bit 1 = Enables the serial port and configures the SDA and SCL pins as the serial port pins <sup>(1)</sup> 0 = Disables serial port and configures these pins as I/O port pins <sup>(1)</sup>							
bit 6 <b>CKP:</b> SCK Release Control bit  In Slave mode: 1 = Release clock 0 = Holds clock low (clock stretch), used to ensure data setup time  In Master mode: Unused in this mode. <b>SSPM3:SSPM0:</b> Master Synchronous Serial Port Mode Select bits 1111 = I <sup>2</sup> C Slave mode, 10-bit address with Start and Stop bit interrupts enabled <sup>(2)</sup> 1110 = I <sup>2</sup> C Slave mode, 7-bit address with Start and Stop bit interrupts enabled <sup>(2)</sup> 1011 = I <sup>2</sup> C Slave mode, Clock stretch mode (slave idle) <sup>(2)</sup> 1010 = I <sup>2</sup> C Slave mode, clock = Fosc/4 ((SSPADD + 1)) <sup>(2,3)</sup> 0111 = I <sup>2</sup> C Slave mode, 10-bit address <sup>(2)</sup> 0110 = I <sup>2</sup> C Slave mode, 7-bit address <sup>(2)</sup>							
bit 5 <b>SSPM3:SSPM0:</b> Master Synchronous Serial Port Mode Select bits 1111 = I <sup>2</sup> C Slave mode, 10-bit address with Start and Stop bit interrupts enabled <sup>(2)</sup> 1110 = I <sup>2</sup> C Slave mode, 7-bit address with Start and Stop bit interrupts enabled <sup>(2)</sup> 1011 = I <sup>2</sup> C Slave mode, Clock stretch mode (slave idle) <sup>(2)</sup> 1010 = I <sup>2</sup> C Slave mode, clock = Fosc/4 ((SSPADD + 1)) <sup>(2,3)</sup> 0111 = I <sup>2</sup> C Slave mode, 10-bit address <sup>(2)</sup> 0110 = I <sup>2</sup> C Slave mode, 7-bit address <sup>(2)</sup>							
bit 4 <b>CKP:</b> SCK Release Control bit  In Slave mode: 1 = Release clock 0 = Holds clock low (clock stretch), used to ensure data setup time  In Master mode: Unused in this mode. <b>SSPM3:SSPM0:</b> Master Synchronous Serial Port Mode Select bits 1111 = I <sup>2</sup> C Slave mode, 10-bit address with Start and Stop bit interrupts enabled <sup>(2)</sup> 1110 = I <sup>2</sup> C Slave mode, 7-bit address with Start and Stop bit interrupts enabled <sup>(2)</sup> 1011 = I <sup>2</sup> C Slave mode, Clock stretch mode (slave idle) <sup>(2)</sup> 1010 = I <sup>2</sup> C Slave mode, clock = Fosc/4 ((SSPADD + 1)) <sup>(2,3)</sup> 0111 = I <sup>2</sup> C Slave mode, 10-bit address <sup>(2)</sup> 0110 = I <sup>2</sup> C Slave mode, 7-bit address <sup>(2)</sup>							
bit 3-0 <b>SSPM3:SSPM0:</b> Master Synchronous Serial Port Mode Select bits 1111 = I <sup>2</sup> C Slave mode, 10-bit address with Start and Stop bit interrupts enabled <sup>(2)</sup> 1110 = I <sup>2</sup> C Slave mode, 7-bit address with Start and Stop bit interrupts enabled <sup>(2)</sup> 1011 = I <sup>2</sup> C Slave mode, Clock stretch mode (slave idle) <sup>(2)</sup> 1010 = I <sup>2</sup> C Slave mode, clock = Fosc/4 ((SSPADD + 1)) <sup>(2,3)</sup> 0111 = I <sup>2</sup> C Slave mode, 10-bit address <sup>(2)</sup> 0110 = I <sup>2</sup> C Slave mode, 7-bit address <sup>(2)</sup>							

Note 1: When enabled, the SDA and SCL pins must be properly configured as input or output.  
 2: Bit combinations not specifically listed here are either reserved or implemented in SPI mode only.  
 3: Guideline only; exact baud rate slightly dependent upon circuit conditions, but the highest clock rate should not exceed this formula. SSPADD values of '0' and '1' are not supported.

20

## El MSSP en modo I<sup>2</sup>C Maestro

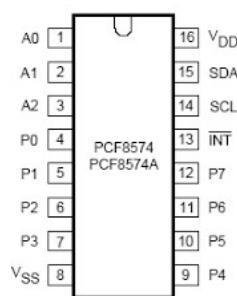
- Registros relacionados: El SSPCON2

REGISTER 19-5: SSPCON2: MSSP CONTROL REGISTER 2 (I <sup>2</sup> C™ MASTER MODE)													
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0						
GCEN	ACKSTAT	ACKDT <sup>(1)</sup>	ACKEN <sup>(2)</sup>	RCEN <sup>(2)</sup>	PEN <sup>(2)</sup>	RSEN <sup>(2)</sup>	SEN <sup>(2)</sup>						
bit 7													
<b>Legend:</b>													
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'											
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared			x = Bit is unknown								
bit 7													
GCEN: General Call Enable bit (Slave mode only) Unused in Master mode.													
bit 6													
ACKSTAT: Acknowledge Status bit (Master Transmit mode only) 1 = Acknowledge was not received from slave 0 = Acknowledge was received from slave													
bit 5													
ACKDT: Acknowledge Data bit (Master Receive mode only) <sup>(1)</sup> 1 = Not Acknowledge 0 = Acknowledge													
bit 4													
ACKEN: Acknowledge Sequence Enable bit <sup>(2)</sup> 1 = Initiate Acknowledge sequence on SDA and SCL pins and transmit ACKDT data bit. Automatically cleared by hardware. 0 = Acknowledge sequence Idle													
bit 3													
RCEN: Receive Enable bit (Master Receive mode only) <sup>(2)</sup> 1 = Enables Receive mode for I <sup>2</sup> C 0 = Receive Idle													
bit 2													
PEN: Stop Condition Enable bit <sup>(2)</sup> 1 = Initiate Stop condition on SDA and SCL pins. Automatically cleared by hardware. 0 = Stop condition Idle													
bit 1													
RSEN: Repeated Start Condition Enable bit <sup>(2)</sup> 1 = Initiate Repeated Start condition on SDA and SCL pins. Automatically cleared by hardware. 0 = Repeated Start condition Idle													
bit 0													
SEN: Start Condition Enable/Stretch Enable bit <sup>(2)</sup> 1 = Initiate Start condition on SDA and SCL pins. Automatically cleared by hardware. 0 = Start condition Idle													
<b>Note 1:</b> Value that will be transmitted when the user initiates an Acknowledge sequence at the end of a receive.													
<b>Note 2:</b> If the I <sup>2</sup> C module is active, these bits may not be set (no spooling) and the SSPBUF may not be written (or writes to the SSPBUF are disabled).													

21

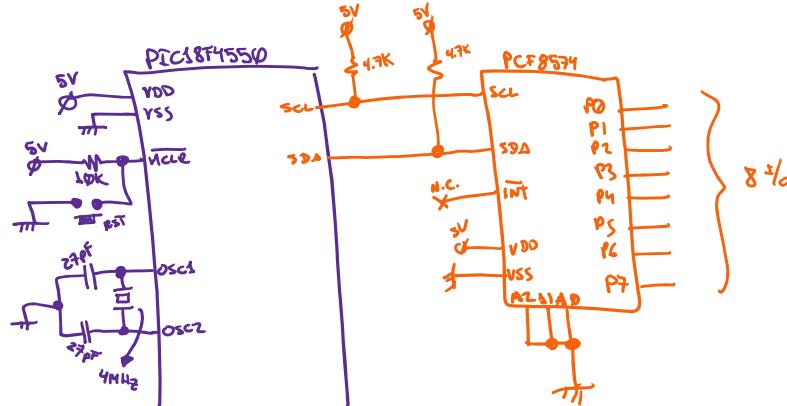
## Ejemplo: I<sup>2</sup>C con el MSSP para conectar un PCF8574

- PCF8574: Expansor de puertos de 8 bits bidireccional
  - Datasheet: <https://www.ti.com/lit/gpn/pcf8574>



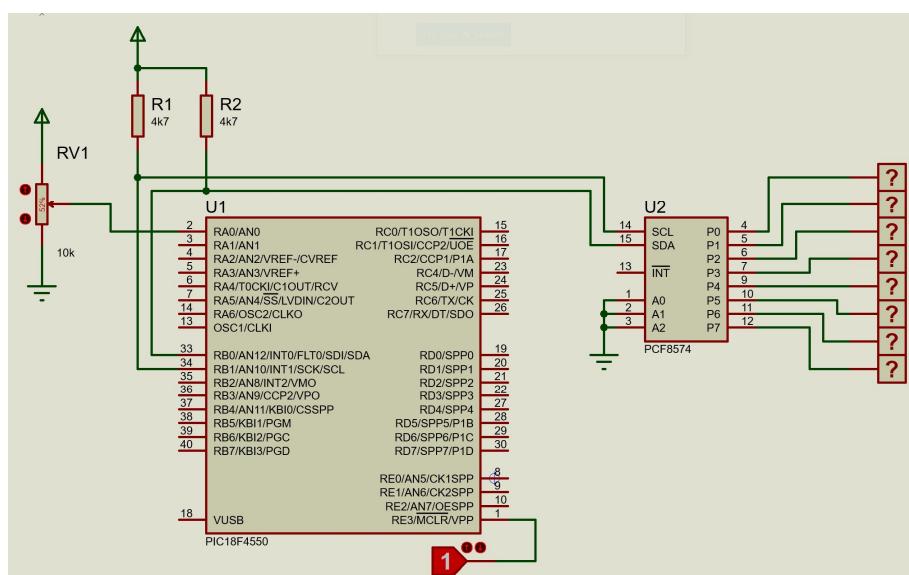
22

## Ejemplo: I2C con el MSSP para conectar un PCF8574



23

## Simulación en Proteus



24

## Palabras de control para el PCF8574

BYTE	BIT							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
I <sup>2</sup> C slave address	P7	P6	P5	P4	P3	P2	P1	R/W
I/O data bus	P7	P6	P5	P4	P3	P2	P1	P0

Evento lectura: 0x41

Evento escritura: 0x40

25

## Procedimiento para escribir un dato en el PCF8574

- Evento de inicio (start)
- Enviar la palabra de control (envío de la dirección del esclavo: 0x40)
- Esperar el ACK
- Enviar el dato a escribir (0xAA)
- Esperar el ACK
- Evento de parada (stop)

$$f_{osc} = \frac{f_{osc}}{(4 \times f_{spdd} + 1)}$$

$$f_{spdd} = 119$$

26

## Configuración del módulo MSSP:

- SSPCON1.SSPEN = 1 (Habilitador del módulo MSSP)
- Modo de trabajo: Master
- 1000 = I<sup>2</sup>C Master mode, clock = Fosc/(4 \* (SSPADD + 1))<sup>(2,3)</sup>
- Valor SSPADD (velocidad)

*Fosc = 48MHz  
Bitrate = 100000*

$$\text{SSPADD} = \frac{\left(\frac{F_{osc}}{4}\right)}{\text{BitRate}} - 1 = 119$$

27

## Código ejemplo en XC8 para escribir 0xAA alternado con 0x55 en el puerto del PCF8574

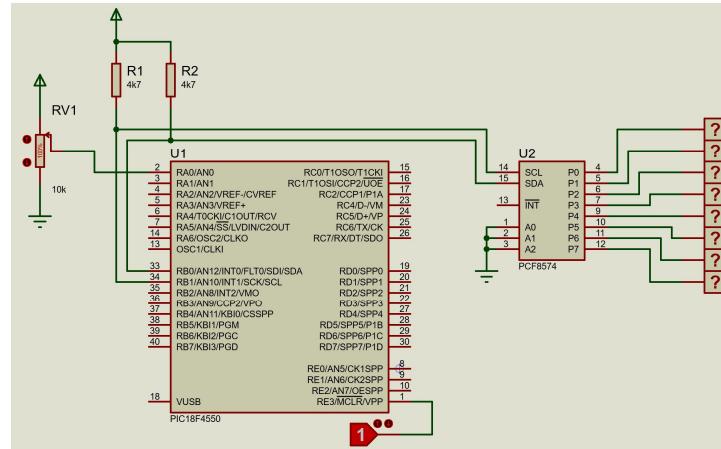
```

1  #pragma config PLLDIV = 1      // PLL Prescaler Sele
2  #pragma config CPUDIV = OSC1_PLL2// System Clock Post
3  #pragma config FOSC = XTPLL_XT // Oscillator Selecti
4  #pragma config FWRT = ON       // Power-up Timer Ena
5  #pragma config BOB = OFF        // Brown-out Reset En
6  #pragma config WDT = OFF        // Watchdog Timer Ena
7  #pragma config CCP2MX = OFF      // CCP2 MUX bit (CCF
8  #pragma config PBADEN = OFF      // PORTB A/D Enable k
9  #pragma config MCLE = ON        // MCLR Pin Enable bi
10 #pragma config LVP = OFF        // Single-Supply ICSE
11
12 #include <xc.h>
13 #define _XTAL_FREQ 48000000UL    //frecuencia de t
14
15 unsigned char dato = 0xAA;
16
17 void init_config(void) {
18     SSPCON1bits.SSPEN = 1;        //Encendemos el MSSP
19     SSPCON1bits.SSPM3 = 1;
20     SSPCON1bits.SSPM2 = 0;
21     SSPCON1bits.SSPM1 = 0;
22     SSPCON1bits.SSPM0 = 0;        //MSSP en I2C master
23     SSPADD = 119;                // clock en 100khz
24 }
25
26 void pcf8574_escribir(unsigned char dato){
27     SSPCON2bits.SEN = 1;          //evento de inicio
28     while(SSPCON2bits.SEN == 1);   //espero a que
29     SSPBUF = 0x40;
30     while(SSPSTATbits.BF == 1);   //espero a que se t
31     while(SSPSTATbits.R_nW == 1);
32     SSPBUF = dato;
33     while(SSPSTATbits.BF == 1);   //espero a que se t
34     while(SSPSTATbits.R_nW == 1);
35     SSPCON2bits.PEN = 1;
36     while(SSPCON2bits.PEN == 1);
37 }
38
39 void main(void){
40     init_config();
41     while(1){
42         pcf8574_escribir(0x55);
43         __delay_ms(100);
44         pcf8574_escribir(0xAA);
45         __delay_ms(100);
46     }
47 }

```

28

Ejemplo: Lectura de señal analógica en AN0 a través del ADC y emisión del resultado de la conversión en 8 bits por los puertos del PCF8574



29

Ejemplo: Lectura de señal analógica en AN0 a través del ADC y emisión del resultado de la conversión en 8 bits por los puertos del PCF8574

```

15 void init_config(void){
16     SSPCON1bits.SSPEN = 1;           //Encendemos el MSSP
17     SSPCON1bits.SSPM3 = 1;
18     SSPCON1bits.SSPM2 = 0;
19     SSPCON1bits.SSPM1 = 0;
20     SSPCON1bits.SSPM0 = 0;          //MSSP en I2C master
21     SSPADD = 119;                  // clock en 100khz
22     ADCON2 = 0x24;                // tiempo de conversion ADFI
23     ADCON1 = 0x0E;                //AN0 como anbalógico
24     ADCON0 = 0x01;                //Activar A/D
25 }
26
27 void pcf8574_escribir(unsigned char dato){
28     SSPCON2bits.SEN = 1;           //evento de inicio
29     while(SSPCON2bits.SEN == 1);   //espero a que sea 0
30     SSPBUF = 0x40;                //palabra de control
31     while(SSPSTATbits.BF == 1);    //espero a que se termine
32     while(SSPSTATbits.R_nW == 1);
33     SSPBUF = dato;               //dato a escribir en
34     while(SSPSTATbits.BF == 1);    //espero a que se termine
35     while(SSPSTATbits.R_nW == 1);
36     SSPCON2bits.PEN = 1;          //evento de parada
37     while(SSPCON2bits.PEN == 1);
38 }
39
40 void main(void){
41     init_config();
42     while(1){
43         ADCON0bits.GODONE = 1;
44         while(ADCON0bits.GODONE == 1);
45         pcf8574_escribir(ADRESH);
46     }
47 }
```

30

Fin de la sesión