

Microcontroladores

Sesión Teoría Semana 4
Profesor: Kalun José Lau Gan

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Preguntas previas:

- Escribir un dato en un puerto y luego leer ese puerto:

*movlw 0x55
movwf LATD
movf PORTD,w*

- Hay instrucciones que duren dos ciclos a parte de GOTO?
 - btfss, btfsc
 - decfsz, incfsz
 - call, return
 - cpfslt, cpfsgt, cpfseq
- Cómo configuro el Timer0 para que sea fuente de interrupción en baja prioridad?
 - Colocando TMR0IP = 0 (previamente RCON.IPEN=1, GIEL=1)

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Preguntas previas:

- Cómo cargo un valor de dirección en FSRx?

Opción 1:

```
lfsr $0, $123
    } 2 ciclos
```

Opción 2:

```
movlw $001
movwf FSR0H
movlw $023
movwf FSR0L
    } 4 ciclos
```

- El EA cuándo va a ser?

- Día viernes 18:00 – 21:00 según programación en aula virtual
- Modalidad de rendición similar a PC1
- Temario: Todo lo visto antes de la rendición de la evaluación

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Agenda:

- Multitarea en el microcontrolador PIC18F4550
- Uso del Timer1
- Uso del LCD alfanumérico 2x16 HD44780

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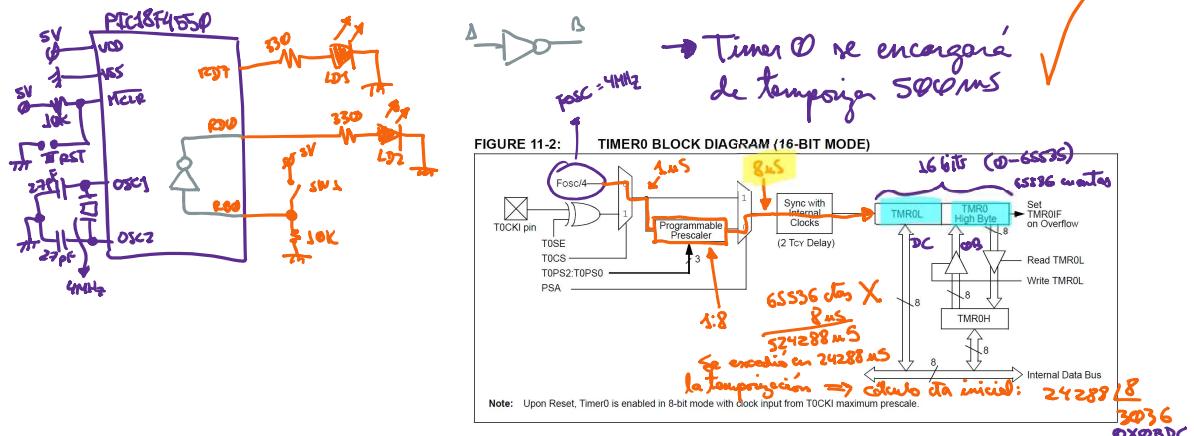
¿Multitarea?

- Ejecución de varias tareas a la vez en el microcontrolador
 - Sistemas RTOS (Real Time Operating System), relacionado con lenguajes de alto nivel generalmente.
 - En ensamblador la multitarea está relacionado con el uso de interrupciones.
 - Ejecución de una instrucción ≠ ejecución de una tarea

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Ejemplo:

- Por el RD7 se deberá titilar un LED con un periodo de 500ms y entre RB0 y RD0 deberá de funcionar un negador lógico.



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Configuración de Timer0

Legend:	R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7	TMR0ON: Timer0 On/Off Control bit 1 = Enables Timer0 0 = Stops Timer0
bit 6	TOBBIT: Timer0 8-Bit/16-Bit Control bit 1 = Timer0 is configured as an 8-bit timer/counter 0 = Timer0 is configured as a 16-bit timer/counter
bit 5	TOCS: Timer0 Clock Source Select bit 1 = Transition on TOCKI pin 0 = Internal instruction cycle clock (CLKO)
bit 4	T0SE: Timer0 Source Edge Select bit 1 = Increment on high-to-low transition on TOCKI pin 0 = Increment on low-to-high transition on TOCKI pin
bit 3	PSA: Timer0 Prescaler Assignment bit 1 = Timer0 prescaler is NOT assigned. Timer0 clock input bypasses prescaler. 0 = Timer0 prescaler is assigned, Timer0 clock input comes from prescaler output.
bit 2-0	TOPS2:TOP0: Timer0 Prescaler Select bits 111 = 1:256 Prescale value 110 = 1:128 Prescale value 101 = 1:64 Prescale value 100 = 1:32 Prescale value 011 = 1:16 Prescale value 010 = 1:8 Prescale value 001 = 1:4 Prescale value 000 = 1:2 Prescale value

TOCON = 0X82

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Configuración de interrupciones

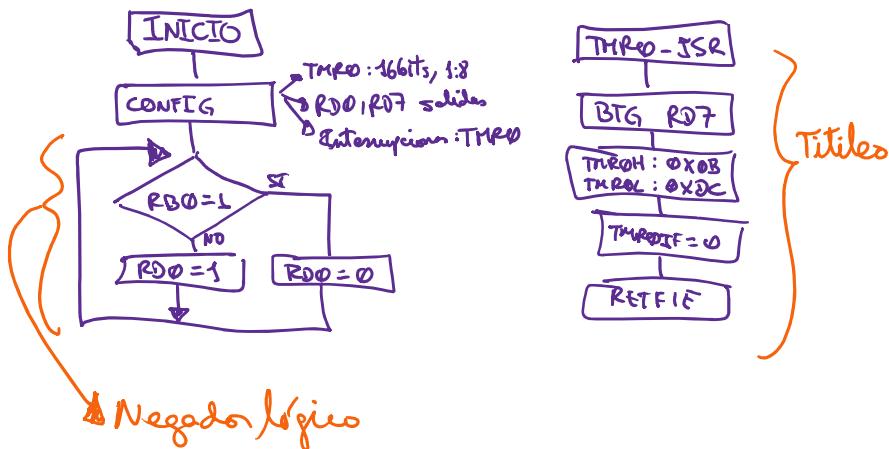
Legend:	R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7	GIE/GIEH: Global Interrupt Enable bit When IPEN = 0: 1 = Enables all unmasked interrupts 0 = Disables all interrupts When IPEN = 1: 1 = Enables all high-priority interrupts 0 = Disables all interrupts	$\text{INTCON} = \text{0XA0}$
bit 6	PEIE/GIEL: Peripheral Interrupt Enable bit When IPEN = 0: 1 = Enables all unmasked peripheral interrupts 0 = Disables all peripheral interrupts When IPEN = 1: 1 = Enables all low-priority peripheral interrupts (if GIE/GIEH = 1) 0 = Disables all low-priority peripheral interrupts	
bit 5	TMR0IE: TMR0 Overflow Interrupt Enable bit 1 = Enables the TMR0 overflow interrupt 0 = Disables the TMR0 overflow interrupt	
bit 4	INT0IE: INT0 External Interrupt Enable bit 1 = Enables the INT0 external interrupt 0 = Disables the INT0 external interrupt	
bit 3	RBI0: RB Port Change Interrupt Enable bit 1 = Enables the RB port change interrupt 0 = Disables the RB port change interrupt	
bit 2	TMR0IF: TMR0 Overflow Interrupt Flag bit 1 = TMR0 register has overflowed (must be cleared in software) 0 = TMR0 register did not overflow	
bit 1	INT0IF: INT0 External Interrupt Flag bit 1 = The INT0 external interrupt occurred (must be cleared in software) 0 = The INT0 external interrupt did not occur	
bit 0	RBI0IF: RB Port Change Interrupt Flag bit ⁽¹⁾ 1 = At least one of the RB7-RB4 pins changed state (must be cleared in software) 0 = None of the RB7-RB4 pins have changed state	

INTCON = 0XA0

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Desarrollo del diagrama de flujo:



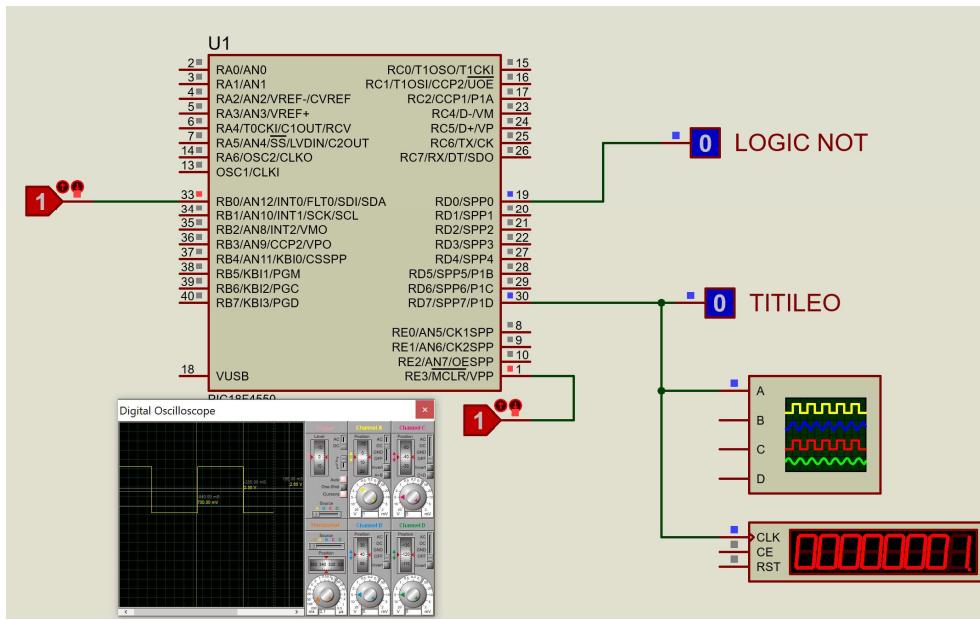
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Código en MPASM

<pre> 1 ;Este es un comentario, se le a 2 list p=18f4550 ;Modelo 3 #include <p18f4550.inc> 4 5 ;Directivas de preprocesado 6 CONFIG PLLDIV = 1 7 CONFIG CPUDIV = OSC1_PLL2 8 CONFIG FOSC = XT_XT 9 CONFIG FWRT = ON 10 CONFIG BOR = OFF 11 CONFIG WDT = OFF 12 CONFIG CCP2MX = ON 13 CONFIG PBADEN = OFF 14 CONFIG MCLRE = ON 15 CONFIG LVP = OFF 16 17 ;Aquí va el cblock o declaraci 18 cblock 0x000 19 endc 20 21 org 0x0000 22 goto init_conf 23 24 org 0x0008 25 goto TMRO_ISR 26 27 ;Aquí se pueden declarar las co 28 </pre>	<pre> 29 org 0x0020 30 init_conf: 31 movlw 0x7E 32 movwf TRISD 33 movlw 0x0B 34 movwf TMROH 35 movlw 0xDC 36 movwf TMROL 37 movlw 0x82 38 movwf TOCON 39 movlw 0xA0 40 movwf INTCON 41 42 loop: 43 btfss PORTB, 0 44 goto negativo 45 positivo: 46 bcf LATD, 0 47 goto loop 48 negativo: 49 bsf LATD, 0 50 goto loop 51 52 TMRO_ISR: 53 btg LATD, 7 54 movlw 0x0B 55 movwf TMROH 56 movlw 0xDC 57 movwf TMROL 58 bcf INTCON, TMROIF 59 retfie 60 61 end </pre>
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Simulación en Proteus



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Módulo Timer 1

- Tres fuentes de reloj para contar: Fosc/4, cristal 32.768KHz y pulsos externos en T13CKI (pin 15)
- Resolución de 16 bits (registros de cuenta TMR1H:TMR1L)
 - Cuentas van desde el 0 hasta 65535
- Cuenta ascendente
- Al desbordarse puede generar evento de interrupción (TMR1IF)
 - El desborde ocurre en 65535 -> 0
- Exclusivo para aplicaciones de RTC (empleando 32.768KHz)
- Opción de reinicio de cuenta con el módulo periférico CCP (modo comparación evento especial de disparo)
- Política de carga de datos en la cuenta: primero TMR1H y luego TMR1L

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Observaciones en el Proteus con respecto al uso del Timer1

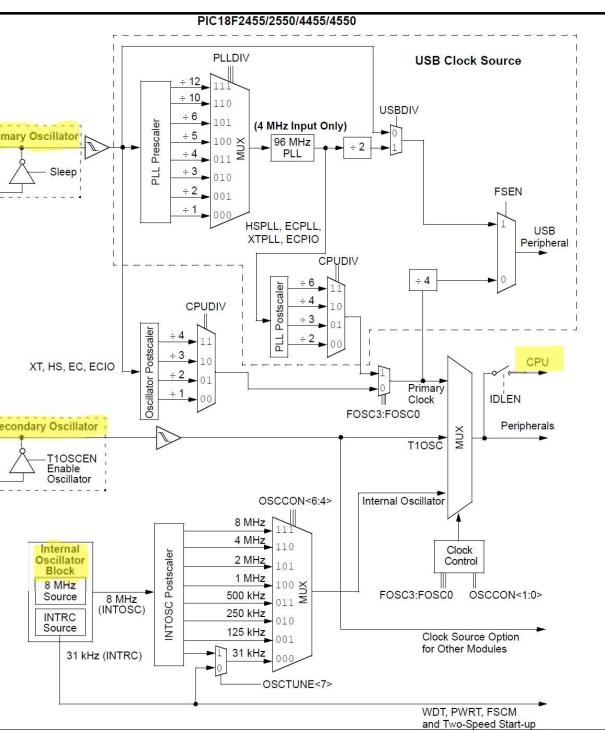
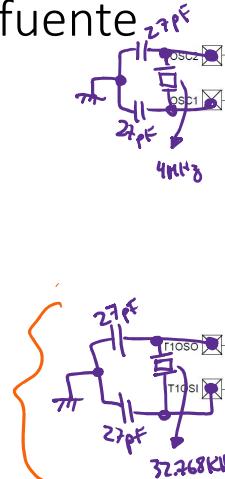
- No se simula correctamente el uso del cristal de 32.768KHz
- Para la simulación usaremos pulsos externos de reloj a la entrada T13CKI



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Recordando la configuración de fuente de reloj del CPU

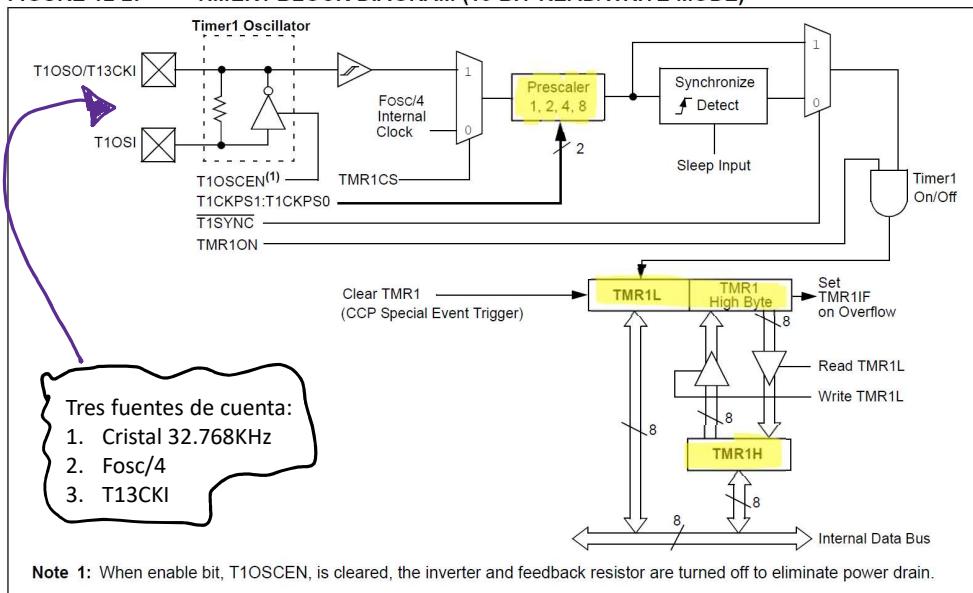
Se usa exclusivamente para el Timer1, pero en algunos casos este oscilador también puede ser direccionado para el CPU



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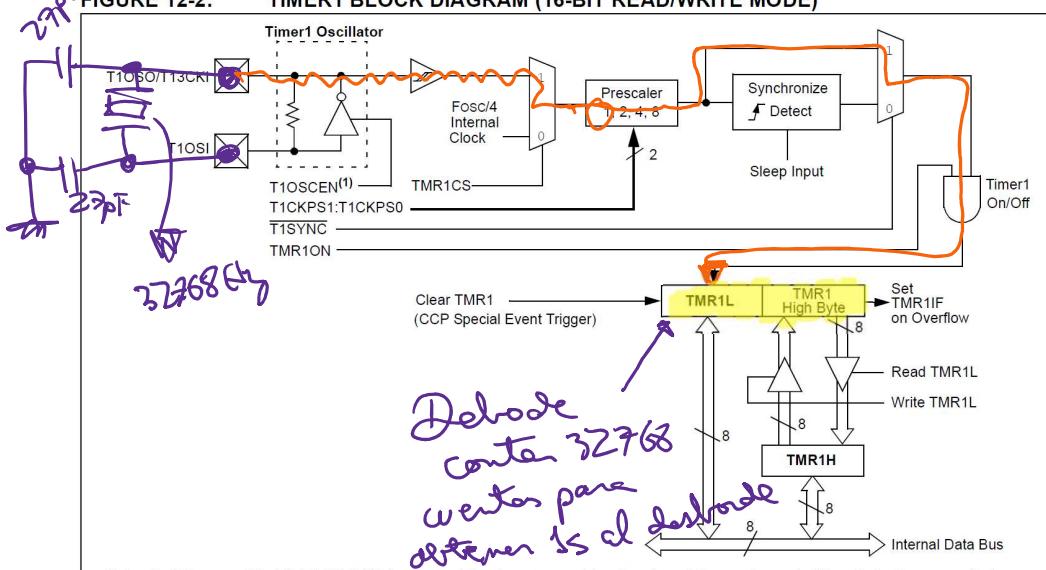
Diagrama de bloques del Timer1

FIGURE 12-2: TIMER1 BLOCK DIAGRAM (16-BIT READ/WRITE MODE)



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FIGURE 12-2: TIMER1 BLOCK DIAGRAM (16-BIT READ/WRITE MODE)



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Preguntas previas

- Se puede usar cristal de 32.768KHz como oscilador primario en OSC1/OSC2?
 - No! Revise hoja técnica!

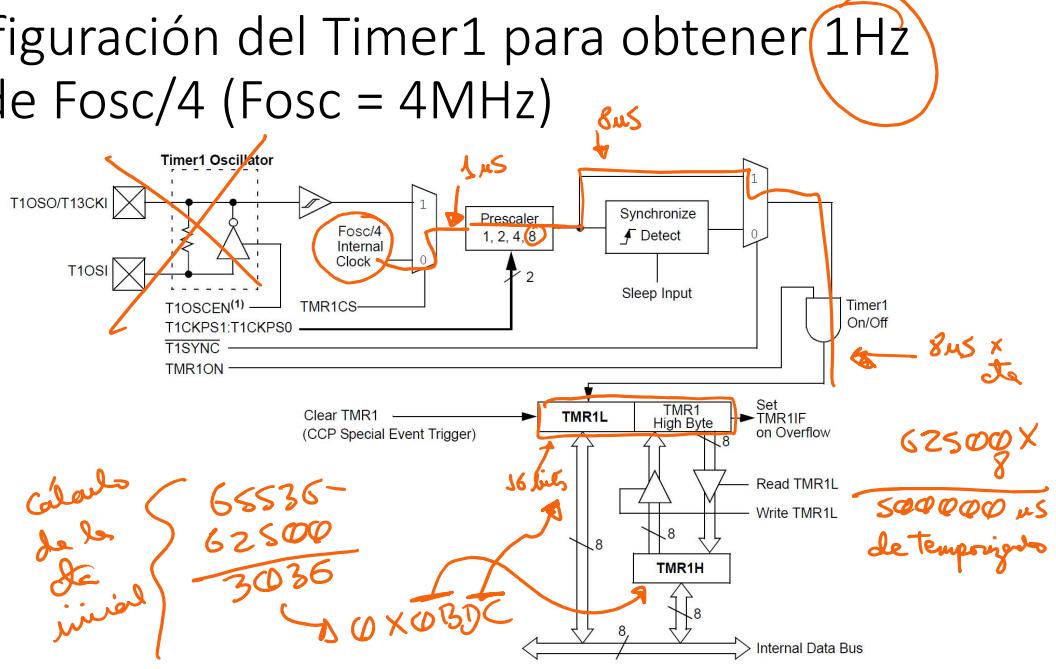
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Agenda

- Ejemplo de aplicación del Timer1 en RTC

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Configuración del Timer1 para obtener 1Hz desde Fosc/4 (Fosc = 4MHz)



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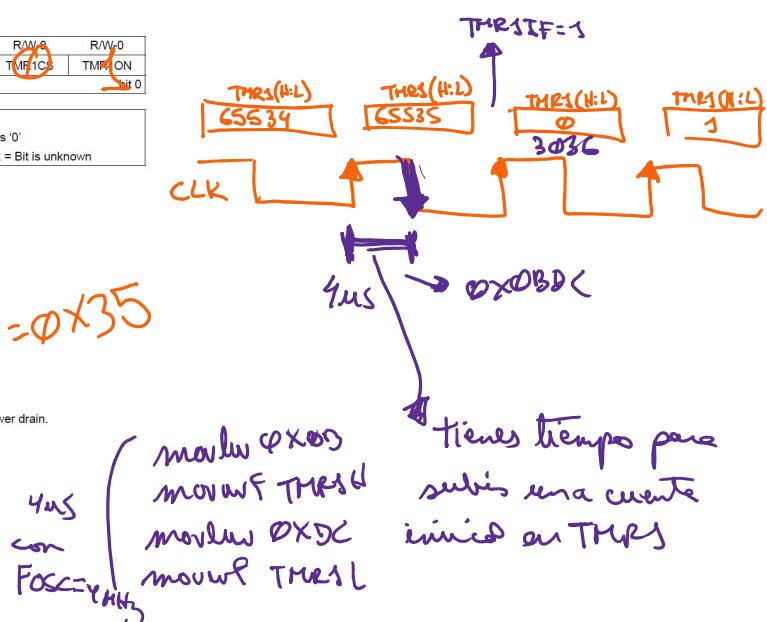
Análisis de la hoja técnica sobre Timer1:

REGISTER 12-1: T1CON: TIMER1 CONTROL REGISTER

bit 15	bit 14	R/W ₀	R/W ₀	W ₋₀	R/W ₀	R/W ₀	R/W ₀	R/W ₀
0	0	T1RUN	T1CKPS1	T1CKPS0	TOSCEN	T1SYNC	TMR1CS	TMR1ON

Legend:
 R = Readable bit W = Writable bit
 -n = Value at POR '1' = Bit is set
 U = Unimplemented bit, read as '0'
 '0' = Bit is cleared x = Bit is unknown

- bit 7 RD16: 16-Bit Read/Write Mode Enable bit
 1 = Enables register read/write of Timer1 in one 16-bit operation
 0 = Enables register read/write of Timer1 in two 8-bit operations
- bit 6 T1RUN: Timer1 System Clock Status bit
 1 = Device clock is derived from Timer1 oscillator
 0 = Device clock is derived from another source
- bit 5-4 T1CKPS1:T1CKPS0: Timer1 Input Clock Prescale Select bits
 11 = 1:8 Prescale value
 10 = 1:4 Prescale value
 01 = 1:2 Prescale value
 00 = 1:1 Prescale value
- bit 3 T1OSCEN: Timer1 Oscillator Enable bit
 1 = Timer1 oscillator is enabled
 0 = Timer1 oscillator is shut off
 The oscillator inverter and feedback resistor are turned off to eliminate power drain.
- bit 2 T1SYNC: Timer1 External Clock Input Synchronization Select bit
 When TMR1CS = 1:
 1 = Do not synchronize external clock input
 0 = Synchronize external clock input
 When TMR1CS = 0:
 This bit is ignored. Timer1 uses the internal clock when TMR1CS = 0.
- bit 1 TMR1CS: Timer1 Clock Source Select bit
 1 = External clock from RC0/T1OSO/T13CKI pin (on the rising edge)
 0 = Internal clock (Fosc/4)
- bit 0 TMR1ON: Timer1 On bit
 1 = Enables Timer1
 0 = Stops Timer1



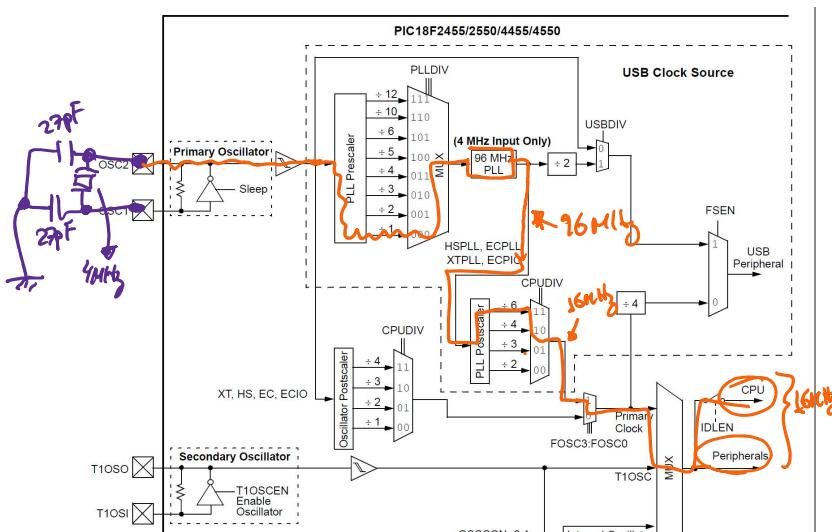
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Notas:

- Empleando Fosc=4MHZ para alimentar al CPU y también al Timer1 (Fosc/4), se tiene una ventana de 4us entre el flanco positivo de reloj que produjo la interrupción por desborde y su siguiente flanco negativo. Y esta ventana es muy corta como para poder colocar una cuenta inicial.

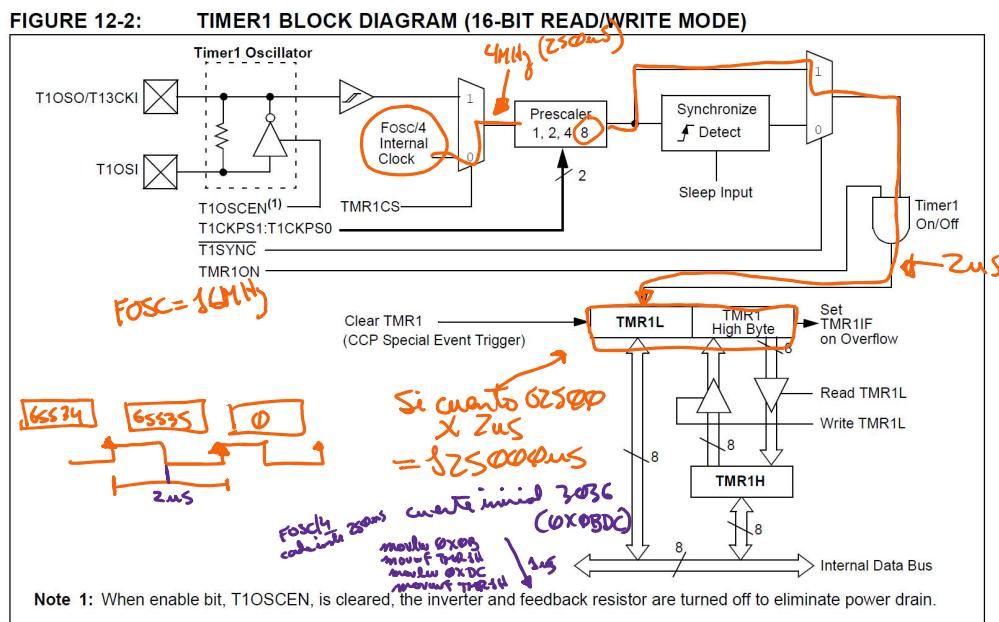
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Alternativa: Utilizando XTPLL corriendo a 16MHz:



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Analizado TMR1 ahora con Fosc=16MHz



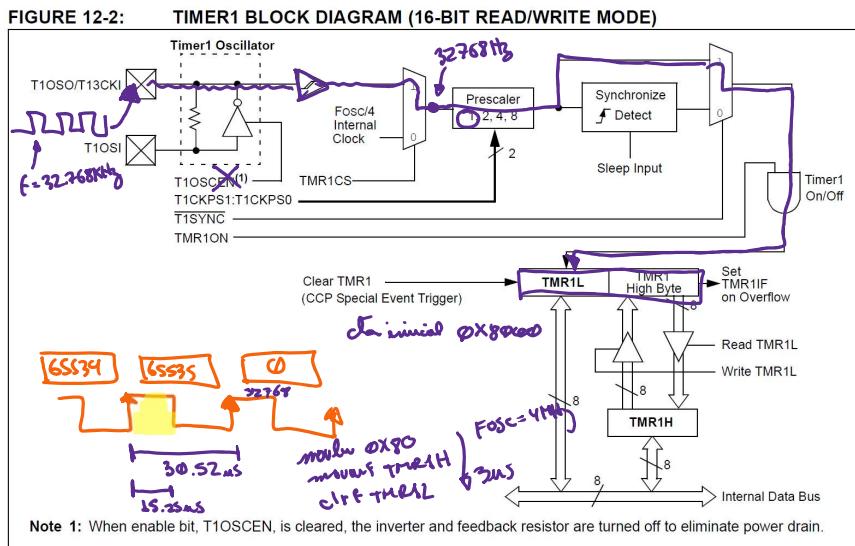
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Conclusiones

- Empleando el mismo cristal principal tanto directo como en PLL, no será posible implementar RTC en Timer1 verificado en los análisis anterior y corroborado con la hoja técnica.
- De todas maneras se tiene que emplear una fuente de reloj de 32.768KHz para las aplicaciones en tiempo real.
- Hay una opción en el cuál es posible emplear un solo cristal (el primario) para aplicaciones en tiempo real con el Timer1 pero tendrá que funcionar en conjunto con el módulo CCP en modo comparador evento especial de disparo.

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Trabajando el Timer1 con T1CKI y reloj de entrada 32.768KHz



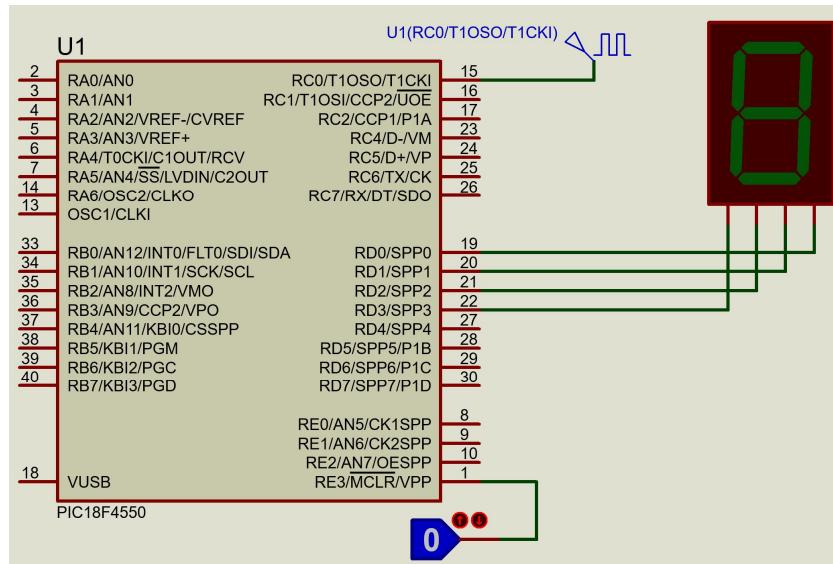
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Configuración del registro T1CON

REGISTER 12-1: T1CON: TIMER1 CONTROL REGISTER							
R/W-0	R-	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
RD16	RD15	T1RUN	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS
bit 7							bit 0
<i>Si esas instel = 1 Si esas sienl cambie = 0</i>							
Legend:							
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'					
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown				
bit 7	RD16: 16-Bit Read/Write Mode Enable bit						
	1 = Enables register read/write of Timer1 in one 16-bit operation						
	0 = Enables register read/write of Timer1 in two 8-bit operations						
bit 6	T1RUN: Timer1 System Clock Status bit						
	1 = Device clock is derived from Timer1 oscillator						
	0 = Device clock is derived from another source						
bit 5-4	T1CKPS1:T1CKPS0: Timer1 Input Clock Prescale Select bits						
	11 = 1:8 Prescale value						
	10 = 1:4 Prescale value						
	01 = 1:2 Prescale value						
	00 = 1:1 Prescale value						
bit 3	T1OSCEN: Timer1 Oscillator Enable bit						
	1 = Timer1 oscillator is enabled						
	0 = Timer1 oscillator is shut off						
	The oscillator inverter and feedback resistor are turned off to eliminate power drain.						
bit 2	T1SYNC: Timer1 External Clock Input Synchronization Select bit						
	When TMR1CS = 1:						
	1 = Do not synchronize external clock input						
	0 = Synchronize external clock input						
	When TMR1CS = 0:						
bit 1	This bit is ignored. Timer1 uses the internal clock when TMR1CS = 0.						
	TMR1CS: Timer1 Clock Source Select bit						
	1 = External clock from RC0/T1OSO/T13CKI pin (on the rising edge)						
	0 = Internal clock (Fosc/4)						
bit 0	TMR1ON: Timer1 On bit						
	1 = Enables Timer1						
	0 = Stops Timer1						

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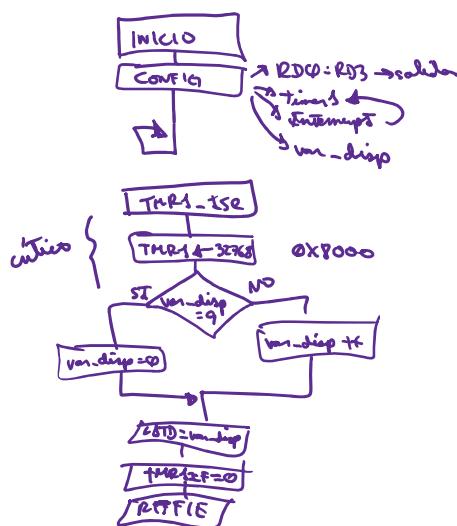
Circuito de simulación en Proteus



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Diagrama de flujo

- Contador 0-9 en RTC con Timer1



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Configuración de interrupciones para TMR1

REGISTER 9-1: INTCON: INTERRUPT CONTROL REGISTER

R/W	bit 7	R/W	R/W	R/W	R/W	R/W	R/W	R/W	bit 0
GIE/GIEH	When (IPEN = 0): 1 = Enables all unmasked interrupts 0 = Disables all interrupts	PEIE/GIEL	T0IE	INT0IE	FREE	TMR0IF	INT0IF	RBIF	

Legend:
 R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7 **GIE/GIEH:** Global interrupt enable bit
 When (IPEN = 0):
 1 = Enables all unmasked interrupts
 0 = Disables all interrupts
 When (IPEN = 1):
 1 = Enables all high-priority interrupts
 0 = Disables all interrupts
 bit 6 **PEIE/GIEL:** Peripheral interrupt enable bit
 When (IPEN = 0):
 1 = Enables all unmasked peripheral interrupts
 0 = Disables all peripheral interrupts
 When (IPEN = 1):
 1 = Enables all low-priority peripheral interrupts (if GIE/GIEH = 1)
 0 = Disables all low-priority peripheral interrupts
 bit 5 **TMR0IE:** TMR0 overflow interrupt enable bit
 1 = Enables the TMR0 overflow interrupt
 0 = Disables the TMR0 overflow interrupt
 bit 4 **INT0IE:** INT0 external interrupt enable bit
 1 = Enables the INT0 external interrupt
 0 = Disables the INT0 external interrupt
 bit 3 **RBIE:** RB port change interrupt enable bit
 1 = Enables the RB port change interrupt
 0 = Disables the RB port change interrupt
 bit 2 **TMR0IF:** TMR0 overflow interrupt flag bit
 1 = TMR0 register has overflowed (must be cleared in software)
 0 = TMR0 register did not overflow
 bit 1 **INT0IF:** INT0 external interrupt flag bit
 1 = The INT0 external interrupt occurred (must be cleared in software)
 0 = The INT0 external interrupt did not occur
 bit 0 **RBIF:** RB port change interrupt flag bit⁽¹⁾
 1 = At least one of the RB7/RB4 pins changed state (must be cleared in software)
 0 = None of the RB7/RB4 pins have changed state

REGISTER 9-6: PIE1: PERIPHERAL INTERRUPT ENABLE REGISTER 1

R/W	bit 7	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
SPPIE	When (IPEN = 0): 1 = Enables the SPP read/write interrupt 0 = Disables the SPP read/write interrupt	ADE	RCIE	TXIE	SSPE	CAP1IE	TMR2IE	TMR1IE	

Legend:
 R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7 **SPPIE:** Streaming Parallel Port Read/Write Interrupt Enable bit⁽¹⁾
 1 = Enables the SPP read/write interrupt
 0 = Disables the SPP read/write interrupt
 bit 6 **ADIE:** A/D converter interrupt enable bit
 1 = Enables the A/D interrupt
 0 = Disables the A/D interrupt
 bit 5 **RCIE:** USART receive interrupt enable bit
 1 = Enables the USART receive interrupt
 0 = Disables the USART receive interrupt
 bit 4 **TXIE:** USART transmit interrupt enable bit
 1 = Enables the USART transmit interrupt
 0 = Disables the USART transmit interrupt
 bit 3 **SSPIE:** Master synchronous serial port interrupt enable bit
 1 = Enables the MSSP interrupt
 0 = Disables the MSSP interrupt
 bit 2 **CCP1IE:** CCP1 interrupt enable bit
 1 = Enables the CCP1 interrupt
 0 = Disables the CCP1 interrupt
 bit 1 **TMR2IE:** TMR2 to PR2 match interrupt enable bit
 1 = Enables the TMR2 to PR2 match interrupt
 0 = Disables the TMR2 to PR2 match interrupt
 bit 0 **TMR1IE:** TMR1 overflow interrupt enable bit
 1 = Enables the TMR1 overflow interrupt
 0 = Disables the TMR1 overflow interrupt

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Código en MPASM:

```

2      list p=18f4550 ;Modelo
3      #include <p18f4550.inc>
4
5      ;Directivas de preprocesador:
6      CONFIG PLLDIV = 1
7      CONFIG CPUDIV = OSC1_PLL2
8      CONFIG FOSC = XT_XT
9      CONFIG PWRT = ON
10     CONFIG BOR = OFF
11     CONFIG WDT = OFF
12     CONFIG CCP2MX = ON
13     CONFIG PBADEN = OFF
14     CONFIG MC1RE = ON
15     CONFIG LVP = OFF
16
17     ;Aquí va el cblock o declaración de variables
18     cblock 0x0000
19     var_disp
20     endc
21
22     org 0x0000
23     goto init_conf
24
25     org 0x0008
26     goto TMR1_ISR
27
28     ;Aquí se pueden declarar las constantes
29
30     org 0x0020
31     init_conf:
32     movlw 0xF0
33     movwf TRISD
34     movlw 0x07
35     movwf TLCN
36     movlw 0x80
37     movwf TMRIH
38     clrf TMRII
39     movlw 0xC0
40     movwf INTCON
41     movlw 0x01
42     movwf PIE1
43     clrf var_disp
44

```

```

45     loop:
46         goto loop
47
48     TMR1_ISR:
49         movlw 0x80
50         movwf TMRIH
51         clrf TMRII ;tejed = 3us cumpliendo que se suba la cta inicial antes de los 15.25us
52         movlw .9
53         cpfsq var_disp
54         goto aumno
55         clrf var_disp
56         goto final
57     aumno:
58         incf var_disp, f
59     final:
60         movff var_disp, LATD
61         bcf PIR1, TMR1IF
62         retfie
63         end

```

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