

Microcontroladores

Laboratorio Sesión 6

Semestre: 2022-1

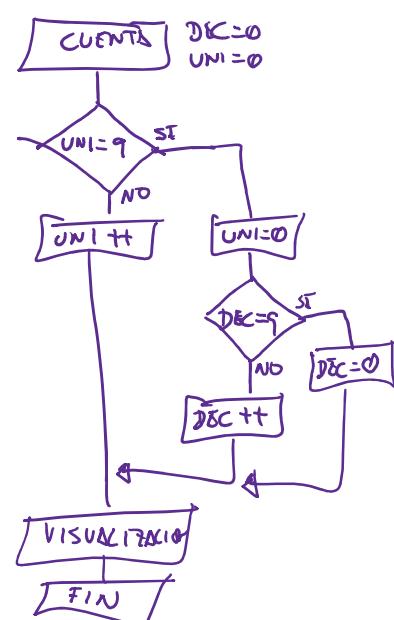
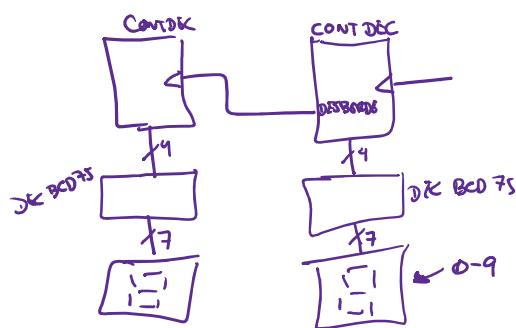
Profesor: Kalun José Lau Gan

1

Preguntas previas (alzar la mano durante la consulta)

Algoritmo para cuenta 00-99:

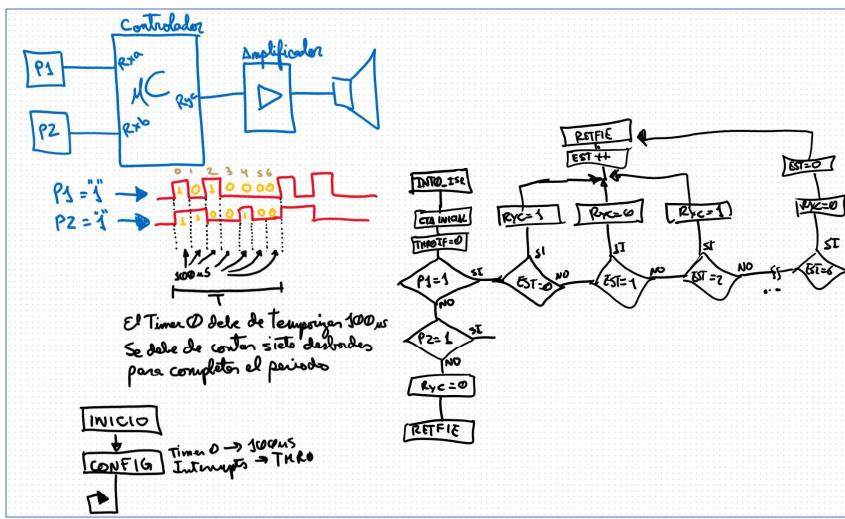
Idea:



2

Preguntas previas (alzar la mano durante la consulta)

- Tuve dificultades para desarrollar la onda requerida en la última pregunta de la PC1



3

Preguntas previas (alzar la mano durante la consulta)

- ?

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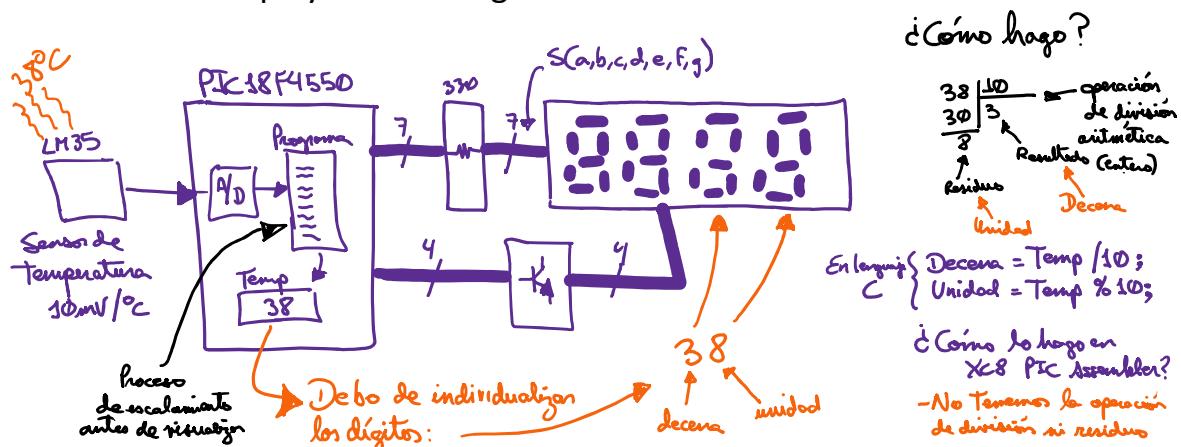
Agenda

- Rutina para obtener los dígitos centena, decena y unidad de un registro de 8 bits
 - Timer 1 para aplicaciones en tiempo real (RTC)
 - Referencia: Unidad 12 de la hoja técnica del PIC18F4550
 - Interrupciones con el Timer 1
 - Ejemplos con el Timer 1

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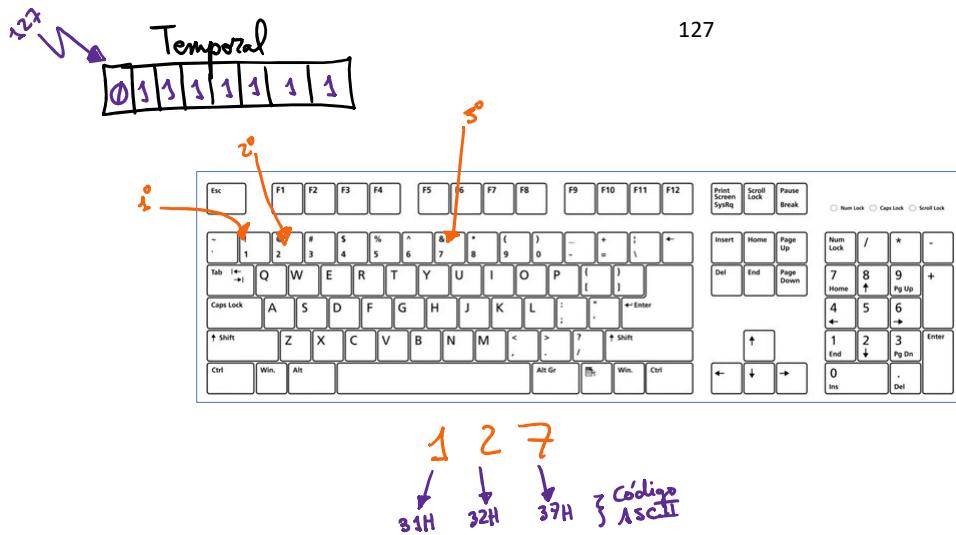
Rutina para obtener los dígitos centena, decena y unidad de un registro de 8 bits

- Sirve para individualizar los dígitos de un registro para así visualizarlos en cada display de siete segmentos.



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Idea: ¿Cómo ingresas el número 127 a la PC?



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Rutina para obtener los dígitos centena, decena y unidad de un registro de 8 bits

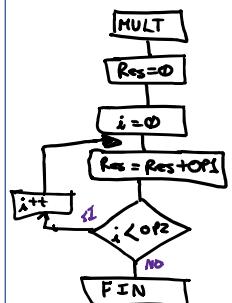
Ejemplo:

$$\begin{array}{r}
 \text{OP1} \quad \text{OP2} \quad \text{Res} \\
 \downarrow \quad \downarrow \quad \downarrow \\
 8 \times 4 = 32 \\
 \begin{array}{r}
 8+ \\
 8 \\
 8 \\
 8 \\
 \hline
 32
 \end{array}
 \qquad
 \begin{array}{r}
 8 \times 6 = 48 \\
 \begin{array}{r}
 8+ \\
 8 \\
 8 \\
 8 \\
 8 \\
 8 \\
 \hline
 48
 \end{array}
 \end{array}
 \\
 \begin{array}{r}
 (8 \times 1 = 8) \\
 8
 \end{array}
 \qquad
 \begin{array}{r}
 8 \times 2 = 16 \\
 \begin{array}{r}
 8+ \\
 8 \\
 \hline
 16
 \end{array}
 \end{array}
 \end{array}$$

Recordando:

```

For (i=0; i<9; i++) {
    } Se va a repetir 9 veces
    → OP1 = 8
    OP2 = 4
    Res = 0
    For (i=0; i<OP2; i++) {
        Res = Res + OP1;
    }
}
  
```



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Rutina para obtener los dígitos centena, decena y unidad de un registro de 8 bits

Tomo el número 133, obtener centena, decena y unidad:

$$\begin{array}{r} \text{Temp} = 133 - \\ \hline 100 \\ 33 - \\ 100 \\ \hline -67 \end{array}$$

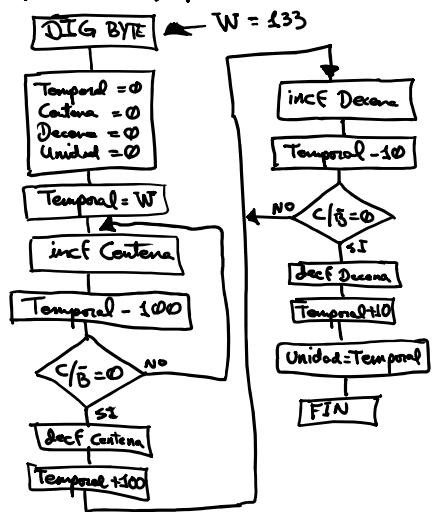
¿Cuántas veces he restado 100?
- Dos veces → centena
Restar uno a centena

$$\begin{array}{r} -67 + \\ 100 \\ \hline 33 - \\ 10 \\ \hline 23 - \\ 10 \\ \hline 13 - \\ 10 \\ \hline 3 - \\ 10 \\ \hline -7 \end{array}$$

¿Cuántas veces he restado 10?
- Cuatro veces.
→ Restar uno y obtengo la decena
Número negativo

Nota:
El bit C/B de STATUS:
Suma: C
Resta: B

Diagrama de flujo:



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Módulo Timer 1

- Tres fuentes de reloj para contar: Fosc/4, pulsos externos en T13CKI (pin 15) y cristal 32.768KHz
- Resolución de 16 bits (registros de cuenta TMR1H:TMR1L)
 - Total de cuentas: 65536
 - Cuentas van desde el 0 hasta 65535
- Cuenta ascendente
- Al desbordarse (overflow) puede generar evento de interrupción (TMR1IF)
 - El desborde ocurre en 65535 -> 0
- **Exclusivo para aplicaciones de RTC (empleando 32.768KHz)**
- Opción de reinicio de cuenta con el módulo periférico CCP (modo comparación evento especial de disparo)
- Política de carga de datos en la cuenta: primero TMR1H y luego TMR1L

Observaciones en el Proteus con respecto al uso del Timer1

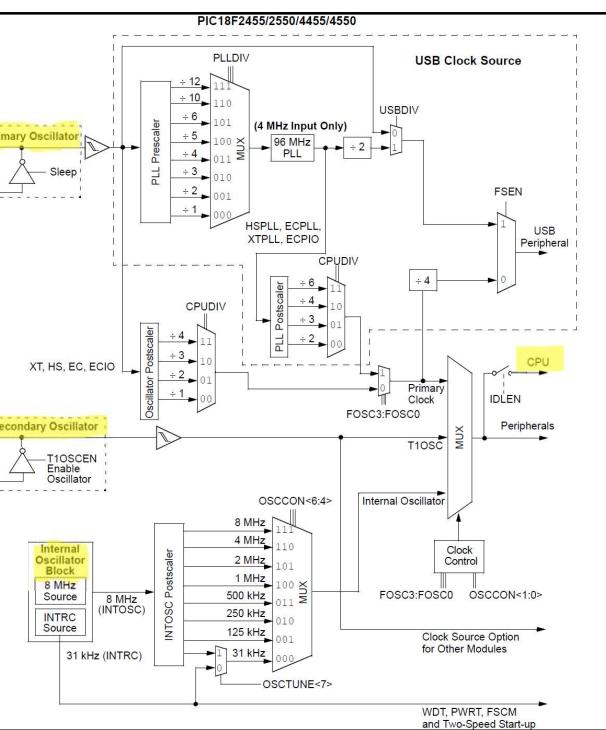
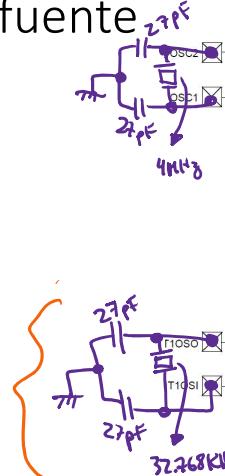
- No se simula correctamente el uso del cristal de 32.768KHz
- Para la simulación usaremos pulsos externos de reloj a la entrada T13CKI



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Recordando la configuración de fuente de reloj del CPU

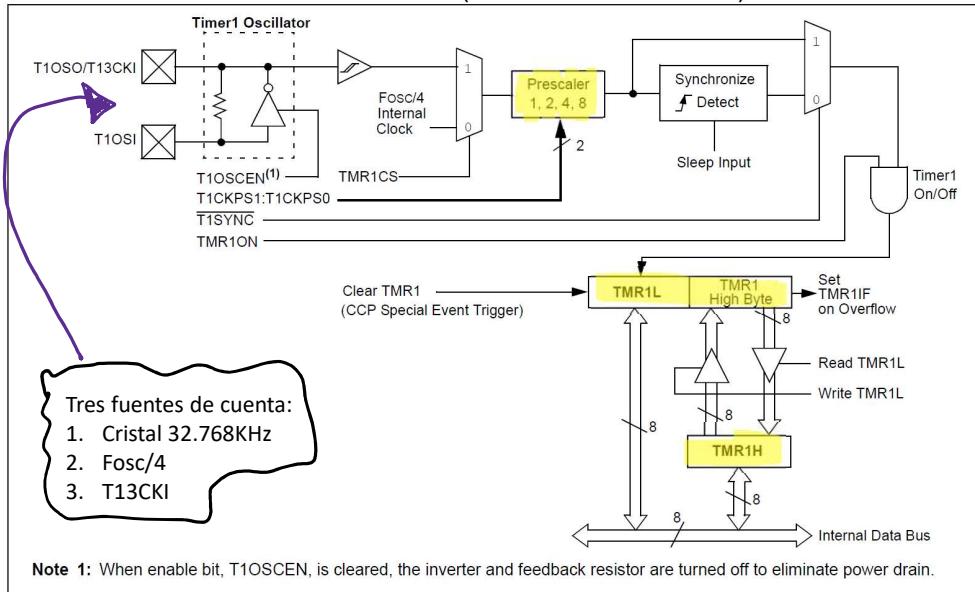
Se usa exclusivamente para el Timer1, pero en algunos casos este oscilador también puede ser direccionado para el CPU



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Diagrama de bloques del Timer1

FIGURE 12-2: TIMER1 BLOCK DIAGRAM (16-BIT READ/WRITE MODE)



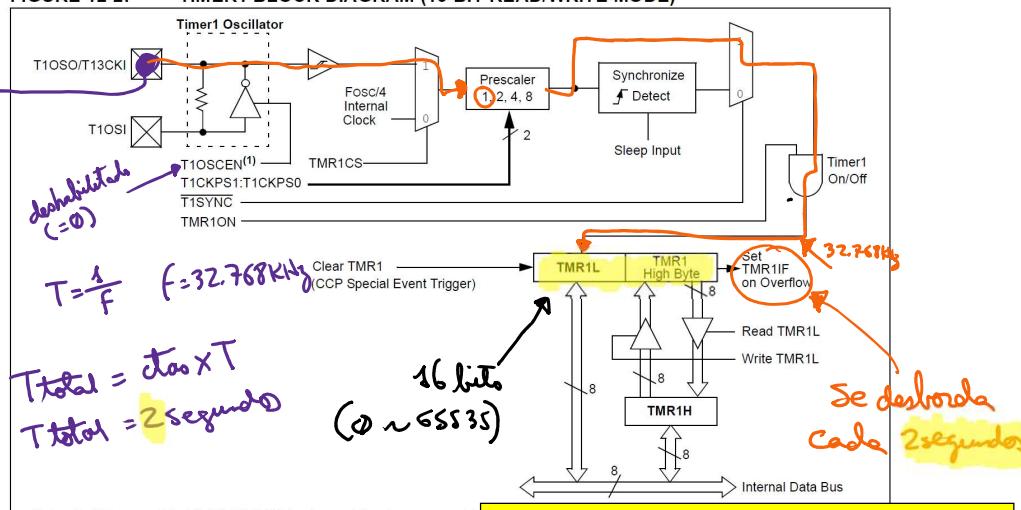
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Opción 1: Ingreso de pulsos de reloj a través de T13CKI

$f = 32.768\text{KHz}$

FUNC
ON

FIGURE 12-2: TIMER1 BLOCK DIAGRAM (16-BIT READ/WRITE MODE)



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Opción 1: Ingreso de pulsos de reloj a través de T13CKI

- Según la configuración anterior, el Timer1 se está desbordando cada 2 segundos
- Si necesitamos que se desborde cada segundo debemos de precargar la cuenta en 32768
- Para precargar la cuenta necesitamos escribir en TMR1H y TMR1L el valor de 32768, este proceso de carga le toma un tiempo al uC para ejecutarlo:

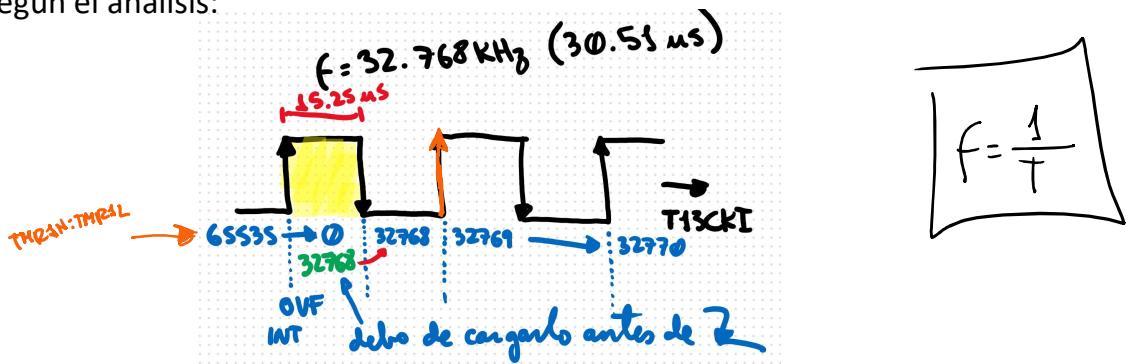


- Mi aplicación se retrasa en el tiempo!
- Tener en cuenta lo estipulado en 12.6 y 12.7 de la hoja técnica

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Opción 1: Ingreso de pulsos de reloj a través de T13CKI

- Según el análisis:



- Se tiene una ventana de tiempo de 15.25μs (antes de que haya el flanko negativo de la señal de reloj) para cargar una cuenta inicial en TMR1 luego de producirse una interrupción por desborde de TMR1. El proceso de carga se realizará en el flanko negativo.
- Para que esto funcione se debe de cumplir con lo estipulado en el último párrafo del 12.6 de la hoja técnica: Modo asíncrono, interrupciones habilitadas y fuente de reloj funcionando todo el tiempo

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Ejemplo 1: Obtener una señal de reloj de 1Hz en la basculación de RD0 empleando el Timer1 en modo RTC.

- Hardware (para Proteus)

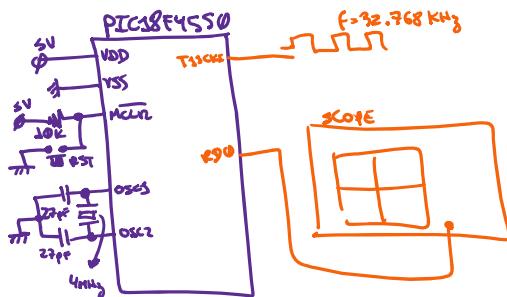
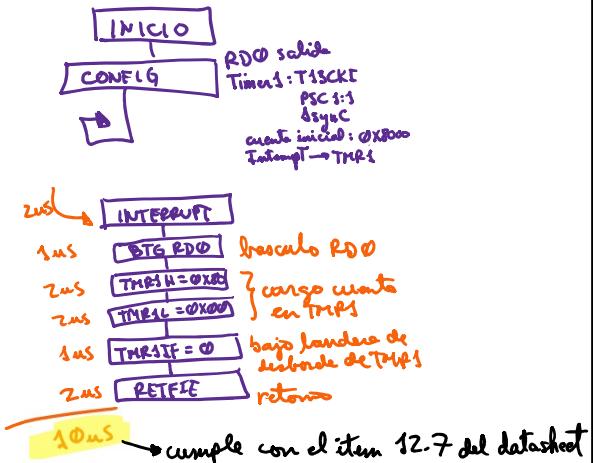


Diagrama de Flujo:



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Ejemplo 1: Obtener una señal de reloj de 1Hz empleando el Timer1 en modo RTC.

- Configuración de TMR1 (registro T1CON)

$\textcircled{0} \times 07$
 07H

| REGISTER 12-1: T1CON: TIMER1 CONTROL REGISTER | | | | | | | |
|--|---|---|---|--|---|--|-------|
| R/W-0 | R-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| bit 7 | bit 6 | bit 5-4 | bit 3 | bit 2 | bit 1 | bit 0 | |
| T1CON: Timer1 Control Register | | | | | | | |
| R = Readable bit -n = Value at POR | W = Writable bit '1' = Bit is set '0' = Bit is cleared | U = Unimplemented bit, read as '0' x = Bit is unknown | | | | | |
| bit 7: RD16: 16-Bit Read/Write Mode Enable bit 1 = Enables register read/write of Timer1 in one 16-bit operation 0 = Enables register read/write of Timer1 in two 8-bit operations | bit 6: T1RUN: Timer1 System Clock Status bit 1 = Device clock is derived from Timer1 oscillator 0 = Device clock is derived from another source | bit 5-4: T1CKPS1:T1CKPS0: Timer1 Input Clock Prescale Select bits 11 = 1:8 Prescale value 10 = 1:4 Prescale value 01 = 1:2 Prescale value 00 = 1:1 Prescale value | bit 3: T1OSCEN: Timer1 Oscillator Enable bit 1 = Timer1 oscillator is enabled 0 = Timer1 oscillator is shut off The oscillator inverter and feedback resistor are turned off to eliminate power drain. | bit 2: T1SYNC: Timer1 External Clock Input Synchronization Select bit When TMR1CS = 1: 1 = Do not synchronize external clock input 0 = Synchronize external clock input When TMR1CS = 0: This bit is ignored. Timer1 uses the internal clock when TMR1CS = 0. | bit 1: TMR1CS: Timer1 Clock Source Select bit 1 = External clock from RCO/T1OSC/T13CKI pin (on the rising edge) 0 = Internal clock (Fosc/4) | bit 0: TMR1ON: Timer1 On bit 1 = Enables Timer1 0 = Stops Timer1 | |

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Ejemplo 1: Obtener una señal de reloj de 1Hz empleando el Timer1 en modo RTC.

- Configuración de la interrupción del TMR1 (TMR1IF se encuentra en PIR1)

| REGISTER 9-1: INTCON: INTERRUPT CONTROL REGISTER | | | | | | | | | |
|--|---------------------------------------|--------------------------------------|------------------------------------|----------------------|--------------------|-------|--------|--|--|
| R/W-A | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | | |
| GIE/H | PEIESEL | TMR0IE | INSE | SSB | TMR0IF | TOIF | PIR1 | | |
| bit 7 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | | |
| Legend: | R = Readable bit -n = Value at POR | W = Writable bit '1' = Bit is set | U = Unimplemented bit, read as '0' | '0' = Bit is cleared | x = Bit is unknown | | | | |
| bit 7 | INTCON: 0X C0 | | | | | | | | |
| bit 6 | 0C0H | | | | | | | | |
| REGISTER 9-6: PIE1: PERIPHERAL INTERRUPT ENABLE REGISTER 1 | | | | | | | | | |
| R/W-A | R/W-0 | PAIN0 | R/W-0 | PAIN0 | R/W-0 | PAIN0 | R/W-0 | | |
| SPIE1 | ADIE | TRIE | TXIE | SPIE | CPIF1 | EWIE | TMR1IE | | |
| bit 7 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | | |
| Legend: | R = Readable bit -n = Value at POR | W = Writable bit '1' = Bit is set | U = Unimplemented bit, read as '0' | '0' = Bit is cleared | x = Bit is unknown | | | | |
| bit 7 | PIE1: 0X 01 | | | | | | | | |
| bit 6 | 01H | | | | | | | | |

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Ejemplo 1: Obtener una señal de reloj de 1Hz empleando el Timer1 en modo RTC.

- Código en MPASM

```

17    org 0x0000
18    goto init_conf
19
20    org 0x0008
21    goto TMR1_ISR
22
23    ;Aqui se pueden declarar las constantes en la memoria de programa
24
25    org 0x0020
26    init_conf:
27        bcf TRISD, 0      ;RD0 como salida
28        movlw 0x07
29        movwf TICON       ;TMR1 on, 1:1PSC, T13CKI
30        movlw 0x01
31        movwf PIE1         ;Interrupcion de TMR1 habilitado
32        movlw 0xC0
33        movwf INTCON       ;Interrupciones habilitadas (globales y de periféricos)
34
35    loop:
36        nop
37        goto loop
38
39    TMR1_ISR:
40        btg LATD, 0      ;Basculo la salida RD0
41        movlw 0x00
42        movwf TMR1H
43        clrf TMR1L        ;Cargo 49152 como cuenta inicial
44        bcf PIR1, TMR1IF   ;Bajo la bandera de desborde de TMR1
45        retfie
46        end

```

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Ejemplo 1: Obtener una señal de reloj de 1Hz empleando el Timer1 en modo RTC.

- Código en XC8 PIC Assembler
- Empleando RD7 como salida de señal.
- Opción para implementación física (líneas 21-22)
- La basculación la está haciendo a 1Hz, si se requiere obtener una señal de reloj se deberá de disminuir la cantidad de cuentas a contar de 16384 en el Timer1 (cuenta inicial de 49152 en TMR1H:TMR1L, líneas 33-35).

```

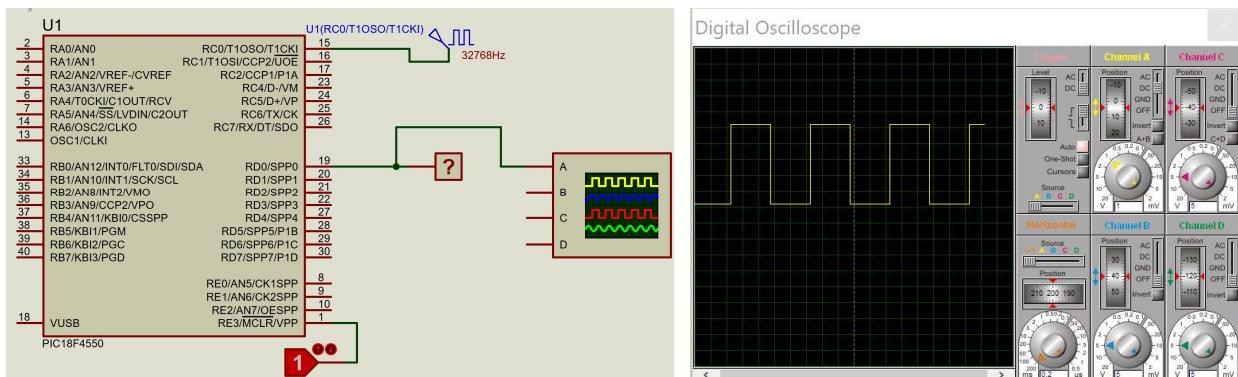
4      PROCESSOR 10f4550
5      #include "cabecera.inc"
6
7      FSECT erretece,class=CODE,reloc=2,abs
8
9      ORG 00000H          ;Vector de reset
10     erretece:    goto configuracion
11
12     ORG 00008H          ;Vector de interrupcion
13     vector_hp:    goto TMRL_ISR
14
15     ORG 00020H
16     configuracion:
17         bcf TRISD, 7      ;RD7 como salida
18         movlw 07H
19         movwf T1CON        ;Tmr1 ON, PSC 1:1, T13CKI (T1OSCEN=0) sin cristal (para Proteus)
20         ; movlw 0FH
21         ; movwf T1CON        ;Tmr1 ON, PSC 1:1, XTAL32K (T1OSCEN=1) con cristal 32K
22         movlw 01H
23         movwf PIE1           ;TMRIIE=1
24         movlw 0C0H
25         movwf INTCON         ;GIE=1,PEIE=1
26
27     loop:
28         nop
29         goto loop
30
31     TMRL_ISR:
32         btg LATD, 7       ;Basculando RD7
33         movlw 080H
34         movwf TMR1H
35         clrf TMR1L          ;49152 ;32768
36         bcf PIR1, 0
37         retfie
38     end erretece

```

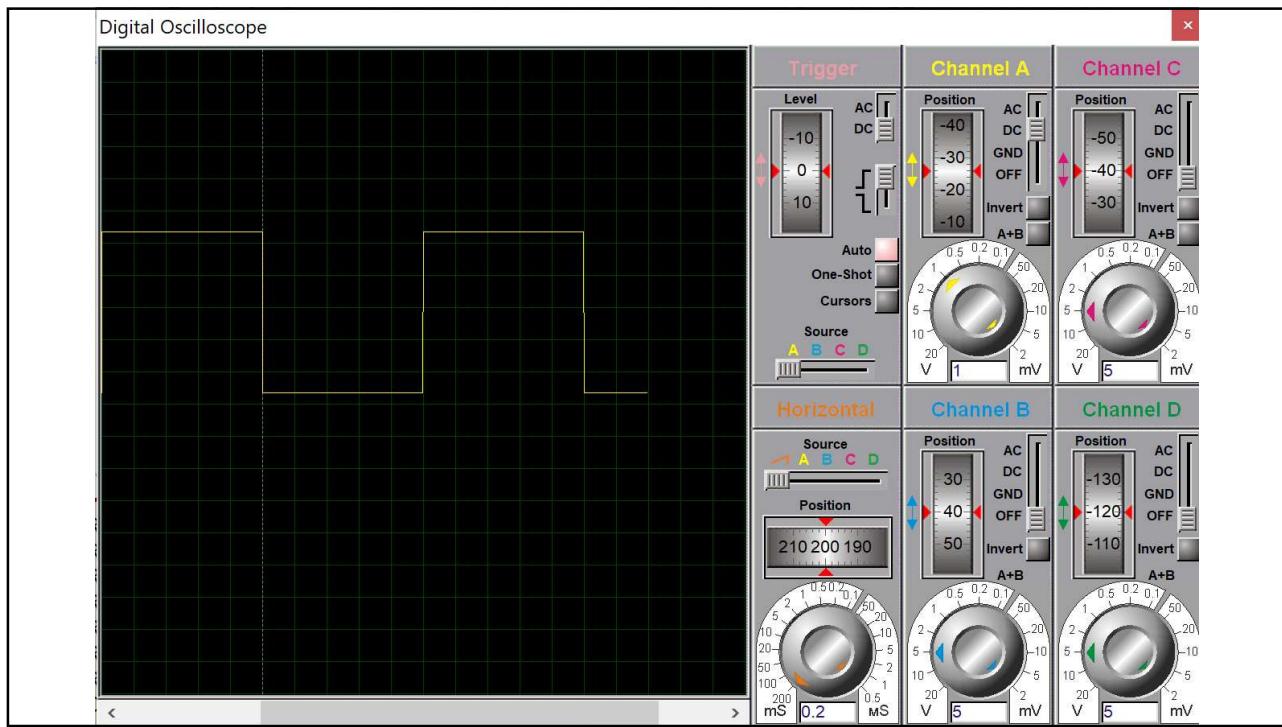
21

Ejemplo 1: Obtener una señal de reloj de 1Hz empleando el Timer1 en modo RTC.

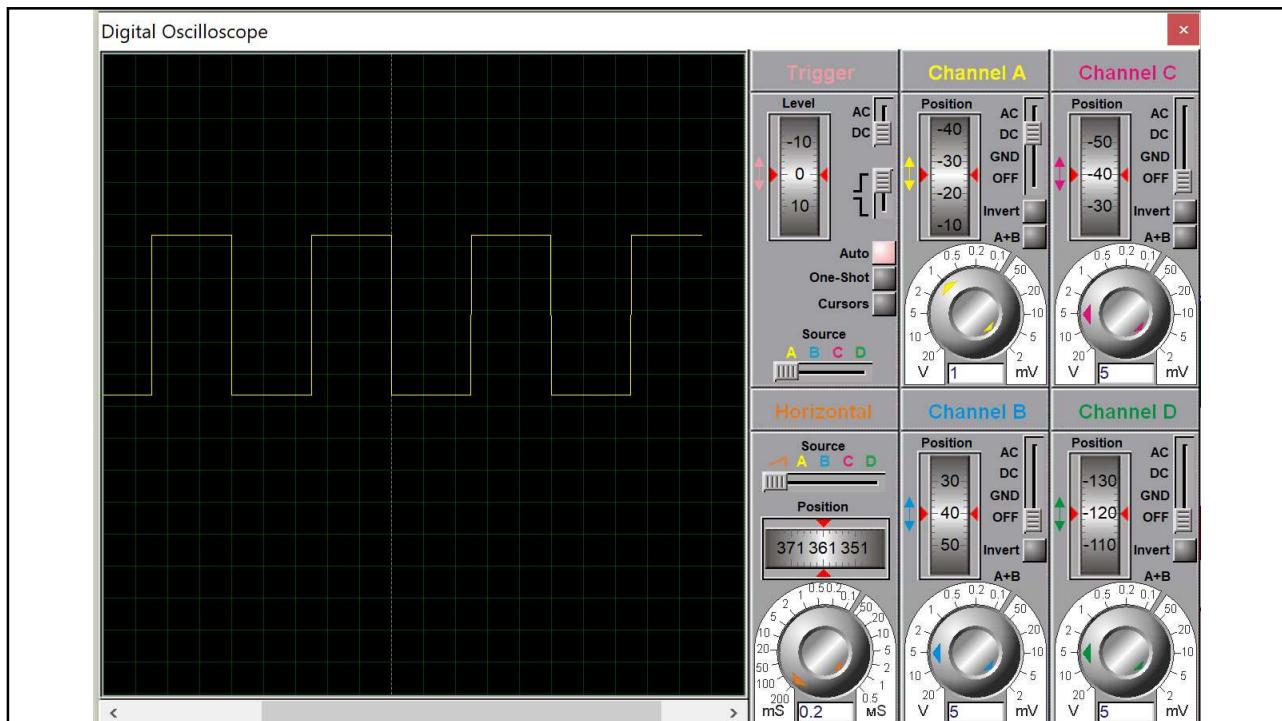
- Simulación



22



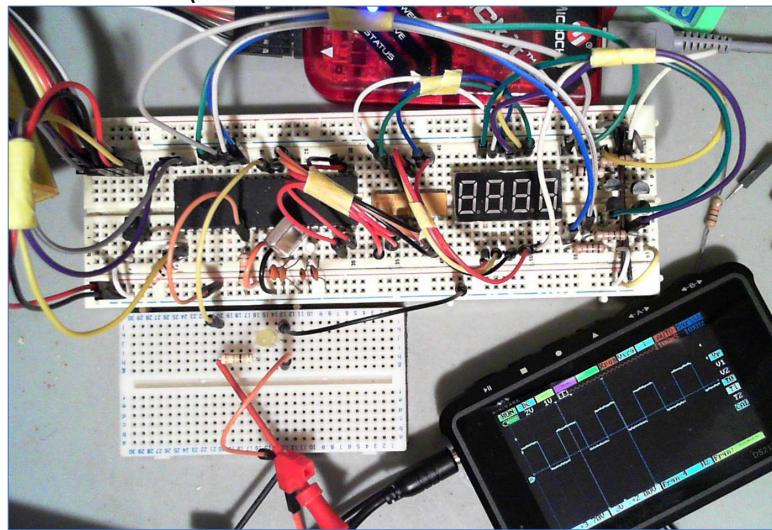
23



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Ejemplo 1: Obtener una señal de reloj de 1Hz empleando el Timer1 en modo RTC.

- Implementación (mostrando señal de 4Hz – cuenta inicial E000H)



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Formato del tiempo:

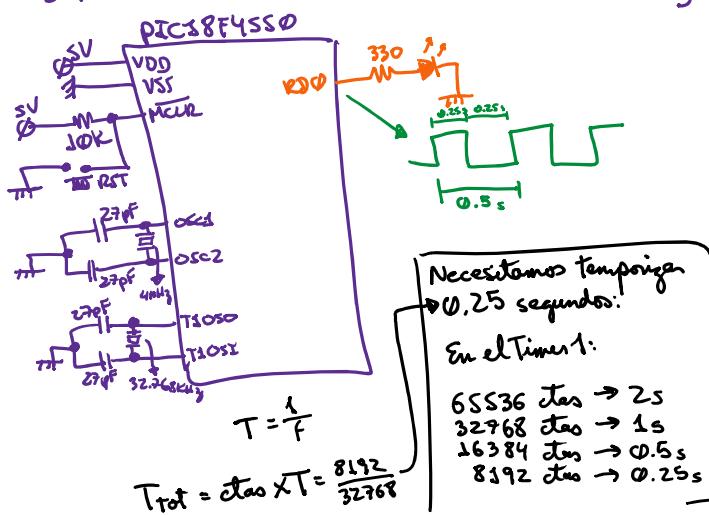
- Horas: 00-23
- Minutos: 00-59
- Segundos: 00-59
- Décimas de Segundo: 0-9
- Centésimas de Segundo: 0-9
- Mílésimas de Segundo: 0-9

milésima
 ↓
 Cronómetro:
 00h 00m 00s 000
 23h 59m 59s 999
 base 24 base 60 ~ decimal
 base 60

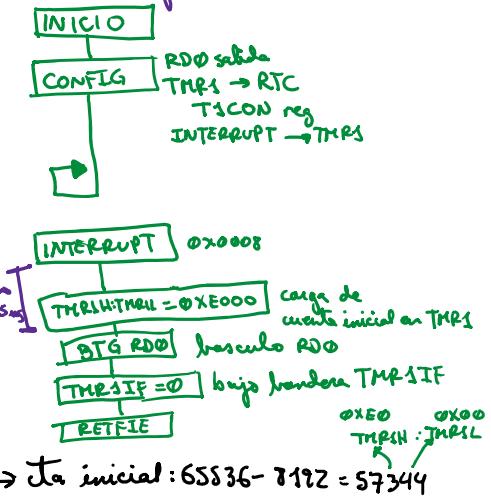
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Ejemplo 2: Desarrollar un titileo de LED con periodo de 0.5s (RTC) empleando TMR1

a) Hardware



b) Diagrama de flujo:



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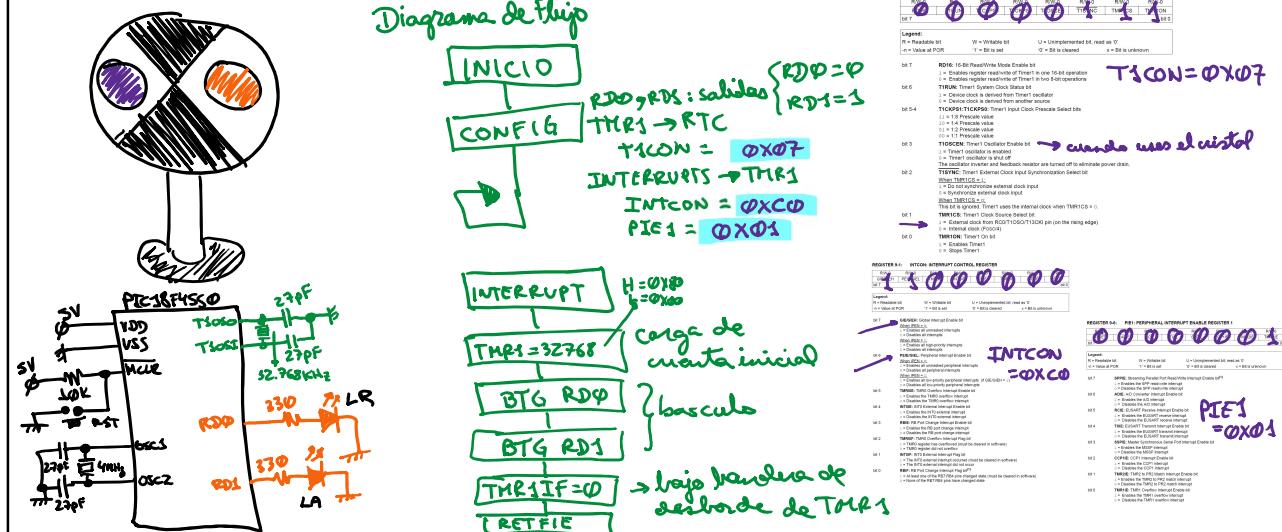
Ejemplo 2: Desarrollar un titileo de LED con periodo de 0.5s (RTC) empleando TMR1

The screenshot shows the MPLAB X IDE interface with several windows open:

- Code Editor:** Displays assembly code for the PIC18F4550 microcontroller. The code includes directives, configuration settings, and a main loop. A red box highlights the TMR1 ISR section.
- Memory Dump:** Shows the memory starting at address 0000. It includes sections for T1CON, TMR1L, TRISD, PORTD, LATD, and WREG registers.
- Logic Analyzer:** A waveform diagram titled "32768Hz" showing digital signals over time. A red box highlights a signal labeled "1".
- Digital Oscilloscope:** A waveform viewer showing a square wave signal. A red box highlights a signal labeled "1".
- Timer Counter:** A digital display showing the value "00000002". Below it are controls for CLK, CE, and RST.

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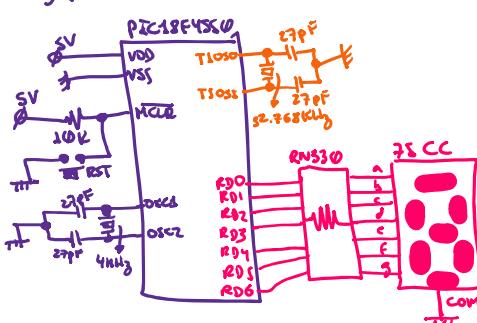
Ejemplo 3: Desarrollar una señal de cruce de tren con periodo de alternancia de 1s (RTC) empleando Timer1



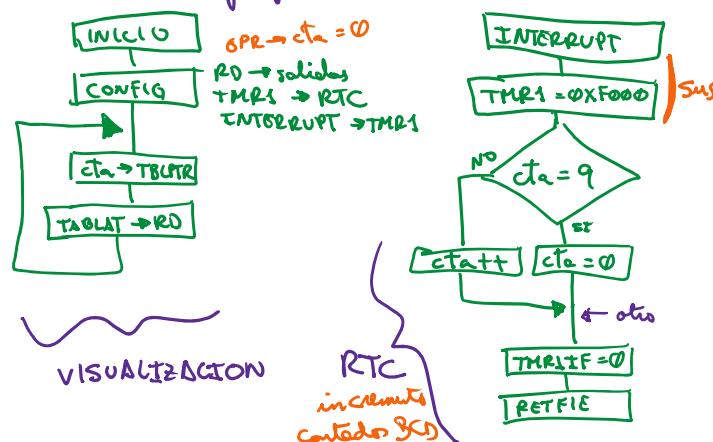
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Ejemplo 4: Desarrollar un contador BCD (0-9) con periodo de cuenta de 0.125segundos (RTC)

a) Hardware:

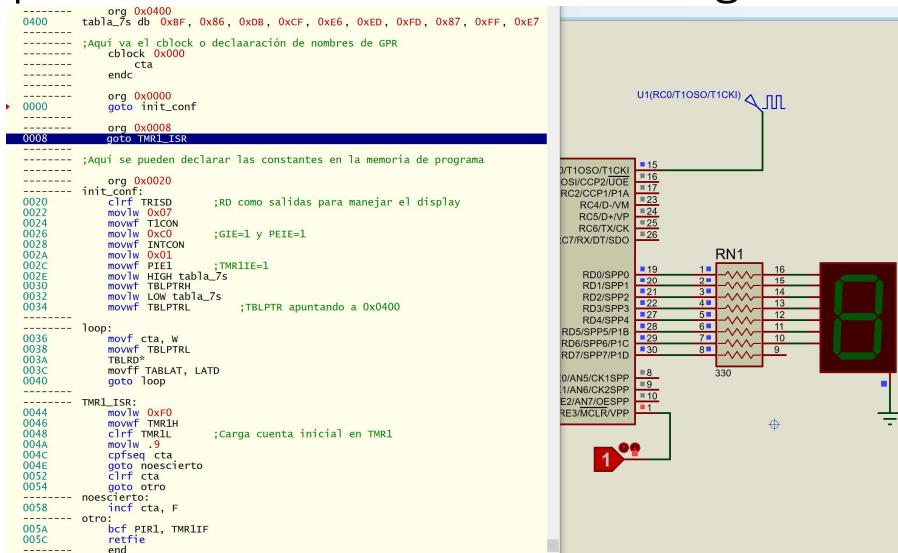


b) Diagrama de flujo:



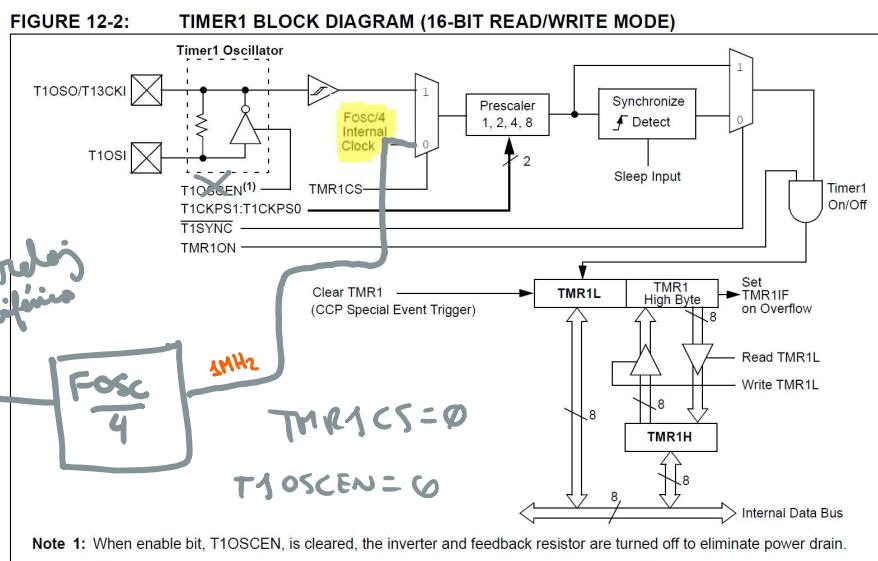
30

Ejemplo 4: Desarrollar un contador BCD (0-9) con periodo de cuenta de 0.125segundos



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Opción 2: Usando fuente de reloj principal del microcontrolador Fosc/4



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Opción 2: Usando fuente de reloj principal del microcontrolador Fosc/4

- Para usarse de manera similar como el Timer0 en modo temporizador
- Es posible hacer RTC pero se deberá usar en conjunto con el CCP1 en modo comparador evento especial de disparo.
- El modo comparador – evento especial de disparo del CCP1 va a permitir reiniciar la cuenta del Timer1 cuando dicha cuenta llegue al mismo valor del registro de CCP1. Por lo que ya no será necesario hacer precarga de cuenta a Timer1. Se usará la interrupción el CCP1 en lugar de la interrupción de Timer1.
- Tener en cuenta que el modulo CCP relacionado con Timer1 es el CCP1, el CCP2 esta relacionado con Timer3

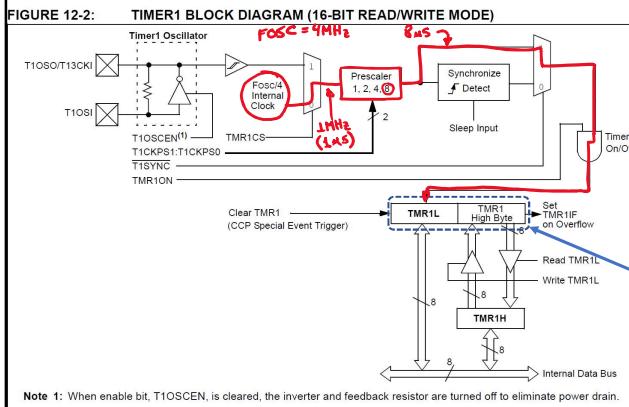
33

Opción 2: Usando fuente de reloj principal del microcontrolador Fosc/4

- Al usar un cristal de 4MHz como oscilador primario, seleccionando Fosc/4 como entrada de reloj y prescaler 1:8 en el Timer1 obtendremos una base de tiempo de 8us por cuenta.
- Establecemos que el número a comparar por el CCP1 sea de 62500, entonces cuando las cuentas del Timer1 llegue a dicho valor habrán pasado exactamente 500000us, el módulo CCP1 al estar configurado en modo comparador evento especial de disparo inmediatamente reiniciará la cuenta del Timer1 en cero y producirá una interrupción (CCP1IF = 1)
- Entonces cada interrupción del CCP1 corresponderá a un lapso de exactamente 0.5s por lo que en el código de la aplicación tendrá que tomarlo en cuenta para llegar a la base de tiempo de 1 segundo.

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Opción 2: Usando fuente de reloj principal del microcontrolador Fosc/4

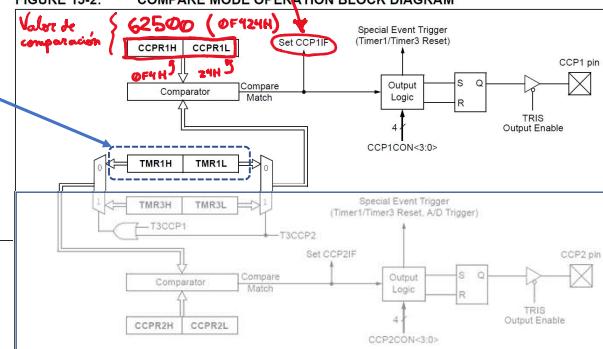


$$62500 \times 8 = 500000 \mu\text{s}$$

\Rightarrow La bandera CCP1IF se levantará cada 0.5s

Cambiará a '1' cuando el registro de cuenta de TMR1 sea igual que valor de comparación en CCP1

FIGURE 15-2: COMPARE MODE OPERATION BLOCK DIAGRAM



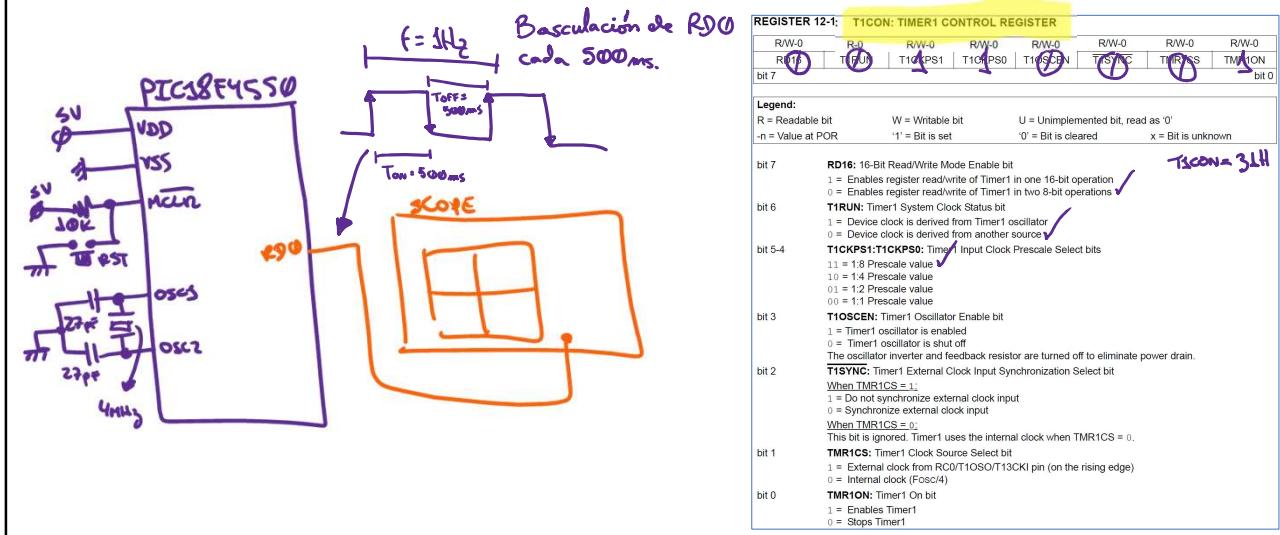
35

Opción 2: Usando fuente de reloj principal del microcontrolador Fosc/4

- Ventajas de usar reloj interno Fosc/4 para RTC:
 - No se requerirá el cristal RTC de 32.768KHz
 - Se puede implementar la porción de fracción del segundo (décimas, centésimas y milésimas).
 - Rutina de interrupción mas sencilla (no es necesario precargar cuenta en TMR1)
- Desventajas:
 - No se podrá emplear SLEEP.
 - CCP1 no se podrá emplear para otra cosa, como por ejemplo generación de PWM.

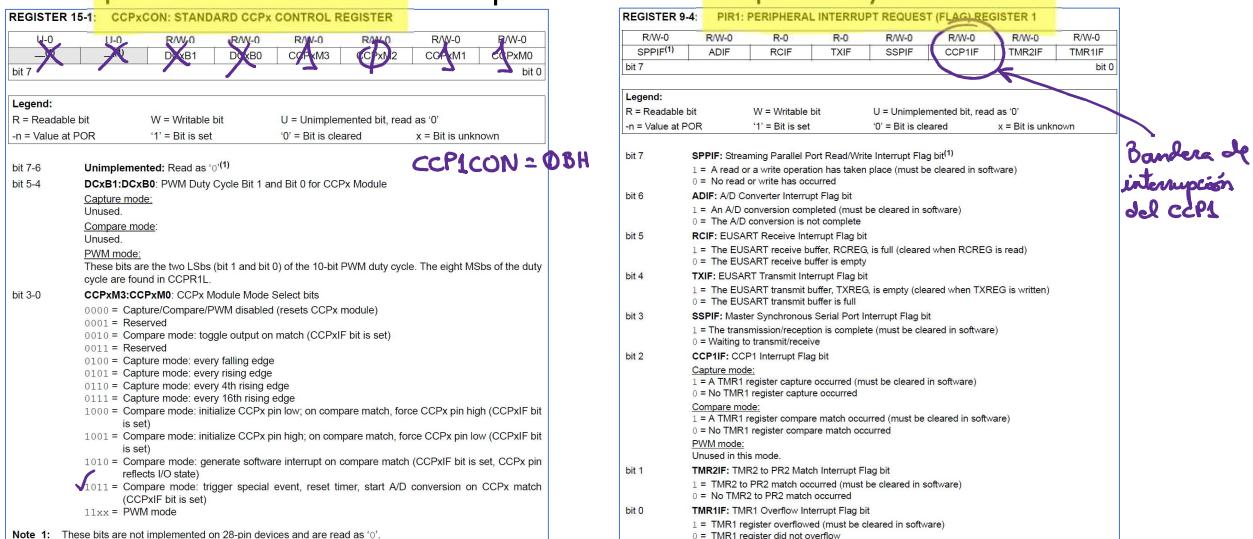
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Ejemplo: Generar una señal cuadrada de 1Hz RTC por RD0 mediante Timer1-CCP1 en configuración comparador evento especial de disparo y Fosc=4MHz



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Ejemplo: Generar una señal cuadrada de 1Hz RTC por RD0 mediante Timer1-CCP1 en configuración comparador evento especial de disparo y Fosc=4MHz



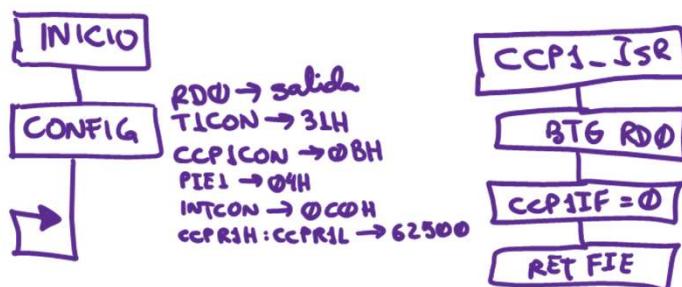
38

Ejemplo: Generar una señal cuadrada de 1Hz RTC por RD0 mediante Timer1-CCP1 en configuración comparador evento especial de disparo y Fosc=4MHz

| REGISTER 9-6 PIE1: PERIPHERAL INTERRUPT ENABLE REGISTER 1 | | | | | | | | REGISTER 9-1 INTCON: INTERRUPT CONTROL REGISTER | | | | | | | | |
|--|--|-------|-------|-------|-------|-------|--------|---|---------|--------|--------|--------|--------|--------|-------|--|
| R/W-C | R/W0 | R/W0 | R/W0 | R/W0 | R/W0 | R/W0 | R/W0 | R/W-C | R/W0 | R/W0 | R/W0 | R/W0 | R/W0 | R/W0 | R/W0 | |
| SPIE ⁽¹⁾ | ADIE | RDIE | FXE | TXIE | SSIE | COIE | TMR1IE | GIE ⁽¹⁾ | PEIEIEL | TMR0IE | INT0IE | TMROIE | INT0IF | TMROIF | RBIF | |
| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | |
| Legend: R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown | Legend: R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown | | | | | | | bit 7 GIE/GIEH: Global Interrupt Enable bit When PEIE = 0: 1 = Enables all unmasked interrupts 0 = Disables all interrupts When PEIE = 1: 1 = Enables all high-priority interrupts 0 = Disables all interrupts bit 6 PEIEIEL: Peripheral Interrupt Enable bit When INTCON = 0: 1 = Enables all unmasked peripheral interrupts 0 = Disables all peripheral interrupts When INTCON = 1: 1 = Enables all low-priority peripheral interrupts (if GIE/GIEH = 1) 0 = Disables all low-priority peripheral interrupts bit 5 TMR0IE: TMRO Overflow Interrupt Enable bit 1 = Enables the TMRO overflow interrupt 0 = Disables the TMRO overflow interrupt bit 4 INT0IE: INT0 External Interrupt Enable bit 1 = Enables the INT0 external interrupt 0 = Disables the INT0 external interrupt bit 3 RBIE: RB Port Change Interrupt Enable bit 1 = Enables the RB port change interrupt 0 = Disables the RB port change interrupt bit 2 TMR0IF: TMRO Overflow Interrupt Flag bit 1 = TMRO register has overflowed (must be cleared in software) 0 = TMRO register did not overflow bit 1 INT0IF: INT0 External Interrupt Flag bit 1 = The INT0 external interrupt occurred (must be cleared in software) 0 = The INT0 external interrupt did not occur bit 0 RBIF: RB Port Change Interrupt Flag bit ⁽¹⁾ 1 = At least one of the RB7-RB4 pins changed state (must be cleared in software) 0 = None of the RB7-RB4 pins have changed state | | | | | | | | |
| PIE1 = 04H | | | | | | | | INTCON = 0C0H | | | | | | | | |

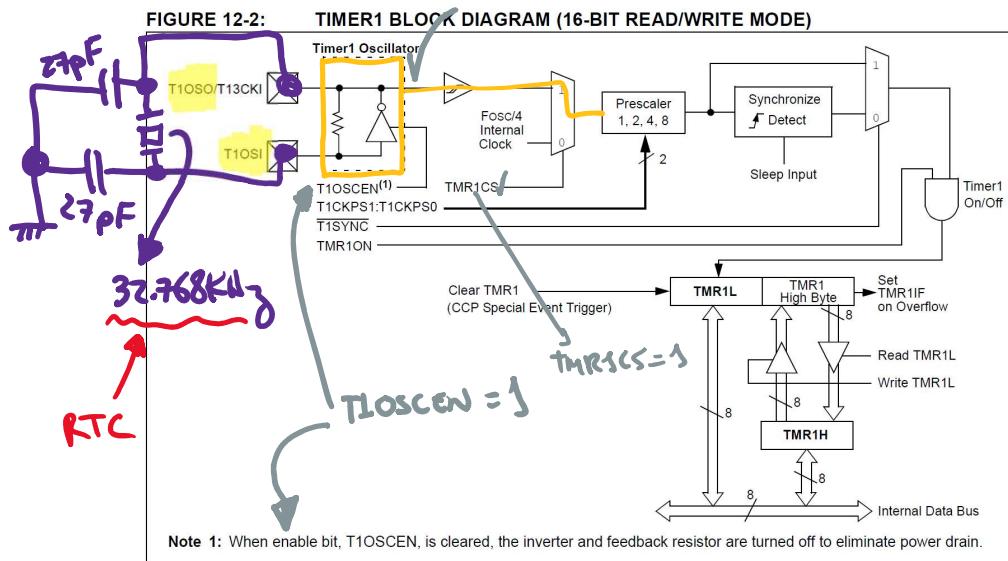
39

Ejemplo: Generar una señal cuadrada de 1Hz RTC por RD0 mediante Timer1-CCP1 en configuración comparador evento especial de disparo y Fosc=4MHz



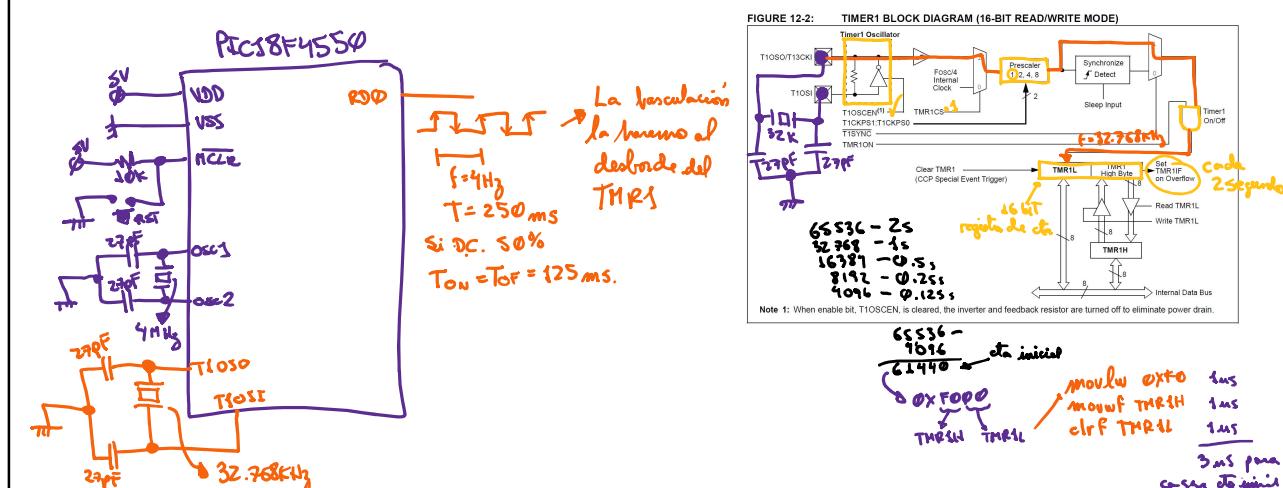
40

Opción 3: Empleando cristal de cuarzo de 32.768KHz



41

Ejemplo 5: El Timer 1 configurado como RTC y empleando el cristal 32K para generar una señal cuadrada de 4Hz a través de RDO



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(cont...)

- Configuración del Timer1

| REGISTER 12-1: T1CON: TIMER1 CONTROL REGISTER | | | | | | | | | | | | | |
|---|--|------------------------------------|---------|---------|--------|---------|--------|--|--|--|--|--|--|
| R/W-0 | R-0 | RW-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | | | | | | |
| R16 | T1RUN | T1CKPS1 | T1CKPS0 | T1OSCEN | T1SYNC | TMRC1CS | TMR1ON | | | | | | |
| bit 7 | | | | | | | | | | | | | |
| Legend: | | | | | | | | | | | | | |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | | | | | | | | | | | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | | | | | | | | | | | |
| | | | | | | | | | | | | | |
| bit 7 | RD16: 16-Bit Read/Write Mode Enable bit | | | | | | | | | | | | |
| | 1 = Enables register read/write of Timer1 in one 16-bit operation | ✓ T1CON = C0X0 | | | | | | | | | | | |
| | 0 = Enables register read/write of Timer1 in two 8-bit operations | | | | | | | | | | | | |
| bit 6 | T1RUN: Timer1 System Clock Status bit | | | | | | | | | | | | |
| | 1 = Device clock is derived from Timer1 oscillator | | | | | | | | | | | | |
| | 0 = Device clock is derived from another source | | | | | | | | | | | | |
| bit 5-4 | T1CKPS1:T1CKPS0: Timer1 Input Clock Prescale Select bits | | | | | | | | | | | | |
| | 11 = 1:8 Prescale value | | | | | | | | | | | | |
| | 10 = 1:4 Prescale value | | | | | | | | | | | | |
| | 01 = 1:2 Prescale value | | | | | | | | | | | | |
| | 00 = 1:1 Prescale value | | | | | | | | | | | | |
| bit 3 | T1OSCEN: Timer1 Oscillator Enable bit | | | | | | | | | | | | |
| | 1 = Timer1 oscillator is enabled | ✓ | | | | | | | | | | | |
| | 0 = Timer1 oscillator is shut off | | | | | | | | | | | | |
| | The oscillator inverter and feedback resistor are turned off to eliminate power drain. | | | | | | | | | | | | |
| bit 2 | T1SYNC: Timer1 External Clock Input Synchronization Select bit | | | | | | | | | | | | |
| | When TMR1CS = 1 : | | | | | | | | | | | | |
| | 1 = Do not synchronize external clock input | ✓ | | | | | | | | | | | |
| | 0 = Synchronize external clock input | | | | | | | | | | | | |
| | When TMR1CS = 0 : | | | | | | | | | | | | |
| | This bit is ignored. Timer1 uses the internal clock when TMR1CS = 0. | | | | | | | | | | | | |
| bit 1 | TMRC1S: Timer1 Clock Source Select bit | | | | | | | | | | | | |
| | 1 = External clock from RC0/T1OSO/T13CK1 pin (on the rising edge) | ✓ | | | | | | | | | | | |
| | 0 = Internal clock (Fosc/4) | | | | | | | | | | | | |
| bit 0 | TMR1ON: Timer1 On bit | | | | | | | | | | | | |
| | 1 = Enables Timer1 | ✓ | | | | | | | | | | | |
| | 0 = Stops Timer1 | | | | | | | | | | | | |

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(cont...)

- Configuración de las interrupciones con el Timer1

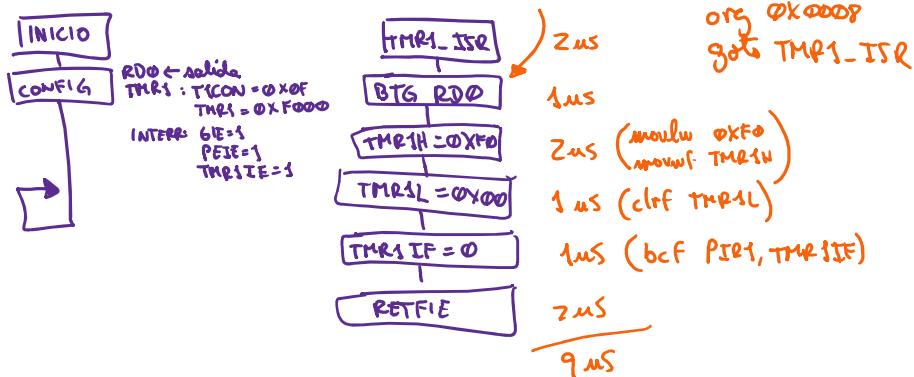
| REGISTER 9-4: | PIR1: PERIPHERAL INTERRUPT REQUEST (FLAG) REGISTER 1 |
|--|--|
| R/W=0 | R/W=0 |
| SPPIF ⁽¹⁾ bit 7 | R=Readable bit W=Writable bit U = Unimplemented bit, read as '0' T = Bit is set. D = Bit is cleared. X = Bit is unknown. |
| Legend: R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' T = Bit is set. D = Bit is cleared. X = Bit is unknown. | |
| bit 7 | SPPIF: Streaming Parallel Port Read/Write Interrupt Flag bit ⁽¹⁾ 1 = A Read or Write operation has taken place (must be cleared in software) 0 = No Read or write has occurred. |
| bit 6 | ADIF: A/D Converter Interrupt Flag bit 1 = An A/D conversion completed (must be cleared in software) 0 = The A/D conversion is not complete. |
| bit 5 | RCIF: USART1 Receive Complete Flag bit 1 = The USART1 receive buffer, ROREG is full (cleared when RCREG is read) 0 = The USART1 receive buffer is empty |
| bit 4 | TXIF: USART1 Transmit Interrupt Flag bit 1 = The USART1 transmit buffer, TXREG is empty (cleared when TXREG is written) 0 = The USART1 transmit buffer is full |
| bit 3 | SSPIF: Master Synchronous Serial Port Interrupt Flag bit 1 = The transmission/reception is complete (must be cleared in software) 0 = Waiting to transmit/receive. |
| bit 2 | CCP1IF: CCP1 Interrupt Flag bit Config mode: 1 = A TMR1 register capture occurred (must be cleared in software) 0 = No TMR1 register capture occurred Compare mode: 1 = A TMR1 register compare match occurred (must be cleared in software) 0 = No TMR1 register compare match occurred PWM mode: 1 = Used in PWM mode |
| bit 1 | TMR2IF: TMR2 to PR2 Match Interrupt Flag bit 1 = TMR2 to PR2 match occurred (must be cleared in software) 0 = No TMR2 to PR2 match occurred |
| bit 0 | TMR1IF: TMR1 Over/Underflow Interrupt Flag bit 1 = TMR1 overflow/underflow (must be cleared in software) 0 = TMR1 register did not overflow |

| REGISTER 9-6: PIE1: PERIPHERAL INTERRUPT ENABLE REGISTER | | | | | |
|--|--|--|-------|-------|-------|
| | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| SPPIE[1] | ADIE | RCIE | TXIE | SSPIE | 1 |
| bit 7 | | | | | |
| Legend: | | | | | |
| R = Readable bit | W = Writable bit | U = Unimplemented | | | |
| = Value at POR | 1 = Bit is set | 0 = Bit is cleared | | | |
| bit 7 | SPPIE: Synchronous Serial Port Receive Interrupt Enable bit | | | | |
| | 0 = Enables the SPPI receive interrupt | 1 = Disables the SPPI receive interrupt | | | |
| bit 6 | ADIE: A/D Converter Interrupt Enable bit | | | | |
| | 1 = Enables the A/D interrupt | 0 = Disables the A/D interrupt | | | |
| bit 5 | RCIE: USART Receive Interrupt Enable bit | | | | |
| | 1 = Enables the USART receive interrupt | 0 = Disables the USART receive interrupt | | | |
| bit 4 | TXIE: USART Transmit Interrupt Enable bit | | | | |
| | 1 = Enables the USART transmit interrupt | 0 = Disables the USART transmit interrupt | | | |
| bit 3 | SSPIE: Master Synchronous Serial Port Interrupt Enable bit | | | | |
| | 1 = Enables the MSSP interrupt | 0 = Disables the MSSP interrupt | | | |
| bit 2 | CPIE: CCP Interrupt Enable bit | | | | |
| | 1 = Enables the CCP1 interrupt | 0 = Disables the CCP1 interrupt | | | |
| bit 1 | TMR2IE: TMR2 to PR2 Match Interrupt Enable bit | | | | |
| | 1 = Enables the TMR2 to PR2 match interrupt | 0 = Disables the TMR2 to PR2 match interrupt | | | |
| bit 0 | TMR1IE: TMR1 overflow interrupt enable bit | | | | |
| | 1 = Enables the TMR1 overflow interrupt | 0 = Disables the TMR1 overflow interrupt | | | |

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(cont...)

- Algoritmo en diagrama de flujo del ejemplo



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(cont...)

- Código en MPASM

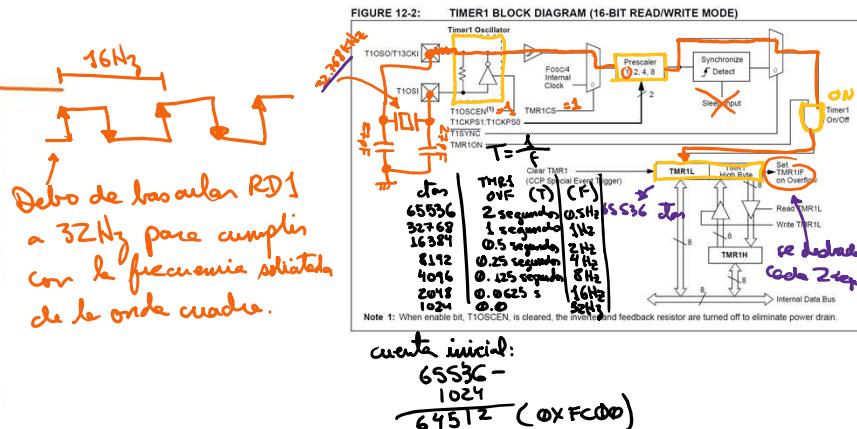
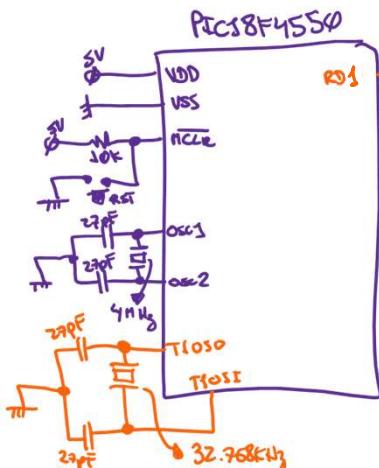
```

17      org 0x0000      ;vector de reset
18      goto init_conf
19
20      org 0x0008      ;vector de interrupcion
21      goto TMRI_ISR
22
23      init_conf: bcf TRISD, 0
24          movlw 0x0F
25          movwf T1CON
26          movlw 0x80
27          movwf TMR1H
28          clrf TMR1L
29          bsf INTCON, GIE
30          bsf INTCON, PEIE
31          bsf PIE1, TMRIIE
32
33      loop:  nop
34          goto loop
35
36      TMRI_ISR:   btg LATD, 0
37          movlw 0x80
38          movwf TMR1H
39          clrf TMR1L
40          bcf PIR1, TMRIIF
41          retfie
42          end

```

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Ejemplo 6: Generar una onda cuadrada de 16Hz exactos a través del puerto RD1 empleando el Timer1 en RTC



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(cont...)

- Configuración del Timer1

| REGISTER 12-1: T1CON: TIMER1 CONTROL REGISTER | | | | | | | |
|---|--|--------|---------|---------|---------|--------|--------|
| R/W | R-0 | R/W-0 | R/M-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| bit 6 | T1RUN | T1CKPS | T1CKPS0 | T1OSCEN | T1OSCNC | TMR1CS | TMR1ON |
| bit 7 | RD16: 16-Bit Read/Write Mode Enable bit 1 = Enables register read/write of Timer1 in one 16-bit operation 0 = Enables register read/write of Timer1 in two 8-bit operations | | | | | | |
| bit 6 | T1RUN: Timer1 System Clock Status bit 1 = Device clock is derived from Timer1 oscillator 0 = Device clock is derived from another source | | | | | | |
| bit 5-4 | T1CKPS1:T1CKPS0: Timer1 Input Clock Prescale Select bits 11 = 1:8 Prescale value 10 = 1:4 Prescale value 01 = 1:2 Prescale value 00 = 1:1 Prescale value | | | | | | |
| bit 3 | T1OSCEN: Timer1 Oscillator Enable bit 1 = Timer1 oscillator is enabled 0 = Timer1 oscillator is shut off The oscillator inverter and feedback resistor are turned off to eliminate power drain. | | | | | | |
| bit 2 | T1SYN: Timer1 External Clock Input Synchronization Select bit When TMR1CS = 1: 1 = Do not synchronize external clock input 0 = Synchronize external clock input When TMR1CS = 0: This bit is ignored. Timer1 uses the internal clock when TMR1CS = 0. | | | | | | |
| bit 1 | TMR1CS: Timer1 Clock Source Select bit 1 = External clock from RC0/T1OSO/T13CKI pin (on the rising edge) 0 = Internal clock (Fosc/4) | | | | | | |
| bit 0 | TMR1ON: Timer1 On bit 1 = Enables Timer1 0 = Stops Timer1 | | | | | | |

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(cont...)

- Configuración de las interrupciones con el Timer1

| REGISTER 9-4: PIR1: PERIPHERAL INTERRUPT REQUEST (FLAG) REGISTER 1 | | | | | | | |
|--|-------|------|-------|-------|--------|--------|--------|
| R/W-0 | R/W-0 | R-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| SPIPIF ⁽¹⁾ | ADIF | RCIF | TXIF | SPIIF | CCP1IF | TMR2IF | TMR1IF |
| bit 7 | | | | | | | bit 0 |

Legend:
R = Readable bit W = Writeable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7: SPIPIF: Streaming Parallel Port Read/Write Interrupt Flag bit⁽¹⁾
1 = A read or a write operation has taken place (must be cleared in software)
0 = No read or write has occurred

bit 6: ADIF: A/D Converter interrupt Flag bit
1 = An A/D conversion completed (must be cleared in software)
0 = No A/D conversion completed

bit 5: CCP1IF: CCP1 Receive Interrupt Flag bit
1 = The USART receive buffer, RCREG, is full (cleared when RCREG is read)
0 = The USART receive buffer is empty

bit 4: TXIF: USART Transmit interrupt Flag bit
1 = The USART transmit buffer, TXREG, is empty (cleared when TXREG is written)
0 = The USART transmit buffer is full

bit 3: SPIIF: Master Synchronous Serial Port interrupt Flag bit
1 = The transmission/reception is complete (must be cleared in software)
0 = Waiting to transmit/receive

bit 2: RCIF: USART receive interrupt Flag bit
Capture mode:
1 = A TMR1 register capture occurred (must be cleared in software)
0 = No TMR1 register capture occurred

Compare mode:
1 = A TMR1 register compare match occurred (must be cleared in software)
0 = No TMR1 register compare match occurred

Overflow mode:
1 = TMR1 register overflowed (must be cleared in software)
0 = TMR1 register did not overflow

bit 1: TMR2IF: TMR2 to PR2 Match interrupt Flag bit
1 = TMR2 to PR2 match occurred (must be cleared in software)
0 = TMR2 to PR2 match did not occur

bit 0: TMR1IF: TMR1 Overflow interrupt Flag bit
1 = TMR1 register overflowed (must be cleared in software)
0 = TMR1 register did not overflow

| REGISTER 9-6: PIE1: PERIPHERAL INTERRUPT ENABLE REGISTER 1 | | | | | | | |
|--|-------|-------|-------|-------|--------|--------|--------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| SPIPEI ⁽¹⁾ | ADIE | RCIE | TXIE | SPIIE | CCPIIE | TMR2IE | TMR1IE |
| bit 7 | | | | | | | bit 0 |

Legend:
R = Readable bit W = Writeable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7: SPIPEI: Streaming Parallel Port Read/Write Interrupt Enable bit⁽¹⁾
1 = Enables the SPIP read/write interrupt
0 = Disables the SPIP read/write interrupt

bit 6: ADIE: A/D Converter Interrupt Enable bit
1 = Enables the A/D converter interrupt
0 = Disables the A/D interrupt

bit 5: TXIE: USART Transmit interrupt Enable bit
1 = Enables the USART transmit interrupt
0 = Disables the USART transmit interrupt

bit 4: CCPIIE: CCP1 Interrupt Enable bit
1 = Enables the CCP1 interrupt
0 = Disables the CCP1 interrupt

bit 3: SPIIE: Master Synchronous Serial Port interrupt Enable bit
1 = Enables the MSSP interrupt
0 = Disables the MSSP interrupt

bit 2: RCIE: USART receive interrupt Enable bit
1 = Enables the USART receive interrupt
0 = Disables the USART receive interrupt

bit 1: TMR2IE: TMR2 to PR2 Match interrupt Enable bit
1 = Enables the TMR2 to PR2 match interrupt
0 = Disables the TMR2 to PR2 match interrupt

bit 0: TMR1IE: TMR1 Overflow interrupt Enable bit
1 = Enables the TMR1 overflow interrupt
0 = Disables the TMR1 overflow interrupt

| REGISTER 9-1: INCON: INTERRUPT CONTROL REGISTER | | | | | | | |
|---|------------|--------|--------|-------|--------|--------|---------------------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-x |
| GIE/GIEH | PEIE/PEIEL | TMR0IE | INT0IE | RBIIE | TMR0IF | INT0IF | RBIF ⁽¹⁾ |
| bit 7 | | | | | | | bit 0 |

Legend:
R = Readable bit W = Writeable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7: GIE/GIEH: Global interrupt enable bit
When IPEN = 0:
1 = Enables all unmasked interrupts
0 = Disables all interrupts

bit 6: PEIE/PEIEL: Peripheral interrupt enable bit
When IPEN = 1:
1 = Enables all unmasked peripheral interrupts
0 = Disables all peripheral interrupts

bit 5: TMR0IE: TMR0 Overflow interrupt enable bit
1 = Enables all low-priority peripheral interrupts (if GIE/GIEH = 1)
0 = Disables all low-priority peripheral interrupts

bit 4: INT0IE: INT0 External interrupt enable bit
1 = Enables the INT0 external interrupt
0 = Disables the INT0 external interrupt

bit 3: RBIIE: RB Port Change interrupt enable bit
1 = Enables the RB port change interrupt
0 = Disables the RB port change interrupt

bit 2: TMR0IF: TMR0 Overflow interrupt flag bit
1 = TMR0 register has overflowed (must be cleared in software)
0 = TMR0 register did not overflow

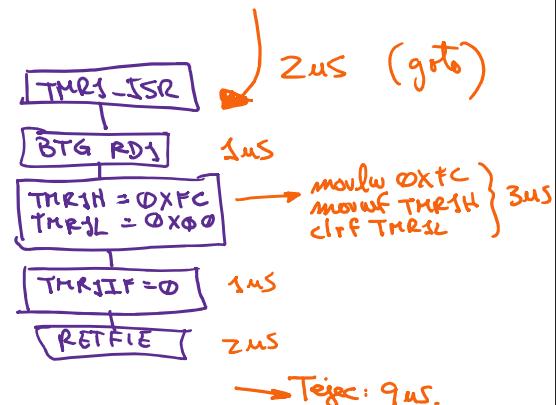
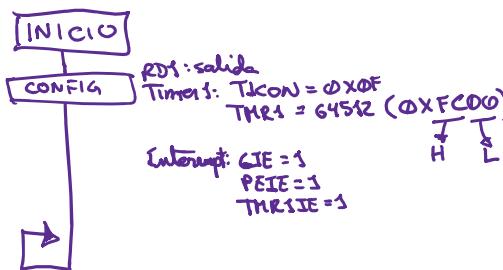
bit 1: INT0IF: INT0 External interrupt flag bit
1 = The INT0 external interrupt occurred (must be cleared in software)
0 = The INT0 external interrupt did not occur

bit 0: RBIF: RB Port Change interrupt flag bit⁽¹⁾
1 = At least one of the RB7/RB4 pins changed state (must be cleared in software)
0 = None of the RB7/RB4 pins have changed state

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(cont...)

- Algoritmo en diagrama de flujo



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(cont...)

- Código en MPASM

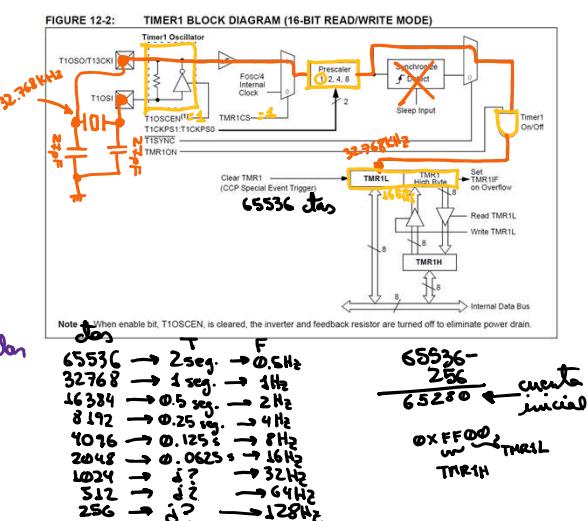
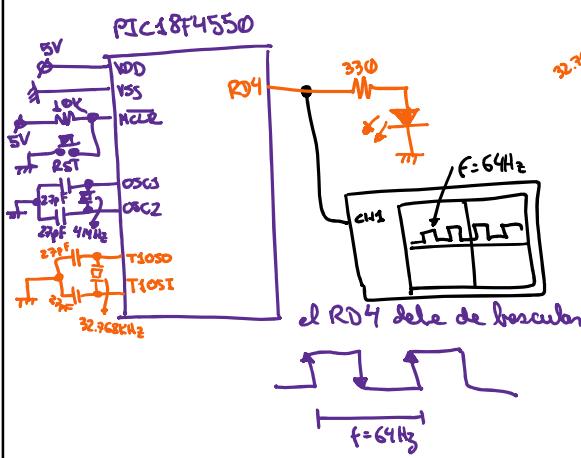
```

1      list p=18f4550      ;Modelo del microcontrolador
2      #include <18f4550.h>          ;Llamada a la librería
3
4
5      ;Directivas de preprocesador o bits de configuración:
6      CONFIG PLLDIV = 1           ; PLL Prescaler
7      CONFIG FCLDIV = OSC1_PLL2   ; System Clock
8      CONFIG FOSC = XT_XT        ; Oscillator
9      CONFIG PWRT = ON           ; Power-up Timer
10     CONFIG BOR = OFF           ; Brown-out Reset
11     CONFIG WDT = OFF           ; Watchdog Timer
12     CONFIG CCP2MX = ON          ; CCP2 MUX bit
13     CONFIG PBADEN = OFF         ; PORTB A/D Enable
14     CONFIG MCLE = ON            ; MCLR Pin Enable
15     CONFIG LVP = OFF            ; Single-Supply
16
17     org 0x0000                ;vector de reset
18     goto init_conf
19
20     org 0x0008                ;vector de interrupción
21     goto TMR1_ISR
22
23 init_conf:
24     bcf TRISD, 1
25     movlw 0x0F
26     movwf TICON
27     movlw 0xFC
28     movwf TMRIH
29     clrf TMRL
30     bsf INTCON, GIE
31     bsf INTCON, PIE
32     bsf PIE1, TMR1IE
33
34 loop:    nop
35     goto loop
36
37 TMR1_ISR:  btg LATD, 1
38     movlw 0x1C
39     movwf TMRIH
40     bcf PIR1, TMR1IF
41     retfie
42     end

```

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Ejemplo 7: Generar una señal cuadrada de 64Hz exactos a través del puerto RD4 y empleando el Timer1 en RTC



(cont...)

• Configuración del Timer1

| REGISTER 12-1: T1CON: TIMER1 CONTROL REGISTER | | | | | | | |
|---|--|---|-------------------------|-------------------------|-------|-------|--------------------|
| R/W-0 | R-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| RD16 | T1RUN | T1CKPS | T1CKPS0 | T1OCEN | T1ONC | TM1CS | TMR1ON |
| bit 7 | | | | | | | bit 0 |
| Legend: | | | | | | | |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | | | | | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | | | | | x = Bit is unknown |
| bit 7 | RD16: 16-Bit Read/Write Mode Enable bit | | | | | | |
| | 1 = Enables register read/write of Timer1 in one 16-bit operation | 0 = Enables register read/write of Timer1 in two 8-bit operations | | | | | |
| bit 6 | T1RUN: Timer1 System Clock Status bit | | | | | | |
| | 1 = Device clock is derived from Timer1 oscillator | 0 = Device clock is derived from another source | | | | | |
| bit 5-4 | T1CKPS1:T1CKPS0: Timer1 Input Clock Prescale Select bits | | | | | | |
| | 11 = 1:8 Prescale value | 10 = 1:4 Prescale value | 01 = 1:2 Prescale value | 00 = 1:1 Prescale value | | | |
| bit 3 | T1OSCEN: Timer1 Oscillator Enable bit | | | | | | |
| | 1 = Timer1 oscillator is enabled | 0 = Timer1 oscillator is shut off | | | | | |
| | The oscillator inverter and feedback resistor are turned off to eliminate power drain. | | | | | | |
| bit 2 | T1SYNC: Timer1 External Clock Input Synchronization Select bit | | | | | | |
| | When TMR1CS = 1: | | | | | | |
| | 1 = Do not synchronize external clock input | 0 = Synchronize external clock input | | | | | |
| | When TMR1CS = 0: | | | | | | |
| | This bit is ignored. Timer1 uses the internal clock when TMR1CS = 0. | | | | | | |
| bit 1 | TMR1CS: Timer1 Clock Source Select bit | | | | | | |
| | 1 = External clock from RC0/T1SO/T1CKI pin (on the rising edge) | 0 = Internal clock (Fosc/4) | | | | | |
| bit 0 | TMR1ON: Timer1 On bit | | | | | | |
| | 1 = Enables Timer1 | 0 = Stops Timer1 | | | | | |

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(cont...)

• Configuración de las interrupciones con el Timer1

| REGISTER 9-4: PIR1: PERIPHERAL INTERRUPT REQUEST (FLAG) REGISTER 1 | | | | | | | |
|--|--|--|-----------------------------------|-------|--------|--------|--------------------|
| R/W-0 | R/W-0 | R-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| SPIPI(R1) | ADIF | RCIF | TXIF | SSPIF | CCP1IF | TMR2IF | TMR1IF |
| bit 7 | | | | | | | bit 0 |
| Legend: | | | | | | | |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | | | | | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | | | | | x = Bit is unknown |
| bit 7 | SPIPI: Streaming Parallel Port Read/Write Interrupt Flag bit ¹ | | | | | | |
| | 1 = A read or a write operation has taken place (must be cleared in software) | 0 = No read or write has occurred | | | | | |
| bit 6 | ADIF: ADC Interrupt Flag bit | | | | | | |
| | 1 = The A/D conversion complete (must be cleared in software) | 0 = The A/D conversion is not complete | | | | | |
| bit 5 | RCIF: USART Receive Interrupt Flag bit | | | | | | |
| | 1 = The USART receive buffer, RCREG, is full (cleared when RCREG is read) | 0 = The USART receive buffer, RCREG, is empty | | | | | |
| bit 4 | TXIF: USART Transmit Interrupt Flag bit | | | | | | |
| | 1 = The USART transmit buffer, TXREG, is empty (cleared when TXREG is written) | 0 = The USART transmit buffer is full | | | | | |
| bit 3 | SSPIF: Master Synchronous Serial Port Interrupt Flag bit | | | | | | |
| | 1 = The master synchronous serial port reception is complete (must be cleared in software) | 0 = Waiting to transmit/receive | | | | | |
| bit 2 | CCP1IF: CCP1 Interrupt Flag bit | | | | | | |
| | Capture mode: 1 = A timer register capture occurred (must be cleared in software) 0 = No timer register capture occurred | Compare mode: 1 = A timer register compare match occurred (must be cleared in software) 0 = No timer register compare match occurred | PWM mode: Unused in this mode. | | | | |
| bit 1 | TMR2IF: TMR2 to PR2 Match Interrupt Flag bit | | | | | | |
| | 1 = TMR2 register match occurred (must be cleared in software) | 0 = No TMR2 to PR2 match occurred | | | | | |
| bit 0 | TMR1IF: TMR1 Overflow Interrupt Flag bit | | | | | | |
| | 1 = TMR1 register overflowed (must be cleared in software) | 0 = TMR1 register did not overflow | | | | | |

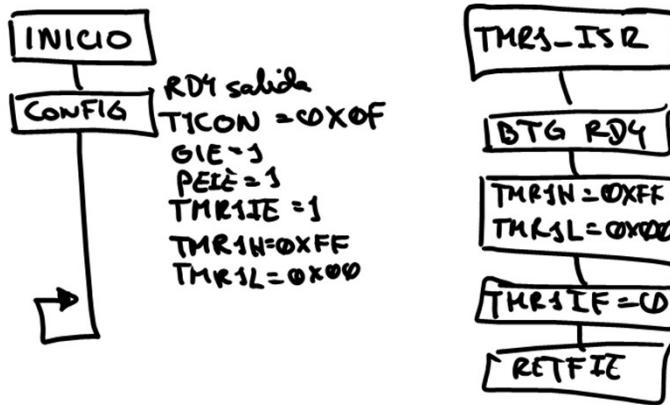
| REGISTER 9-6: PIE1: PERIPHERAL INTERRUPT ENABLE REGISTER 1 | | | | | | | |
|--|---|--|-------|-------|--------|--------|--------------------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| SPIE(R1) | ADIE | RCIE | TXIE | SSPIE | CCP1IE | TMR2IE | TMR1IE |
| bit 7 | | | | | | | bit 0 |
| Legend: | | | | | | | |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | | | | | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | | | | | x = Bit is unknown |
| bit 7 | SPIE: Streaming Parallel Port Read/Write Interrupt Enable bit ¹ | | | | | | |
| | 1 = Enables the SPIP read/write interrupt | 0 = Disables the SPIP read/write interrupt | | | | | |
| bit 6 | ADIE: A/D Converter Interrupt Enable bit | | | | | | |
| | 1 = Enables the A/D interrupt | 0 = Disables the A/D interrupt | | | | | |
| bit 5 | RCIE: USART Receive Interrupt Enable bit | | | | | | |
| | 1 = Enables the USART receive interrupt | 0 = Disables the USART receive interrupt | | | | | |
| bit 4 | TXIE: USART Transmit Interrupt Enable bit | | | | | | |
| | 1 = Enables the USART transmit interrupt | 0 = Disables the USART transmit interrupt | | | | | |
| bit 3 | SPIE: Master Synchronous Serial Port Interrupt Enable bit | | | | | | |
| | 1 = Enables the MSSP interrupt | 0 = Disables the MSSP interrupt | | | | | |
| bit 2 | CCP1IE: CCP1 Interrupt Enable bit | | | | | | |
| | 1 = Enables the CCP1 interrupt | 0 = Disables the CCP1 interrupt | | | | | |
| bit 1 | TMR2IE: TMR2 to PR2 Match Interrupt Enable bit | | | | | | |
| | 1 = Enables the TMR2 to PR2 match interrupt | 0 = Disables the TMR2 to PR2 match interrupt | | | | | |
| bit 0 | TMR1IE: TMR1 Overflow Interrupt Enable bit | | | | | | |
| | 1 = Enables the TMR1 overflow interrupt | 0 = Disables the TMR1 overflow interrupt | | | | | |

| REGISTER 9-1: INTC1: INTERRUPT CONTROL REGISTER | | | | | | | |
|---|---|------------------------------------|--------|-------|--------|--------|--------------------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| GIE/GIEH | PEIE/PEIEL | TMR0IE | INT0IE | RBIE | TMR0IF | INT0IF | RBFI |
| bit 7 | | | | | | | bit 0 |
| Legend: | | | | | | | |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | | | | | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | | | | | x = Bit is unknown |
| bit 7 | GIE/GIEH: Global Interrupt Enable bit When IPEN = 0: 1 = Enables all unmasked interrupts 0 = Disables all interrupts | | | | | | |
| | When IPEN = 1: 1 = Enables all high-priority interrupts 0 = Disables all interrupts | | | | | | |
| bit 6 | PEIE/PEIEL: Peripheral Interrupt Enable bit When IPEN = 0: 1 = Enables all peripheral interrupts 0 = Disables all peripheral interrupts | | | | | | |
| | When IPEN = 1: 1 = Enables all low-priority peripheral interrupts (if GIE/GIEH = 1) 0 = Disables all low-priority peripheral interrupts | | | | | | |
| bit 5 | TMR0IE: TMR0 Overflow Interrupt Enable bit 1 = Enables the TMR0 overflow interrupt 0 = Disables the TMR0 overflow interrupt | | | | | | |
| bit 4 | INT0IE: INT0 External Interrupt Enable bit 1 = Enables the INT0 external interrupt 0 = Disables the INT0 external interrupt | | | | | | |
| bit 3 | RBIE: RB Change Interrupt Enable bit 1 = Enables the RB change interrupt 0 = Disables the RB port change interrupt | | | | | | |
| bit 2 | TMR0IF: TMR0 Overflow Interrupt Flag bit 1 = TMR0 register has overflowed (must be cleared in software) 0 = TMR0 register did not overflow | | | | | | |
| bit 1 | INT0IF: INT0 External Interrupt Flag bit 1 = The INT0 external interrupt occurred (must be cleared in software) 0 = The INT0 external interrupt did not occur | | | | | | |
| bit 0 | RBIF: RB Port Change Interrupt Flag bit 1 = At least one of the RB7/RB4 pins changed state (must be cleared in software) 0 = None of the RB7/RB4 pins have changed state | | | | | | |

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(cont...)

- Algoritmo en diagrama de flujo



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(cont...)

- Código en MPASM

```

;Este es un comentario, se le antecede un punto y coma
list p=18f4550           ;Modelo del microcontrolador
#include <p18f4550.inc>      ;Llamada a la librería de nombre de los registros

;Directivas de preprocesador o bits de configuración
CONFIG PLLDIV = 1          ; PLL Prescaler Selection bits (N prescale (4
CONFIG CPUDIV = OSC1_PLL2  ; System Clock Postscaler Selection bits (1(Prim
CONFIG FOSC = XT_XT       ; Oscillator Selection bits (XT oscillator (XT)
CONFIG PWRT = ON            ; Power-up Timer Enable bit (PWRT enabled)
CONFIG BOR = OFF           ; Brown-out Reset Enable bits (Brown-out Reset
CONFIG WDT = OFF            ; Watchdog Timer Enable bit (WDT disabled (cont
CONFIG CCP2MX = ON          ; CCP2 MUX bit (CCP2 input/output is multiplexe
CONFIG PBADEN = OFF         ; PORTB A/D Enable bit (PORTB<4:0> pins are con
CONFIG MCLE = ON            ; MCLR Pin Enable bit (MCLR pin enabled: RE3 in
CONFIG LVP = OFF             ; Single-Supply ICSP Enable bit (Single-Supply

org 0x0000      ;vector de reset
goto init_conf

org 0x0008      ;vector de interrupcion
goto TMRI_ISR

org 0x0020      ;zona de programa de usuario

init_conf: bcf TRISD, 4      ;RD4 como salida
           movlw 0x0F
           movwf TICON           ;Timer1 on, psc 1:1, cristal 3K habilitado, asyn
           ;bcl TICON, TIOSCEN ;Si es qué vas a usar el Proteus
           bcf PIE1, TMRIIE     ;Interrupción de TMRI activada
           bsf INTCON, PEIE      ;Habilitador de int de perifericos activo
           bsf INTCON, GIE       ;interruptor global de interrupciones activado
           setf TMRIH
           clrf TMRIL           ;Cuenta inicial en TMRI
loop:         goto loop

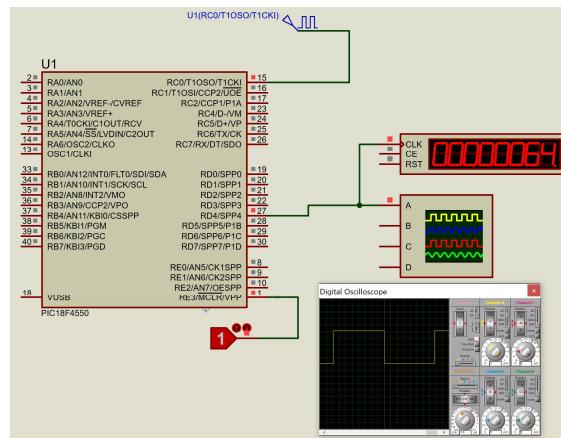
TMRI_ISR:   btg LATD, 4      ;basculo RD4
           setf TMRIH
           clrf TMRIL           ;Cuenta inicial en TMRI
           bcf PIE1, TMRIIF     ;Bajamos la bandera de desborde del TMRI
           retfie
end

```

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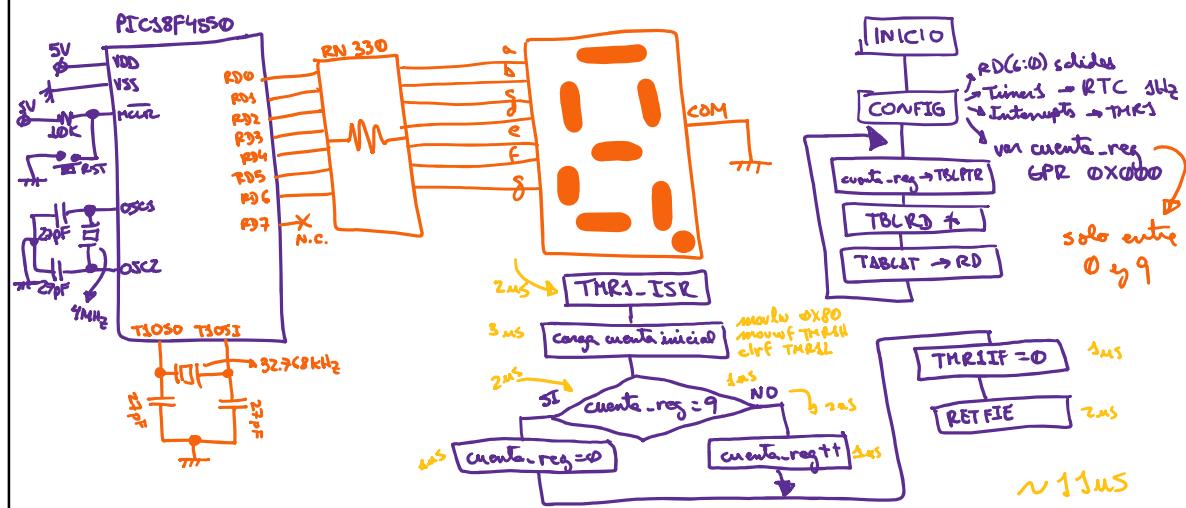
(cont...)

- Simulación en Proteus ($T1OSCEN = 0$)



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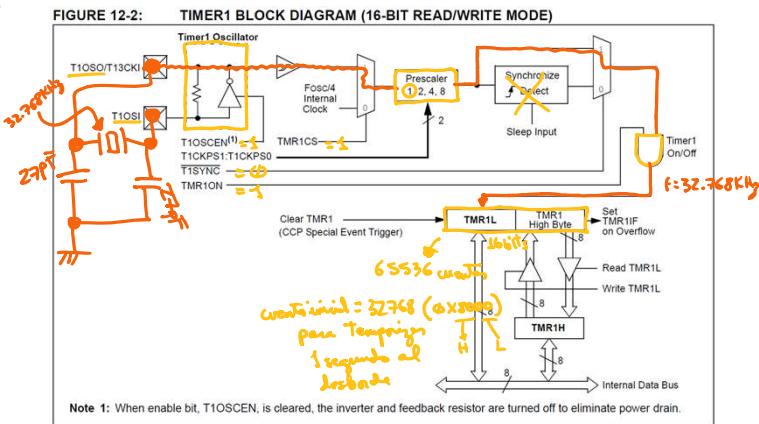
Ejemplo 8: Realizar una cuenta automática 0-9 con un display de siete segmentos cátodo común donde el periodo de cuenta sea de 1Hz dado por el Timer1 en RTC con cristal de 32.768KHz



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(cont...)

- Configuración del Timer1 para RTC 1Hz con cristal 32.768KHz



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(cont...)

- Configuración del Timer1

| REGISTER 12-1: T1CON: TIMER1 CONTROL REGISTER | | | | | | | |
|---|--|--------|---------|---------|---------|--------|--------|
| R/W-0 | R-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| bit 6 | T1RUN | T1CKPS | T1CKPS0 | T1OSCEN | T1OSCNC | TMR1CS | TMR1ON |
| Legend: | | | | | | | |
| R = Readable bit W = Writable bit U = Unimplemented bit, reads as '0' | | | | | | | |
| -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown | | | | | | | |
| bit 7 | RD16: 16-Bit Read/Write Mode Enable bit | | | | | | |
| | 1 = Enables register read/write of Timer1 in one 16-bit operation | | | | | | |
| | 0 = Enables register read/write of Timer1 in two 8-bit operations | | | | | | |
| bit 6 | T1RUN: Timer1 System Clock Status bit | | | | | | |
| | 1 = Device clock is derived from Timer1 oscillator | | | | | | |
| | 0 = Device clock is derived from another source | | | | | | |
| bit 5-4 | T1CKPS1:T1CKPS0: Timer1 Input Clock Prescale Select bits | | | | | | |
| | 11 = 1:8 Prescale value | | | | | | |
| | 10 = 1:4 Prescale value | | | | | | |
| | 01 = 1:2 Prescale value | | | | | | |
| | 00 = 1:1 Prescale value | | | | | | |
| bit 3 | T1OSCEN: Timer1 Oscillator Enable bit | | | | | | |
| | 1 = Timer1 oscillator is enabled | | | | | | |
| | 0 = Timer1 oscillator is shut off | | | | | | |
| | The oscillator inverter and feedback resistor are turned off to eliminate power drain. | | | | | | |
| bit 2 | T1OSCNC: Timer1 External Clock Input Synchronization Select bit | | | | | | |
| | When TMR1CS = 1 | | | | | | |
| | 1 = Do not synchronize external clock input | | | | | | |
| | 0 = Synchronize external clock input | | | | | | |
| | When TMR1CS = 0 | | | | | | |
| | This bit is ignored. Timer1 uses the internal clock when TMR1CS = 0. | | | | | | |
| bit 1 | TMR1CS: Timer1 Clock Source Select bit | | | | | | |
| | 1 = External clock from RC0/T1OSO/T13CKI pin (on the rising edge) | | | | | | |
| | 0 = Internal clock (Fosc/4) | | | | | | |
| bit 0 | TMR1ON: Timer1 On bit | | | | | | |
| | 1 = Enables Timer1 | | | | | | |
| | 0 = Stops Timer1 | | | | | | |

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(cont...)

- Configuración de las interrupciones con el Timer1

| REGISTER 9-4: PIR1: PERIPHERAL INTERRUPT REQUEST (FLAG) REGISTER 1 | | | | | | | |
|--|--|------------------------------------|--------------------|-------|--------|---------|--------|
| R/W-0 | R/W-0 | R-0 | R-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| SPPIR1[7] | ADIF | RCIF | TXIF | SSPIF | CPIIIF | TMRIIF2 | TMRIIF |
| bit 7 | | | | | | | bit 7 |
| Legend: | | | | | | | |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | | | | | |
| = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown | | | | |
| bit 7 | SPPIF: Synchronization Port Post Write Interrupt Flag bit ¹ | | | | | | |
| | 1 = A read or a write operation has taken place (must be cleared in software) | | | | | | |
| | 0 = No read or write has occurred | | | | | | |
| bit 6 | ADIF: A/D Converter Interrupt Flag | | | | | | |
| | 1 = An A/D conversion completed (must be cleared in software) | | | | | | |
| | 0 = No conversion has occurred | | | | | | |
| bit 5 | RCIF: USART Receive Interrupt Flag | | | | | | |
| | 1 = The USART receive buffer, RCREG, is full (cleared when RCREG is read) | | | | | | |
| | 0 = The USART receive buffer is empty | | | | | | |
| bit 4 | TXIF: USART Transmit Interrupt Flag bit | | | | | | |
| | 1 = The USART transmit buffer, TXREG, is empty (cleared when TXREG is written) | | | | | | |
| | 0 = The USART transmit buffer is full | | | | | | |
| bit 3 | SPSIIF: Master Synchronous Serial Port Interrupt Flag bit | | | | | | |
| | 1 = The transmission/reception is complete (must be cleared in software) | | | | | | |
| | 0 = No transmission/reception is in progress | | | | | | |
| bit 2 | CCPHIF: COP1 Interrupt Flag bit | | | | | | |
| | Capture mode | | | | | | |
| | 1 = A TMRI1 register capture occurred (must be cleared in software) | | | | | | |
| | 0 = No TMRI1 register capture occurred | | | | | | |
| | Compare mode | | | | | | |
| | 1 = A TMRI1 register compare match occurred (must be cleared in software) | | | | | | |
| | 0 = No TMRI1 register compare match occurred | | | | | | |
| | PWMIF: PWM1 Interrupt Flag bit | | | | | | |
| | Unused in this mode | | | | | | |
| bit 1 | TMRIIF2: TMRI2 to PR2 Match Interrupt Flag bit | | | | | | |
| | 1 = TMRI2 to PR2 match occurred (must be cleared in software) | | | | | | |
| | 0 = No TMRI2 to PR2 match occurred | | | | | | |
| bit 0 | TMRIIF1: TMRI1 Overflow Interrupt Flag bit | | | | | | |
| | 1 = TMRI1 register overflowed (must be cleared in software) | | | | | | |
| | 0 = TMRI1 register did not overflow | | | | | | |

| REGISTER 9-6: PIE1: PERIPHERAL INTERRUPT ENABLE REGISTER 1 | | | | | | | |
|--|---|-------|-------|------------------------------------|--------|--------|-----------------------------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| SSPIE ⁽¹⁾ | ADIE | RCIE | TXIE | SSPIE | CCP1IE | TMR2IE | TMRIE ⁽¹⁾ bit |
| bit 7 | | | | | | | |
| Legend: | | | | | | | |
| R = Readable bit | W = Writable bit | | | U = Unimplemented bit, read as '0' | | | |
| .n = Value at Power Up | '1' = Bit is set | | | '0' = Bit is cleared | | | x = Bit is unknown |
| bit 7 | SSPIE: Streaming Parallel Port Read/write Interrupt Enable bit ⁽¹⁾ | | | | | | |
| | = Enables the SSPI read/write interrupt | | | | | | |
| | = Disables the SSPI read/write interrupt | | | | | | |
| bit 6 | ADIE: A/D Converter Interrupt Enable bit | | | | | | |
| | = Enables the A/D interrupt | | | | | | |
| | = Disables the A/D interrupt | | | | | | |
| bit 5 | RCIE: USART Receive Interrupt Enable bit | | | | | | |
| | = Enables the USART receive interrupt | | | | | | |
| | = Disables the USART receive interrupt | | | | | | |
| bit 4 | TXIE: USART Transmit Interrupt Enable bit | | | | | | |
| | = Enables the USART transmit interrupt | | | | | | |
| | = Disables the USART transmit interrupt | | | | | | |
| bit 3 | SSPIE: Master Synchronous Serial Port Interrupt Enable bit | | | | | | |
| | = Enables the MSSP interrupt | | | | | | |
| | = Disables the MSSP interrupt | | | | | | |
| bit 2 | CCP1IE: CCP1 Interrupt Enable bit | | | | | | |
| | = Enables the CCP1 interrupt | | | | | | |
| | = Disables the CCP1 interrupt | | | | | | |
| bit 1 | TMR2IE: TMR2 to PR2 Match Interrupt Enable bit | | | | | | |
| | = Enables the TMR2 to PR2 match interrupt | | | | | | |
| | = Disables the TMR2 to PR2 match interrupt | | | | | | |
| bit 0 | TMRIE: TMRI1 Overflow Interrupt Enable bit | | | | | | |
| | = Enables the TMRI1 overflow interrupt | | | | | | |
| | = Disables the TMRI1 overflow interrupt | | | | | | |

| REGISTER 9-1: INTCON: INTERRUPT CONTROL REGISTER | | | | | | | |
|--|--|------------------------------------|--------------------|-------|--------|--------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-x |
| GIE/GIEH | PEIE/GIEL | TMR0IE | INT0IE | RBIE | TMR0IF | INT0IF | RBIF |
| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| Legend: | | | | | | | |
| R = Readable bit | W = Writeable bit | U = Unimplemented bit, read as '0' | | | | | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown | | | | |
| bit 7 | GIE/GIEH: Global Interrupt Enable bit When IPEN = 0: 1 = Enables all unmasked interrupts 0 = Disables all interrupts When IPEN = 1: 1 = Enables all high-priority interrupts 0 = Disables all interrupts | | | | | | |
| bit 6 | PEIE/GIEL: Peripheral Interrupt Enable bit When IPEN = 0: 1 = Enables all unmasked peripheral interrupts 0 = Disables all peripheral interrupts When IPEN = 1: 1 = Enables all low-priority peripheral interrupts (if GIE/GIEH = 1) 0 = Disables all low-priority peripheral interrupts | | | | | | |
| bit 5 | TMR0IE: TMR0 Overflow Interrupt Enable bit 1 = Enables the TMR0 overflow interrupt 0 = Disables the TMR0 overflow interrupt | | | | | | |
| bit 4 | INT0IE: INT0 External Interrupt Enable bit 1 = Enables the INT0 external interrupt 0 = Disables the INT0 external interrupt | | | | | | |
| bit 3 | RBIE: RB Port Change Interrupt Enable bit 1 = Enables the RB port change interrupt 0 = Disables the RB port change interrupt | | | | | | |
| bit 2 | TMR0IF: TMR0 Overflow Interrupt Flag bit 1 = TMR0 register has overflowed (must be cleared in software) 0 = TMR0 register has not overflowed | | | | | | |
| bit 1 | INT0IF: INT0 External Interrupt Flag bit 1 = The INT0 external interrupt occurred (must be cleared in software) 0 = The INT0 external interrupt did not occur | | | | | | |
| bit 0 | RBIF: RB Port Change Interrupt Flag bit 1 = At least one of the RB ports has changed state 0 = None of the RB7/RB4 ports have changed state | | | | | | |

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(cont...)

- Código en MPASM

```

;Este es un comentario, se le antecede un punto y coma
list p=18f4550      ;Modelo del microcontrolador
#include <p18f4550.inc>    ;Llamada a la libreria de los
                           ;Directivas de preprocesador o bits de configuracion
CONFIG PLLDIV = 1          ; PLL Prescaler Selection bits (No pr
CONFIG CPUDIV = OSC1_PLL2   ; System Clock Postscaler Selection b
CONFIG FOSC = XT_XT        ; Oscillator Selection bits (XT oscil
CONFIG PWRT = ON            ; Power-up Timer Enable bit (PWRT ena
CONFIG BOR = OFF           ; Brown-out Reset Enable bits (Brown-
                           ; Watchdog Timer Enable bit (WDT dise
CONFIG CCP2MX = ON          ; CCP2 MUX bit (CCP2 input/output is
CONFIG PBADEN = OFF         ; PORTB A/D Enable bit (PORTB<4:0> pi
CONFIG MCLRE = ON           ; MCLR Pin Enable bit (MCLR pin enab
CONFIG LVP = OFF            ; Single-Supply ICSP Enable bit (Sing

cuenta_reg EQU 0x000
org 0x0500
tabla_7s db 0x3F, 0x06, 0x5B, 0x4F, 0x66, 0x6D, 0x7D, 0x07, 0x7F, 0x67

```

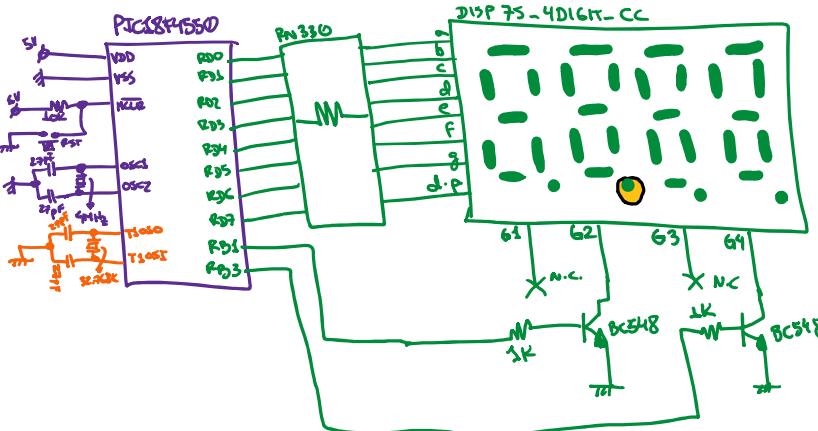
```

22         org 0x0000      ;vector de reset
23         goto init_conf
24
25         org 0x0008      ;vector de interrupcion
26         goto TMRL_ISR
27
28         init_conf: movlw 0x80
29                 movwf TMRSD      ;RD(6:0) como salidas
30                 movlw 0xF
31                 movwf TICON      ;TMRL on, PSC 1:1, tloscen =1, asynd
32                 movlw 0x80
33                 movwf TMRLH
34                 clrf TMRLL      ;carga de cuenta inicial a TMRL
35                 bsf PIEL, TMRLIE   ;interrupcion de TMRL habilitada
36                 bsf INTCON, PEIE    ;interruptor de interrupciones d
37                 bsf INTCON, GIE     ;interruptor global de interrupc
38                 clrf cuenta_reg    ;limpiamos cuenta_reg
39                 movlw 0x05
40                 movwf TBLPTRH
41                 movlw 0x00
42                 movwf TBLPTRL      ;TBLPTR apuntando a 0x0500
43
44         loop:    movff cuenta_reg, TBLPTRL
45                 TBLRD*
46                 movff TABLAT, LATD
47                 goto loop
48
49         TMRL_ISR: movlw 0x80
50                 movwf TMRLH
51                 clrf TMRLL      ;carga de cuenta inicial a TMRL
52                 movlw .9
53                 cpfseg cuenta_reg  ;pregunto si cuenta_reg=9
54                 goto falso
55                 clrf cuenta_reg    ;verdadero, limpia cuenta_reg
56                 goto otro
57         falso:   incf cuenta_reg, f ;falso, incrementa cuenta_reg
58         otro:    bcf PIEL, TMRLIF   ;bajamos bandera TMRLIF
59                 retfie           ;retorno
60                 end

```

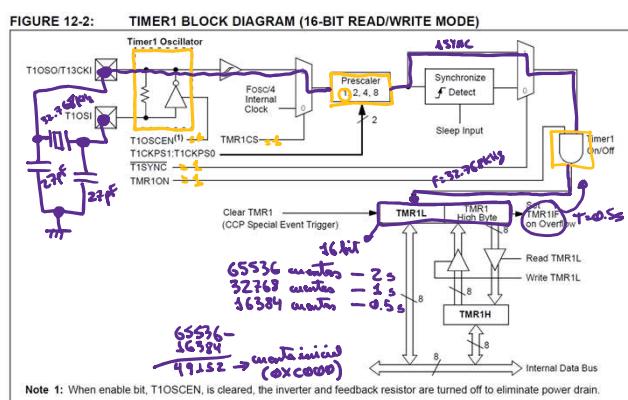
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Ejemplo 9: Desarrollar un basculador de LED con periodo de 0.5s y una cuenta 0-9 con periodo de 1s empleando el Timer1 en RTC



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(cont...)



solo lectura

| REGISTER 12-1: T1CON: TIMER1 CONTROL REGISTER | | | | | | | |
|---|---|--|--|---|---|--|---|
| R/W-0 | R-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| bit 7 | RD16: 16-Bit Read/Write Mode Enable bit 1 = Enables register read/write of Timer1 in one 16-bit operation 0 = Enables register read/write of Timer1 in two 8-bit operations | T1RUN: Timer1 System Clock Status bit 1 = Device clock is derived from Timer1 oscillator 0 = Device clock is derived from another source | T1CKPS1:T1CKPS0: Timer1 Input Clock Prescale Select bits 11 = 1 Prescale value 10 = 1/4 Prescale value 01 = 1/2 Prescale value 00 = 1/1 Prescale value | T1SCEN: Timer1 Oscillator Enable bit 1 = Timer1 oscillator is enabled 0 = Timer1 oscillator is shut off | T1SYNC: Timer1 External Clock Input Synchronization Select bit When TMR1CS = 1: 1 = Do not synchronize external clock input 0 = Synchronize external clock input | T1SC: Timer1 Clock Source Select bit 1 = External clock from RC0/T1OSO/T13CKI pin (on the rising edge) 0 = Internal clock (Fosc/4) | TMR1ON: Timer1 On bit 1 = Enables Timer1 0 = Stops Timer1 |
| <i>bit 0</i> | | | | | | | |
| <i>Legend:</i> R = Readable bit W = Writable bit -n = Value at POR U = Unimplemented bit, read as '0' '1' = Bit is set '0' = Bit is cleared x = Bit is unknown | | | | | | | |
| <i>T1CON = 0XF0F</i> | | | | | | | |

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(cont...)

- Configuración de las interrupciones con el Timer1

REGISTER 9-4: PIR1: PERIPHERAL INTERRUPT REQUEST (FLAG) REGISTER 1

| | | | | | | | | | | | | | | | |
|-------|-------|-----|-------|-------|-------|-------|---------------------|------|------|------|------|--------|--------|--------|------|
| R/W-0 | R/W-0 | R-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | SPIR ⁽¹⁾ | ADIF | RCIF | TXIF | SPIF | CCP1IF | TMR2IF | TMR1IF | b7 D |
| bit 7 | | | | | | | | | | | | | | | |

Legend:
R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
-n = Value at POR
'1' = Bit is set
'0' = Bit is cleared
x = Bit is unknown

REGISTER 9-6: PIE1: PERIPHERAL INTERRUPT ENABLE REGISTER 1

| | | | | | | | | | | | | | | | |
|-------|-------|-------|-------|-------|-------|-------|---------------------|------|------|------|------|--------|--------|--------|------|
| R/W-0 | SPIE ⁽¹⁾ | ADIE | RCIE | TXIE | SPIE | CCP1IE | TMR2IE | TMR1IE | b7 D |
| bit 7 | | | | | | | | | | | | | | | |

Legend:
R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
-n = Value at POR
'1' = Bit is set
'0' = Bit is cleared
x = Bit is unknown

REGISTER 9-1: INCON: INTERRUPT CONTROL REGISTER

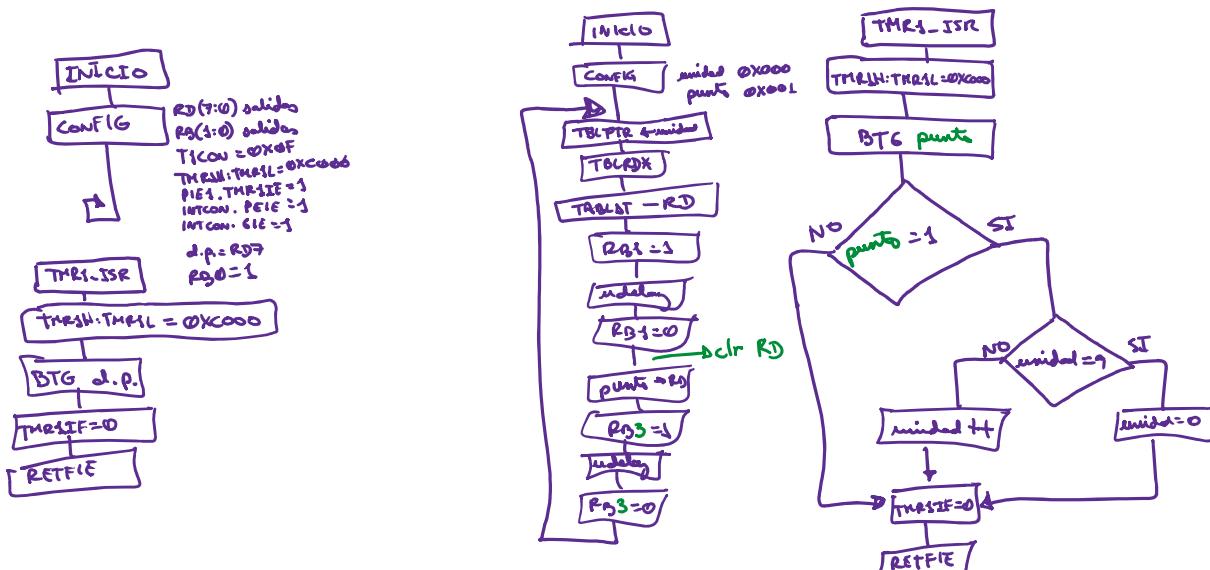
| | | | | | | | | | | | | | | | | |
|-------|-------|-------|-------|-------|-------|-------|-------|----------|-----------|--------|--------|-----|--------|--------|--------------------|------|
| R/W-0 | R/W-x | GIE/GIEH | PIE1/GIEL | TMR0IE | INT0IE | RBE | TMR0IF | INT0IF | RBE ⁽¹⁾ | b7 D |
| bit 7 | | | | | | | | | | | | | | | | |

Legend:
R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
-n = Value at POR
'1' = Bit is set
'0' = Bit is cleared
x = Bit is unknown

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(cont...)

- Algoritmo en diagrama de flujo



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(cont...)

- Código en MPASM

```

2      list p=18f4550      ;Modelo del microcontrolador
3      #include <p18f4550.inc>          ;Llamada a la librería de nombre de los
4
5      ;Directivas de preprocesador o bits de configuración
6      CONFIG PLDIV = 1                ; PLL Prescaler Selection bits (No pr
7      CONFIG CPUDIV = OSC1_PLL2       ; System Clock Postscaler Selection b
8      CONFIG FOSC = XT_XT            ; Oscillator Selection bits (XT oscil
9      CONFIG FWRT = ON               ; Power-up Timer Enable bit (FWRT en
10     CONFIG BOR = OFF              ; Brown-out Reset Enable bits (Brown-
11     CONFIG WDT = OFF              ; Watchdog Timer Enable bit (WDT disa
12     CONFIG CCPMX = ON              ; CCP2 MUX bit (CCP2 input/output is
13     CONFIG PBADEN = OFF           ; PORTB A/D Enable bit (PORTB<4:0> pi
14     CONFIG MCLE = ON              ; MCLR Pin Enable bit (MCLR pin enab
15     CONFIG LVP = OFF              ; Single-Supply ICSP Enable bit (Sing
16
17     cblock 0x000
18     unidad
19     punto
20     endc
21
22     ;Valores de la tabla de búsqueda para el siete segmentos
23     org 0x400
24     tabla_7s db 0x3F, 0x06, 0x5B, 0x4F, 0x66, 0x6D, 0x7D, 0x07, 0x7F, 0x67
25
26     org 0x0000      ;vector de reset
27     goto init_conf
28
29     org 0x0008      ;vector de interrupcion
30     goto TMR1_ISR
31

```

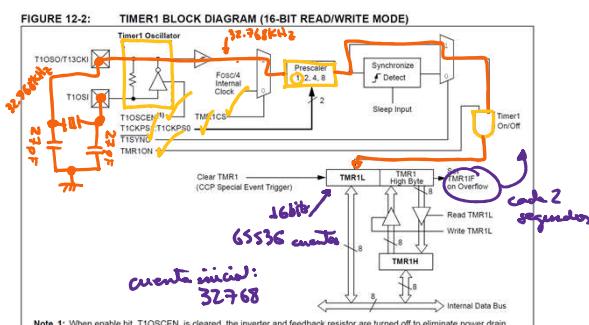
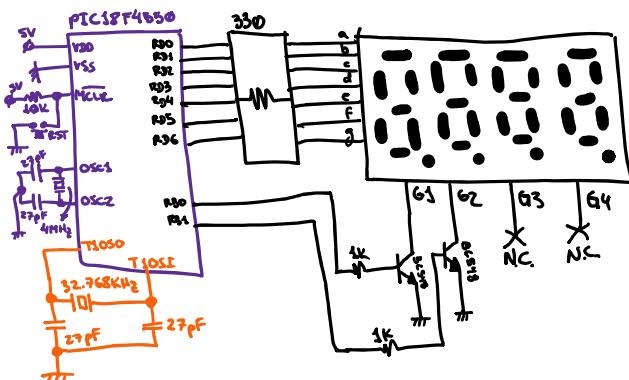
```

32      org 0x0020      ;zona de progr
33      init_conf: clrf TRISD      ;RD con
34      movlw 0xF0
35      movwf TMR1B      ;RB(1)
36      movlw 0x0F
37      movwf TICON      ;config
38      movlw 0x0C
39      movwf TMRIH
40      clrf TMR1L      ;cuent
41      bsf PIE1, TMR1IE    ;i
42      bsf INTCON, PEIE    ;i
43      bsf INTCON, GIE     ;i
44      bcf LATB, 1
45      bcf LATB, 3      ;ai
46      movlw 0x04
47      movwf TBLPTRH
48      clrf TBLPTRL      ;Ti
49      clrf unidad      ;ui
50
51      loop: movff unidad, TBLPTRL
52      TBLRD*
53      movff TABLAT, LATD
54      bsf LATB, 3
55      call udelay
56      bcf LATB, 3
57      clrf LATD
58      btfs punto, 0
59      goto apaga
60      bsf LATD, 7
61      goto otro
62      apaga: bcf LATD, 7
63      otro: bsf LATB, 1
64      call udelay
65      bcf LATB, 1
66      goto loop
67
68      udelay: nop
69      nop
70      nop
71      nop
72      nop
73      nop
74      nop
75      nop
76      nop
77      nop
78      nop
79      return
80
81      TMR1_ISR: movlw 0x0C
82      movwf TMRIH
83      clrf TMR1L
84      btgs punto, 0
85      goto final
86      movlw .9
87      cpfseq unidad
88      goto noescierto
89      clrf unidad
90      goto final
91      noescierto: incf unidad, f
92      final: bcf PIR1, TMR1IF
93      retfie
94      end

```

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Ejemplo 10: Desarrollar un Contador 00-59 con periodo de cuenta 1s exacto empleando el Timer1 en RTC y usando el display de cuatro dígitos de siete segmentos de cátodo común multiplexados



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(cont...)

- Configuración del Timer1

| REGISTER 12-1: T1CON: TIMER1 CONTROL REGISTER | | | | | | | |
|---|--|------------------------------------|--------------------|--------|-------|-------|--------|
| R/W-0 | R-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| RD16 | T1RUN | T1CKPS | T1CKPS0 | T1OCEN | T1ONC | TM1CS | TMR1ON |
| bit 7 | | | | | | | |
| Legend: | | | | | | | |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | | | | | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | | | | | |
| | | | x = Bit is unknown | | | | |
| bit 7 | RD16: 16-Bit Read/Write Mode Enable bit | | | | | | |
| | 1 = Enables register read/write of Timer1 in one 16-bit operation | | | | | | |
| | 0 = Enables register read/write of Timer1 in two 8-bit operations | | | | | | |
| bit 6 | T1RUN: Timer1 System Clock Status bit | | | | | | |
| | 1 = Device clock is derived from Timer1 oscillator | | | | | | |
| | 0 = Device clock is derived from another source | | | | | | |
| bit 5-4 | T1CKPS1:T1CKPS0: Timer1 Input Clock Prescale Select bits | | | | | | |
| | 11 = 1:8 Prescale value | | | | | | |
| | 10 = 1:4 Prescale value | | | | | | |
| | 01 = 1:2 Prescale value | | | | | | |
| | 00 = 1:1 Prescale value ✓ | | | | | | |
| bit 3 | T1OSCEN: Timer1 Oscillator Enable bit | | | | | | |
| | 1 = Timer1 oscillator is enabled | | | | | | |
| | 0 = Timer1 oscillator is shut off | | | | | | |
| | The oscillator inverter and feedback resistor are turned off to eliminate power drain. | | | | | | |
| bit 2 | T1SYNC: Timer1 External Clock Input Synchronization Select bit | | | | | | |
| | When TMR1CS = 1: | | | | | | |
| | 1 = Do not synchronize external clock input ✓ | | | | | | |
| | 0 = Synchronize external clock input ✓ | | | | | | |
| | When TMR1CS = 0: | | | | | | |
| | This bit is ignored. Timer1 uses the internal clock when TMR1CS = 0. | | | | | | |
| bit 1 | TMR1CS: Timer1 Clock Source Select bit | | | | | | |
| | 1 = External clock from RC0/T1SO/T1CKI pin (on the rising edge) ✓ | | | | | | |
| | 0 = Internal clock (Fosc/4) | | | | | | |
| bit 0 | TMR1ON: Timer1 On bit | | | | | | |
| | 1 = Enables Timer1 ✓ | | | | | | |
| | 0 = Stops Timer1 | | | | | | |

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(cont...)

- Configuración de las interrupciones con el Timer1

| REGISTER 9-4: PIR1: PERIPHERAL INTERRUPT REQUEST (FLAG) REGISTER 1 | | | | | | | |
|--|---|------------------------------------|--------------------|-------|--------|--------|--------|
| R/W-0 | R/W-0 | R-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| SPIPI(R1) | ADIF | RCIF | TXIF | SSPIF | CCP1IF | TMR2IF | TMR1IF |
| bit 7 | | | | | | | |
| Legend: | | | | | | | |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | | | | | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown | | | | |
| bit 7 | SPIPI: Streaming Parallel Port Read/Write Interrupt Flag bit ¹ | | | | | | |
| | 1 = A read or a write operation has taken place (must be cleared in software) | | | | | | |
| | 0 = No read or write has occurred | | | | | | |
| bit 6 | ADIF: ADC Interrupt Flag bit | | | | | | |
| | 1 = The A/D conversion complete (must be cleared in software) | | | | | | |
| | 0 = The A/D conversion is not complete | | | | | | |
| bit 5 | RCIF: USART Receive Interrupt Flag bit | | | | | | |
| | 1 = The USART receive buffer, RCREG, is full (cleared when RCREG is read) | | | | | | |
| | 0 = No USART receive interrupt | | | | | | |
| bit 4 | TXIF: USART Transmit Interrupt Flag bit | | | | | | |
| | 1 = The USART transmit buffer, TXREG, is empty (cleared when TXREG is written) | | | | | | |
| | 0 = The USART transmit buffer is full | | | | | | |
| bit 3 | SSPIF: Master Synchronous Serial Port Interrupt Flag bit | | | | | | |
| | 1 = The master synchronous serial port receive complete (must be cleared in software) | | | | | | |
| | 0 = Waiting to transmit/receive ² | | | | | | |
| bit 2 | CCP1IF: CCP1 Interrupt Flag bit | | | | | | |
| | Capture mode: | | | | | | |
| | 1 = A CCP1 register capture occurred (must be cleared in software) | | | | | | |
| | 0 = No CCP1 register capture occurred | | | | | | |
| | Compare mode: | | | | | | |
| | 1 = A CCP1 register compare match occurred (must be cleared in software) | | | | | | |
| | 0 = No CCP1 register compare match occurred | | | | | | |
| | PWM mode: | | | | | | |
| | Unused in this mode. | | | | | | |
| bit 1 | TMR2IF: TMR2 to PR2 Match Interrupt Flag bit | | | | | | |
| | 1 = A TMR2 register PR2 match occurred (must be cleared in software) | | | | | | |
| | 0 = No TMR2 to PR2 match occurred | | | | | | |
| bit 0 | TMR1IF: TMR1 Overflow Interrupt Flag bit | | | | | | |
| | 1 = TMR1 register overflowed (must be cleared in software) | | | | | | |
| | 0 = TMR1 register did not overflow | | | | | | |

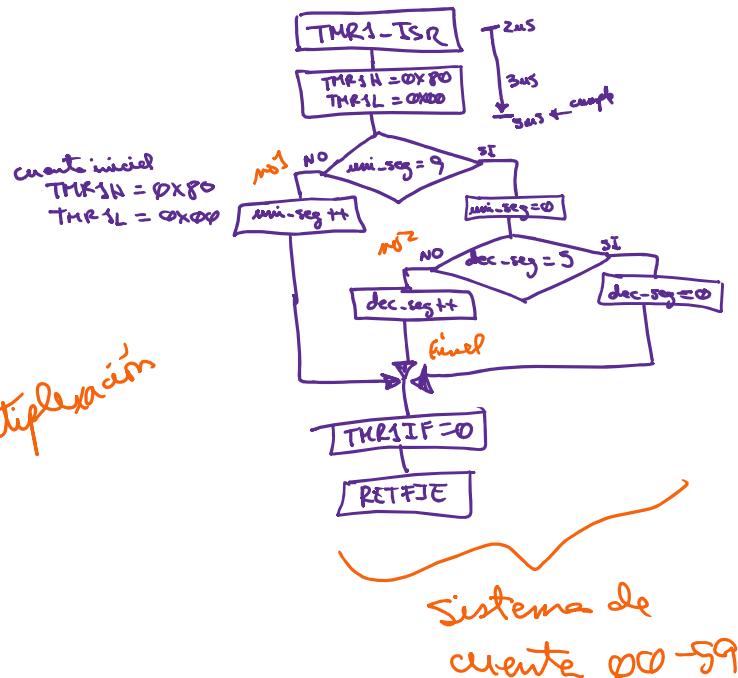
| REGISTER 9-5: PIE1: PERIPHERAL INTERRUPT ENABLE REGISTER 1 | | | | | | | |
|--|--|------------------------------------|--------------------|-------|--------|--------|--------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| SPIPE(R1) | ADIE | RCIE | TXIE | SSPIE | CCP1IE | TMR2IE | TMR1IE |
| bit 7 | | | | | | | |
| Legend: | | | | | | | |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | | | | | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown | | | | |
| bit 7 | SPIPE: Streaming Parallel Port Read/Write Interrupt Enable bit ¹ | | | | | | |
| | 1 = Enables the SPIPE read/write interrupt | | | | | | |
| | 0 = Disables the SPIPE read/write interrupt | | | | | | |
| bit 6 | ADIE: A/D Converter Interrupt Enable bit | | | | | | |
| | 1 = Enables the A/D interrupt | | | | | | |
| | 0 = Disables the A/D interrupt | | | | | | |
| bit 5 | RCIE: USART Receive Interrupt Enable bit | | | | | | |
| | 1 = Enables the USART receive interrupt | | | | | | |
| | 0 = Disables the USART receive interrupt | | | | | | |
| bit 4 | TXIE: USART Transmit Interrupt Enable bit | | | | | | |
| | 1 = Enables the USART transmit interrupt | | | | | | |
| | 0 = Disables the USART transmit interrupt | | | | | | |
| bit 3 | SPIE: Master Synchronous Serial Port Interrupt Enable bit | | | | | | |
| | 1 = Enables the MSSP interrupt | | | | | | |
| | 0 = Disables the MSSP interrupt | | | | | | |
| bit 2 | CCP1IE: CCP1 Interrupt Enable bit | | | | | | |
| | 1 = Enables the CCP1 interrupt | | | | | | |
| | 0 = Disables the CCP1 interrupt | | | | | | |
| bit 1 | TMR2IE: TMR2 to PR2 Match Interrupt Enable bit | | | | | | |
| | 1 = Enables the TMR2 to PR2 match interrupt | | | | | | |
| | 0 = Disables the TMR2 to PR2 match interrupt | | | | | | |
| bit 0 | TMR1IE: TMR1 Overflow Interrupt Enable bit | | | | | | |
| | 1 = Enables the TMR1 overflow interrupt | | | | | | |
| | 0 = Disables the TMR1 overflow interrupt | | | | | | |

| REGISTER 9-6: INCON: INTERRUPT CONTROL REGISTER | | | | | | | |
|---|--|------------------------------------|--------------------|---------------|--------------|-----------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| GIE/GIEH | PEIE/PEIEL | INTOE/INTOIE | RBIE/RBIEH | TMR0IE/TMR0IF | INTOF/INTOIF | RB7/RB7IF | bit 0 |
| bit 7 | | | | | | | |
| Legend: | | | | | | | |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | | | | | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown | | | | |
| bit 7 | GIE/GIEH: Global Interrupt Enable bit | | | | | | |
| | When IPEN = 0: | | | | | | |
| | 1 = Enables all unmasked interrupts | | | | | | |
| | 0 = Disables all interrupts | | | | | | |
| bit 6 | INTOE/INTOIE: INT0 External Interrupt Enable bit | | | | | | |
| | 1 = Enables all high-priority interrupts | | | | | | |
| | 0 = Disables all interrupts | | | | | | |
| bit 6 | PEIE/PEIEL: Peripheral Interrupt Enable bit | | | | | | |
| | 1 = Enables all unmasked peripheral interrupts | | | | | | |
| | 0 = Disables all peripheral interrupts | | | | | | |
| bit 5 | TMR0IE: TMR0 Overflow Interrupt Enable bit | | | | | | |
| | 1 = Enables the TMR0 overflow interrupt | | | | | | |
| | 0 = Disables the TMR0 overflow interrupt | | | | | | |
| bit 4 | INTOE: INTO External Interrupt Enable bit | | | | | | |
| | 1 = Enables the INTO external interrupt | | | | | | |
| | 0 = Disables the INTO external interrupt | | | | | | |
| bit 3 | RBIE: RB Change Interrupt Enable bit | | | | | | |
| | 1 = Enables the RB change interrupt | | | | | | |
| | 0 = Disables the RB port change interrupt | | | | | | |
| bit 2 | TMR0IF: TMR0 Overflow Interrupt Flag bit | | | | | | |
| | 1 = TMR0 register has overflowed (must be cleared in software) | | | | | | |
| | 0 = TMR0 register did not overflow | | | | | | |
| bit 1 | INTOF: INTO External Interrupt Flag bit | | | | | | |
| | 1 = The INTO external interrupt occurred (must be cleared in software) | | | | | | |
| | 0 = The INTO external interrupt did not occur | | | | | | |
| bit 0 | RBIF: RB Port Change Interrupt Flag bit ¹ | | | | | | |
| | 1 = At least one of the RB7/RB4 pins changed state (must be cleared in software) | | | | | | |
| | 0 = None of the RB7/RB4 pins have changed state | | | | | | |

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(cont...)

- Diagrama de flujo



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Ejercicios:

- Desarrollar un cronómetro mm:ss de 00 minutos 00 segundos hasta 59 minutos 59 segundos empleando la configuración de Timer1 visto en esta sesión de clase, la visualización será en cuatro displays de siete segmentos de cátodo común multiplexados, se deberá usar el Timer1 como RTC. Se tendrá dos entradas de interrupción externa: una para el inicio de la cuenta y otra para la parada. Para colocar la cuenta del cronómetro en 00:00 se usará el botón de RESET.

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Fin de la sesión!