

Celdas lógicas configurables (CLC) en el microcontrolador PIC18F57Q43

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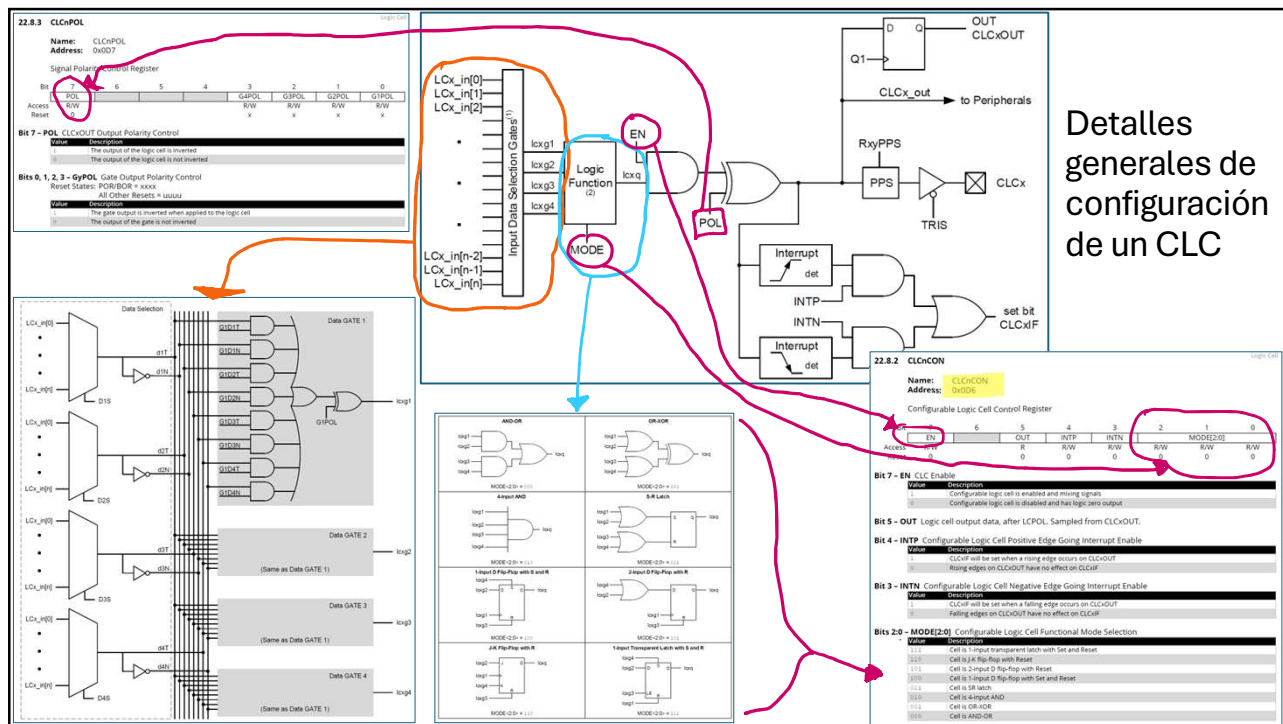
Agenda

- El periférico Celda Lógica Configurable (CLC)
 - Descripción funcional
 - Configuración de entradas
 - Selección de función lógica
 - Gestión de la salida
 - Registros de configuración
 - El PPS para el CLC
- Ejemplo de un contador síncrono de 3 bits

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Las Celdas Lógicas Configurables (CLC)

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- The diagram illustrates the internal logic of the CLCx module. It features an 'Input Data Selection Gates' block with multiple inputs labeled LCx_in[0], LCx_in[1], LCx_in[2], and LCx_in[n-2] through LCx_in[n]. These gates output signals cxg1, cxg2, cxg3, and cxg4 to a 'Logic Function' block. The 'Logic Function' block also receives an 'EN' signal and outputs 'LCxOUT'. A 'MODE' block is connected to the 'Logic Function' and the 'LCxOUT' signal. The 'LCxOUT' signal is then processed by a 'POL' block, which outputs to a 'PPS' block. The 'PPS' block is also influenced by 'RxyPPS' and 'TRIS' signals. The final output is 'CLCxOUT', which is also labeled 'OUT CLCxOUT'. The 'CLCx' signal is derived from the 'PPS' block and is connected to 'Interrupt' blocks, which in turn control the 'set bit CLCxIF'.



CLC: Selección de señales de entrada

- Tener en cuenta el PPS si es que la señal de entrada proviene de pines del microcontrolador.
- Los puertos disponibles para recibir señales son:

Peripheral	PPS Input Register	Default Pin Selection at POR	Register Reset Value at POR	Available Input Port					
				28-Pin Devices		40-Pin Devices		48-Pin Devices	
CLCx Input 1	CLCIN0PPS	RA0	'b000 000	A	—	C	A	—	C
CLCx Input 2	CLCIN1PPS	RA1	'b000 001	A	—	C	A	—	C
CLCx Input 3	CLCIN2PPS	RB6	'b001 110	—	B	C	—	B	D
CLCx Input 4	CLCIN3PPS	RB7	'b001 111	—	B	C	—	B	D
CLCx Input 5	CLCIN4PPS	RA0	'b000 000	A	—	C	A	—	C
CLCx Input 6	CLCIN5PPS	RA1	'b000 001	A	—	C	A	—	C
CLCx Input 7	CLCIN6PPS	RB6	'b001 110	—	B	C	—	B	D
CLCx Input 8	CLCIN7PPS	RB7	'b001 111	—	B	C	—	B	D

Ejemplo: Si necesitamos conectar la entrada RC1 para CLC5:
CLCIN5PPS = 11H (Revisar hoja técnica 21.8.1)

22.8.4 CLCnSELO

Name: CLCnSELO
Address: 0x008

Generic CLCn Data 1 Select Register

Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	x	x	x	x	x	x	x	x

Bits 7:0 - D15[7:0] CLCn Data 1 Input Selection

Table 22-2. CLC Input Selection

DS	DS (cont.)	Input Source (cont.)	DS (cont.)	Input Source (cont.)
[0] 0000 0000	CLCIN0PPS	CCP3	[8] 0100 0000	SP11_SCK
[1] 0000 0001	CLCIN1PPS	CCP3	[9] 0100 0001	SP11_SS
[2] 0000 0010	CLCIN2PPS	PWM1SP1_OUT	[10] 0100 0010	SP12_SCK
[3] 0000 0011	CLCIN3PPS	PWM1SP2_OUT	[11] 0100 0011	SP12_SS
[4] 0000 0100	CLCIN4PPS	PWM2SP1_OUT	[12] 0100 0100	SP12_SCK
[5] 0000 0101	CLCIN5PPS	PWM2SP2_OUT	[13] 0100 0101	SP12_SS
[6] 0000 0110	CLCIN6PPS	PWM3SP1_OUT	[14] 0100 0110	PC_SCL
[7] 0000 0111	CLCIN7PPS	PWM3SP2_OUT	[15] 0100 0111	PC_SDA
[8] 0000 1000	Fosc	—	[16] 0100 1000	CWG1A
[9] 0000 1001	HRINTOSC(1)	—	[17] 0100 1001	CWG1B
[10] 0000 1010	LFINTOSC(1)	NC01	[18] 0100 1010	CWG2A
[11] 0000 1011	MFINTOSC(1)	NC02	[19] 0100 1011	CWG2B
[12] 0000 1100	MFINTOSC(1.25 kHz)(1)	NC03	[20] 0100 1100	CWG3A
[13] 0000 1101	SPINTOSC(1 kHz)(1)	CMP1_OUT	[21] 0100 1101	CWG3B
[14] 0000 1110	SDC0(1)	CMP2_OUT	—	—
[15] 0000 1111	EXOSC0(1)	JC0	—	—
[16] 0001 0000	ADCB0(1)	IOC	—	—
[17] 0001 0001	CLKR	DSM1	—	—
[18] 0001 0010	TMR0	HVD_OUT	—	—
[19] 0001 0011	TMR1	CLC7	—	—
[20] 0001 0100	TMR2	CLC2	—	—
[21] 0001 0101	TMR3	CLC3	—	—
[22] 0001 0110	TMR4	CLC4	—	—
[23] 0001 0111	TMR5	CLC5	—	—
[24] 0001 1000	TMR6	CLC6	—	—
[25] 0001 1001	—	CLC7	—	—
[26] 0001 1010	—	CLC8	—	—
[27] 0001 1011	—	UTX	—	—
[28] 0001 1100	—	UTX	—	—
[29] 0001 1101	—	UTX	—	—
[30] 0001 1110	SM1	UTX	—	—
[31] 0001 1111	CCP1	UTX	[127] 0111 1111	—

Note:
1. Requests clock.
Reset States: POR/BOR = xxxxxxxx
All Other Resets = uuuuuuuu

22.8.5 CLCnSEL1

Name: CLCnSEL1
Address: 0x009

Generic CLCn Data 1 Select Register

Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	x	x	x	x	x	x	x	x

Bits 7:0 - D15[7:0] CLCn Data 2 Input Selection

Reset States: POR/BOR = xxxxxxxx
All Other Resets = uuuuuuuu

Refer to the CLC Input Selection table for input selections.

Refer to the CLC Input Selection table for input selections.

Registros de selección de entrada

22.8.6 CLCnPOL

Name: CLCnPOL
Address: 0x007

Signal Polarity Control Register

Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	x	x	x	x	x	x	x	x

Bits 7:0 - CLCn Data 2 Input Selection

Reset States: POR/BOR = xxx
All Other Resets = uuuuuuuu

The input of the signal is inverted.

The input of the signal is not inverted.

Bits 6, 1, 2, 3 - GATE Output Polarity Control

Reset States: POR/BOR = xxx
All Other Resets = uuuuuuuu

The gate output is inverted when applied to the logic cell.

The gate output is not inverted when applied to the logic cell.

22.8.8 CLCnGSL0

Name: CLCnGSL0
Address: 0x00C

Gate Select Register

Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	x	x	x	x	x	x	x	x

Bits 1, 3, 5, 7 - GATE Data Y (non-inverted)

Reset States: POR/BOR = xxx
All Other Resets = uuuuuuuu

Bits 0, 2, 4, 6 - GATE Data Y (negated/inverted)

Reset States: POR/BOR = xxx
All Other Resets = uuuuuuuu

Bits 0, 2, 4, 6 - GATE Data Y (negated/inverted)

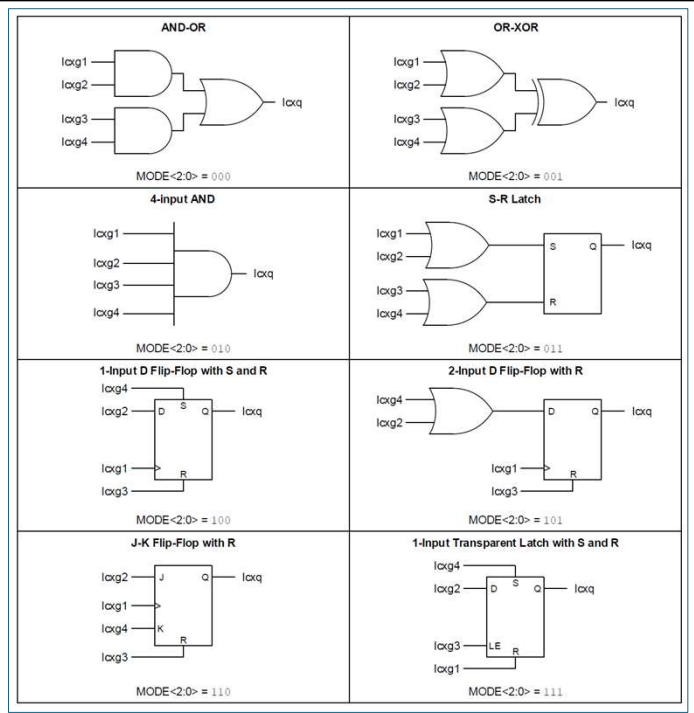
Reset States: POR/BOR = xxx
All Other Resets = uuuuuuuu

Bits 0, 2, 4, 6 - GATE Data Y (negated/inverted)

Reset States: POR/BOR = xxx
All Other Resets = uuuuuuuu

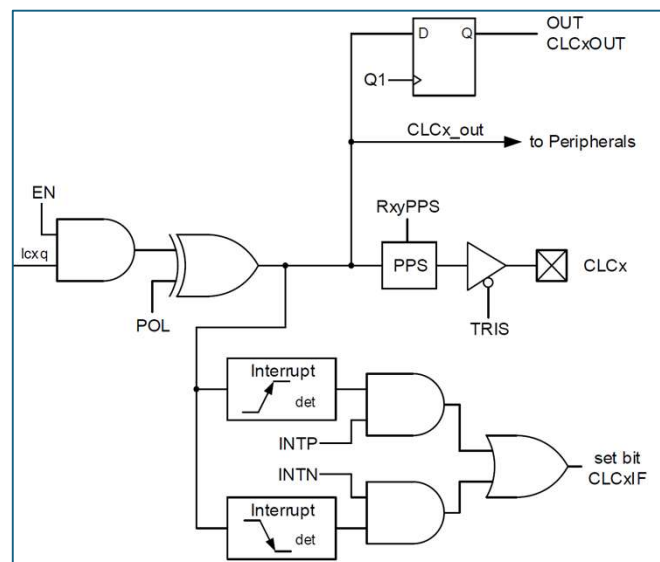
CLC: Selección de función lógica

- Se tienen como opción ocho tipos de función lógica para un CLC.
- Tener en cuenta que las entradas $lcxg1$, $lcxg2$, $lcxg3$ y $lcxg4$ provienen de la etapa de selección de entrada vista anteriormente.
- La señal de salida $lcxq$ esta conectado a la etapa de la gestión de salida del CLC



CLC: Gestión de salida del CLC

- En esta etapa se configura lo siguiente:
 - Habilitador del CLC con EN (registro CLCnCON bit 7)
 - Inversor de la señal de salida con POL (registro CLCnPOL bit 7)
 - Opción para que salga por un pin de E/S configurando el PPS
 - Configuración del flanco para generación de interrupción



CLC: Gestión de salida del CLC

- Hay que tener en cuenta los puertos permitidos por el PPS para el periférico CLC y es que se requiere que la señal salga a un pin del microcontrolador

RxyPPS	Output Source	Available Output Ports											
		28-Pin Devices			40-Pin Devices			48-Pin Devices					
0x08	CLC8OUT	—	B	C	—	B	—	D	—	—	B	—	D
0x07	CLC7OUT	—	B	C	—	B	—	D	—	—	B	—	D
0x06	CLC6OUT	A	—	C	A	—	C	—	—	A	—	—	F
0x05	CLC5OUT	A	—	C	A	—	C	—	—	A	—	—	F
0x04	CLC4OUT	—	B	C	—	B	—	D	—	—	B	—	D
0x03	CLC3OUT	—	B	C	—	B	—	D	—	—	B	—	D
0x02	CLC2OUT	A	—	C	A	—	C	—	—	A	—	—	F
0x01	CLC1OUT	A	—	C	A	—	C	—	—	A	—	—	F

Ejemplo: Si necesitamos conectar la salida de CLC3 hacia RD5:
RD5PPS = 03H

CLC: Resumen de registros implicados

22.9 Register Summary - CLC Control

Logic Cell

Address	Name	Bit Pos.	7	6	5	4	3	2	1	0
0xD4	CLCDATA	7:0	CLC8OUT	CLC7OUT	CLC6OUT	CLC5OUT	CLC4OUT	CLC3OUT	CLC2OUT	CLC1OUT
0xD5	CLCSELECT	7:0							SLCT[2:0]	
0xD6	CLCnCON	7:0	EN		OUT	INTP	INTN		MODE[2:0]	
0xD7	CLCnPOL	7:0	POL				G4POL	G3POL	G2POL	G1POL
0xD8	CLCnSEL0	7:0					D1S[7:0]			
0xD9	CLCnSEL1	7:0					D2S[7:0]			
0xDA	CLCnSEL2	7:0					D3S[7:0]			
0xDB	CLCnSEL3	7:0					D4S[7:0]			
0xDC	CLCnGLS0	7:0	G1D4T	G1D4N	G1D3T	G1D3N	G1D2T	G1D2N	G1D1T	G1D1N
0xDD	CLCnGLS1	7:0	G2D4T	G2D4N	G2D3T	G2D3N	G2D2T	G2D2N	G2D1T	G2D1N
0xDE	CLCnGLS2	7:0	G3D4T	G3D4N	G3D3T	G3D3N	G3D2T	G3D2N	G3D1T	G3D1N
0xDF	CLCnGLS3	7:0	G4D4T	G4D4N	G4D3T	G4D3N	G4D2T	G4D2N	G4D1T	G4D1N

CLC: Resumen de registros implicados

Address	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x0362	IPR0	7:0	IOCIP		CLC1IP		CSWIP	OSFIP	HLVDIP	SWIP
0x0368	IPR6	7:0	DMA2AIP	DMA2ORIP	DMA2DCNTIP	DMA2SCNTIP	NCO1IP	CWG1IP	CLC2IP	INT1IP
0x0369	IPR7	7:0	PWM3IP	PWM3PIP	CLC3IP		I2C1EIP	I2C1IP	I2C1TXIP	I2C1RXIP
0x036B	IPR9	7:0			CLC4IP		U3IP	U3EIP	U3TXIP	U3RXIP
0x036C	IPR10	7:0	DMA3AIP	DMA3ORIP	DMA3DCNTIP	DMA3SCNTIP	NCO2IP	CWG2IP	CLC5IP	INT2IP
0x036D	IPR11	7:0	DMA4AIP	DMA4ORIP	DMA4DCNTIP	DMA4SCNTIP	TMR4IP	CWG3IP	CLC6IP	CCP3IP
0x0370	IPR14	7:0					NCO3IP	CM2IP	CLC7IP	
0x0371	IPR15	7:0					TMR6IP	CRCIP	CLC8IP	NVMIP
0x049E	PIE0	7:0	IOCIE		CLC1IE		CSWIE	OSFIE	HLVDIE	SWIE
0x04A4	PIE6	7:0	DMA2AIE	DMA2ORIE	DMA2DCNTIE	DMA2SCNTIE	NCO1IE	CWG1IE	CLC2IE	INT1IE
0x04A5	PIE7	7:0	PWM3IE	PWM3PIE	CLC3IE		I2C1EIE	I2C1IE	I2C1TXIE	I2C1RXIE
0x04A7	PIE9	7:0			CLC4IE		U3IE	U3EIE	U3TXIE	U3RXIE
0x04A8	PIE10	7:0	DMA3AIE	DMA3ORIE	DMA3DCNTIE	DMA3SCNTIE	NCO2IE	CWG2IE	CLC5IE	INT2IE
0x04A9	PIE11	7:0	DMA4AIE	DMA4ORIE	DMA4DCNTIE	DMA4SCNTIE	TMR4IE	CWG3IE	CLC6IE	CCP3IE
0x04AC	PIE14	7:0					NCO3IE	CM2IE	CLC7IE	
0x04AD	PIE15	7:0					TMR6IE	CRCIE	CLC8IE	NVMIE
0x04AE	PIR0	7:0	IOCIF		CLC1IF		CSWIF	OSFIF	HLVDIF	SWIF
0x04B4	PIR6	7:0	DMA2AIF	DMA2ORIF	DMA2DCNTIF	DMA2SCNTIF	NCO1IF	CWG1IF	CLC2IF	INT1IF
0x04B5	PIR7	7:0	PWM3IF	PWM3PIF	CLC3IF		I2C1EIF	I2C1IF	I2C1TXIF	I2C1RXIF
0x04B7	PIR9	7:0			CLC4IF		U3IF	U3EIF	U3TXIF	U3RXIF
0x04B8	PIR10	7:0	DMA3AIF	DMA3ORIF	DMA3DCNTIF	DMA3SCNTIF	NCO2IF	CWG2IF	CLC5IF	INT2IF
0x04B9	PIR11	7:0	DMA4AIF	DMA4ORIF	DMA4DCNTIF	DMA4SCNTIF	TMR4IF	CWG3IF	CLC6IF	CCP3IF
0x04BC	PIR14	7:0					NCO3IF	CM2IF	CLC7IF	
0x04BD	PIR15	7:0					TMR6IF	CRCIF	CLC8IF	NVMIF

Detalle de registros para el CLC:

22.8.1 CLCSELECT Logic Cell

Name: CLCSELECT
Address: 0x0D5

CLC Instance Selection Register

Selects which CLC instance is accessed by the CLC registers

Bit	7	6	5	4	3	2	1	0
Access						R/W	R/W	R/W
Reset						0	0	0

Bits 2:0 – SLCT[2:0] CLC instance selection

Value	Description
n	Shared CLC registers of instance n+1 are selected for read and write operations

NOTA: Tener en cuenta que para configurar un CLC, se deberá especificar primero el CLC a través de este registro

Detalle de registros para el CLC:

- CLCnCON es el registro principal de configuración de un CLC, aquí encontrarás lo siguiente:

- EN : habilitador del CLC
- INTP/INTF : establecer si la interrupción del CLC es en flanco ascendente o descendente
- MODE: selección de la función lógica del CLC

22.8.2 CLCnCON Logic Cell

Name: CLCnCON
Address: 0x0D6

Configurable Logic Cell Control Register

Bit	7	6	5	4	3	2	1	0
Access	R/W			R/W	R/W	R/W	R/W	R/W
Reset	0		0	0	0	0	0	0

Bit 7 - EN CLC Enable

Value	Description
1	Configurable logic cell is enabled and mixing signals
0	Configurable logic cell is disabled and has logic zero output

Bit 5 - OUT Logic cell output data, after LCPOL. Sampled from CLCxOUT.

Bit 4 - INTP Configurable Logic Cell Positive Edge Going Interrupt Enable

Value	Description
1	CLCxIF will be set when a rising edge occurs on CLCxOUT
0	Rising edges on CLCxOUT have no effect on CLCxIF

Bit 3 - INTN Configurable Logic Cell Negative Edge Going Interrupt Enable

Value	Description
1	CLCxIF will be set when a falling edge occurs on CLCxOUT
0	Falling edges on CLCxOUT have no effect on CLCxIF

Bits 2:0 - MODE[2:0] Configurable Logic Cell Functional Mode Selection

Value	Description
111	Cell is 1-input transparent latch with Set and Reset
110	Cell is J-K flip-flop with Reset
101	Cell is 2-input D flip-flop with Reset
100	Cell is 1-input D flip-flop with Set and Reset
011	Cell is SR latch
010	Cell is 4-input AND
001	Cell is OR-XOR
000	Cell is AND-OR

Detalle de registros para el CLC:

- CLCnPOL es el registro de polaridad de la señal lógica:
- POL: polaridad de la señal de salida del CLC
- GxPOL: polaridad de la señal de cada puerta antes de ingresar a la función lógica del CLC

22.8.3 CLCnPOL Logic Cell

Name: CLCnPOL
Address: 0x0D7

Signal Polarity Control Register

Bit	7	6	5	4	3	2	1	0
Access	R/W				R/W	R/W	R/W	R/W
Reset	0				x	x	x	x

Bit 7 - POL CLCxOUT Output Polarity Control

Value	Description
1	The output of the logic cell is inverted
0	The output of the logic cell is not inverted

Bits 0, 1, 2, 3 - GxPOL Gate Output Polarity Control
Reset States: POR/BOR = xxxx
All Other Resets = uuuu

Value	Description
1	The gate output is inverted when applied to the logic cell
0	The output of the gate is not inverted

Detalle de registros para el CLC:

- CLCnSELx es el registro de selección de la señal de entrada a cada puerta.

22.8.4 CLCnSEL0

Name: CLCnSEL0
Address: 0x0D8

Generic CLCn Data 1 Select Register

Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	x	x	x	x	x	x	x	x

Bits 7:0 - D15[7:0] CLCn Data1 Input Selection

Table 22-2. CLC Input Selection

Dy5	Input Source	Dy5 (cont.)	Input Source (cont.)	Dy5 (cont.)	Input Source (cont.)
[0] 0000 0000	CLCIN0PPS	[32] 0010 0000	CCP2	[64] 0100 0000	SP1_SDO
[1] 0000 0001	CLCIN1PPS	[33] 0010 0001	CCP3	[65] 0100 0001	SP1_SCK
[2] 0000 0010	CLCIN2PPS	[34] 0010 0010	PWM1S1P1_OUT	[66] 0100 0010	SP1_SS
[3] 0000 0011	CLCIN3PPS	[35] 0010 0011	PWM1S1P2_OUT	[67] 0100 0011	SP2_SDO
[4] 0000 0100	CLCIN4PPS	[36] 0010 0100	PWM2S1P1_OUT	[68] 0100 0100	SP2_SCK
[5] 0000 0101	CLCIN5PPS	[37] 0010 0101	PWM2S1P2_OUT	[69] 0100 0101	SP2_SS
[6] 0000 0110	CLCIN6PPS	[38] 0010 0110	PWM3S1P1_OUT	[70] 0100 0110	I/C_SCL
[7] 0000 0111	CLCIN7PPS	[39] 0010 0111	PWM3S1P2_OUT	[71] 0100 0111	I/C_SDA
[8] 0000 1000	Fosc	[40] 0010 1000	---	[72] 0100 1000	CWG1A
[9] 0000 1001	HFINTOSC(1)	[41] 0010 1001	---	[73] 0100 1001	CWG1B
[10] 0000 1010	LFINTOSC(1)	[42] 0010 1010	NCO1	[74] 0100 1010	CWG2A
[11] 0000 1011	MFINTOSC(1)	[43] 0010 1011	NCO2	[75] 0100 1011	CWG2B
[12] 0000 1100	MFINTOSC (31.25 kHz)(1)	[44] 0010 1100	NCO3	[76] 0100 1100	CWG3A
[13] 0000 1101	SFINTOSC (1 MHz)(1)	[45] 0010 1101	CMP1_OUT	[77] 0100 1101	CWG3B
[14] 0000 1110	SOSC(1)	[46] 0010 1110	CMP2_OUT	---	---
[15] 0000 1111	EXTOSC(1)	[47] 0010 1111	ZCD	---	---
[16] 0001 0000	ADCON(1)	[48] 0001 0000	IDC	---	---
[17] 0001 0001	CLKR	[49] 0001 0001	DSM1	---	---
[18] 0001 0010	TMR0	[50] 0001 0010	HLVD_OUT	---	---
[19] 0001 0011	TMR1	[51] 0001 0011	CLC1	---	---
[20] 0001 0100	TMR2	[52] 0001 0100	CLC2	---	---
[21] 0001 0101	TMR3	[53] 0001 0101	CLC3	---	---
[22] 0001 0110	TMR4	[54] 0001 0110	CLC4	---	---
[23] 0001 0111	TMR5	[55] 0001 0111	CLC5	---	---
[24] 0001 1000	TMR6	[56] 0001 1000	CLC6	---	---
[25] 0001 1001	---	[57] 0001 1001	CLC7	---	---
[26] 0001 1010	---	[58] 0001 1010	CLC8	---	---
[27] 0001 1011	---	[59] 0001 1011	U1TX	---	---
[28] 0001 1100	---	[60] 0001 1100	U2TX	---	---
[29] 0001 1101	---	[61] 0001 1101	U3TX	---	---
[30] 0001 1110	SMT1	[62] 0001 1110	U4TX	---	---
[31] 0001 1111	CCP1	[63] 0001 1111	U5TX	[127] 0111 1111	---

Note:
1. Requests clock.

Reset States: POR/BOR = xxxxxxxx
All Other Resets = uuuuuuuu

Detalle de registros para el CLC:

- CLCnGLSx es el registro donde se selecciona qué señales van a ingresar al sector de puerta, tener en cuenta que hay la opción de ingreso invertido o no invertido.

22.8.8 CLCnGLS0

Name: CLCnGLS0
Address: 0x0DC

CLCn Gate1 Logic Select Register

Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	x	x	x	x	x	x	x	x

Bits 1, 3, 5, 7 - G1DyT dyT: Gate1 Data 'Y' True (noninverted)
Reset States: POR/BOR = xxxx
All Other Resets = uuuu

Value	Description
1	dyT is gated into g1
0	dyT is not gated into g1

Bits 0, 2, 4, 6 - G1DyN dyN: Gate1 Data 'Y' Negated (inverted)
Reset States: POR/BOR = xxxx
All Other Resets = uuuu

Value	Description
1	dyN is gated into g1
0	dyN is not gated into g1

22.8.9 CLCnGLS1

Name: CLCnGLS1
Address: 0x0DD

CLCn Gate2 Logic Select Register

Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	x	x	x	x	x	x	x	x

Bits 1, 3, 5, 7 - G2DyT dyT: Gate2 Data 'Y' True (noninverted)
Reset States: POR/BOR = xxxx
All Other Resets = uuuu

Value	Description
1	dyT is gated into g2
0	dyT is not gated into g2

Bits 0, 2, 4, 6 - G2DyN dyN: Gate2 Data 'Y' Negated (inverted)
Reset States: POR/BOR = xxxx
All Other Resets = uuuu

Value	Description
1	dyN is gated into g2
0	dyN is not gated into g2

22.8.10 CLCnGLS2

Name: CLCnGLS2
Address: 0x0DE

CLCn Gate3 Logic Select Register

Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	x	x	x	x	x	x	x	x

Bits 1, 3, 5, 7 - G3DyT dyT: Gate3 Data 'Y' True (noninverted)
Reset States: POR/BOR = xxxx
All Other Resets = uuuu

Value	Description
1	dyT is gated into g3
0	dyT is not gated into g3

Bits 0, 2, 4, 6 - G3DyN dyN: Gate3 Data 'Y' Negated (inverted)
Reset States: POR/BOR = xxxx
All Other Resets = uuuu

Value	Description
1	dyN is gated into g3
0	dyN is not gated into g3

22.8.11 CLCnGLS3

Name: CLCnGLS3
Address: 0x0DF

CLCn Gate4 Logic Select Register

Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	x	x	x	x	x	x	x	x

Bits 1, 3, 5, 7 - G4DyT dyT: Gate4 Data 'Y' True (noninverted)
Reset States: POR/BOR = xxxx
All Other Resets = uuuu

Value	Description
1	dyT is gated into g4
0	dyT is not gated into g4

Bits 0, 2, 4, 6 - G4DyN dyN: Gate4 Data 'Y' Negated (inverted)
Reset States: POR/BOR = xxxx
All Other Resets = uuuu

Value	Description
1	dyN is gated into g4
0	dyN is not gated into g4

Detalle de registros para el CLC:

- CLCDATA contiene una copia de las señales de salida de cada CLC

22.8.12 CLCDATA Logic Cel

Name: CLCDATA
Address: 0x0D4

CLC Data Output Register
 Mirror copy of CLC outputs

Bit	7	6	5	4	3	2	1	0
	CLC8OUT	CLC7OUT	CLC6OUT	CLC5OUT	CLC4OUT	CLC3OUT	CLC2OUT	CLC1OUT
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 0, 1, 2, 3, 4, 5, 6, 7 - CLCxOUT Mirror copy of CLCx_out

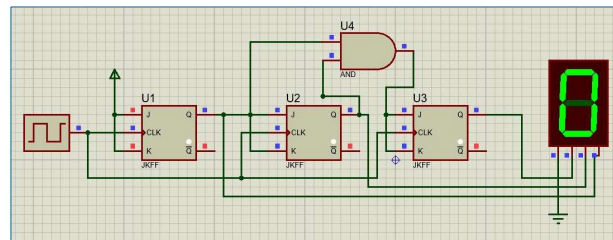
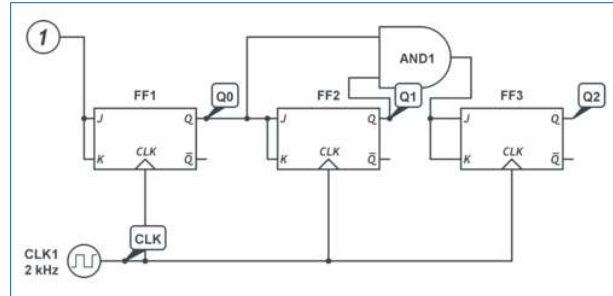
Value	Description
1	CLCx_out is 1
0	CLCx_out is 0

Referencias sobre uso de CLC

- Microchip TB3273 - Getting Started with CLC on PIC18:
<https://ww1.microchip.com/downloads/aemDocuments/documents/MCU08/ApplicationNotes/ApplicationNotes/Getting-Started-With-CLC-on-PIC18-90003273A.pdf>
- Microchip AN2912 - Using CLCs in Real-Time Applications:
https://ww1.microchip.com/downloads/en/AppNotes/AN2912-Using-CLCs-in-Real-Time-Apps_00002912A.pdf
- Microchip DS40002188A - Configurable Logic Cell (CLC) Tips and Tricks:
<https://ww1.microchip.com/downloads/en/DeviceDoc/40002188A.pdf>

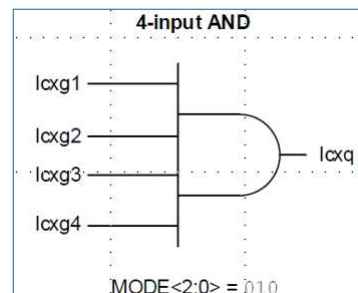
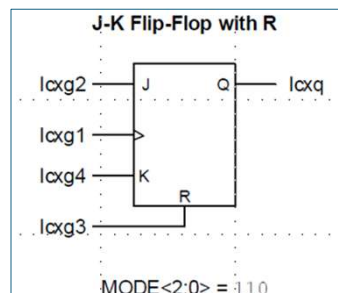
Ejemplo: Contador síncrono de 3 bits e implementado con FF JK

- Contador tipo síncrono (entrada de reloj para todos los FFs)
- Cuenta ascendente de uno en uno



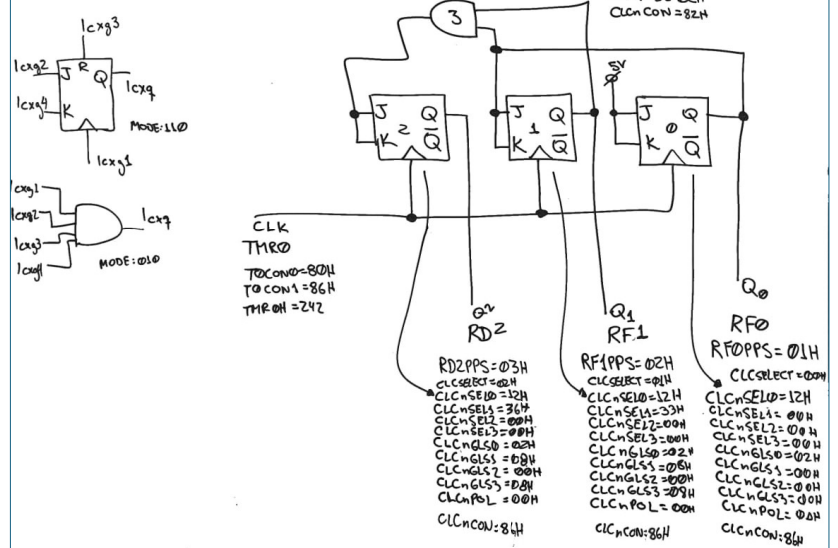
Ejemplo: Contador síncrono de 3 bits e implementado con FF JK

- Se emplearán cuatro celdas lógicas configurables: tres en modo FFJK y uno en modo AND de cuatro entradas



Ejemplo: Contador síncrono de 3 bits e implementado con FF JK

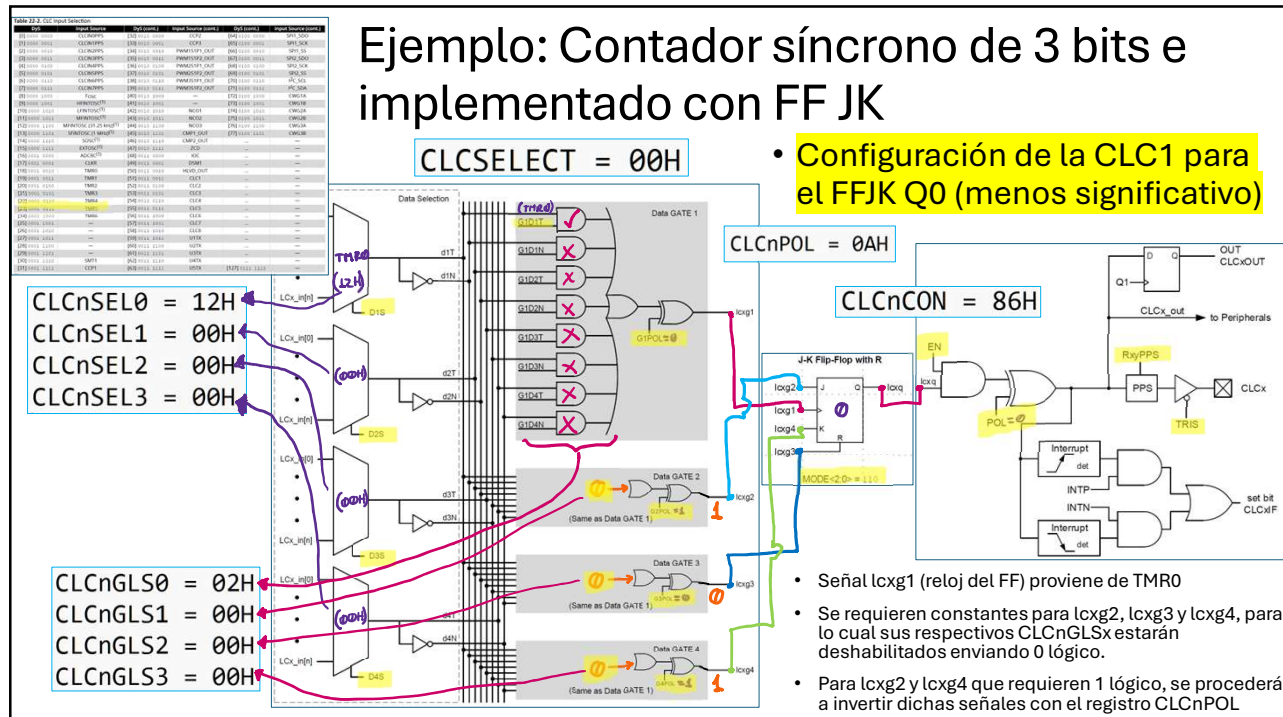
- Análisis y conexiones entre CLCs



Ejemplo: Contador síncrono de 3 bits e implementado con FF JK

CLCSELECT = 00H

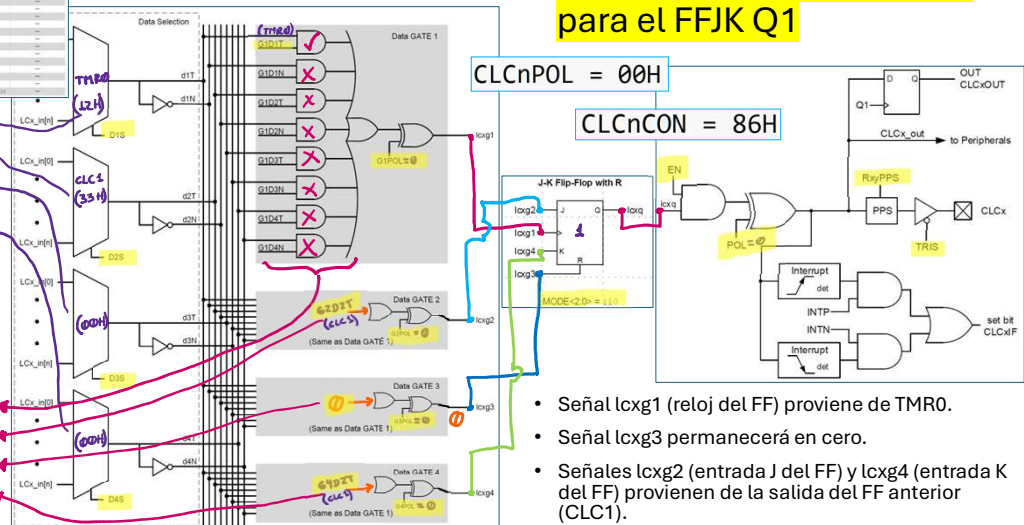
- Configuración de la CLC1 para el FFJK Q0 (menos significativo)



CLCSELECT = 01H

- | | | |
|----------|---|-----|
| CLCnSEL0 | = | 12H |
| CLCnSEL1 | = | 33H |
| CLCnSEL2 | = | 00H |
| CLCnSEL3 | = | 00H |

```
CLCnGLS0 = 02H
CLCnGLS1 = 08H
CLCnGLS2 = 00H
CLCnGLS3 = 08H
```



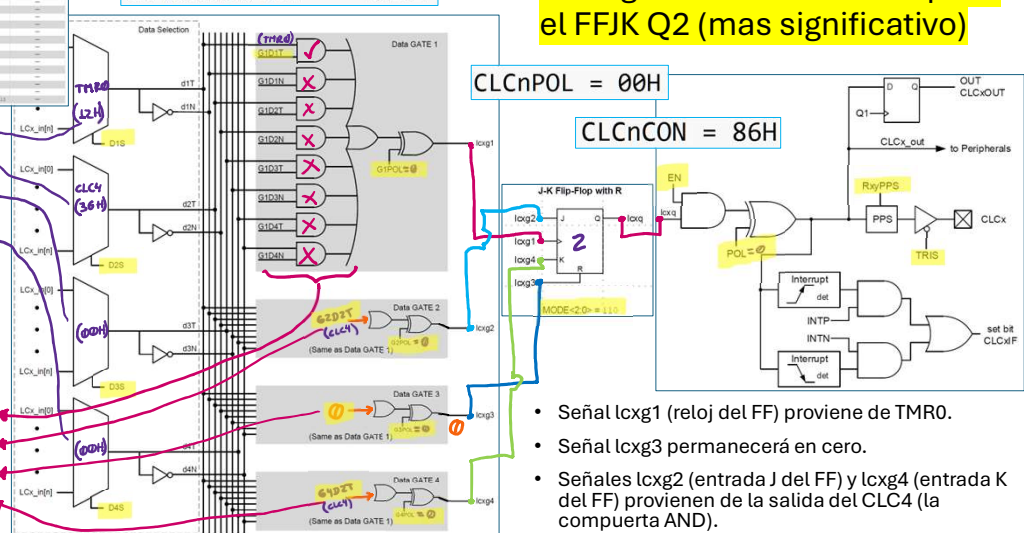
- Señal $lcxg1$ (reloj del FF) proviene de TMR0.
- Señal $lcxg3$ permanecerá en cero.
- Señales $lcxg2$ (entrada J del FF) y $lcxg4$ (entrada K del FF) provienen de la salida del FF anterior (CLC1).

[illegible]

```
CLCSELECT = 02H
```

- ```
CLCnSEL0 = 12H
CLCnSEL1 = 36H
CLCnSEL2 = 00H
CLCnSEL3 = 00H
```

```
CLCnGLS0 = 02H
CLCnGLS1 = 08H
CLCnGLS2 = 00H
CLCnGLS3 = 08H
```



- Señal lcxg1 (reloj del FF) proviene de TMR0.
- Señal lcxg3 permanecerá en cero.
- Señales lcxg2 (entrada J del FF) y lcxg4 (entrada K del FF) provienen de la salida del CLC4 (la compuerta AND).



Table 22-2: CLC Input Selection

| CLCn  | Input Source | CLCnSEL0 | CLCnSEL1 | CLCnSEL2 | CLCnSEL3 | CLCnGLS0 | CLCnGLS1 | CLCnGLS2 | CLCnGLS3 |
|-------|--------------|----------|----------|----------|----------|----------|----------|----------|----------|
| CLC0  | CLC0IN0      | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 |
| CLC1  | CLC1IN0      | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 |
| CLC2  | CLC2IN0      | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 |
| CLC3  | CLC3IN0      | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 |
| CLC4  | CLC4IN0      | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 |
| CLC5  | CLC5IN0      | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 |
| CLC6  | CLC6IN0      | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 |
| CLC7  | CLC7IN0      | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 |
| CLC8  | CLC8IN0      | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 |
| CLC9  | CLC9IN0      | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 |
| CLC10 | CLC10IN0     | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 |
| CLC11 | CLC11IN0     | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 |
| CLC12 | CLC12IN0     | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 |
| CLC13 | CLC13IN0     | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 |
| CLC14 | CLC14IN0     | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 |
| CLC15 | CLC15IN0     | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 |
| CLC16 | CLC16IN0     | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 |
| CLC17 | CLC17IN0     | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 |
| CLC18 | CLC18IN0     | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 |
| CLC19 | CLC19IN0     | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 |
| CLC20 | CLC20IN0     | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 |
| CLC21 | CLC21IN0     | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 |
| CLC22 | CLC22IN0     | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 |
| CLC23 | CLC23IN0     | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 |
| CLC24 | CLC24IN0     | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 |
| CLC25 | CLC25IN0     | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 |
| CLC26 | CLC26IN0     | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 |
| CLC27 | CLC27IN0     | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 |
| CLC28 | CLC28IN0     | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 |
| CLC29 | CLC29IN0     | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 |
| CLC30 | CLC30IN0     | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 |
| CLC31 | CLC31IN0     | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 | 00000000 |

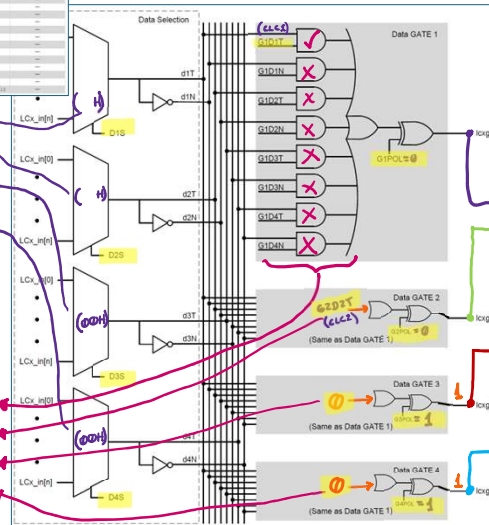
## Ejemplo: Contador síncrono de 3 bits e implementado con FF JK

CLCSELECT = 03H

- Configuración de la CLC4 para la AND4 (combinatoria para las entradas J y K del tercer FFJK)

CLCnSEL0 = 33H  
CLCnSEL1 = 34H  
CLCnSEL2 = 00H  
CLCnSEL3 = 00H

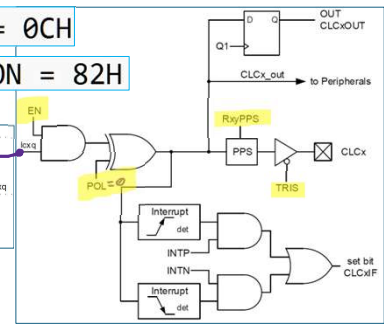
CLCnGLS0 = 02H  
CLCnGLS1 = 08H  
CLCnGLS2 = 00H  
CLCnGLS3 = 00H



CLCnPOL = 0CH

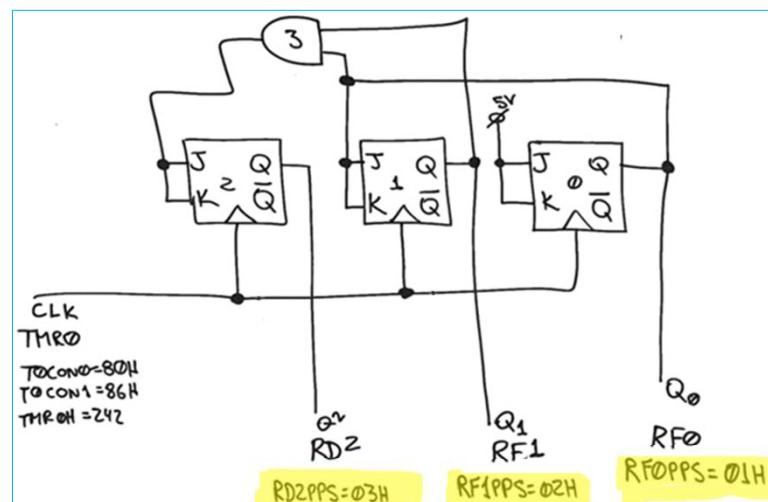
CLCnCON = 82H

- Señal lcxg1 proviene de CLC1 mientras que lcxg2 proviene de CLC2.
- Como solo se están empleando dos entradas para la función lógica AND4, lcxg3 y lcxg4 tendrán valor uno lógico usando el CLCnPOL.



## Ejemplo: Contador síncrono de 3 bits e implementado con FF JK

- Configuración de PPS para las salidas del contador (salidas de los FFs)
- La configuración del reloj del contador es el Timer0 que está temporizando 500ms (modo 8bit, fuente LFINTOSC, presc 1:64, posts 1:1, sync, TMR0H=242)





## Ejemplo: Contador síncrono de 3 bits e implementado con FF JK

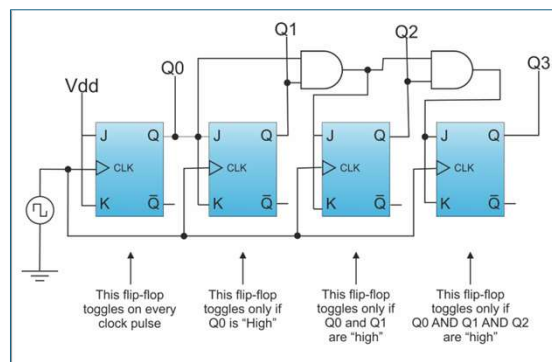
```

1 PROCESSOR 18F57Q43
2 #include "cabecera.inc"
3
4 PSECT upecenos, class=CODE, reloc=2, abs
5
6 upecenos:
7 ORG 000000H
8 bra configur0
9
10 ORG 000200H
11 configur0:
12 ;conf modulo de oscilador
13 movlb 08H
14 movlb 60H
15 movwf OSCCON1, 1
16 movwf OSCFREQ, 1
17 movlb 50H
18 movwf OSCEN, 1 ;HFINTOSC & LFINTOSC enabled
19 ;conf del CLC1
20 movlb 00H
21 movwf CLCSELECT, 1 ;CLC1 seleccionado
22 movlb 0AH
23 movwf CLCnPOL, 1 ;invertido para GATE2 y GATE4
24 movlb 12H
25 movwf CLCnSEL0, 1 ;D1S=THR0
26 clrf CLCnSEL1, 1 ;D2S no usado
27 clrf CLCnSEL2, 1 ;D3S no usado
28 clrf CLCnSEL3, 1 ;D4S no usado
29 movlb 02H
30 movwf CLCnGLS0, 1 ;GATE1 con G1D1T
31 clrf CLCnGLS1, 1 ;GATE2 en cero
32 clrf CLCnGLS2, 1 ;GATE3 en cero
33 clrf CLCnGLS3, 1 ;GATE4 en cero
34 clrf CLCDATA, 1
35 movlb 86H
36 movwf CLCnCON, 1 ;CLC1 enabled, FFJK mode
37 ;conf del CLC2
38 movlb 01H
39 movwf CLCSELECT, 1 ;CLC2 seleccionado
40 clrf CLCnPOL, 1 ;sin negar
41 movlb 12H
42 movwf CLCnSEL0, 1 ;D1S=THR0
43
44 movlb 33H
45 movwf CLCnSEL1, 1 ;D2S=CLC1
46 clrf CLCnSEL2, 1 ;D3S no usado
47 clrf CLCnSEL3, 1 ;D4S no usado
48 movlb 02H
49 movwf CLCnGLS0, 1 ;GATE1 con G1D1T
50 movlb 08H
51 movwf CLCnGLS1, 1 ;GATE2 en cero
52 clrf CLCnGLS2, 1 ;GATE3 en cero
53 clrf CLCnGLS3, 1 ;GATE4 en cero
54 clrf CLCDATA, 1
55 movlb 08H
56 movwf CLCnCON, 1 ;GATE4 en cero
57
58 movlb 86H
59 movwf CLCnCON, 1 ;CLC2 enabled, FFJK mode
60 ;conf del CLC3
61 movlb 02H
62 movwf CLCSELECT, 1 ;CLC3 seleccionado
63 clrf CLCnPOL, 1 ;sin negar
64 movlb 12H
65 movwf CLCnSEL0, 1 ;D1S=THR0
66 movlb 36H
67 movwf CLCnSEL1, 1 ;D2S=CLC4
68 clrf CLCnSEL2, 1 ;D3S no usado
69 clrf CLCnSEL3, 1 ;D4S no usado
70 movlb 02H
71 movwf CLCnGLS0, 1 ;GATE1 con G1D1T
72 movlb 08H
73 movwf CLCnGLS1, 1 ;GATE2 con G2D2T
74 clrf CLCnGLS2, 1 ;GATE3 en cero
75 movlb 08H
76 movwf CLCnGLS3, 1 ;GATE4 con G2D2T
77 clrf CLCDATA, 1
78 movlb 86H
79 movwf CLCnCON, 1 ;CLC3 enabled, FFJK mode
80 ;conf del CLC4
81 movlb 03H
82 movwf CLCSELECT, 1 ;CLC4 seleccionado
83 movlb 0CH
84 movwf CLCnPOL, 1 ;negados GATE3 y GATE4
85
86 movlb 33H
87 movwf CLCnSEL0, 1 ;D1S=CLC1
88 movlb 34H
89 movwf CLCnSEL1, 1 ;D2S=CLC2
90 clrf CLCnSEL2, 1 ;D3S no usado
91
92 clrf CLCnSEL3, 1 ;D4S no usado
93 movlb 02H
94 movwf CLCnGLS0, 1 ;GATE1 con G1D1T
95 movlb 08H
96 movwf CLCnGLS1, 1 ;GATE2 con G2D2T
97 clrf CLCnGLS2, 1 ;GATE3 en cero
98 clrf CLCnGLS3, 1 ;GATE4 en cero
99 clrf CLCDATA, 1
100 movlb 82H
101 movwf CLCnCON, 1 ;CLC4 enabled, AND4 mode
102 ;conf del FPS
103 movlb 2H
104 movlb 39H
105 movwf RC5PPS, 1 ;RC5 conectado a THR0
106 movlb 01H
107 movwf RF0PPS, 1 ;RF0 conectado a CLC1
108 movlb 02H
109 movwf RF1PPS, 1 ;RF1 conectado a CLC2
110 movlb 03H
111 movwf RD2PPS, 1 ;RD2 conectado a CLC3
112 ;conf del THR0
113 movlb 3H
114 movlb 80H
115 movwf TOCON0, 1 ;THR0 enabled, 8bit mode, post
116 movlb 86H
117 movwf TOCON1, 1 ;clksrc = LFINTOSC, sync, pres
118 movlb 242
119 movwf THROH, 1 ;valor de ref de comp 250
120 ;conf E/S
121 movlb 4H
122 bcf TRISC, 5, 1 ;RC5 como salida
123 bcf ANSEL0, 5, 1 ;RC5 como digital
124 movlb 0FCH
125 movwf TRISF, 1 ;RF0 y RF1 como salidas
126 movwf ANSEL1, 1 ;RF0 y RF1 como digitales
127 bcf TRISD, 2, 1 ;RD2 como salida
128 bcf ANSEL0, 2, 1 ;RD2 como digital
129
130 inicio:
131 bra inicio
132
133 end upecenos

```

## Ejemplo: Contador síncrono de 4 bits e implementado con FF JK

- Aumentando la resolución del contador anterior a 4 bits se tiene el siguiente circuito lógico digital:



- Basta añadir un flip flop JK adicional para el dígito mas significativo y una compuerta AND



## Ejemplo: Contador síncrono de 4 bits e implementado con FF JK

- Configuración del CLC5:

```
;conf del CLC5
movlw 04H
movwf CLCSELECT, 1 ;CLC4 seleccionado
movlw 0AH
movwf CLCnPOL, 1 ;Negados G2 y G4
movlw 12H
movwf CLCnSEL0, 1 ;D1S=TMR0
movlw 36H
movwf CLCnSEL1, 1 ;D2S=CLC4
movlw 35H
movwf CLCnSEL2, 1 ;D3S=CLC3
clrf CLCnSEL3, 1 ;D4S no usado
movlw 02H
movwf CLCnGLS0, 1 ;GATE1 con G1D1T
movlw 14H
movwf CLCnGLS1, 1 ;GATE2 con G2D2N AND G2D3N
clrf CLCnGLS2, 1 ;GATE3 en cero
movlw 14H
movwf CLCnGLS3, 1 ;GATE4 con G4D2N AND G4D3N
clrf CLCDATA, 1
movlw 86H
movwf CLCnCON, 1 ;CLC5 enabled, FFJK mode
```

Fin de la sesión