

# Celdas lógicas configurables (CLC) en el microcontrolador PIC18F57Q43

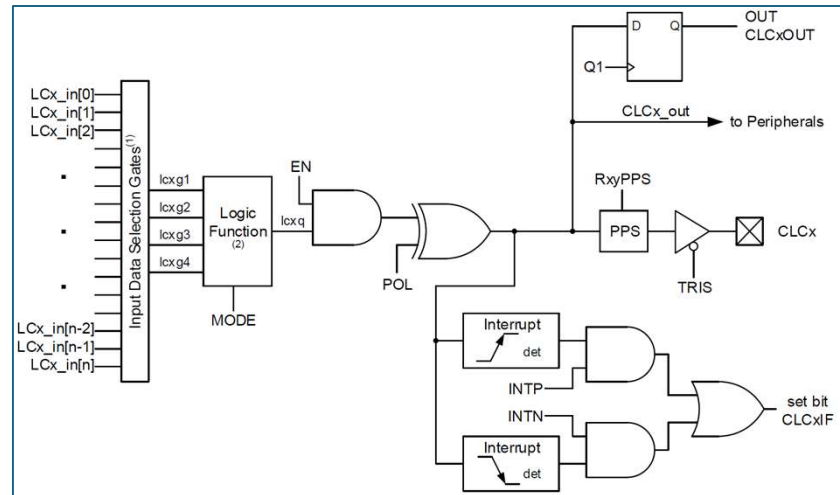
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Octubre del 2025

## Agenda

- El periférico Celda Lógica Configurable (CLC)
  - Descripción funcional
  - Configuración de entradas
  - Selección de función lógica
  - Gestión de la salida
  - Registros de configuración
  - El PPS para el CLC
- Ejemplo de un contador síncrono de 3 bits

## Las Celdas Lógicas Configurables (CLC)

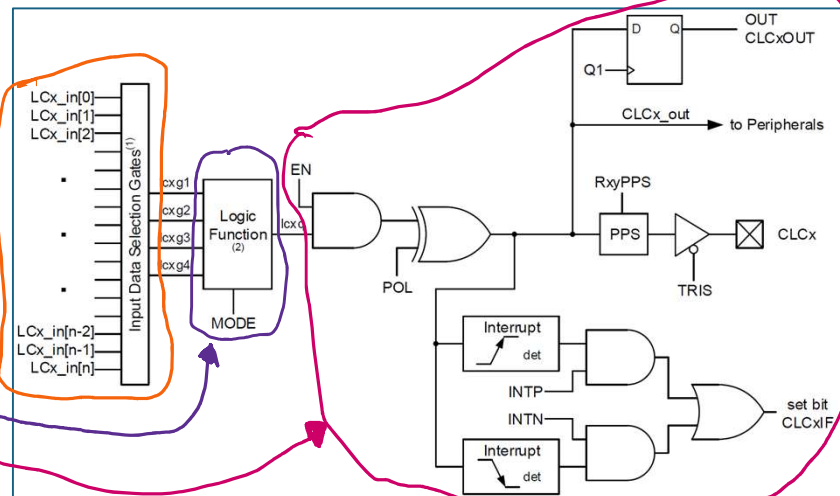
- Periférico donde se puede implementar funciones lógicas en hardware, similar a un PLD (programmable logic device).
- Se tienen ocho celdas lógicas configurables disponibles.



## Las Celdas Lógicas Configurables (CLC)

- Cada celda lógica configurable posee las siguientes partes:

- Configuración de las entradas
- Selección de la función lógica
- Gestionador de la salida





## CLC: Selección de señales de entrada

- Tener en cuenta el PPS si es que la señal de entrada proviene de pines del microcontrolador.
- Los puertos disponibles para recibir señales son:

Peripheral	PPS Input Register	Default Pin Selection at POR	Register Reset Value at POR	Available Input Port					
				28-Pin Devices		40-Pin Devices		48-Pin Devices	
CLCx Input 1	CLCIN0PPS	RA0	'b000 000	A	—	C	A	—	C
CLCx Input 2	CLCIN1PPS	RA1	'b000 001	A	—	C	A	—	C
CLCx Input 3	CLCIN2PPS	RB6	'b001 110	—	B	C	—	B	D
CLCx Input 4	CLCIN3PPS	RB7	'b001 111	—	B	C	—	B	D
CLCx Input 5	CLCIN4PPS	RA0	'b000 000	A	—	C	A	—	C
CLCx Input 6	CLCIN5PPS	RA1	'b000 001	A	—	C	A	—	C
CLCx Input 7	CLCIN6PPS	RB6	'b001 110	—	B	C	—	B	D
CLCx Input 8	CLCIN7PPS	RB7	'b001 111	—	B	C	—	B	D

Ejemplo: Si necesitamos conectar la entrada RC1 para CLC5:  
CLCIN5PPS = 11H (Revisar hoja técnica 21.8.1)

### 22.8.4 CLCnSELO

Name: CLCnSELO  
Address: 0x008

Generic CLCn Data 1 Select Register

Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	x	x	x	x	x	x	x	x

Bits 7:0 - D15[7:0] CLCn Data 1 Input Selection

Table 22-2. CLC Input Selection

CLCn	Input Source	CLCn	Input Source	CLCn	Input Source	CLCn	Input Source
[0] 0000 0000	CLCIN0PPS	[32] 0010 0000	CCP3	[64] 0100 0000	SP11_SCK		
[1] 0000 0001	CLCIN1PPS	[33] 0010 0001	CCP3	[65] 0100 0001	SP11_SS		
[2] 0000 0010	CLCIN2PPS	[34] 0010 0010	PWM5SP1_OUT	[66] 0100 0010	SP12_SCK		
[3] 0000 0011	CLCIN3PPS	[35] 0010 0011	PWM5SP2_OUT	[67] 0100 0011	SP12_SS		
[4] 0000 0100	CLCIN4PPS	[36] 0010 0100	PWM2SP1_OUT	[68] 0100 0100	SP12_SCK		
[5] 0000 0101	CLCIN5PPS	[37] 0010 0101	PWM2SP2_OUT	[69] 0100 0101	SP12_SS		
[6] 0000 0110	CLCIN6PPS	[38] 0010 0110	PWM3SP1_OUT	[70] 0100 0110	PC_SCL		
[7] 0000 0111	CLCIN7PPS	[39] 0010 0111	PWM3SP2_OUT	[71] 0100 0111	PC_SDA		
[8] 0000 1000	Fosc	[40] 0010 1000	—	[72] 0100 1000	CWG1A		
[9] 0000 1001	HFINTOSC(1)	[41] 0010 1001	—	[73] 0100 1001	CWG1B		
[10] 0000 1010	LFINTOSC(1)	[42] 0010 1010	NC01	[74] 0100 1010	CWG2A		
[11] 0000 1011	MFINTOSC(1)	[43] 0010 1011	NC02	[75] 0100 1011	CWG2B		
[12] 0000 1100	MFINTOSC(1.25 kHz)(1)	[44] 0010 1100	NC03	[76] 0100 1100	CWG3A		
[13] 0000 1101	SPINTOSC(1 MHz)(1)	[45] 0010 1101	CMP1_OUT	[77] 0100 1101	CWG3B		
[14] 0000 1110	SDC1(1)	[46] 0010 1110	CMP2_OUT	—	—		
[15] 0000 1111	EXTOSC(1)	[47] 0010 1111	ZC0	—	—		
[16] 0001 0000	ADRC1(1)	[48] 0011 0000	IOC	—	—		
[17] 0001 0001	CLKR	[49] 0011 0001	DSM1	—	—		
[18] 0001 0010	TMR0	[50] 0011 0010	HVD_OUT	—	—		
[19] 0001 0011	TMR1	[51] 0011 0011	CLC7	—	—		
[20] 0001 0100	TMR2	[52] 0011 0100	CLC2	—	—		
[21] 0001 0101	TMR3	[53] 0011 0101	CLC3	—	—		
[22] 0001 0110	TMR4	[54] 0011 0110	CLC4	—	—		
[23] 0001 0111	TMR5	[55] 0011 0111	CLC5	—	—		
[24] 0001 1000	TMR6	[56] 0011 1000	CLC6	—	—		
[25] 0001 1001	—	[57] 0011 1001	CLC7	—	—		
[26] 0001 1010	—	[58] 0011 1010	CLC8	—	—		
[27] 0001 1011	—	[59] 0011 1011	U2TX	—	—		
[28] 0001 1100	—	[60] 0011 1100	U2TX	—	—		
[29] 0001 1101	—	[61] 0011 1101	U3TX	—	—		
[30] 0001 1110	SM1	[62] 0011 1110	U4TX	—	—		
[31] 0001 1111	CCP1	[63] 0011 1111	U5TX	[127] 0111 1111	—		

Note:  
1. Requests clock.  
Reset States: POR/BOR = xxxxxxxx  
All Other Resets = uuuuuuuu

### 22.8.5 CLCnSEL1

Name: CLCnSEL1  
Address: 0x009

Generic CLCn Data 1 Select Register

Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	x	x	x	x	x	x	x	x

Bits 7:0 - D15[7:0] CLCn Data 2 Input Selection

Reset States: POR/BOR = xxxxxxxx  
All Other Resets = uuuuuuuu

Refer to the CLC Input Selection table for input selections.

### 22.8.6 CLCnPOL

Name: CLCnPOL  
Address: 0x007

Signal Polarity Control Register

Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	x	x	x	x	x	x	x	x

Bits 7:0 - CLCn Data 2 Input Polarity Control

Reset States: POR/BOR = xxx  
All Other Resets = uuuuu

The input of the signal is inverted when the bit is set.

### 22.8.8 CLCnGLS0

Name: CLCnGLS0  
Address: 0x00C

Generic CLCn Data 1 Select Register

Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	x	x	x	x	x	x	x	x

Bits 1, 3, 5, 7 - G1[7:0] dy: Gate 1 Data Y True (noninverted)

Reset States: POR/BOR = xxx  
All Other Resets = uuuuu

Bits 0, 2, 4, 6 - G1[7:0] dy: Gate 1 Data Y Negated (inverted)

Reset States: POR/BOR = xxx  
All Other Resets = uuuuu

Bits 1, 3, 5, 7 - G2[7:0] dy: Gate 2 Data Y True (noninverted)

Reset States: POR/BOR = xxx  
All Other Resets = uuuuu

Bits 0, 2, 4, 6 - G2[7:0] dy: Gate 2 Data Y Negated (inverted)

Reset States: POR/BOR = xxx  
All Other Resets = uuuuu

### 22.8.9 CLCnGLS1

Name: CLCnGLS1  
Address: 0x00D

Generic CLCn Data 1 Select Register

Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	x	x	x	x	x	x	x	x

Bits 1, 3, 5, 7 - G2[7:0] dy: Gate 2 Data Y True (noninverted)

Reset States: POR/BOR = xxx  
All Other Resets = uuuuu

Bits 0, 2, 4, 6 - G2[7:0] dy: Gate 2 Data Y Negated (inverted)

Reset States: POR/BOR = xxx  
All Other Resets = uuuuu

### 22.8.10 CLCnGLS2

Name: CLCnGLS2  
Address: 0x00E

Generic CLCn Data 1 Select Register

Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	x	x	x	x	x	x	x	x

Bits 1, 3, 5, 7 - G3[7:0] dy: Gate 3 Data Y True (noninverted)

Reset States: POR/BOR = xxx  
All Other Resets = uuuuu

Bits 0, 2, 4, 6 - G3[7:0] dy: Gate 3 Data Y Negated (inverted)

Reset States: POR/BOR = xxx  
All Other Resets = uuuuu

### 22.8.11 CLCnGLS3

Name: CLCnGLS3  
Address: 0x00F

Generic CLCn Data 1 Select Register

Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	x	x	x	x	x	x	x	x

Bits 1, 3, 5, 7 - G4[7:0] dy: Gate 4 Data Y True (noninverted)

Reset States: POR/BOR = xxx  
All Other Resets = uuuuu

Bits 0, 2, 4, 6 - G4[7:0] dy: Gate 4 Data Y Negated (inverted)

Reset States: POR/BOR = xxx  
All Other Resets = uuuuu

### 22.8.12 CLCnGLS4

Name: CLCnGLS4  
Address: 0x010

Generic CLCn Data 1 Select Register

Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	x	x	x	x	x	x	x	x

Bits 1, 3, 5, 7 - G5[7:0] dy: Gate 5 Data Y True (noninverted)

Reset States: POR/BOR = xxx  
All Other Resets = uuuuu

Bits 0, 2, 4, 6 - G5[7:0] dy: Gate 5 Data Y Negated (inverted)

Reset States: POR/BOR = xxx  
All Other Resets = uuuuu

### 22.8.13 CLCnGLS5

Name: CLCnGLS5  
Address: 0x011

Generic CLCn Data 1 Select Register

Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	x	x	x	x	x	x	x	x

Bits 1, 3, 5, 7 - G6[7:0] dy: Gate 6 Data Y True (noninverted)

Reset States: POR/BOR = xxx  
All Other Resets = uuuuu

Bits 0, 2, 4, 6 - G6[7:0] dy: Gate 6 Data Y Negated (inverted)

Reset States: POR/BOR = xxx  
All Other Resets = uuuuu

### 22.8.14 CLCnGLS6

Name: CLCnGLS6  
Address: 0x012

Generic CLCn Data 1 Select Register

Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	x	x	x	x	x	x	x	x

Bits 1, 3, 5, 7 - G7[7:0] dy: Gate 7 Data Y True (noninverted)

Reset States: POR/BOR = xxx  
All Other Resets = uuuuu

Bits 0, 2, 4, 6 - G7[7:0] dy: Gate 7 Data Y Negated (inverted)

Reset States: POR/BOR = xxx  
All Other Resets = uuuuu

### 22.8.15 CLCnGLS7

Name: CLCnGLS7  
Address: 0x013

Generic CLCn Data 1 Select Register

Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	x	x	x	x	x	x	x	x

Bits 1, 3, 5, 7 - G8[7:0] dy: Gate 8 Data Y True (noninverted)

Reset States: POR/BOR = xxx  
All Other Resets = uuuuu

Bits 0, 2, 4, 6 - G8[7:0] dy: Gate 8 Data Y Negated (inverted)

Reset States: POR/BOR = xxx  
All Other Resets = uuuuu

### 22.8.16 CLCnGLS8

Name: CLCnGLS8  
Address: 0x014

Generic CLCn Data 1 Select Register

Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	x	x	x	x	x	x	x	x

Bits 1, 3, 5, 7 - G9[7:0] dy: Gate 9 Data Y True (noninverted)

Reset States: POR/BOR = xxx  
All Other Resets = uuuuu

Bits 0, 2, 4, 6 - G9[7:0] dy: Gate 9 Data Y Negated (inverted)

Reset States: POR/BOR = xxx  
All Other Resets = uuuuu

### 22.8.17 CLCnGLS9

Name: CLCnGLS9  
Address: 0x015

Generic CLCn Data 1 Select Register

Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	x	x	x	x	x	x	x	x

Bits 1, 3, 5, 7 - G10[7:0] dy: Gate 10 Data Y True (noninverted)

Reset States: POR/BOR = xxx  
All Other Resets = uuuuu

Bits 0, 2, 4, 6 - G10[7:0] dy: Gate 10 Data Y Negated (inverted)

Reset States: POR/BOR = xxx  
All Other Resets = uuuuu

### 22.8.18 CLCnGLS10

Name: CLCnGLS10  
Address: 0x016

Generic CLCn Data 1 Select Register

Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	x	x	x	x	x	x	x	x

Bits 1, 3, 5, 7 - G11[7:0] dy: Gate 11 Data Y True (noninverted)

Reset States: POR/BOR = xxx  
All Other Resets = uuuuu

Bits 0, 2, 4, 6 - G11[7:0] dy: Gate 11 Data Y Negated (inverted)

Reset States: POR/BOR = xxx  
All Other Resets = uuuuu

### 22.8.19 CLCnGLS11

Name: CLCnGLS11  
Address: 0x017

Generic CLCn Data 1 Select Register

Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	x	x	x	x	x	x	x	x

Bits 1, 3, 5, 7 - G12[7:0] dy: Gate 12 Data Y True (noninverted)

Reset States: POR/BOR = xxx  
All Other Resets = uuuuu

Bits 0, 2, 4, 6 - G12[7:0] dy: Gate 12 Data Y Negated (inverted)

Reset States: POR/BOR = xxx  
All Other Resets = uuuuu

### 22.8.20 CLCnGLS12

Name: CLCnGLS12  
Address: 0x018

Generic CLCn Data 1 Select Register

Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	x	x	x	x	x	x	x	x

Bits 1, 3, 5, 7 - G13[7:0] dy: Gate 13 Data Y True (noninverted)

Reset States: POR/BOR = xxx  
All Other Resets = uuuuu

Bits 0, 2, 4, 6 - G13[7:0] dy: Gate 13 Data Y Negated (inverted)

Reset States: POR/BOR = xxx  
All Other Resets = uuuuu

### 22.8.21 CLCnGLS13

Name: CLCnGLS13  
Address: 0x019

Generic CLCn Data 1 Select Register

Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	x	x	x	x	x	x	x	x

Bits 1, 3, 5, 7 - G14[7:0] dy: Gate 14 Data Y True (noninverted)

Reset States: POR/BOR = xxx  
All Other Resets = uuuuu

Bits 0, 2, 4, 6 - G14[7:0] dy: Gate 14 Data Y Negated (inverted)

Reset States: POR/BOR = xxx  
All Other Resets = uuuuu

### 22.8.22 CLCnGLS14

Name: CLCnGLS14  
Address: 0x01A

Generic CLCn Data 1 Select Register

Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	x	x	x	x	x	x	x	x

Bits 1, 3, 5, 7 - G15[7:0] dy: Gate 15 Data Y True (noninverted)

Reset States: POR/BOR = xxx  
All Other Resets = uuuuu

Bits 0, 2, 4, 6 - G15[7:0] dy: Gate 15 Data Y Negated (inverted)

Reset States: POR/BOR = xxx  
All Other Resets = uuuuu

### 22.8.23 CLCnGLS15

Name: CLCnGLS15  
Address: 0x01B

Generic CLCn Data 1 Select Register

Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	x	x	x	x	x	x	x	x

Bits 1, 3, 5, 7 - G16[7:0] dy: Gate 16 Data Y True (noninverted)

Reset States: POR/BOR = xxx  
All Other Resets = uuuuu

Bits 0, 2, 4, 6 - G16[7:0] dy: Gate 16 Data Y Negated (inverted)

Reset States: POR/BOR = xxx  
All Other Resets = uuuuu

### 22.8.24 CLCnGLS16

Name: CLCnGLS16  
Address: 0x01C

Generic CLCn Data 1 Select Register

Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	x	x	x	x	x	x	x	x

Bits 1, 3, 5, 7 - G17[7:0] dy: Gate 17 Data Y True (noninverted)

Reset States: POR/BOR = xxx  
All Other Resets = uuuuu

Bits 0, 2, 4, 6 - G17[7:0] dy: Gate 17 Data Y Negated (inverted)

Reset States: POR/BOR = xxx  
All Other Resets = uuuuu

### 22.8.25 CLCnGLS17

Name: CLCnGLS17  
Address: 0x01D

Generic CLCn Data 1 Select Register

Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	x	x	x	x	x	x	x	x

Bits 1, 3, 5, 7 - G18[7:0] dy: Gate 18 Data Y True (noninverted)

Reset States: POR/BOR = xxx  
All Other Resets = uuuuu

Bits 0, 2, 4, 6 - G18[7:0] dy: Gate 18 Data Y Negated (inverted)

Reset States: POR/BOR = xxx  
All Other Resets = uuuuu

### 22.8.26 CLCnGLS18

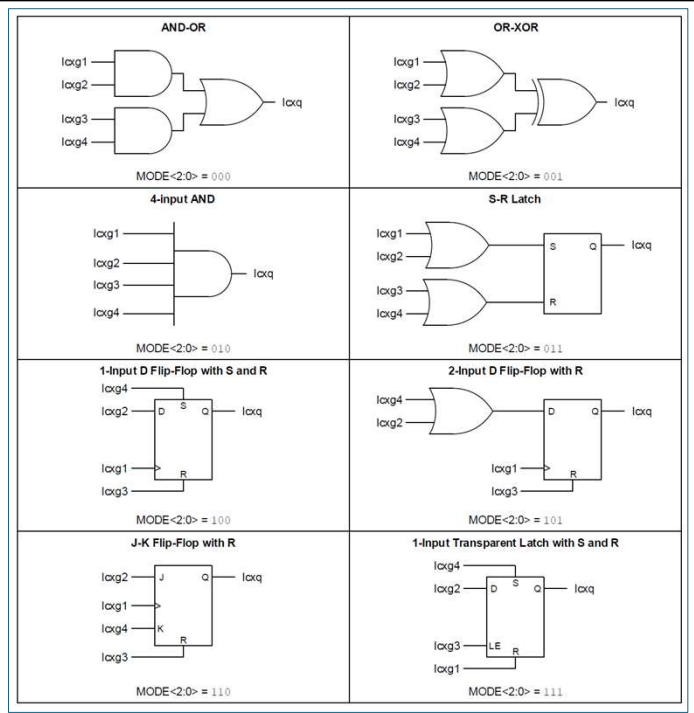
Name: CLCnGLS18  
Address: 0x01E

Generic CLCn Data 1 Select Register

Bit	7	6	5
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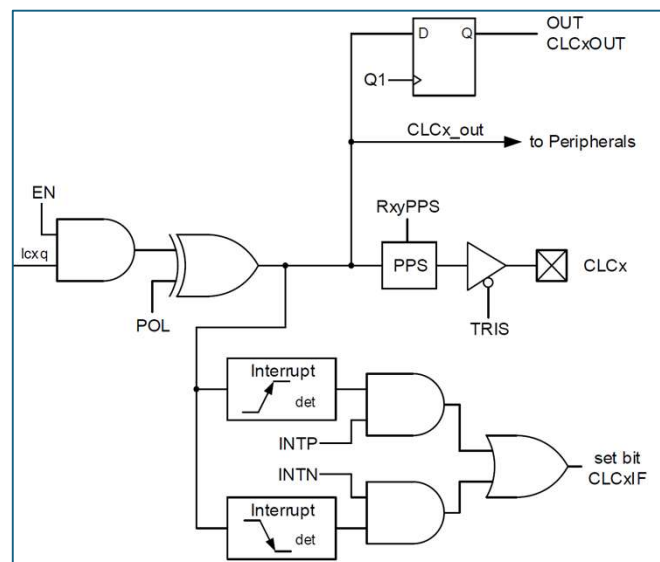
## CLC: Selección de función lógica

- Se tienen como opción ocho tipos de función lógica para un CLC.
- Tener en cuenta que las entradas  $lcxg1$ ,  $lcxg2$ ,  $lcxg3$  y  $lcxg4$  provienen de la etapa de selección de entrada vista anteriormente.
- La señal de salida  $lcxq$  esta conectado a la etapa de la gestión de salida del CLC



## CLC: Gestión de salida del CLC

- En esta etapa se configura lo siguiente:
  - Habilitador del CLC con EN (registro CLCnCON bit 7)
  - Inversor de la señal de salida con POL (registro CLCnPOL bit 7)
  - Opción para que salga por un pin de E/S configurando el PPS
  - Configuración del flanco para generación de interrupción



## CLC: Gestión de salida del CLC

- Hay que tener en cuenta los puertos permitidos por el PPS para el periférico CLC y es que se requiere que la señal salga a un pin del microcontrolador

RxyPPS	Output Source	Available Output Ports											
		28-Pin Devices			40-Pin Devices			48-Pin Devices					
0x08	CLC8OUT	—	B	C	—	B	—	D	—	—	B	—	D
0x07	CLC7OUT	—	B	C	—	B	—	D	—	—	B	—	D
0x06	CLC6OUT	A	—	C	A	—	C	—	—	A	—	—	F
0x05	CLC5OUT	A	—	C	A	—	C	—	—	A	—	—	F
0x04	CLC4OUT	—	B	C	—	B	—	D	—	—	B	—	D
0x03	CLC3OUT	—	B	C	—	B	—	D	—	—	B	—	D
0x02	CLC2OUT	A	—	C	A	—	C	—	—	A	—	—	F
0x01	CLC1OUT	A	—	C	A	—	C	—	—	A	—	—	F

Ejemplo: Si necesitamos conectar la salida de CLC3 hacia RD5:  
RD5PPS = 03H

## CLC: Resumen de registros implicados

### 22.9 Register Summary - CLC Control

Logic Cell

Address	Name	Bit Pos.	7	6	5	4	3	2	1	0
0xD4	CLCDATA	7:0	CLC8OUT	CLC7OUT	CLC6OUT	CLC5OUT	CLC4OUT	CLC3OUT	CLC2OUT	CLC1OUT
0xD5	CLCSELECT	7:0							SLCT[2:0]	
0xD6	CLCnCON	7:0	EN		OUT	INTP	INTN		MODE[2:0]	
0xD7	CLCnPOL	7:0	POL				G4POL	G3POL	G2POL	G1POL
0xD8	CLCnSEL0	7:0					D1S[7:0]			
0xD9	CLCnSEL1	7:0					D2S[7:0]			
0xDA	CLCnSEL2	7:0					D3S[7:0]			
0xDB	CLCnSEL3	7:0					D4S[7:0]			
0xDC	CLCnGLS0	7:0	G1D4T	G1D4N	G1D3T	G1D3N	G1D2T	G1D2N	G1D1T	G1D1N
0xDD	CLCnGLS1	7:0	G2D4T	G2D4N	G2D3T	G2D3N	G2D2T	G2D2N	G2D1T	G2D1N
0xDE	CLCnGLS2	7:0	G3D4T	G3D4N	G3D3T	G3D3N	G3D2T	G3D2N	G3D1T	G3D1N
0xDF	CLCnGLS3	7:0	G4D4T	G4D4N	G4D3T	G4D3N	G4D2T	G4D2N	G4D1T	G4D1N



## CLC: Resumen de registros implicados

Address	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x0362	IPR0	7:0	IOCIP		CLC1IP		CSWIP	OSFIP	HLVDIP	SWIP
0x0368	IPR6	7:0	DMA2AIP	DMA2ORIP	DMA2DCNTIP	DMA2SCNTIP	NCO1IP	CWG1IP	CLC2IP	INT1IP
0x0369	IPR7	7:0	PWM3IP	PWM3PIP	CLC3IP		I2C1EIP	I2C1IP	I2C1TXIP	I2C1RXIP
0x036B	IPR9	7:0			CLC4IP		U3IP	U3EIP	U3TXIP	U3RXIP
0x036C	IPR10	7:0	DMA3AIP	DMA3ORIP	DMA3DCNTIP	DMA3SCNTIP	NCO2IP	CWG2IP	CLC5IP	INT2IP
0x036D	IPR11	7:0	DMA4AIP	DMA4ORIP	DMA4DCNTIP	DMA4SCNTIP	TMR4IP	CWG3IP	CLC6IP	CCP3IP
0x0370	IPR14	7:0					NCO3IP	CM2IP	CLC7IP	
0x0371	IPR15	7:0					TMR6IP	CRCIP	CLC8IP	NVMIP
0x049E	PIE0	7:0	IOCIE		CLC1IE		CSWIE	OSFIE	HLVDIE	SWIE
0x04A4	PIE6	7:0	DMA2AIE	DMA2ORIE	DMA2DCNTIE	DMA2SCNTIE	NCO1IE	CWG1IE	CLC2IE	INT1IE
0x04A5	PIE7	7:0	PWM3IE	PWM3PIE	CLC3IE		I2C1EIE	I2C1IE	I2C1TXIE	I2C1RXIE
0x04A7	PIE9	7:0			CLC4IE		U3IE	U3EIE	U3TXIE	U3RXIE
0x04A8	PIE10	7:0	DMA3AIE	DMA3ORIE	DMA3DCNTIE	DMA3SCNTIE	NCO2IE	CWG2IE	CLC5IE	INT2IE
0x04A9	PIE11	7:0	DMA4AIE	DMA4ORIE	DMA4DCNTIE	DMA4SCNTIE	TMR4IE	CWG3IE	CLC6IE	CCP3IE
0x04AC	PIE14	7:0					NCO3IE	CM2IE	CLC7IE	
0x04AD	PIE15	7:0					TMR6IE	CRCIE	CLC8IE	NVMIE
0x04AE	PIR0	7:0	IOCIF		CLC1IF		CSWIF	OSFIF	HLVDIF	SWIF
0x04B4	PIR6	7:0	DMA2AIF	DMA2ORIF	DMA2DCNTIF	DMA2SCNTIF	NCO1IF	CWG1IF	CLC2IF	INT1IF
0x04B5	PIR7	7:0	PWM3IF	PWM3PIF	CLC3IF		I2C1EIF	I2C1IF	I2C1TXIF	I2C1RXIF
0x04B7	PIR9	7:0			CLC4IF		U3IF	U3EIF	U3TXIF	U3RXIF
0x04B8	PIR10	7:0	DMA3AIF	DMA3ORIF	DMA3DCNTIF	DMA3SCNTIF	NCO2IF	CWG2IF	CLC5IF	INT2IF
0x04B9	PIR11	7:0	DMA4AIF	DMA4ORIF	DMA4DCNTIF	DMA4SCNTIF	TMR4IF	CWG3IF	CLC6IF	CCP3IF
0x04BC	PIR14	7:0					NCO3IF	CM2IF	CLC7IF	
0x04BD	PIR15	7:0					TMR6IF	CRCIF	CLC8IF	NVMIF

## Detalle de registros para el CLC:

**22.8.1 CLCSELECT** Logic Cell

**Name:** CLCSELECT  
**Address:** 0x0D5

CLC Instance Selection Register

Selects which CLC instance is accessed by the CLC registers

Bit	7	6	5	4	3	2	1	0
Access						R/W	R/W	R/W
Reset						0	0	0

**Bits 2:0 – SLCT[2:0]** CLC instance selection

Value	Description
n	Shared CLC registers of instance n+1 are selected for read and write operations

NOTA: Tener en cuenta que para configurar un CLC, se deberá especificar primero el CLC a través de este registro

## Detalle de registros para el CLC:

- CLCnCON es el registro principal de configuración de un CLC, aquí encontrarás lo siguiente:

- EN : habilitador del CLC
- INTP/INTF : establecer si la interrupción del CLC es en flanco ascendente o descendente
- MODE: selección de la función lógica del CLC

**22.8.2 CLCnCON** Logic Cell

**Name:** CLCnCON  
**Address:** 0x0D6

Configurable Logic Cell Control Register

Bit	7	6	5	4	3	2	1	0
Access	R/W			R/W	R/W	R/W	R/W	R/W
Reset	0		0	0	0	0	0	0

**Bit 7 - EN** CLC Enable

Value	Description
1	Configurable logic cell is enabled and mixing signals
0	Configurable logic cell is disabled and has logic zero output

**Bit 5 - OUT** Logic cell output data, after LCPOL. Sampled from CLCxOUT.

**Bit 4 - INTP** Configurable Logic Cell Positive Edge Going Interrupt Enable

Value	Description
1	CLCxIF will be set when a rising edge occurs on CLCxOUT
0	Rising edges on CLCxOUT have no effect on CLCxIF

**Bit 3 - INTN** Configurable Logic Cell Negative Edge Going Interrupt Enable

Value	Description
1	CLCxIF will be set when a falling edge occurs on CLCxOUT
0	Falling edges on CLCxOUT have no effect on CLCxIF

**Bits 2:0 - MODE[2:0]** Configurable Logic Cell Functional Mode Selection

Value	Description
111	Cell is 1-input transparent latch with Set and Reset
110	Cell is J-K flip-flop with Reset
101	Cell is 2-input D flip-flop with Reset
100	Cell is 1-input D flip-flop with Set and Reset
011	Cell is SR latch
010	Cell is 4-input AND
001	Cell is OR-XOR
000	Cell is AND-OR

## Detalle de registros para el CLC:

- CLCnPOL es el registro de polaridad de la señal lógica:
- POL: polaridad de la señal de salida del CLC
- GxPOL: polaridad de la señal de cada puerta antes de ingresar a la función lógica del CLC

**22.8.3 CLCnPOL** Logic Cell

**Name:** CLCnPOL  
**Address:** 0x0D7

Signal Polarity Control Register

Bit	7	6	5	4	3	2	1	0
Access	R/W				R/W	R/W	R/W	R/W
Reset	0				x	x	x	x

**Bit 7 - POL** CLCxOUT Output Polarity Control

Value	Description
1	The output of the logic cell is inverted
0	The output of the logic cell is not inverted

**Bits 0, 1, 2, 3 - GxPOL** Gate Output Polarity Control  
Reset States: POR/BOR = xxxx  
All Other Resets = uuuu

Value	Description
1	The gate output is inverted when applied to the logic cell
0	The output of the gate is not inverted



## Detalle de registros para el CLC:

- CLCnSELx es el registro de selección de la señal de entrada a cada puerta.

**22.8.4 CLCnSEL0**

Name: CLCnSEL0  
Address: 0x0D8

Generic CLCn Data 1 Select Register

Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	x	x	x	x	x	x	x	x

Bits 7:0 - D15[7:0] CLCn Data1 Input Selection

Table 22-2. CLC Input Selection

Dy5	Input Source	Dy5 (cont.)	Input Source (cont.)	Dy5 (cont.)	Input Source (cont.)
[0] 0000 0000	CLCIN0PPS	[32] 0010 0000	CCP2	[64] 0100 0000	SP1_SDO
[1] 0000 0001	CLCIN1PPS	[33] 0010 0001	CCP3	[65] 0100 0001	SP1_SCK
[2] 0000 0010	CLCIN2PPS	[34] 0010 0010	PWM1S1P1_OUT	[66] 0100 0010	SP1_SS
[3] 0000 0011	CLCIN3PPS	[35] 0010 0011	PWM1S1P2_OUT	[67] 0100 0011	SP2_SDO
[4] 0000 0100	CLCIN4PPS	[36] 0010 0100	PWM2S1P1_OUT	[68] 0100 0100	SP2_SCK
[5] 0000 0101	CLCIN5PPS	[37] 0010 0101	PWM2S1P2_OUT	[69] 0100 0101	SP2_SS
[6] 0000 0110	CLCIN6PPS	[38] 0010 0110	PWM3S1P1_OUT	[70] 0100 0110	I <sup>2</sup> C_SCL
[7] 0000 0111	CLCIN7PPS	[39] 0010 0111	PWM3S1P2_OUT	[71] 0100 0111	I <sup>2</sup> C_SDA
[8] 0000 1000	Fosc	[40] 0010 1000	—	[72] 0100 1000	CWG1A
[9] 0000 1001	HFINTOSC(1)	[41] 0010 1001	—	[73] 0100 1001	CWG1B
[10] 0000 1010	LFINTOSC(1)	[42] 0010 1010	NCO1	[74] 0100 1010	CWG2A
[11] 0000 1011	MFINTOSC(1)	[43] 0010 1011	NCO2	[75] 0100 1011	CWG2B
[12] 0000 1100	MFINTOSC (31.25 kHz)(1)	[44] 0010 1100	NCO3	[76] 0100 1100	CWG3A
[13] 0000 1101	SPINTOSC (1 MHz)(1)	[45] 0010 1101	CMP1_OUT	[77] 0100 1101	CWG3B
[14] 0000 1110	SOSC(1)	[46] 0010 1110	CMP2_OUT	—	—
[15] 0000 1111	EXTOSC(1)	[47] 0010 1111	ZCD	—	—
[16] 0001 0000	ADCON(1)	[48] 0001 0000	IDC	—	—
[17] 0001 0001	CLKR	[49] 0001 0001	DSM1	—	—
[18] 0001 0010	TMR0	[50] 0001 0010	HLVD_OUT	—	—
[19] 0001 0011	TMR1	[51] 0001 0011	CLC1	—	—
[20] 0001 0100	TMR2	[52] 0001 0100	CLC2	—	—
[21] 0001 0101	TMR3	[53] 0001 0101	CLC3	—	—
[22] 0001 0110	TMR4	[54] 0001 0110	CLC4	—	—
[23] 0001 0111	TMR5	[55] 0001 0111	CLC5	—	—
[24] 0001 1000	TMR6	[56] 0001 1000	CLC6	—	—
[25] 0001 1001	—	[57] 0001 1001	CLC7	—	—
[26] 0001 1010	—	[58] 0001 1010	CLC8	—	—
[27] 0001 1011	—	[59] 0001 1011	U1TX	—	—
[28] 0001 1100	—	[60] 0001 1100	U2TX	—	—
[29] 0001 1101	—	[61] 0001 1101	U3TX	—	—
[30] 0001 1110	SMT1	[62] 0001 1110	U4TX	—	—
[31] 0001 1111	CCP1	[63] 0001 1111	U5TX	[127] 0111 1111	—

Note:  
1. Requests clock.

Reset States: POR/BOR = xxxxxxxx  
All Other Resets = uuuuuuuu

## Detalle de registros para el CLC:

- CLCnGLSx es el registro donde se selecciona qué señales van a ingresar al sector de puerta, tener en cuenta que hay la opción de ingreso invertido o no invertido.

**22.8.8 CLCnGLS0**

Name: CLCnGLS0  
Address: 0x0DC

CLCn Gate1 Logic Select Register

Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	x	x	x	x	x	x	x	x

Bits 1, 3, 5, 7 - G1DyT dyT: Gate1 Data 'Y' True (noninverted)  
Reset States: POR/BOR = xxxx  
All Other Resets = uuuu

Value:

Bits 0, 2, 4, 6 - G1DyN dyN: Gate1 Data 'Y' Negated (inverted)  
Reset States: POR/BOR = xxxx  
All Other Resets = uuuu

Value:

**22.8.9 CLCnGLS1**

Name: CLCnGLS1  
Address: 0x0DD

CLCn Gate2 Logic Select Register

Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	x	x	x	x	x	x	x	x

Bits 1, 3, 5, 7 - G2DyT dyT: Gate2 Data 'Y' True (noninverted)  
Reset States: POR/BOR = xxxx  
All Other Resets = uuuu

Value:

Bits 0, 2, 4, 6 - G2DyN dyN: Gate2 Data 'Y' Negated (inverted)  
Reset States: POR/BOR = xxxx  
All Other Resets = uuuu

Value:

**22.8.10 CLCnGLS2**

Name: CLCnGLS2  
Address: 0x0DE

CLCn Gate3 Logic Select Register

Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	x	x	x	x	x	x	x	x

Bits 1, 3, 5, 7 - G3DyT dyT: Gate3 Data 'Y' True (noninverted)  
Reset States: POR/BOR = xxxx  
All Other Resets = uuuu

Value:

Bits 0, 2, 4, 6 - G3DyN dyN: Gate3 Data 'Y' Negated (inverted)  
Reset States: POR/BOR = xxxx  
All Other Resets = uuuu

Value:

**22.8.11 CLCnGLS3**

Name: CLCnGLS3  
Address: 0x0DF

CLCn Gate4 Logic Select Register

Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	x	x	x	x	x	x	x	x

Bits 1, 3, 5, 7 - G4DyT dyT: Gate4 Data 'Y' True (noninverted)  
Reset States: POR/BOR = xxxx  
All Other Resets = uuuu

Value:

Bits 0, 2, 4, 6 - G4DyN dyN: Gate4 Data 'Y' Negated (inverted)  
Reset States: POR/BOR = xxxx  
All Other Resets = uuuu

Value:

## Detalle de registros para el CLC:

- CLCDATA contiene una copia de las señales de salida de cada CLC

**22.8.12 CLCDATA** Logic Cell

**Name:** CLCDATA  
**Address:** 0x0D4

CLC Data Output Register  
 Mirror copy of CLC outputs

Bit	7	6	5	4	3	2	1	0
	CLC8OUT	CLC7OUT	CLC6OUT	CLC5OUT	CLC4OUT	CLC3OUT	CLC2OUT	CLC1OUT
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

**Bits 0, 1, 2, 3, 4, 5, 6, 7 - CLCxOUT** Mirror copy of CLCx\_out

Value	Description
1	CLCx_out is 1
0	CLCx_out is 0

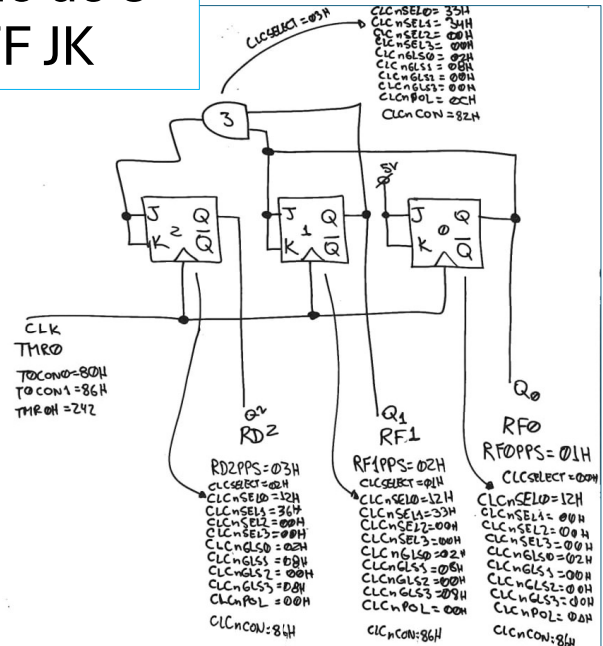
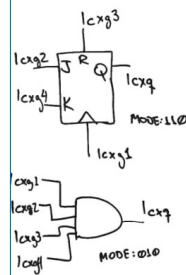
## Referencias sobre uso de CLC

- Microchip TB3273 - Getting Started with CLC on PIC18:  
<https://ww1.microchip.com/downloads/aemDocuments/documents/MCU08/ApplicationNotes/ApplicationNotes/Getting-Started-With-CLC-on-PIC18-90003273A.pdf>
- Microchip AN2912 - Using CLCs in Real-Time Applications:  
[https://ww1.microchip.com/downloads/en/AppNotes/AN2912-Using-CLCs-in-Real-Time-Apps\\_00002912A.pdf](https://ww1.microchip.com/downloads/en/AppNotes/AN2912-Using-CLCs-in-Real-Time-Apps_00002912A.pdf)
- Microchip DS40002188A - Configurable Logic Cell (CLC) Tips and Tricks:  
<https://ww1.microchip.com/downloads/en/DeviceDoc/40002188A.pdf>



## Ejemplo: Contador síncrono de 3 bits e implementado con FF JK

- Análisis y conexiones entre CLCs



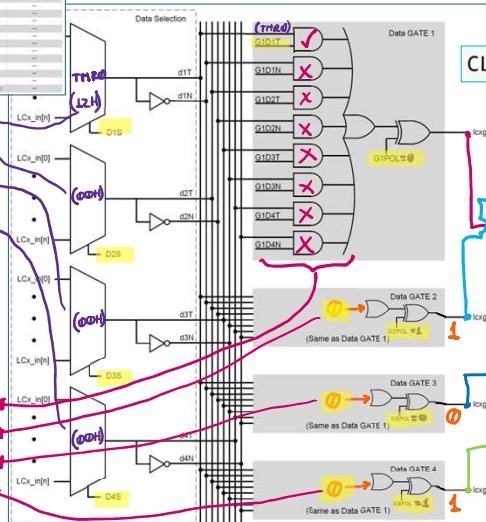
## Ejemplo: Contador síncrono de 3 bits e implementado con FF JK

CLCSELECT = 00H

- Configuración de la CLC1 para el FFJK Q0 (menos significativo)

CLCnSEL0 = 12H  
CLCnSEL1 = 00H  
CLCnSEL2 = 00H  
CLCnSEL3 = 00H

CLCnGLS0 = 02H  
CLCnGLS1 = 00H  
CLCnGLS2 = 00H  
CLCnGLS3 = 00H



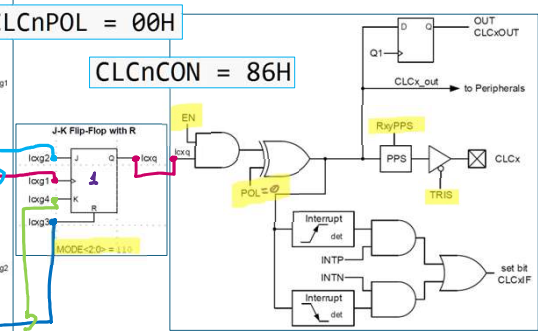
CLCnPOL = 0AH

CLCnCON = 86H

- Señal lcxg1 (reloj del FF) proviene de TMRO
- Se requieren constantes para lcxg2, lcxg3 y lcxg4, para lo cual sus respectivos CLCnGLSx estarán deshabilitados enviando 0 lógico.
- Para lcxg2 y lcxg4 que requieren 1 lógico, se procederá a invertir dichas señales con el registro CLCnPOL

- Configuración de la CLC2 para el FFJK Q1

CLCnCON = 86H

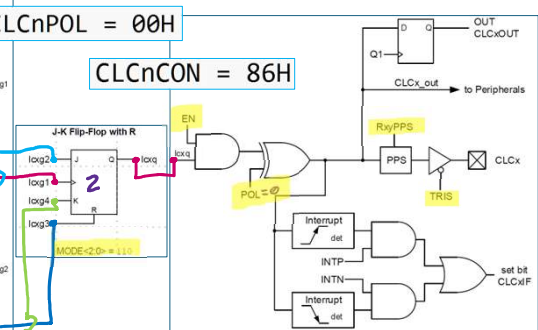


- Señal  $lcxg1$  (reloj del FF) proviene de TMR0.
- Señal  $lcxg3$  permanecerá en cero.
- Señales  $lcxg2$  (entrada J del FF) y  $lcxg4$  (entrada K del FF) provienen de la salida del FF anterior (CLC1).

[illegible]

- Configuración de la CLC3 para el FFJK Q2 (mas significativo)

CLCnCON = 86H



- Señal *lcxg1* (reloj del FF) proviene de TMR0.
- Señal *lcxg3* permanecerá en cero.
- Señales *lcxg2* (entrada J del FF) y *lcxg4* (entrada K del FF) provienen de la salida del CLC4 (la compuerta AND).



### Ejemplo: Contador síncrono de 3 bits e implementado con FF JK

**CLCSELECT = 03H**

- Configuración de la CLC4 para la AND4 (combinatoria para las entradas J y K del tercer FFJK)

**CLCnPOL = 0CH**

**CLCnCON = 82H**

**CLCnSEL0 = 33H**  
**CLCnSEL1 = 34H**  
**CLCnSEL2 = 00H**  
**CLCnSEL3 = 00H**

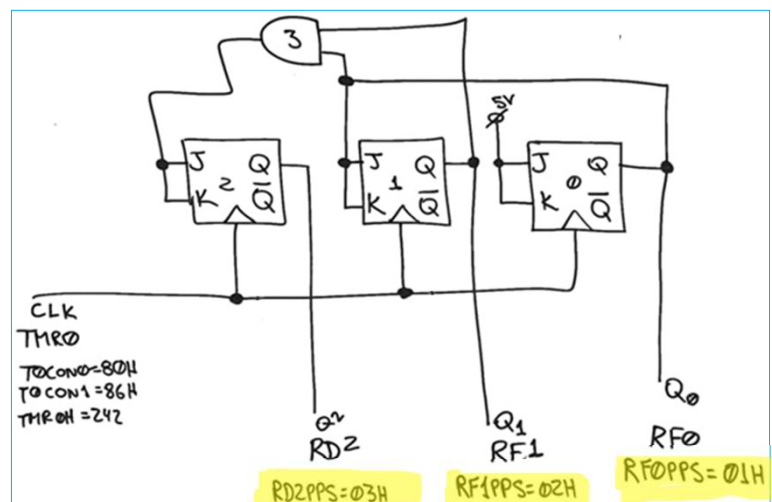
**CLCnGLS0 = 02H**  
**CLCnGLS1 = 08H**  
**CLCnGLS2 = 00H**  
**CLCnGLS3 = 00H**

Señal  $lcxg1$  proviene de CLC1 mientras que  $lcxg2$  proviene de CLC2.

Como solo se están empleando dos entradas para la función lógica AND4,  $lcxg3$  y  $lcxg4$  tendrán valor uno lógico usando el CLCnPOL.

### Ejemplo: Contador síncrono de 3 bits e implementado con FF JK

- Configuración de PPS para las salidas del contador (salidas de los FFs)
- La configuración del reloj del contador es el Timer0 que está temporizando 500ms (modo 8bit, fuente LFINTOSC, presc 1:64, posts 1:1, sync, TMR0H=242)





## Ejemplo: Contador síncrono de 3 bits e implementado con FF JK

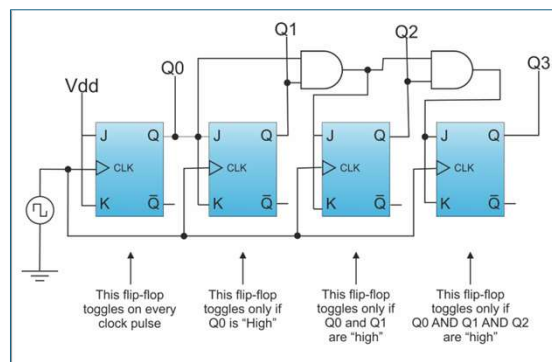
```

1  PROCESSOR 18F57Q43
2  #include "cabecera.inc"
3
4  PSECT upecenos, class=CODE, reloc=2, abs
5
6  upecenos:
7  ORG 000000H
8  bra configur0
9
10 ORG 000200H
11
12 configur0:
13 ;conf modulo de oscilador
14 movlb 08H
15 movlb 60H
16 movwf OSCCON1, 1
17 movlb 02H
18 movwf OSCFRQ, 1
19 movlb 50H
20 movwf OSCEN, 1 ;HFINTOSC & LFINTOSC enabled
21 ;conf del CLC1
22 movlb 00H
23 movwf CLCSELECT, 1 ;CLC1 seleccionado
24 movlb 0AH
25 movwf CLCnPOL, 1 ;invertido para GATE2 y GATE4
26 movlb 12H
27 movwf CLCnSEL0, 1 ;D1S=THR0
28 clrf CLCnSEL1, 1 ;D2S no usado
29 clrf CLCnSEL2, 1 ;D3S no usado
30 clrf CLCnSEL3, 1 ;D4S no usado
31 movlb 02H
32 movwf CLCnGLS0, 1 ;GATE1 con G1D1T
33 clrf CLCnGLS1, 1 ;GATE2 en cero
34 clrf CLCnGLS2, 1 ;GATE3 en cero
35 clrf CLCnGLS3, 1 ;GATE4 en cero
36 movlb 86H
37 movwf CLCnCON, 1 ;CLC1 enabled, FFJK mode
38 ;conf del CLC2
39 movlb 01H
40 movwf CLCSELECT, 1 ;CLC2 seleccionado
41 clrf CLCnPOL, 1 ;sin negar
42 movlb 12H
43 movwf CLCnSEL0, 1 ;D1S=THR0
44 movlb 33H
45 movwf CLCnSEL1, 1 ;D2S=CLC1
46 clrf CLCnSEL2, 1 ;D3S no usado
47 clrf CLCnSEL3, 1 ;D4S no usado
48 movlb 02H
49 movwf CLCnGLS0, 1 ;GATE1 con G1D1T
50 movlb 08H
51 movwf CLCnGLS1, 1 ;GATE2 con G2D2T
52 clrf CLCnGLS2, 1 ;GATE3 en cero
53 clrf CLCnGLS3, 1 ;GATE4 en cero
54 movlb 86H
55 movwf CLCnCON, 1 ;CLC2 enabled, FFJK mode
56 ;conf del CLC3
57 movlb 02H
58 movwf CLCSELECT, 1 ;CLC3 seleccionado
59 clrf CLCnPOL, 1 ;sin negar
60 movlb 12H
61 movwf CLCnSEL0, 1 ;D1S=THR0
62 movlb 36H
63 movwf CLCnSEL1, 1 ;D2S=CLC4
64 clrf CLCnSEL2, 1 ;D3S no usado
65 clrf CLCnSEL3, 1 ;D4S no usado
66 movlb 02H
67 movwf CLCnGLS0, 1 ;GATE1 con G1D1T
68 movlb 08H
69 movwf CLCnGLS1, 1 ;GATE2 con G2D2T
70 clrf CLCnGLS2, 1 ;GATE3 en cero
71 movlb 08H
72 movwf CLCnGLS3, 1 ;GATE4 con G2D2T
73 clrf CLCnDATA, 1
74 movlb 86H
75 movwf CLCnCON, 1 ;CLC3 enabled, FFJK mode
76 ;conf del CLC4
77 movlb 03H
78 movwf CLCSELECT, 1 ;CLC4 seleccionado
79 movlb 0CH
80 movwf CLCnPOL, 1 ;negados GATE3 y GATE4
81 movlb 33H
82 movwf CLCnSEL0, 1 ;D1S=CLC1
83 movlb 34H
84 movwf CLCnSEL1, 1 ;D2S=CLC2
85 clrf CLCnSEL2, 1 ;D3S no usado
86
87 clrf CLCnSEL3, 1 ;D4S no usado
88 movlb 02H
89 movwf CLCnGLS0, 1 ;GATE1 con G1D1T
90 movlb 08H
91 movwf CLCnGLS1, 1 ;GATE2 con G2D2T
92 clrf CLCnGLS2, 1 ;GATE3 en cero
93 clrf CLCnGLS3, 1 ;GATE4 en cero
94 clrf CLCnDATA, 1
95 movlb 82H
96 movwf CLCnCON, 1 ;CLC4 enabled, AND4 mode
97 ;conf del PPS
98 movlb 28H
99 movlb 39H
100 movwf RC5PPS, 1 ;RC5 conectado a THR0
101 movlb 01H
102 movwf RF0PPS, 1 ;RF0 conectado a CLC1
103 movlb 02H
104 movwf RF1PPS, 1 ;RF1 conectado a CLC2
105 movlb 03H
106 movwf RD2PPS, 1 ;RD2 conectado a CLC3
107 ;conf del THR0
108 movlb 3H
109 movlb 80H
110 movwf TOCON0, 1 ;THR0 enabled, 8bit mode, post
111 movlb 86H
112 movwf TOCON1, 1 ;clksrc = LFINTOSC, sync, pres
113 movlb 242
114 movwf THROH, 1 ;valor de ref de comp 250
115 ;conf E/S
116 movlb 4H
117 bcf TRISC, 5, 1 ;RC5 como salida
118 bcf ANSEL0, 5, 1 ;RC5 como digital
119 movlb 0FCH
120 movwf TRISF, 1 ;RF0 y RF1 como salidas
121 movwf ANSEL1, 1 ;RF0 y RF1 como digitales
122 bcf TRISD, 2, 1 ;RD2 como salida
123 bcf ANSEL0, 2, 1 ;RD2 como digital
124
125 inicio:
126 bra inicio
127
128 end upecenos

```

## Ejemplo: Contador síncrono de 4 bits e implementado con FF JK

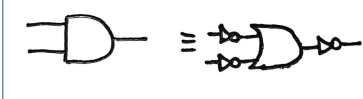
- Aumentando la resolución del contador anterior a 4 bits se tiene el siguiente circuito lógico digital:



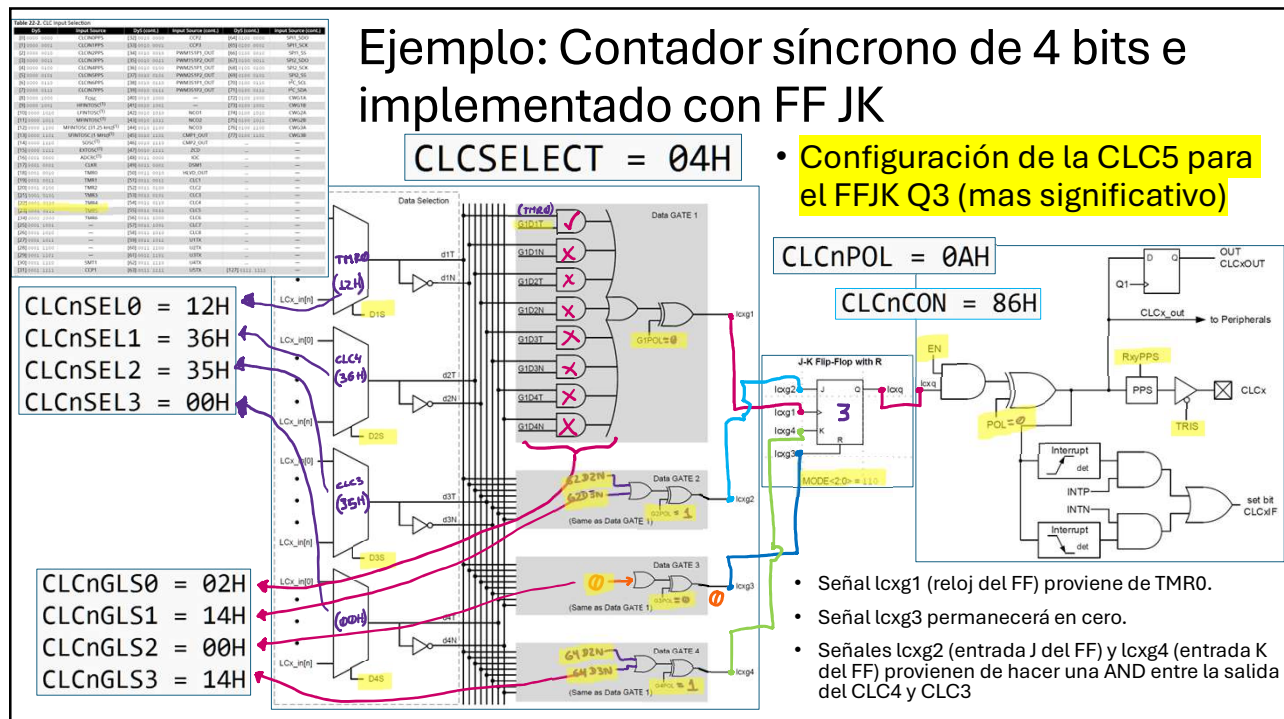
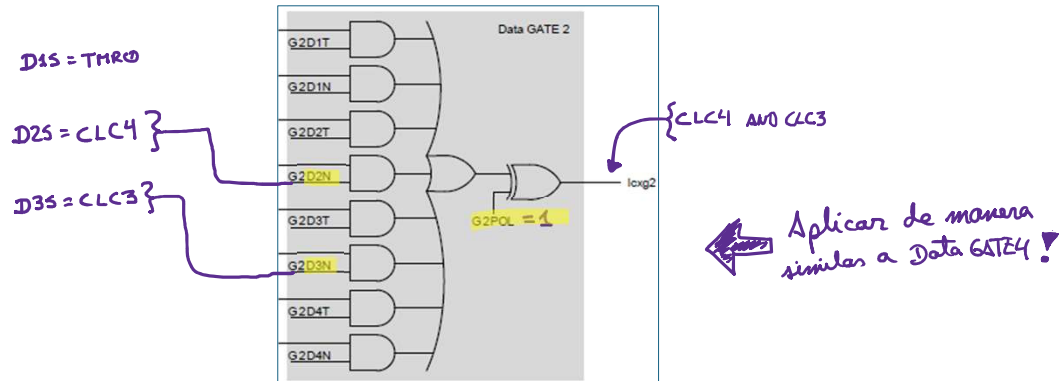
- Basta añadir un flip flop JK adicional para el dígito mas significativo y una compuerta AND

## Ejemplo: Contador síncrono de 4 bits e implementado con FF JK

- Recordando Demorgan:



- Para implementar la compuerta AND se usarán las entradas negadas y salida invertida en el GATE 2 y 4 (entradas J y K del FFJK)



## Ejemplo: Contador síncrono de 4 bits e implementado con FF JK

- Configuración del CLC5:

```
;conf del CLC5
movlw 04H
movwf CLCSELECT, 1 ;CLC4 seleccionado
movlw 0AH
movwf CLCnPOL, 1 ;Negados G2 y G4
movlw 12H
movwf CLCnSEL0, 1 ;D1S=TMR0
movlw 36H
movwf CLCnSEL1, 1 ;D2S=CLC4
movlw 35H
movwf CLCnSEL2, 1 ;D3S=CLC3
clrf CLCnSEL3, 1 ;D4S no usado
movlw 02H
movwf CLCnGLS0, 1 ;GATE1 con G1D1T
movlw 14H
movwf CLCnGLS1, 1 ;GATE2 con G2D2N AND G2D3N
clrf CLCnGLS2, 1 ;GATE3 en cero
movlw 14H
movwf CLCnGLS3, 1 ;GATE4 con G4D2N AND G4D3N
clrf CLCDATA, 1
movlw 86H
movwf CLCnCON, 1 ;CLC5 enabled, FFJK mode
```

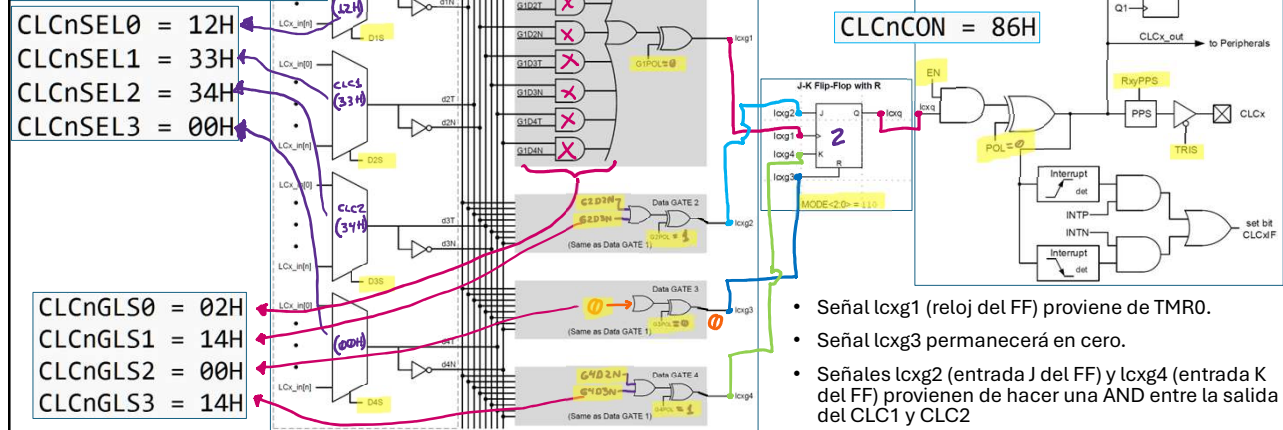
## Ejemplo: Contador síncrono de 4 bits e implementado con FF JK

- Como propuesta de mejora, se puede obviar el uso de la CLC4 con la configuración vista en CLC5 (armar la AND usando las entradas del Data GATE) y aplicarla en CLC3.
- El detalle de la configuración se muestra a continuación:

CLCSELECT = 02H

- CLCnPOL = 0AH

CLCnCON = 86H



- Señal  $lcxg1$  (reloj del FF) proviene de TMR0.
- Señal  $lcxg3$  permanecerá en cero.
- Señales  $lcxg2$  (entrada J del FF) y  $lcxg4$  (entrada K del FF) provienen de hacer una AND entre la salida del CLC1 y CLC2

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