**190905514**  **MOHAMMAD TOFIK**

**WEEK 7 LAB 7 :**

1. Design and simulate the following counters
2. 4 bit synchronous up counter

**module fourbitup(clk,rstn,out);**

**input clk;**

**input rstn;**

**output [3:0] out;**

**reg [3:0] out;**

**always @ (posedge clk) begin**

**if (! rstn)**

**out <= 0;**

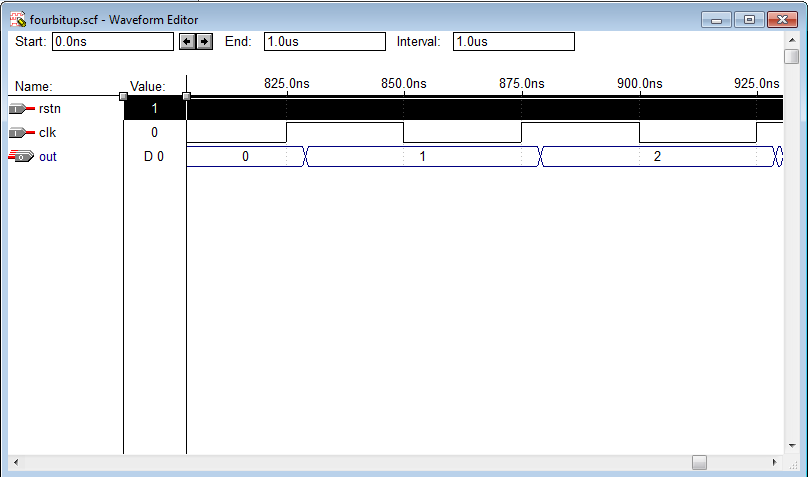
**else**

**out <= out + 1;**

**end**

**endmodule**

**OUTPUT :**

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**1.(b)** 3 bit synchronous up/down counter with a control input up/𝑑𝑜𝑤𝑛.

If up/𝑑𝑜𝑤𝑛 = 1, then the circuit should behave as an up counter. If up/𝑑𝑜𝑤𝑛= 0, then the circuit should behave as a down counter.

**module threebit(Clock, updown, resetn, c);**

**input Clock, resetn, updown;**

**output [2:0]c;**

**reg [2:0]c;**

**always @(posedge Clock)**

**begin**

**if(!resetn)**

**c <= 0;**

**else**

**begin**

**if(updown)**

**c <= c+1;**

**else**

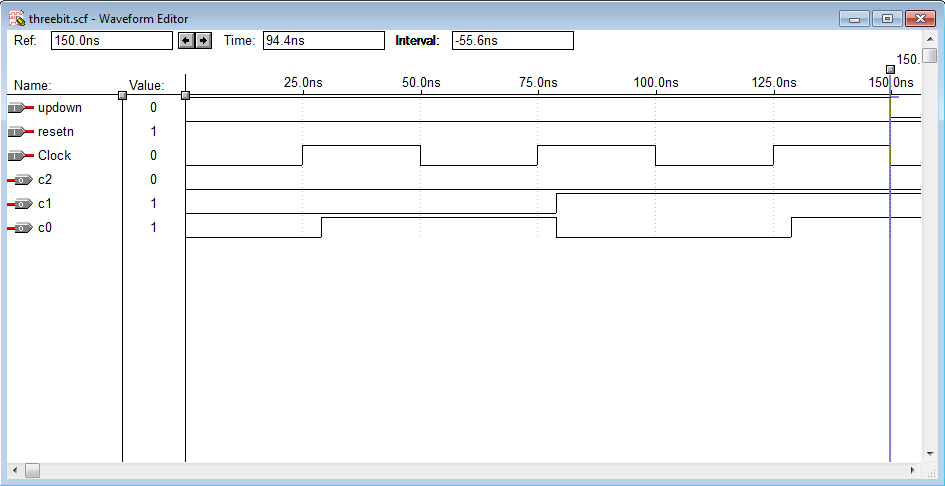
**c <=c-1;**

**end**

**end**

**endmodule**

**OUTPUT :**

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