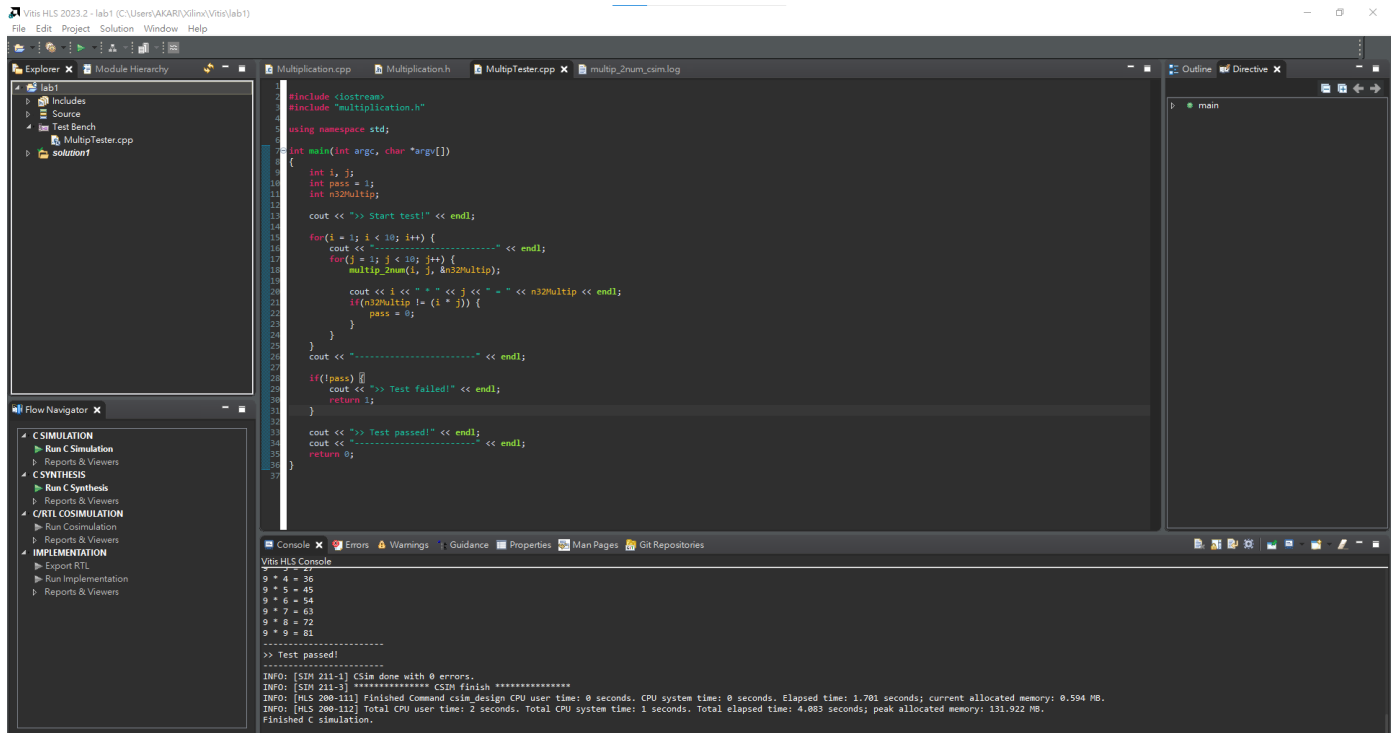
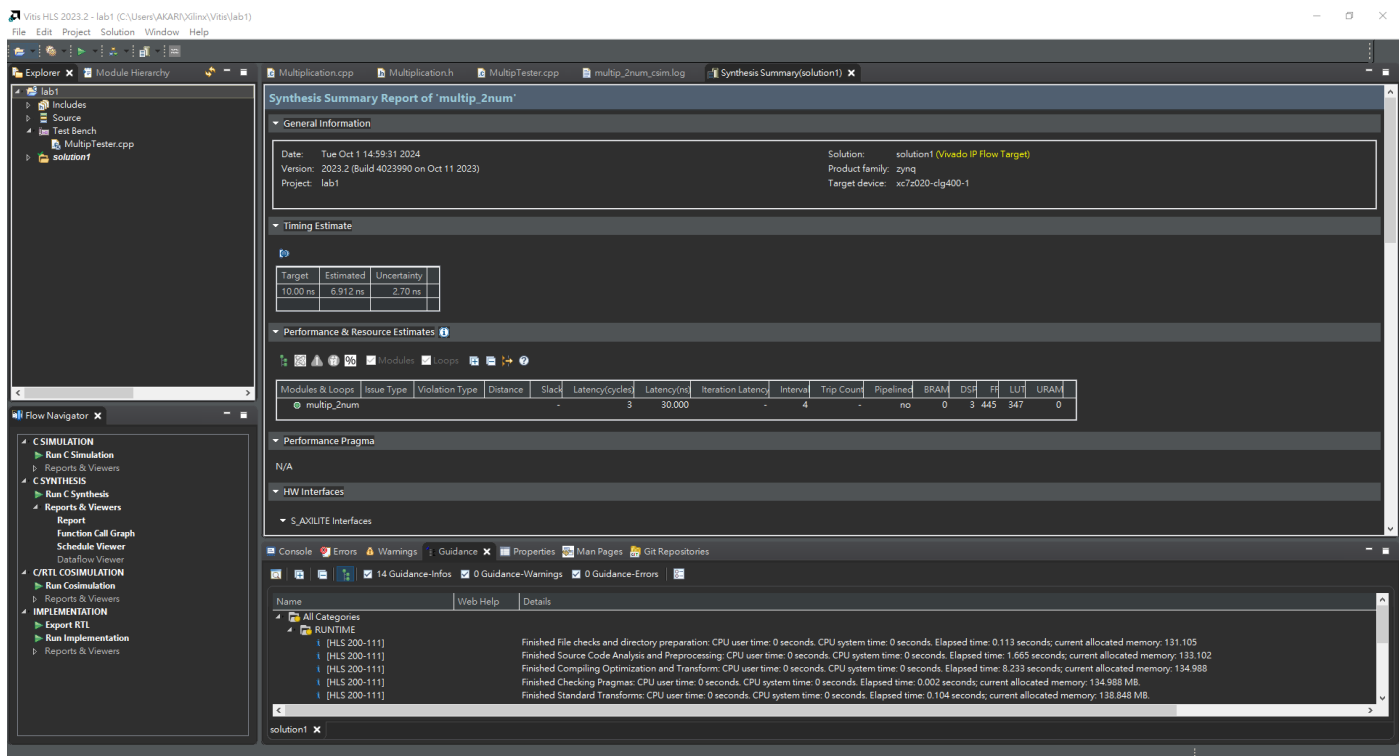


# Lab1

## 1. Simulation result



## 2. Synthesis Summary



HW Interfaces

S\_AXI4LITE Interfaces

Interface	Data Width	Address Width	Offset	Register
s_axi_control	32	6	16	0
s_axi_n32In1	32	4		

S\_AXI4LITE Registers

Interface	Register	Offset	Width	Access	Description	Bit Fields
s_axi_control	n32In1	0x10	32	W	Data signal of n32In1	
s_axi_control	n32In2	0x18	32	W	Data signal of n32In2	
s_axi_control	pn32ResOut	0x20	32	R	Data signal of pn32ResOut	
s_axi_control	pn32ResOut_ctrl	0x24	32	R	Control signal of pn32ResOut	0=pn32ResOut_ap_vld

TOP LEVEL CONTROL

Interface	Type	Ports
ap_clk	clock	ap_clk
ap_rst_n	reset	ap_rst_n
ap_ctrl	ap_ctrl_none	

Synthesis Summary Report of 'multip\_2num'

General Information

Date: Tue Oct 1 14:59:31 2024

Version: 2023.2 (Build 4023990 on Oct 11 2023)

Project: lab1

Solution: solution1 (Vivado IP Flow Target)

Product family: zynq

Target device: xc7z020-clg400-1

Timing Estimate

Target	Estimated	Uncertainty
10.00 ns	6.912 ns	2.70 ns

Performance & Resource Estimates

Modules & Loops

Modules & Loops	Issue Type	Violation Type	Distance	Slack	Latency(cycles)	Latency(ns)	Iteration Latency	Interval	Trip Count	Pipelined	BRAM	DSF	FF	LUT	URAM	
● multip_2num				-	3	30.000		-	4	-	no	0	3	445	347	0

Performance Pragma

N/A

SW I/O Information

Top Function Arguments

Argument	Direction	Datatype
n32In1	in	int
n32In2	in	int
pn32ResOut	out	int*

SW-to-HW Mapping

Argument	HW Interface	HW Type	HW Info
n32In1	s_axi_control	register	name=n32In1 offset=0x10 range=32
n32In2	s_axi_control	register	name=n32In2 offset=0x18 range=32
pn32ResOut	s_axi_control	register	name=pn32ResOut offset=0x20 range=32
pn32ResOut	s_axi_control	register	name=pn32ResOut_ctrl offset=0x24 range=32

Pragma Report

Valid Pragma Syntax

Bind Op Report

No filter settings

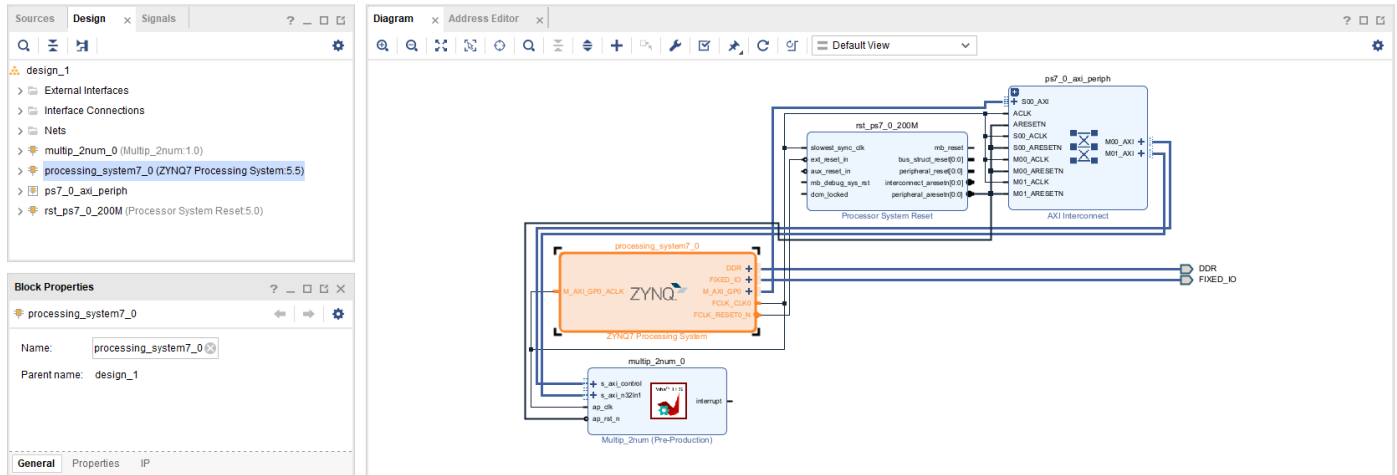
Name	DSF	Pragma	Variable	Op	Imp	Latency
● multip_2num	3					
mul_32x_32x_32_1_U1	3		mul_in11	mul	auto	1

No user config\_op information

Storage Report

No bind storage, config\_storage information

### 3. Interface



### 4. Co-simulation

Cosimulation Report for 'multip\_2num'

General Information

Date: Tue Oct 1 15:03:06 2024  
Version: 2023.2 (Build 4023990 on Oct 11 2023)  
Project: lab1  
Status: Pass

Solution: solution1 (Vivado IP Flow Target)  
Product family: zynq  
Target device: xc7z020-clg400-1

Cosim Options

Tool: Vivado XSIM  
RTL: Verilog

Performance Estimates

Modules & Loops	Avg II	Max II	Min II	Avg Latency	Max Latency	Min Latency	Total Execution Time
● multip_2num	35	41	35	3	3	3	2885

### 5.

