Lab2

1. FIRN11MAXI

1. Simulation result

```
INFO: [SIM 2] *************** CSIM start ***************
INFO: [SIM 4] CSIM will launch GCC as the compiler.
   Compiling ../../../FIRTester.cpp in debug mode
   Compiling ../../../FIR.cpp in debug mode
   Generating csim.exe
>> Start test!
>> Comparing against output data...
正在比較檔案 .\out.dat 和 ..\..\..\OUT_GOLD.DAT
FC: 找不到相異處

>> Test passed!
-------------------------
INFO: [SIM 1] CSim done with 0 errors.
INFO: [SIM 3] *************** CSIM finish ***************

```

2. Synthesis Summary

Synthesis Summary Report of 'fir_n11_maxi'

General Information

Date: Wed Oct 2 23:47:17 2024
Version: 2023.2 (Build 4023990 on Oct 11 2023)
Project: lab2_1
Solution: solution1 (Vivado IP Flow Target)
Product family: zynq
Target device: xc7z020-clg400-1

Timing Estimate

Target	Estimated	Uncertainty
10.00 ns	7.300 ns	2.70 ns

Performance & Resource Estimates

Modules Loops

Modules & Loops	Issue Type	Violation Type	Distance	Slack	Latency(cycles)	Latency(ns)	Iteration Latency	Interval	Trip Count	Pipelined	BRAM	DSP	FF	LUT	URAM
fir_n11_maxi				-	-	-	-	-	-	no	4	33	4622	2606	0
fir_n11_maxi_Pipeline_XFER_LOOP				-	-	-	-	-	-	no	0	33	2973	1221	0
XFER_LOOP				-	-	-	20	1	-	yes	-	-	-	-	-

Performance Pragma

N/A

HW Interfaces

M_AXI

Interface	Data Width (SW->HW)	Address Width	Latency	Offset	Register	Max Widen Bitwidth	Max Read Burst Length	Max Write Burst Length	Num Read Outstanding	Num Write Outstanding	Resource Estimate
m_axi_gmem	32 -> 32	64	0	slave	0	0	16	16	16	16	BRAM=4

S_AXILITE Interfaces

Interface	Data Width	Address Width	Offset	Register
s_axi_control	32	7	16	0

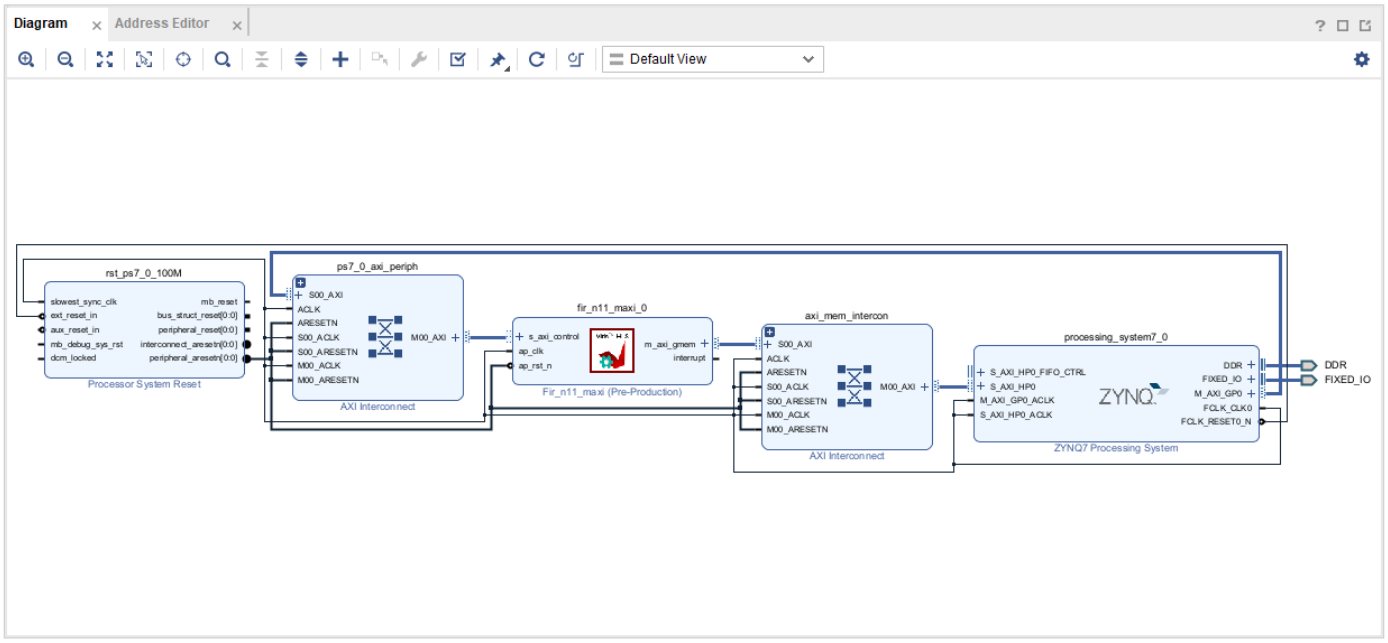
S_AXILITE Registers

Interface	Register	Offset	Width	Access	Description	Bit Fields
s_axi_control	CTRL	0x00	32	RW	Control signals	0=AP_START 1=AP_DONE 2=AP_IDLE 3=AP_READY 7=AUTO_RESTART 9=INTERRUPT
s_axi_control	GIER	0x04	32	RW	Global Interrupt Enable Register	0=Enable
s_axi_control	IP_IER	0x08	32	RW	IP Interrupt Enable Register	0=CHAN0_INT_EN 1=CHAN1_INT_EN
s_axi_control	IP_ISR	0x0c	32	RW	IP Interrupt Status Register	0=CHAN0_INT_ST 1=CHAN1_INT_ST
s_axi_control	pn32HPInput_1	0x10	32	W	Data signal of pn32HPInput	
s_axi_control	pn32HPInput_2	0x14	32	W	Data signal of pn32HPInput	
s_axi_control	pn32HPOutput_1	0x1c	32	W	Data signal of pn32HPOutput	
s_axi_control	pn32HPOutput_2	0x20	32	W	Data signal of pn32HPOutput	
s_axi_control	regXferLeng	0x28	32	W	Data signal of regXferLeng	

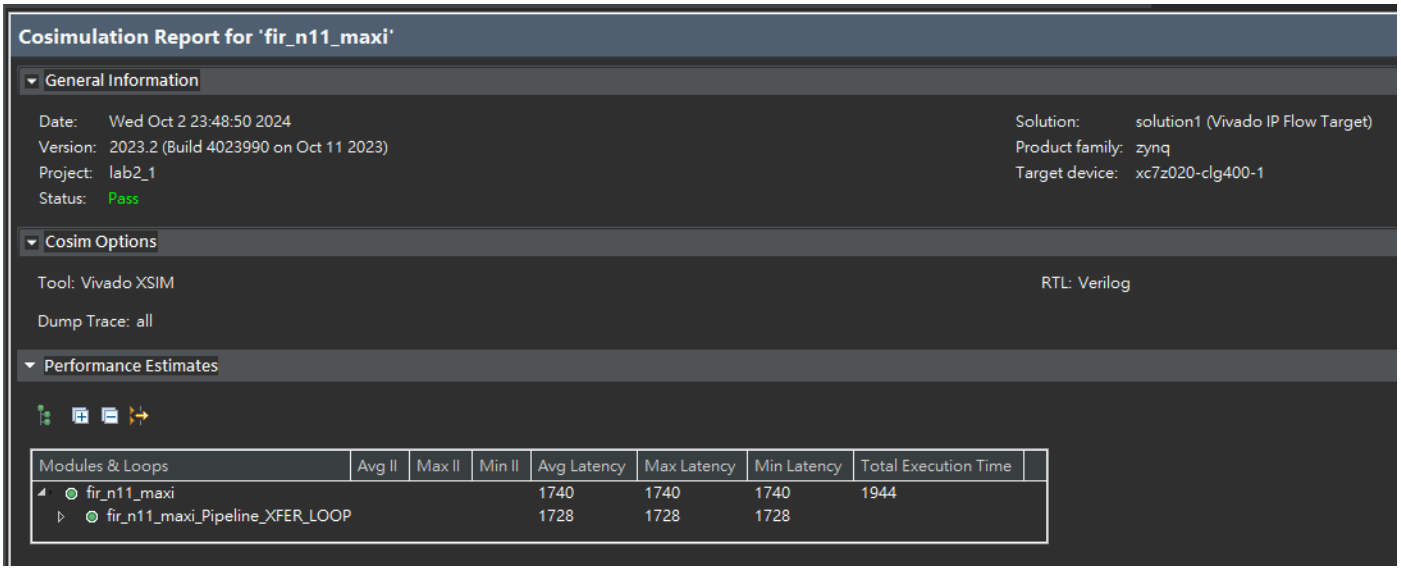
TOP LEVEL CONTROL

Interface	Type	Ports
ap_clk	clock	ap_clk
ap_rst_n	reset	ap_rst_n
interrupt	interrupt	interrupt
ap_ctrl	ap_ctrl_hs	

3. Interface



4. Co-simulation



Cosimulation Report for 'fir_n11_maxi'

General Information

Date: Wed Oct 2 23:48:50 2024
Version: 2023.2 (Build 4023990 on Oct 11 2023)
Project: lab2_1
Status: Pass

Solution: solution1 (Vivado IP Flow Target)
Product family: zynq
Target device: xc7z020-clg400-1

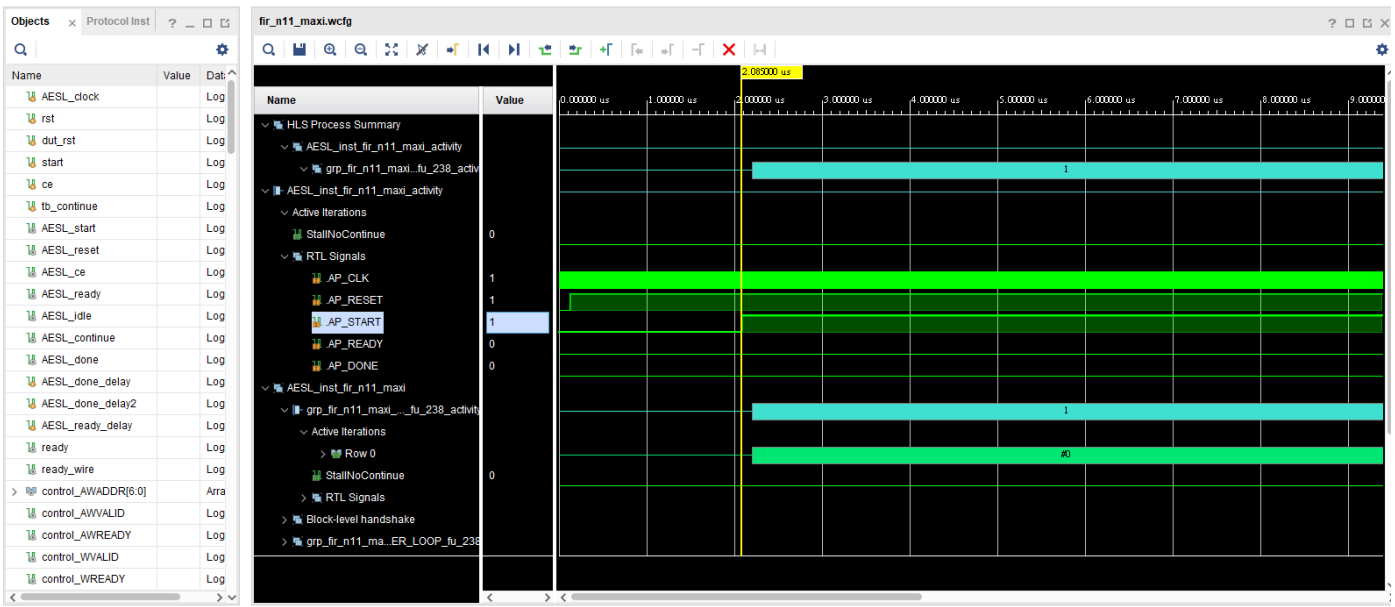
Cosim Options

Tool: Vivado XSIM
RTL: Verilog
Dump Trace: all

Performance Estimates

Modules & Loops	Avg II	Max II	Min II	Avg Latency	Max Latency	Min Latency	Total Execution Time
fir_n11_maxi				1740	1740	1740	1944
fir_n11_maxi_Pipeline_XFER_LOOP				1728	1728	1728	

5. Waveform



2. FIRN11Stream

1. Simulation result

```
INFO: [SIM 2] *************** CSIM start ***************
INFO: [SIM 4] CSIM will launch GCC as the compiler.
   Compiling ../../../FIRTester.cpp in debug mode
   Compiling ../../../FIR.cpp in debug mode
   Generating csim.exe
>> Start test!
>> Comparing against output data...
正在比較檔案 .\out.dat 和 ..\..\..\OUT_GOLD.DAT
FC: 找不到相異處

>> Test passed!
-----------------------
INFO [HLS SIM]: The maximum depth reached by any hls::stream() instance in the design is 600
INFO: [SIM 1] CSim done with 0 errors.
INFO: [SIM 3] *************** CSIM finish ***************

```

2. Synthesis Summary

Synthesis Summary Report of 'fir_n11_strm'

General Information

Date: Thu Oct 3 14:54:32 2024
Version: 2023.2 (Build 4023990 on Oct 11 2023)
Project: lab2_2

Solution: solution1 (Vivado IP Flow Target)
Product family: zynq
Target device: xc7z020-clg400-1

Timing Estimate

Target	Estimated	Uncertainty
10.00 ns	7.936 ns	2.70 ns

Performance & Resource Estimates

Modules & Loops	Issue Type	Violation Type	Distance	Slack	Latency(cycles)	Latency(ns)	Iteration Latency	Interval	Trip Count	Pipelined	BRAM	DSP	FF	LUT	URAM
fir_n11_strm				-0.64	-	-	-	-	-	no	0	3	1162	962	0
fir_n11_strm_Pipeline_XFER_LOOP				-0.64	-	-	-	-	-	no	0	3	972	706	0
XFER_LOOP	II Violation	Resource Limitation			-	-	16	11	-	yes	-	-	-	-	-

Performance Pragma

N/A

HW Interfaces

S_AXILITE Interfaces

Interface	Data Width	Address Width	Offset	Register
s_axi_control	32	7	64	0

S_AXILITE Registers

Interface	Register	Offset	Width	Access	Description	Bit Fields
s_axi_control	CTRL	0x00	32	RW	Control signals	0=AP_START 1=AP_DONE 2=AP_IDLE 3=AP_READY 7=AUTO_RESTART 9=INTERRUPT
s_axi_control	GIER	0x04	32	RW	Global Interrupt Enable Register	0=Enable
s_axi_control	IP_IER	0x08	32	RW	IP Interrupt Enable Register	0=CHAN0_INT_EN 1=CHAN1_INT_EN
s_axi_control	IP_ISR	0x0c	32	RW	IP Interrupt Status Register	0=CHAN0_INT_ST 1=CHAN1_INT_ST
s_axi_control	regXferLeng	0x10	32	W	Data signal of regXferLeng	

AXIS

Interface	Direction	Register Mode	TDATA	TDEST	TID	TKEEP	TLAST	TREADY	TSTRB	TUSER	TVALID
pstrmInput	in	both	32	1	1	4	1	1	4	1	1
pstrmOutput	out	both	32	1	1	4	1	1	4	1	1

TOP LEVEL CONTROL

Interface	Type	Ports
ap_clk	clock	ap_clk
ap_rst_n	reset	ap_rst_n
interrupt	interrupt	interrupt
ap_ctrl	ap_ctrl_hs	

SW-to-HW Mapping

Argument	HW Interface	HW Type	HW Info
pstrmInput	pstrmInput	interface	
pstrmOutput	pstrmOutput	interface	
an32Coef	s_axi_control	memory	name=an32Coef offset=64 range=64
regXferLeng	s_axi_control	register	name=regXferLeng offset=0x10 range=32

Pragma Report

Valid Pragma Syntax

Bind Op Report

No filter settings

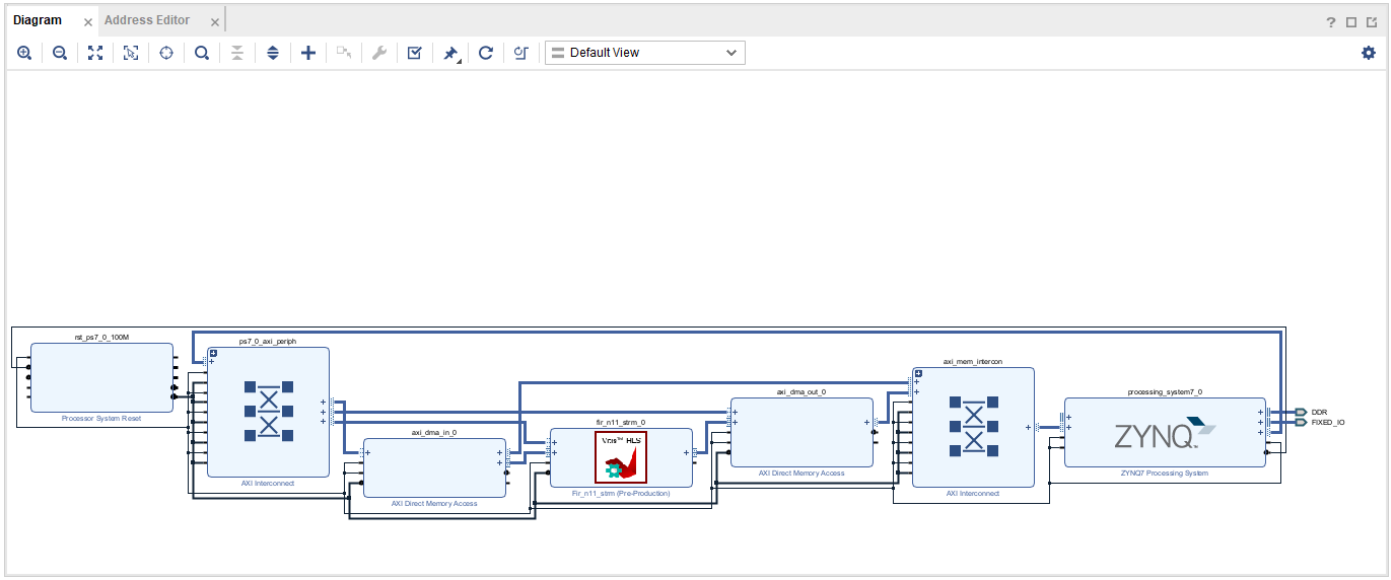
Name	DSP	Pragma	Variable	Op	Impl	Latency
fir_n11_strm	3					
add_ln20_fu_177_p2	-		add_ln20	add	fabric	0
fir_n11_strm_Pipeline_XFER_LOOP	3					

No user config_op information

Storage Report

No bind storage, config_storage information

3. Interface



4. Co-simulation

Cosimulation Report for 'fir_n11_strm'

General Information

Date: Thu Oct 3 14:56:06 2024
Version: 2023.2 (Build 4023990 on Oct 11 2023)
Project: lab2_2
Status: Pass

Solution: solution1 (Vivado IP Flow Target)
Product family: zynq
Target device: xc7z020-clg400-1

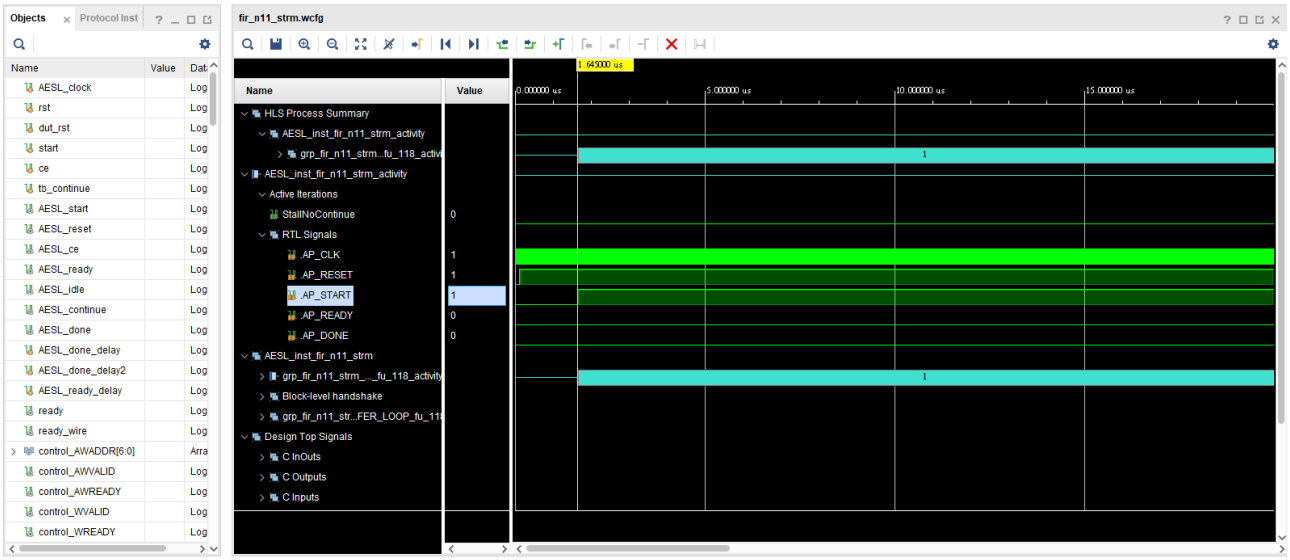
Cosim Options

Tool: Vivado XSIM
RTL: Verilog
Dump Trace: all

Performance Estimates

Modules & Loops	Avg II	Max II	Min II	Avg Latency	Max Latency	Min Latency	Total Execution Time
fir_n11_strm				6607	6607	6607	6768
fir_n11_strm_Pipeline_XFER_LOOP				6604	6604	6604	

5. Waveform


Objects
Protocol Inst
Name
Value
AESL_clock
rst
dut_rst
start
ce
tb_continue
AESL_start
AESL_reset
AESL_ce
AESL_ready
AESL_idle
AESL_continue
AESL_done
AESL_done_delay
AESL_done_delay2
AESL_ready_delay
ready
ready_wire
control_AWADDR[6:0]
control_AWVALID
control_AWREADY
control_WVALID
control_WREADY
fir_n11_strm.wcfg
Name
Value
HLS Process Summary
AESL_inst_fir_n11_strm_activity
AESL_inst_fir_n11_strm_activity
Active Iterations
StallNoContinue
0
RTL Signals
AP_CLK
1
AP_RESET
1
AP_START
1
AP_READY
0
AP_DONE
0
AESL_inst_fir_n11_strm
Block-level handshake
Design Top Signals
C InOuts
C Outputs
C Inputs
1 649000 us
0.000000 us
5.000000 us
10.000000 us
15.000000 us