

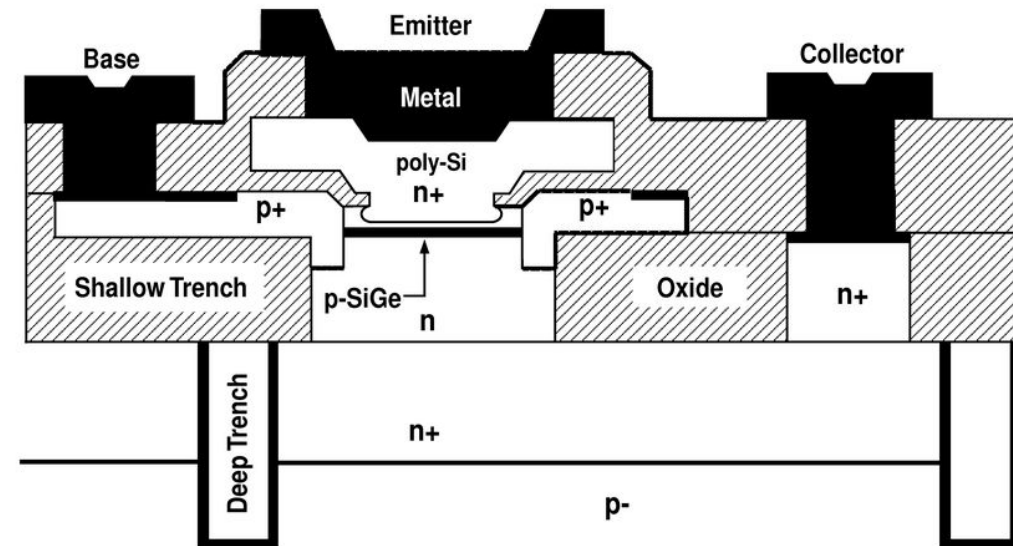
Fabrication of SiGe Heterojunction Bipolar Transistors

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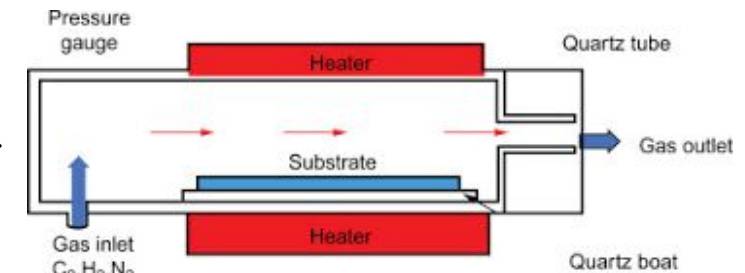
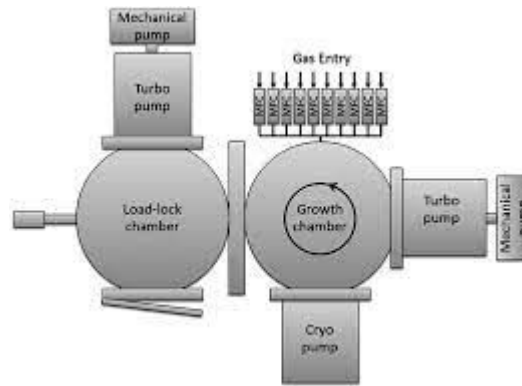
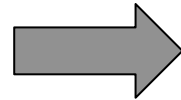
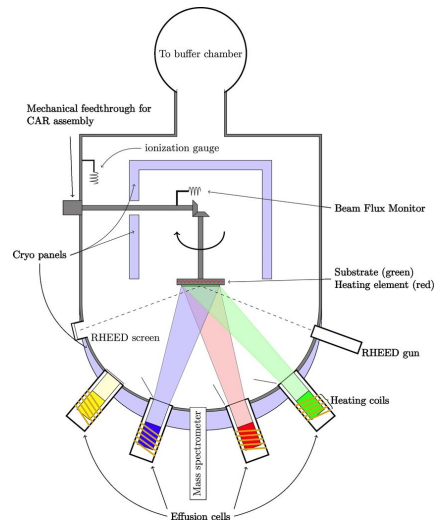
Introduction - What is an HBT?

- Si (N) - SiGe:C (P) - Si (N) bipolar transistor.
 - Allows one to carry out bandgap engineering in Silicon.
- Ge grading allows for variations in bandgap. (III-V like behavior in Si)
- Can integrate with CMOS.
- No more since this is a fab class.



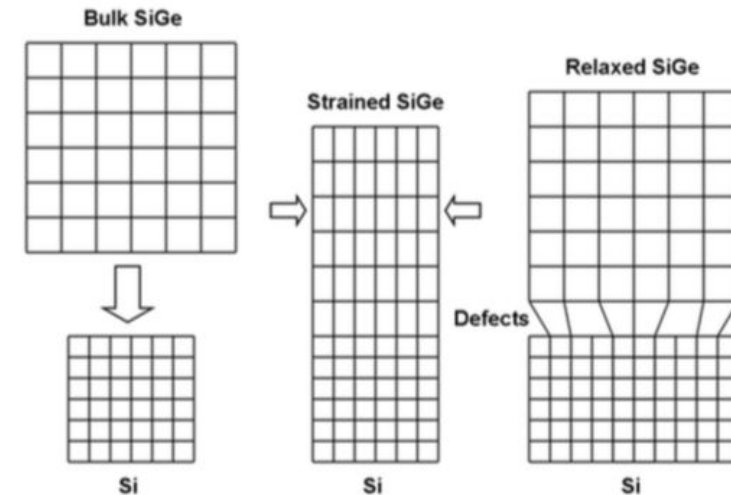
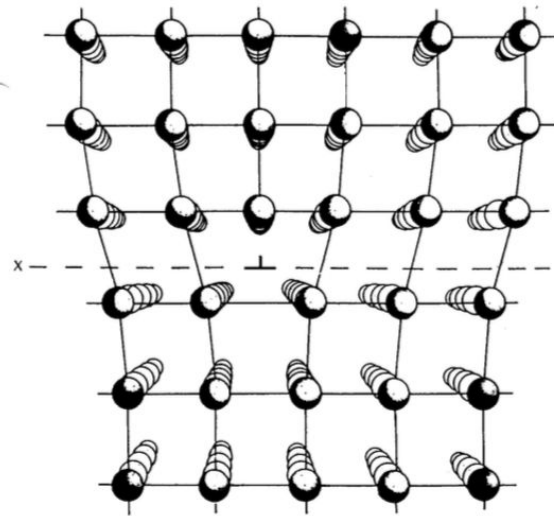
Introduction - History of SiGe Growth

- 1985 - First molecular beam epitaxy grown device (IBM).
- 1987 - First UHV CVD grown device.
- 1990 - First APCVD grown device.
- Noteworthy trend here is epitaxial growth.

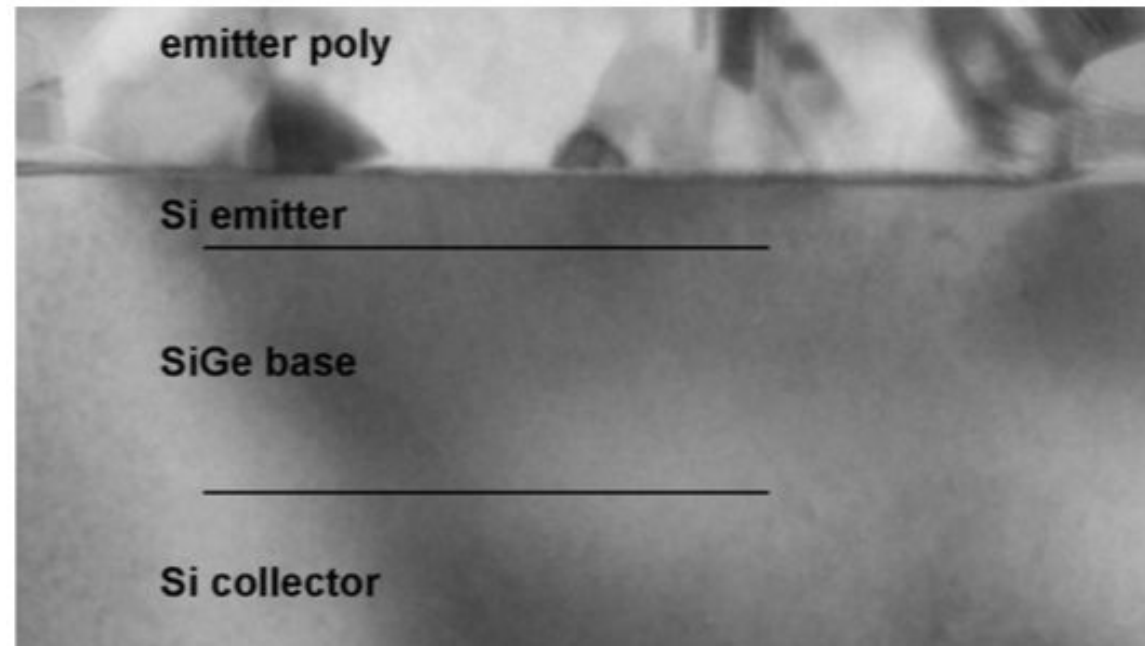


Challenges with SiGe Growth

- Different sized crystals, mismatch in lattice constant.
 - Results in strain being put on interface (hence strained layer epitaxy).
 - Too much strain results in defects.
- Can't use high temperatures ($>600^{\circ}\text{C}$) during SiGe epitaxy.
 - Causes unwanted diffusion or relaxation of strained layer (bad).
 - Polysilicon emitter is on purpose (Increased current gain).



- Utilizes CVD growth for SiGe base layer.
 - Ion implantation for collector (As or P but probably As).
 - In situ doping for the emitter.
 - 4-40 Angstrom/Minute. Control of 1-2 atomic layers across wafer.
- Emitter on top to minimize series resistance/shunt capacitance to the substrate.

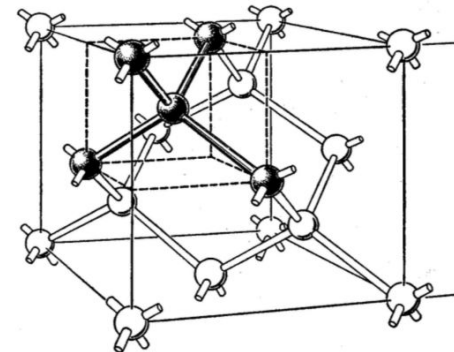
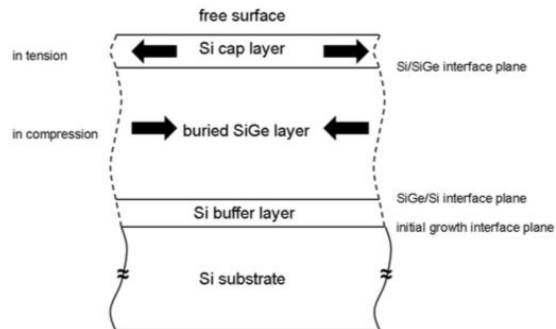


General Growth Process - Wafer Cleansing

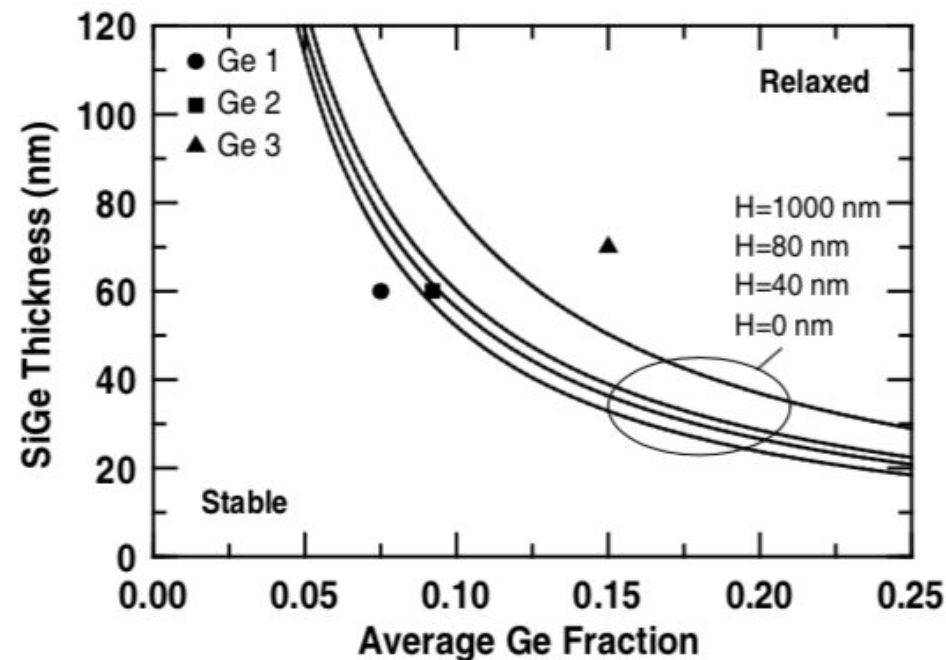
- Need pure wafer for the growth process.
- Can purify in two ways:
 - High heat
 - H₂O/HF cleansing.
- H₂O/HF far better if vacuum is available.
 - Only need about 10 seconds in 10:1 H₂O/HF mixture (compared to minutes at temperature) for low oxide result.
- APCVD uses prebake (10 minutes) and gaseous HCl etch.
- Clean wafer important for epitaxy as well as subsequent doping.

- SiGe layer deposited over clean silicon buffer layer.
 - Performed at 400-500 C, 10^{-6} torr.
 - Utilize GeH₄ in H₂ carrier for Ge.
 - Use SiH₄ for Si. In APCVD, use SiH₂Cl₂.
- Some chemistry happens. SiGe pops up.
- Modern process' most likely use RPCVD (reduced pressure) in order to experiment with pressure profile.

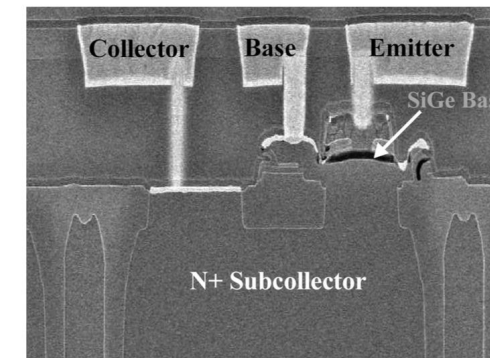
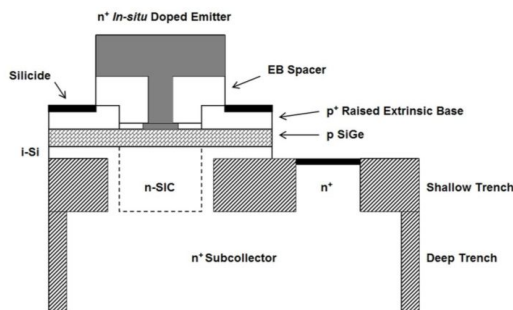
- Si Cap over SiGe base
 - Allows growth of oxide over SiGe (SiGe poor oxidizer).
 - Allows room for base out diffusion, and emitter out diffusion.
 - Provides added stability.
- SiGe Layer
 - Can use Carbon ($10^{20}/\text{cm}^3$) to reduce out diffusion of Boron.
- Buffer Layer
 - Used to ensure good growth interface.
- Substrate (Si).



- Some critical SiGe thickness where device fails.
 - Can get very complex very quickly (force vs. energy balance at interface)
 - Practically stability can easily be determined from SiGe layer thickness vs. Ge fraction (more Ge = less stable).



- Hard to build high Q passives in SiGe.
 - Not so good substrate/dielectric coupling.
 - Can't use gold as a conductor (forms deep traps in Si).
 - Advantage in SiGe over III-V is passives are quite far from substrate.
 - Use Cu instead of Al, lower sheet resistance. (Cu deep trap formation solved)
- When integrating with CMOS use BAG method.
 - Base after Gate.
 - Saves HBT from pain of high temperatures.
- Raising the base physically is favorable (reduces resistance).



- SiGe HBT is a useful device.
 - Very fast, still get more power output from III-V.
- Various epitaxial fabrication methods.
 - MBE
 - UHVCVD
 - APCVD
- General process is to clean the wafer, then deposit material.
 - How this is done is dependent on pressure/temperature.
- Can get very accurate profiles
- SiGe layer can become unstable quickly. Must consider Ge fraction and layer thickness.

Citations:

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