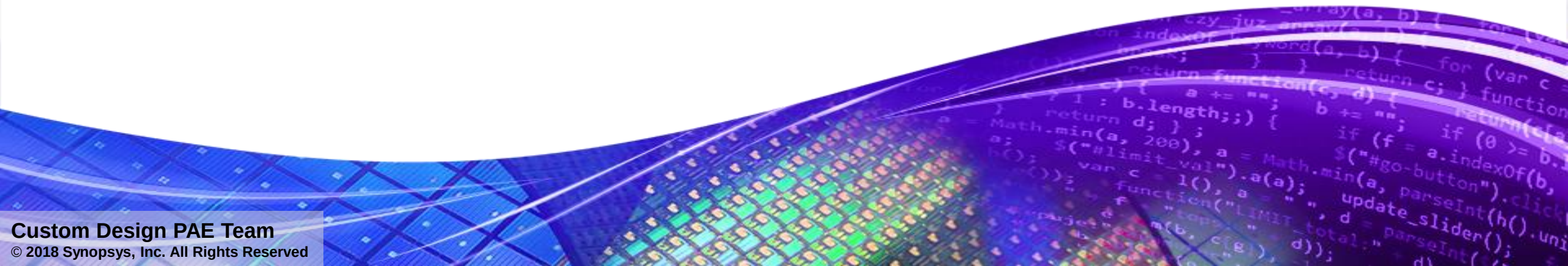
SYNOPSYS®
Silicon to Software™

Custom Compiler

Schematic Editor and Simulation Analyses Environment (SE SAE) Utilities

O-2018.09



Custom Design PAE Team
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Unit Objectives

- **After completing this unit, you should be able to use:**
  - Compare Designs
  - Power Domain Analyzer
  - Net Tracer
  - Constraint Editor
  - Plot Signals From Simulator Output Files
  - Colorize Nets
  - Operating Point Report
  - Timestamps Dashboard

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Schematic Editor Utilities

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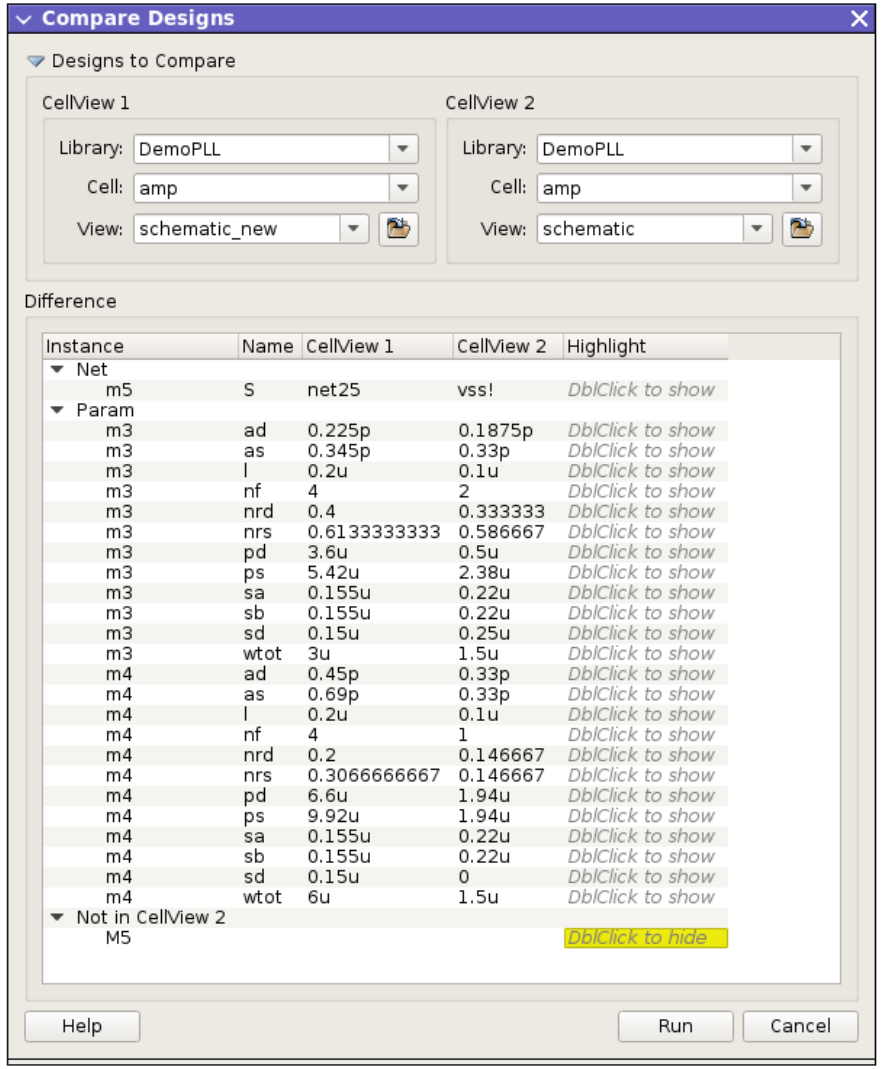
Compare Designs

- **Choose Utilities > Compare Designs from the Schematic Editor main menu bar**
  - Highlight differences between any two schematic views
  - Detect mismatches for
    - instance terminal
    - Parameter
    - Instance Masters
  - Detect missing objects
    - Instance
    - Terminal
  - Display both designs in the same window



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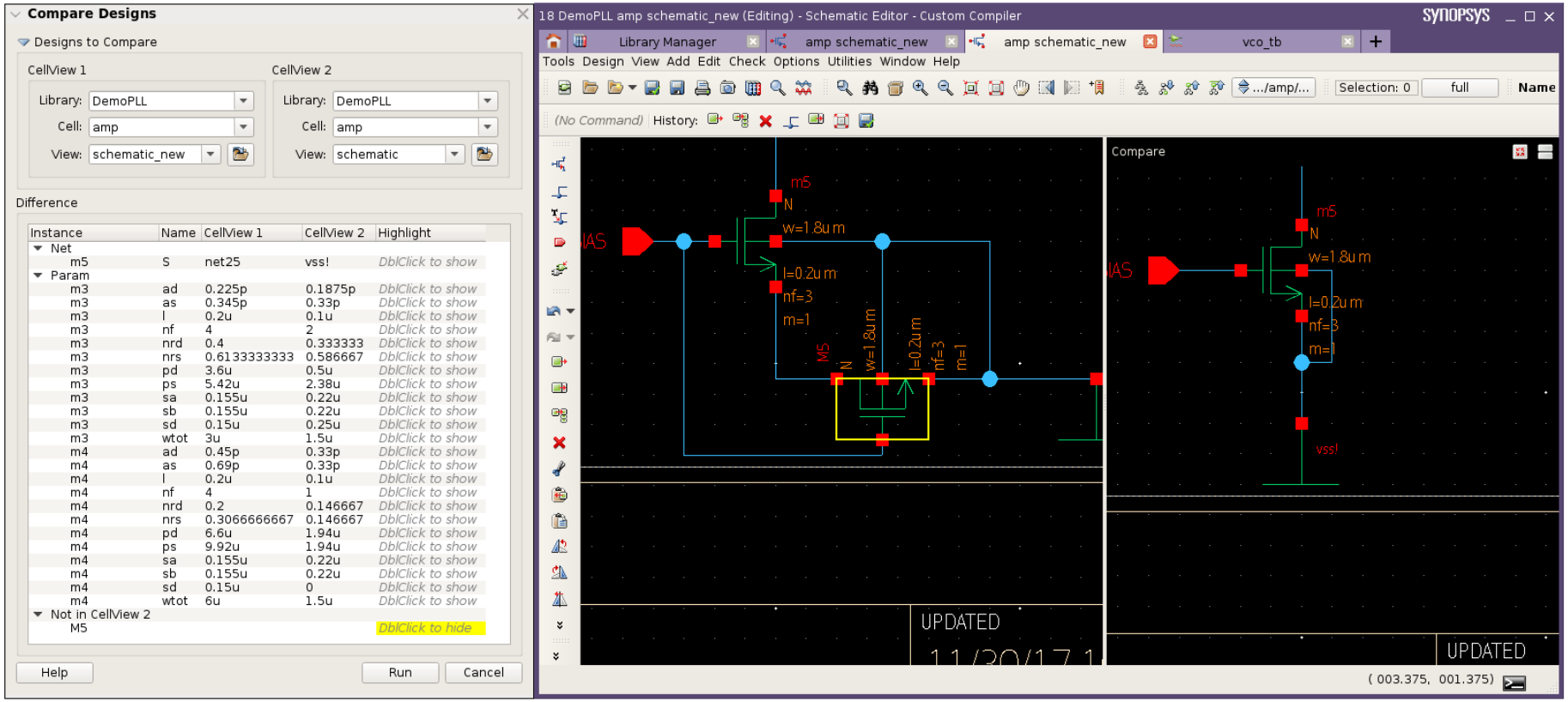
Compare Designs

- **Cross-probing with schematic**
  - Double-click on the row of interest to zoom to schematic view



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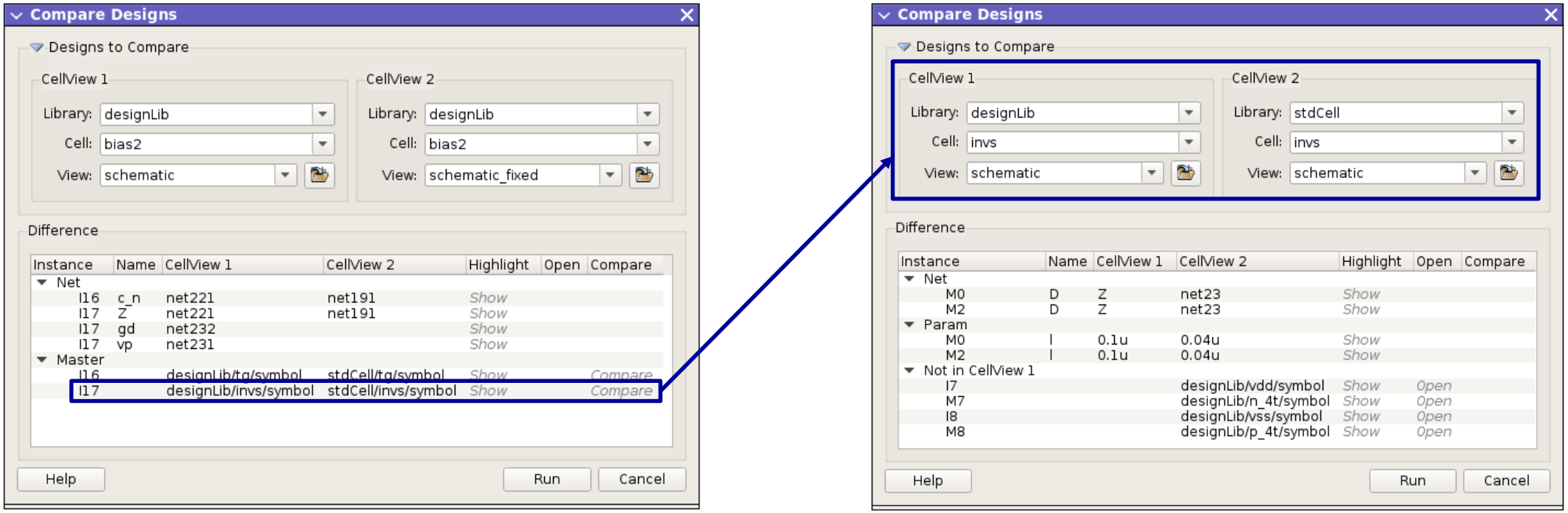
Compare Designs (O-2018.09-SP1)

- **Quickly compare and see differences inside different master designs**
  - Double Click on *Compare* text to compare



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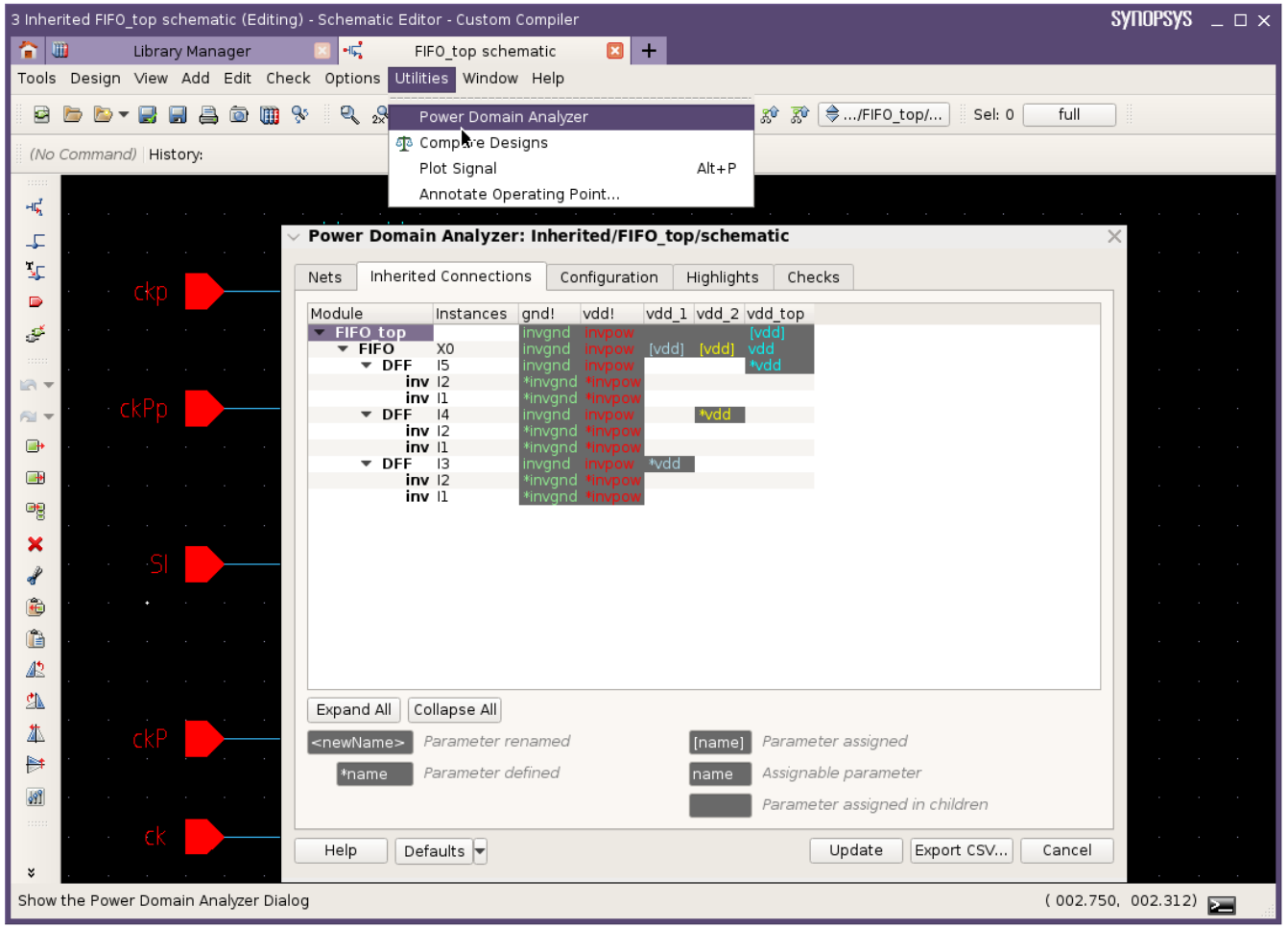
Power Domain Analyzer

- **Power Design Analyzer dialog**
  - **Nets**
    - Power domain nets through design hierarchy
    - User defined nets (clock, reset, etc.)
    - Modules using Power/Ground nets
    - Instances using Power/Ground nets
  - **Inherited Connections**
    - NetSet assignments
    - Connection Definition assignments
  - **Configuration**
    - Viewer related settings



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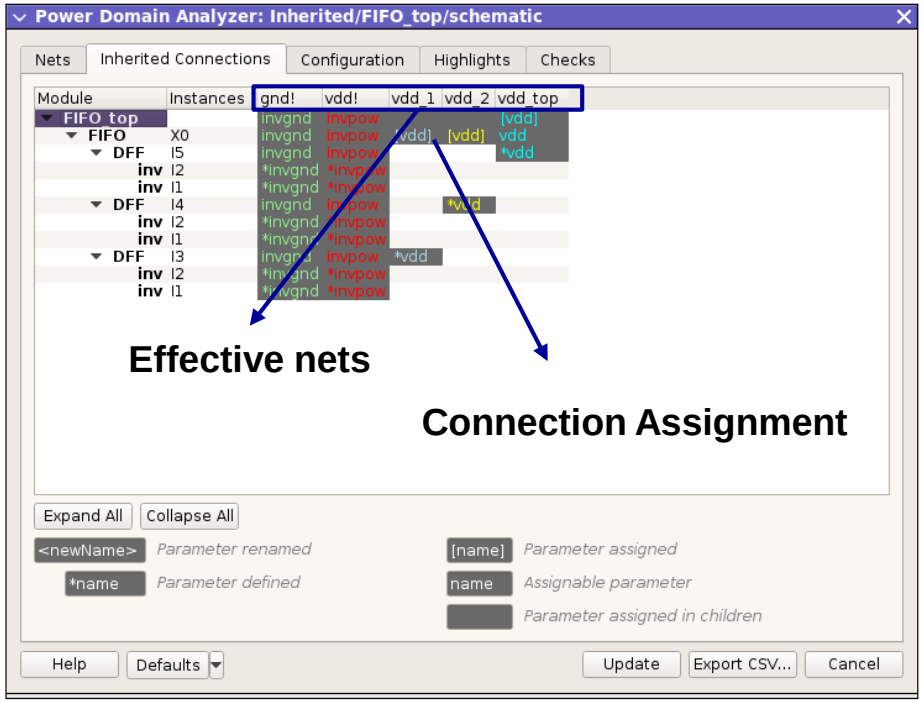
Power Domain Analyzer

- **Inherited Connections tab like Nets tab shows**
  - **Modules**: shows design folded modules
  - **Instances**: shows instances of corresponding module instantiations in the parent design
  - **Effective Nets**: shows effective nets as column headers, which is connected using connection definitions listed in that particular column
- **Is available only if Inherited Connections Tracer check box is set in Configuration tab**



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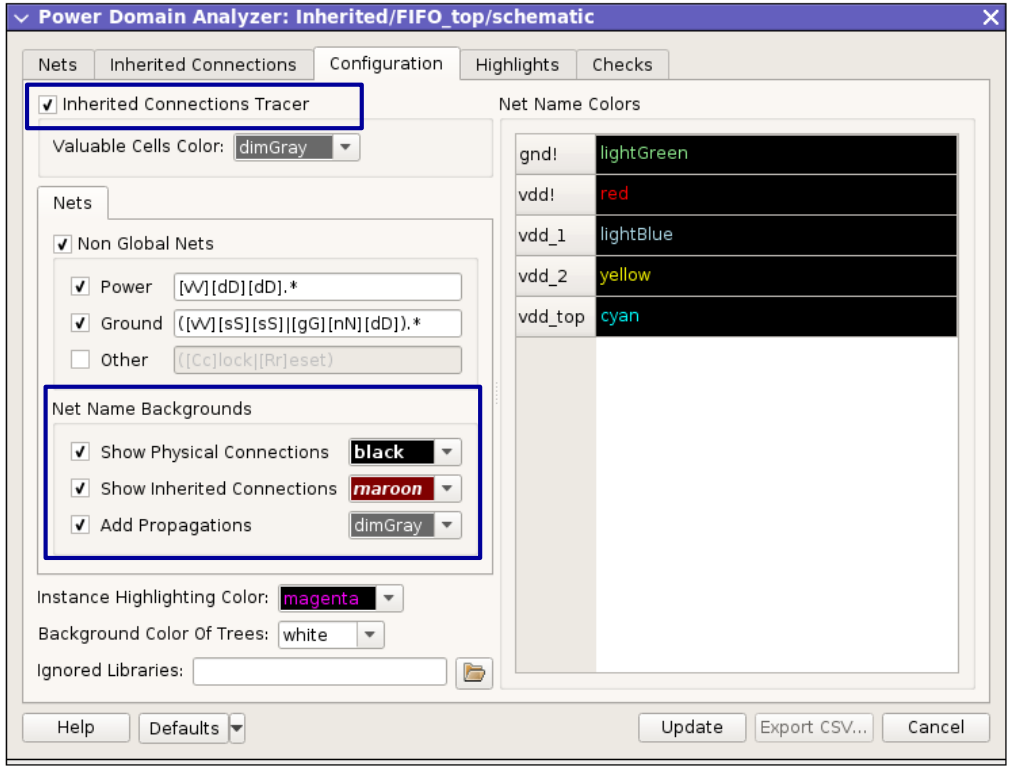
Power Domain Analyzer

- **Is available only if Inherited Connections Tracer check box is set in Configuration tab**
- **Different Backgrounds for Nets with**
  - Physical Connections
  - Inherited Connections
  - Propagations through design hierarchy
- **Ignored Libraries**
  - List of libraries from which the cells will not be processed, together with their entire lower hierarchy



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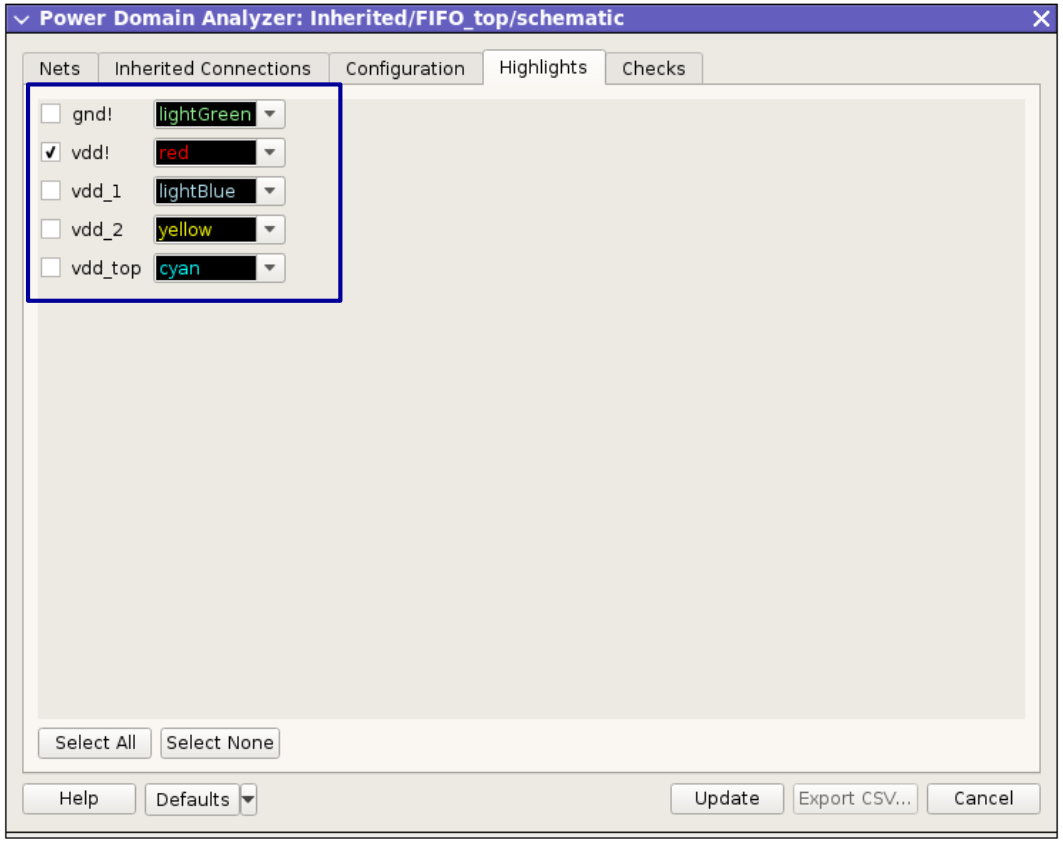
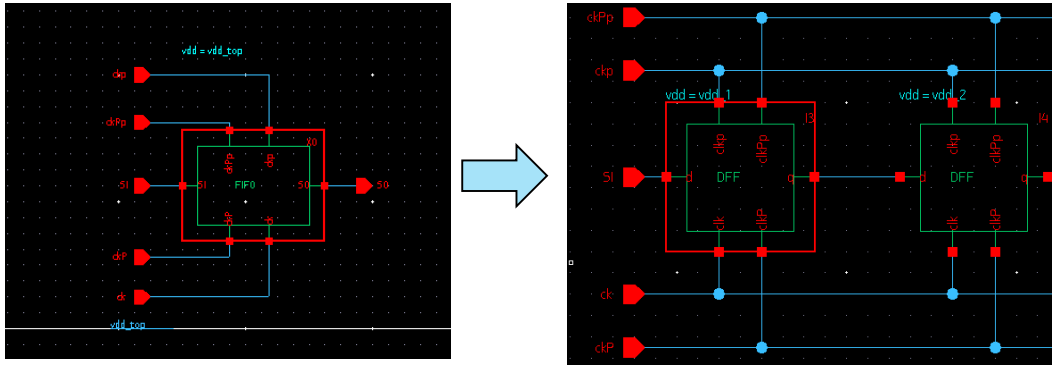
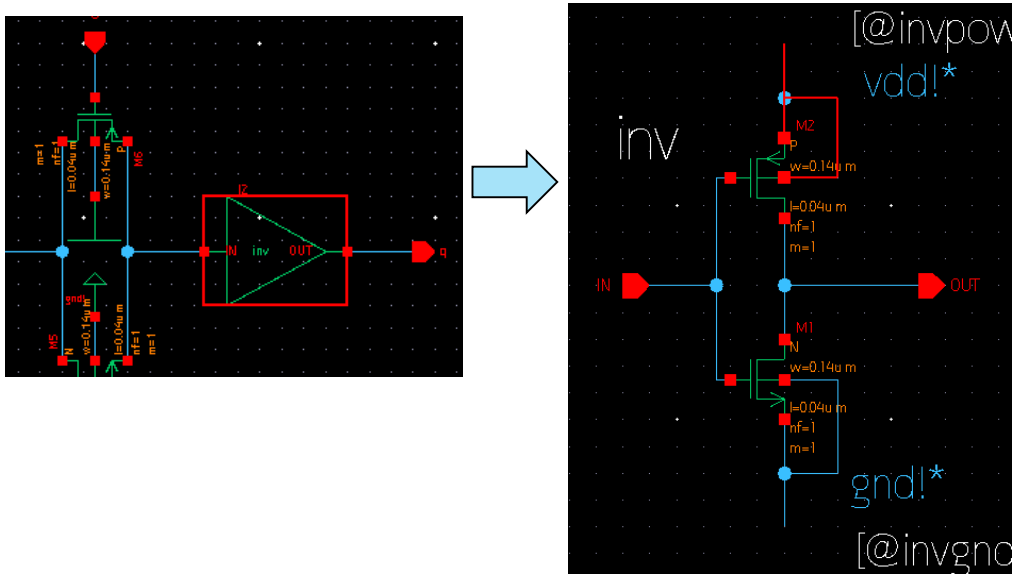
Power Domain Analyzer

- Highlight nets through hierarchy







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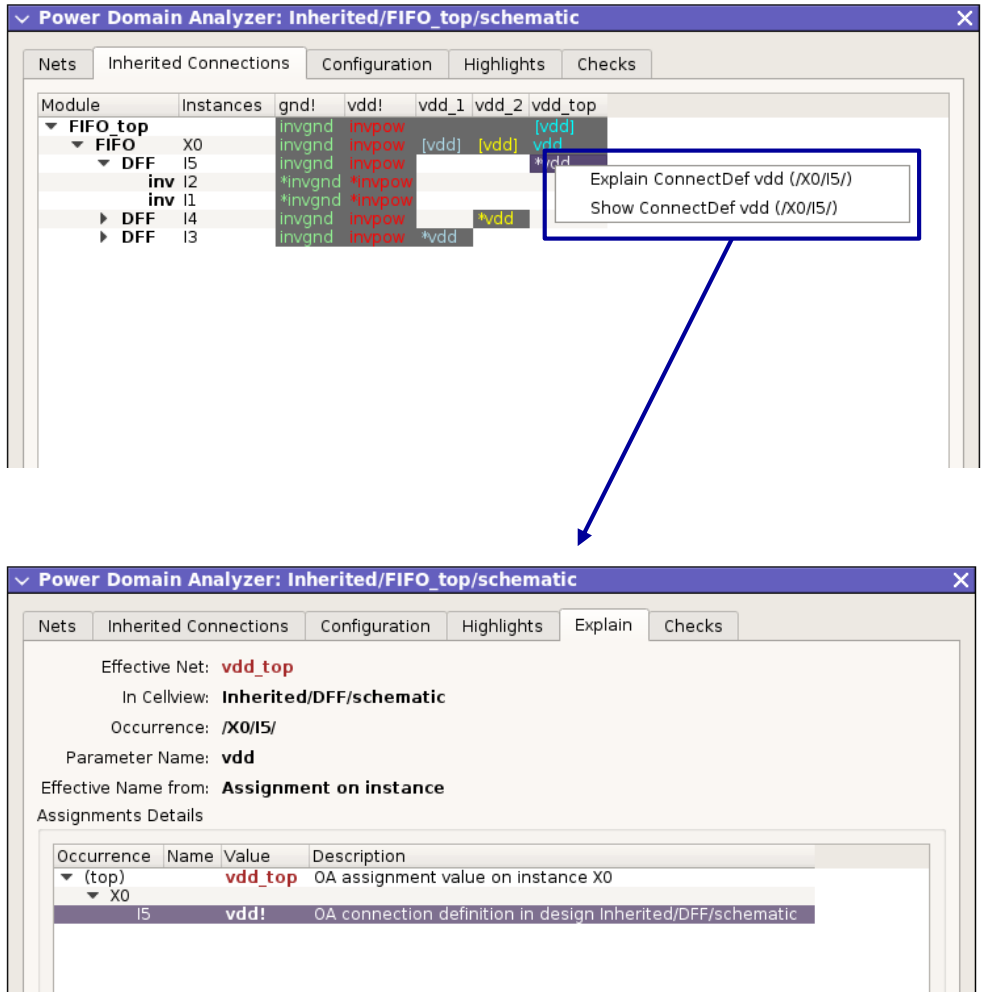
Power Domain Analyzer

- **Explain Connection**
  - Describes all the details of the connection (effective net name calculation) for the selected connection definition in the Inherited Connection results table
- **Assignments Details table**
  - Shows assignments and assign-assignments throughout the hierarchy for given connection definition



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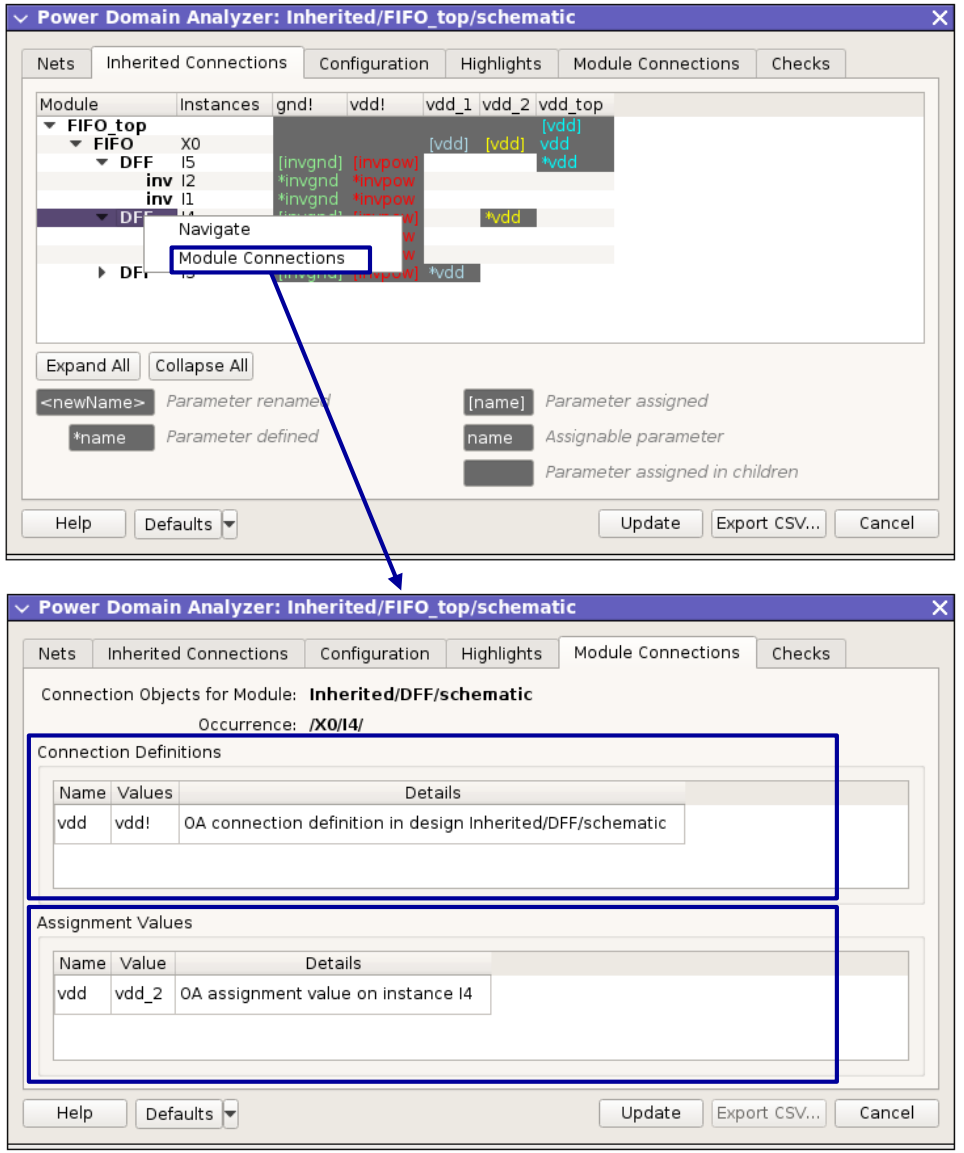
Power Domain Analyzer

- **Module Connections tab**
  - Gets opened from appropriate module's CSM selected
  - Lists the connection definitions defined in the module
  - Shows assignment values related to this module through the hierarchy
    - Details highlights assignment type (assign value or assign-assignment)



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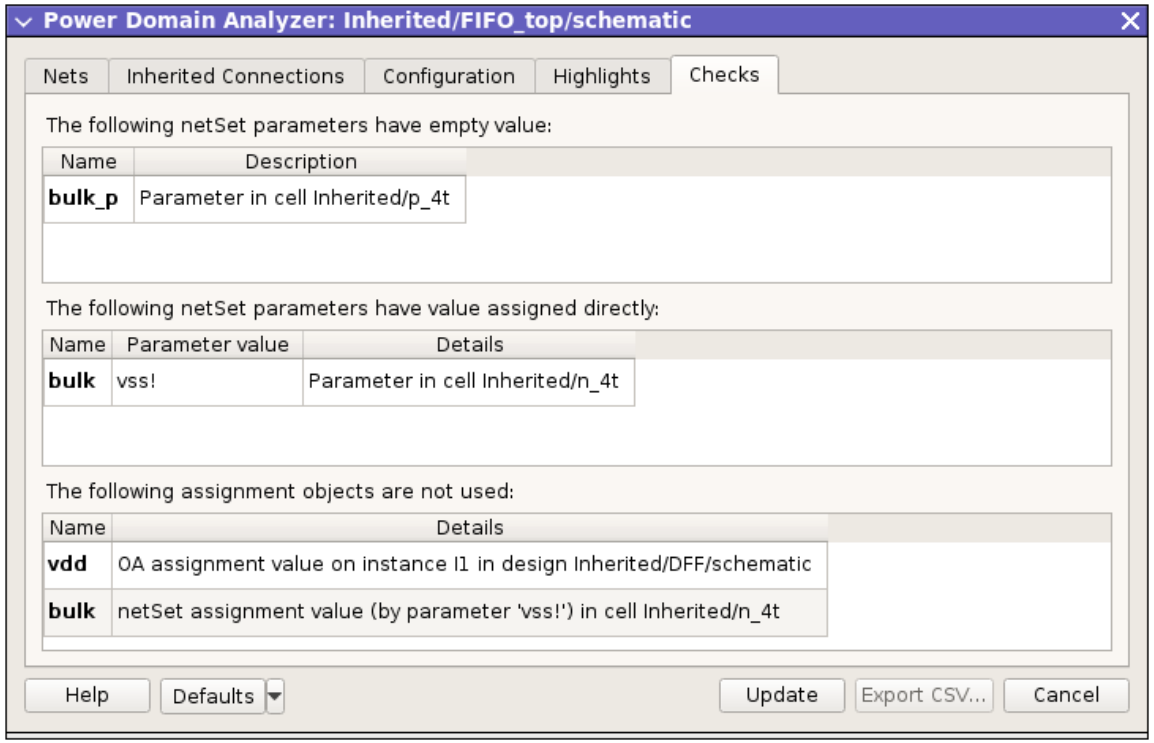
Power Domain Analyzer

- **Checks tab**
  - Shows connection definition violations in the design hierarchy
  - Includes violations for
    - NetSet parameters with empty value
    - NetSet parameters with direct assignments
    - Unused assignment objects



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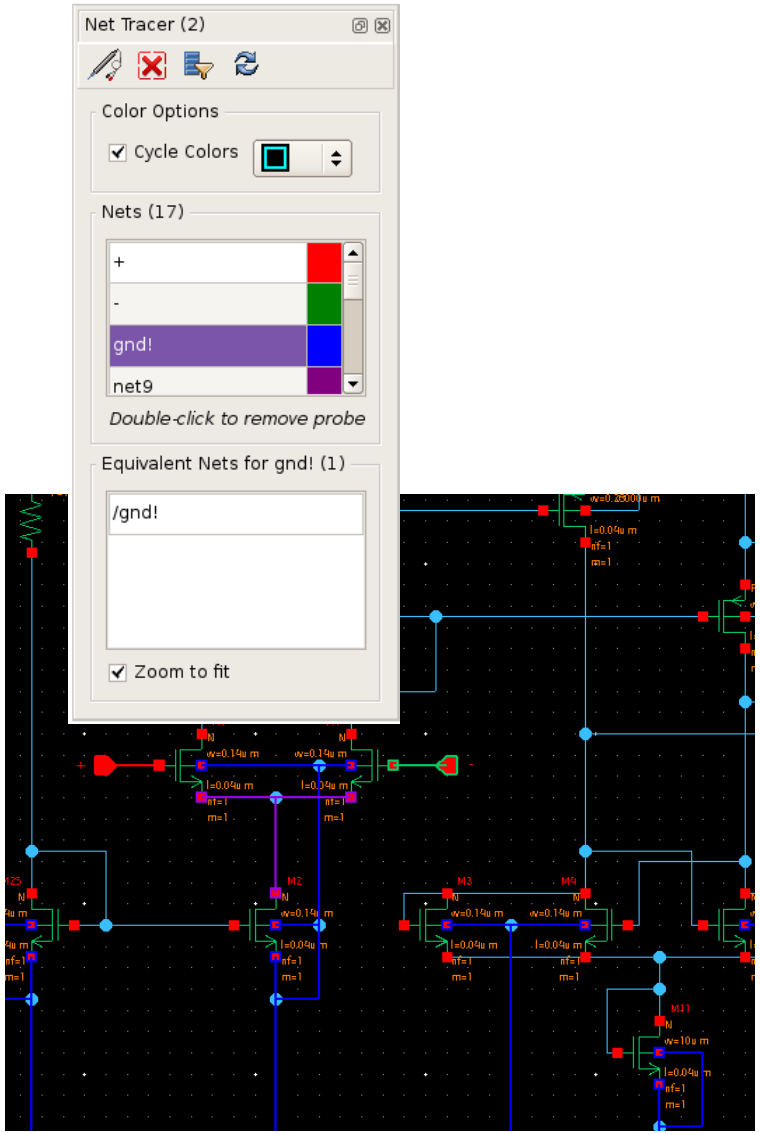
Net Tracer

- **Can be used for interactive probing of nets throughout the design hierarchy**
- **Net is highlight with the same color across hierarchy**
  - Multiple nets can be highlighted with different colors
- **Nets section lists the nets found in the current edit design**
- **Equivalent Nets section lists the hierarchical electrically equivalent nets for currently selected net in Nets section**
- **Zoom to fit equivalent nets at any level in hierarchy**



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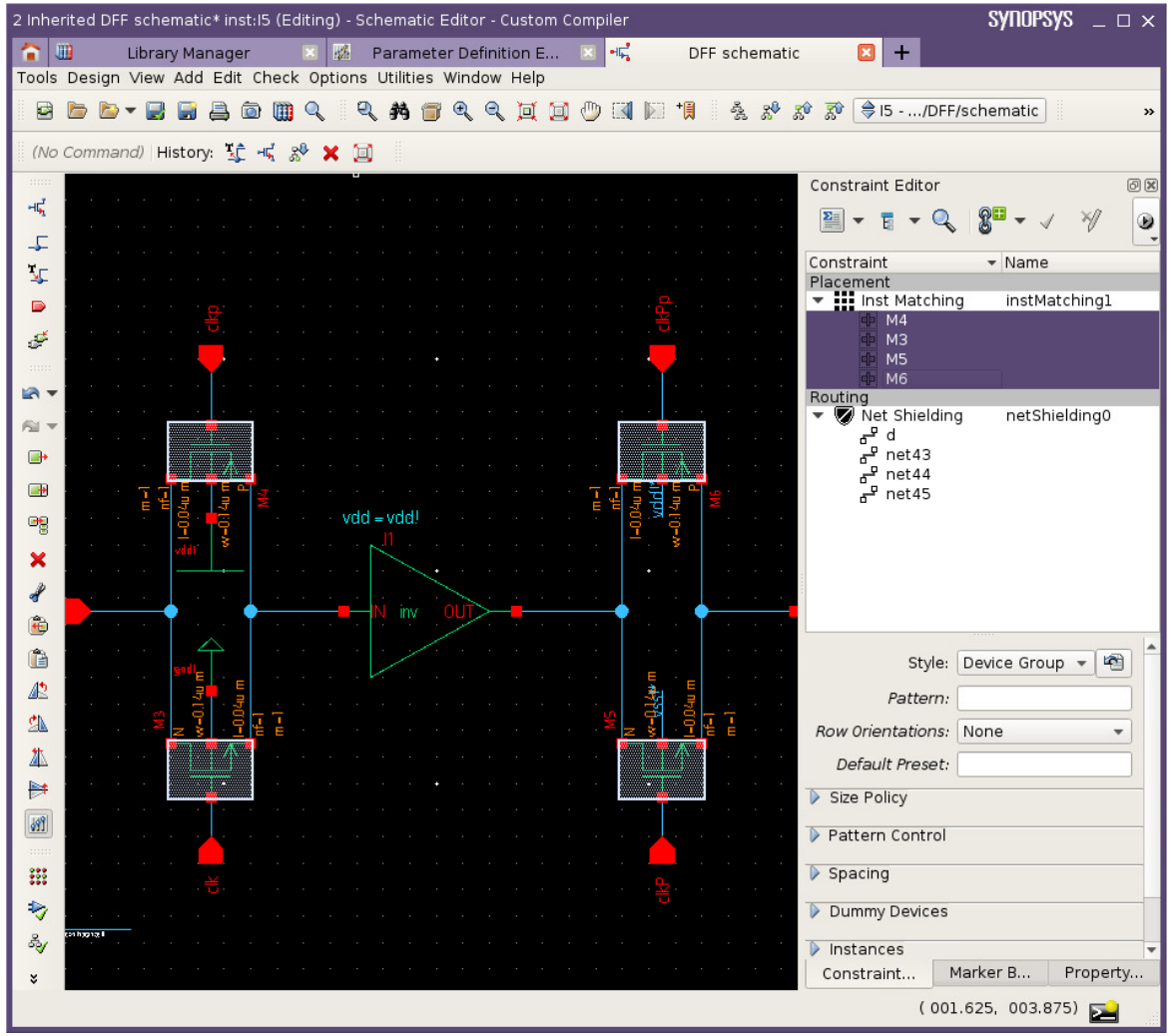
Constraint Editor

- **Choose Window > Assistants > Constraint Editor from the Schematic Editor main menu bar**
  - Placement Constraints
    - CMOS
    - Inst Matching
  - Routing Constraints
    - Color Matching
    - Net Shielding
- **Create, delete, modify and highlight constraints in Schematic Editor Windows**
  - Constrains get transferred to layout through SDL
  - Layout constrains get updated automatically during SDL initialization if necessary



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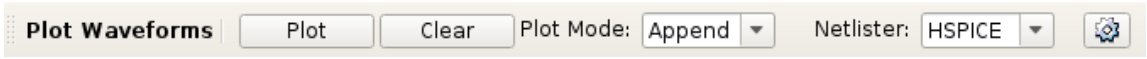
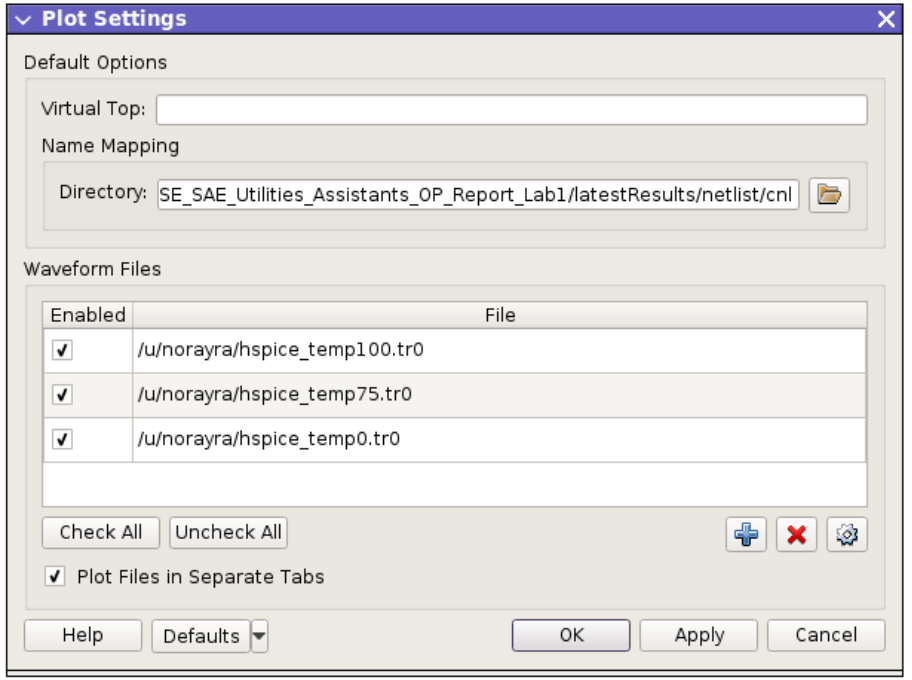
Plot Signal

- **Use Utilities > Plot Signal command**
- **Directly plot signals from simulator output files**
  - Interactively pick signals from Schematic Editor
  - Append and Replace plot mode support
- **Setup Name Mapping and add simulator files**





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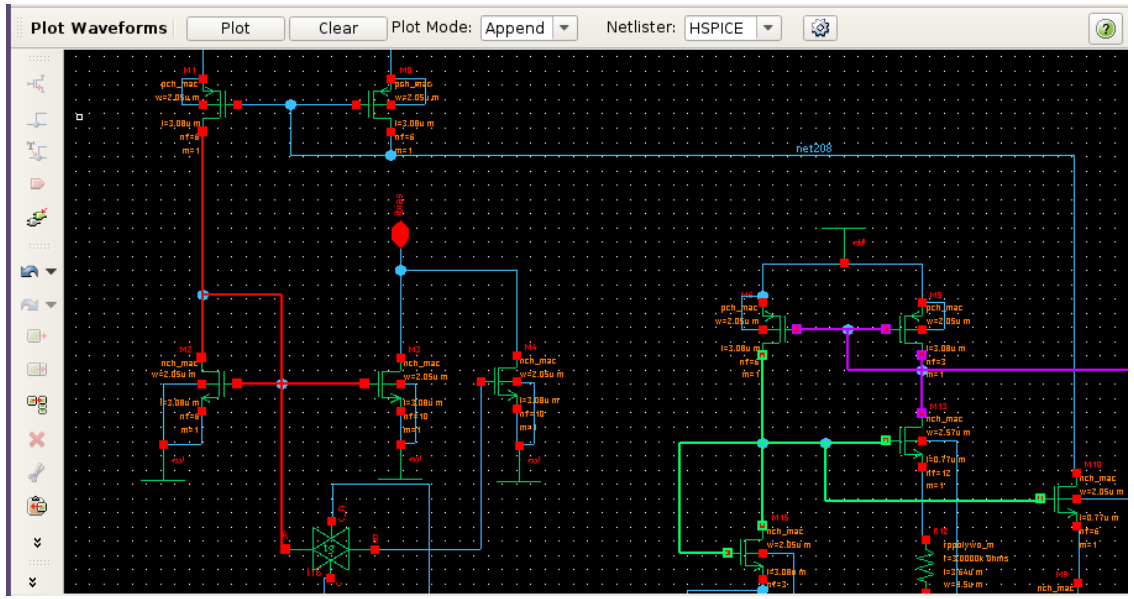
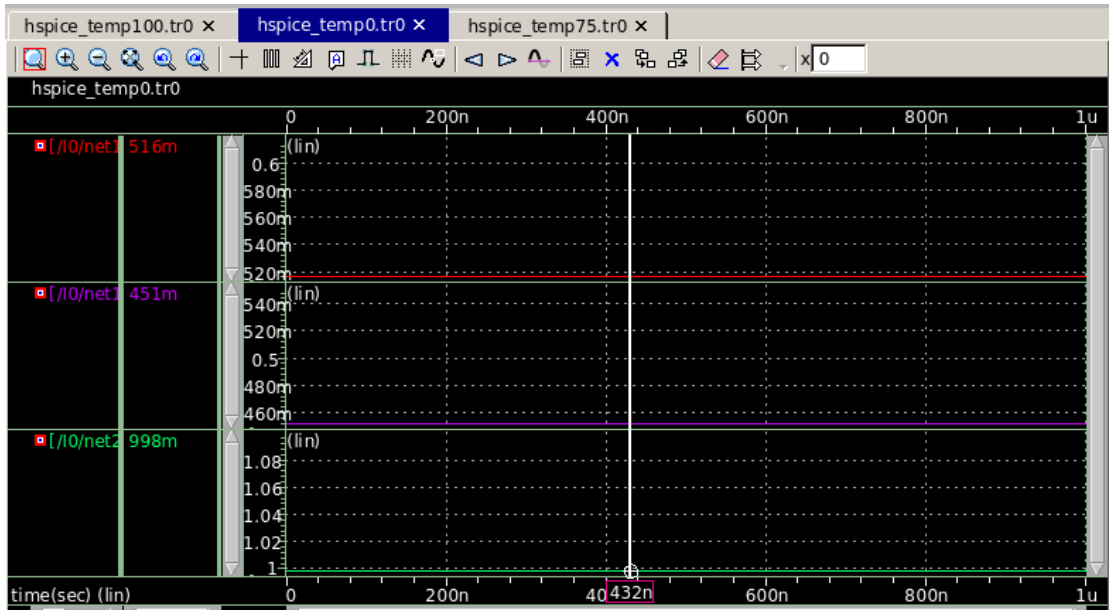
Plot Signal

- **Cross Probe signals from Schematic Editor**
  - Select net and press **Plot** button





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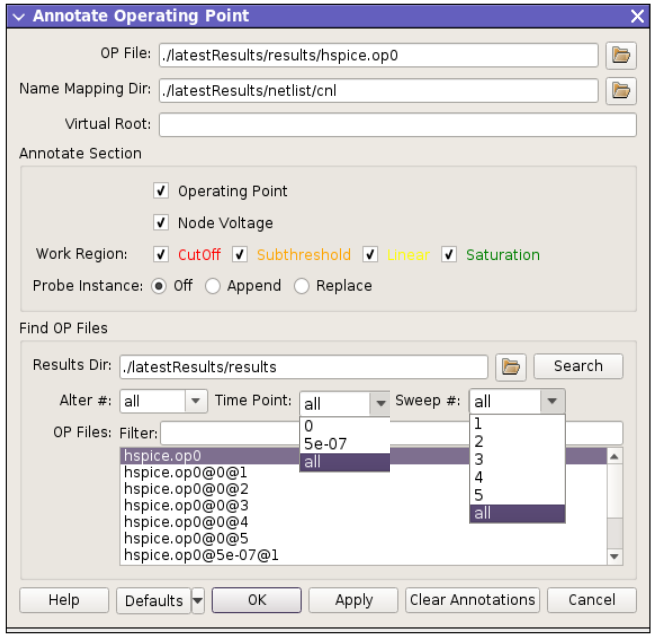
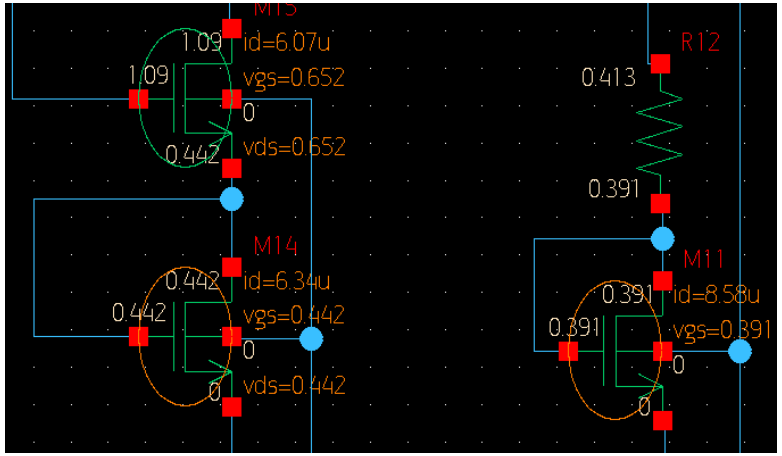
Annotate Operating Point

- **Use Utilities > Annotate Operating Point command**
- **Setup OP file and Name Mapping settings**
  - Search for OP files inside results directory
  - Filter by Alter #, Time Point or Sweep #
- **Specify what to annotate**
  - Operating Point
  - Node Voltages
  - Work Region





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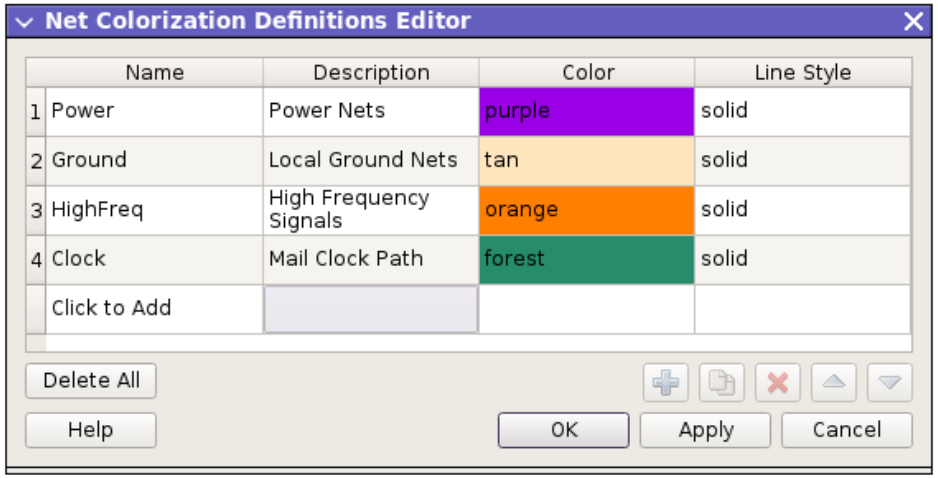
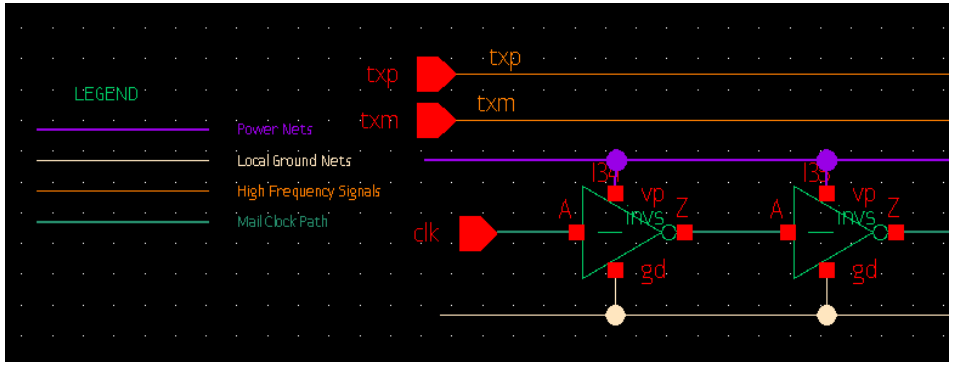
Colorize Nets (O-2018.09-SP1)

- **Colorize special nets based on designers preferences**
  - Power and ground nets
  - High frequency paths
  - Clock signals
  - Etc.
- **Setup through Utilities > Net Colorization Definitions dialog**
- **Colorize nets using Edit > Colorize Nets command**
  - Choose color and click on a net
  - Check Apply by Name, select net name and apply color
- **Add color legend instance**
  - Library: basic
  - Cell: net_legend
  - View: symbol





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SAE Utilities

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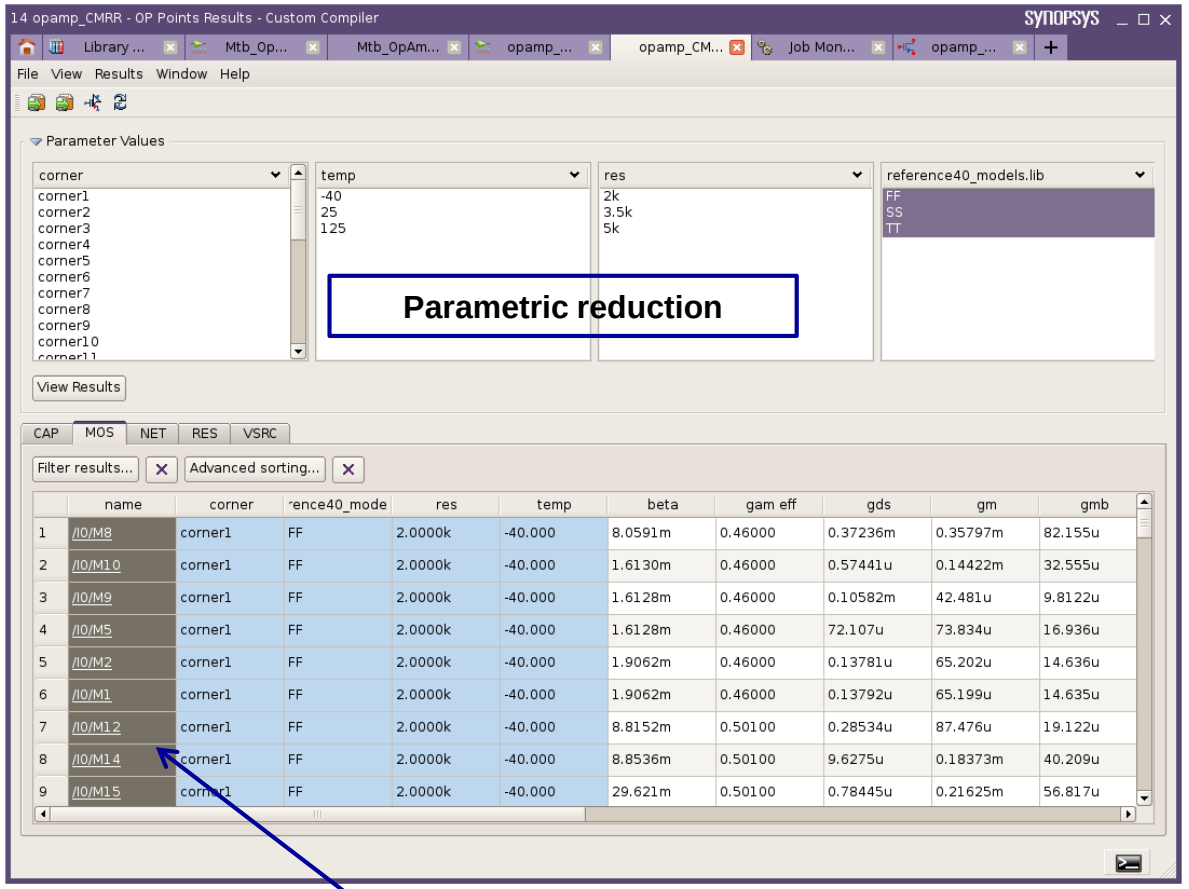
Operating Point Report

- **DC Operating Point Viewer can be invoked using Results > Print > Operating Point Report**
- **Displays DC OP for all leaf cells in hierarchy**
  - Separate tab is used for each type of device
- **Supports**
  - Parametric reduction
  - Cross probing with Schematic Editor
  - Showing/Hiding operating points of interest
  - Filtering
  - Sorting
- **Export results to CSV or HTML formats**



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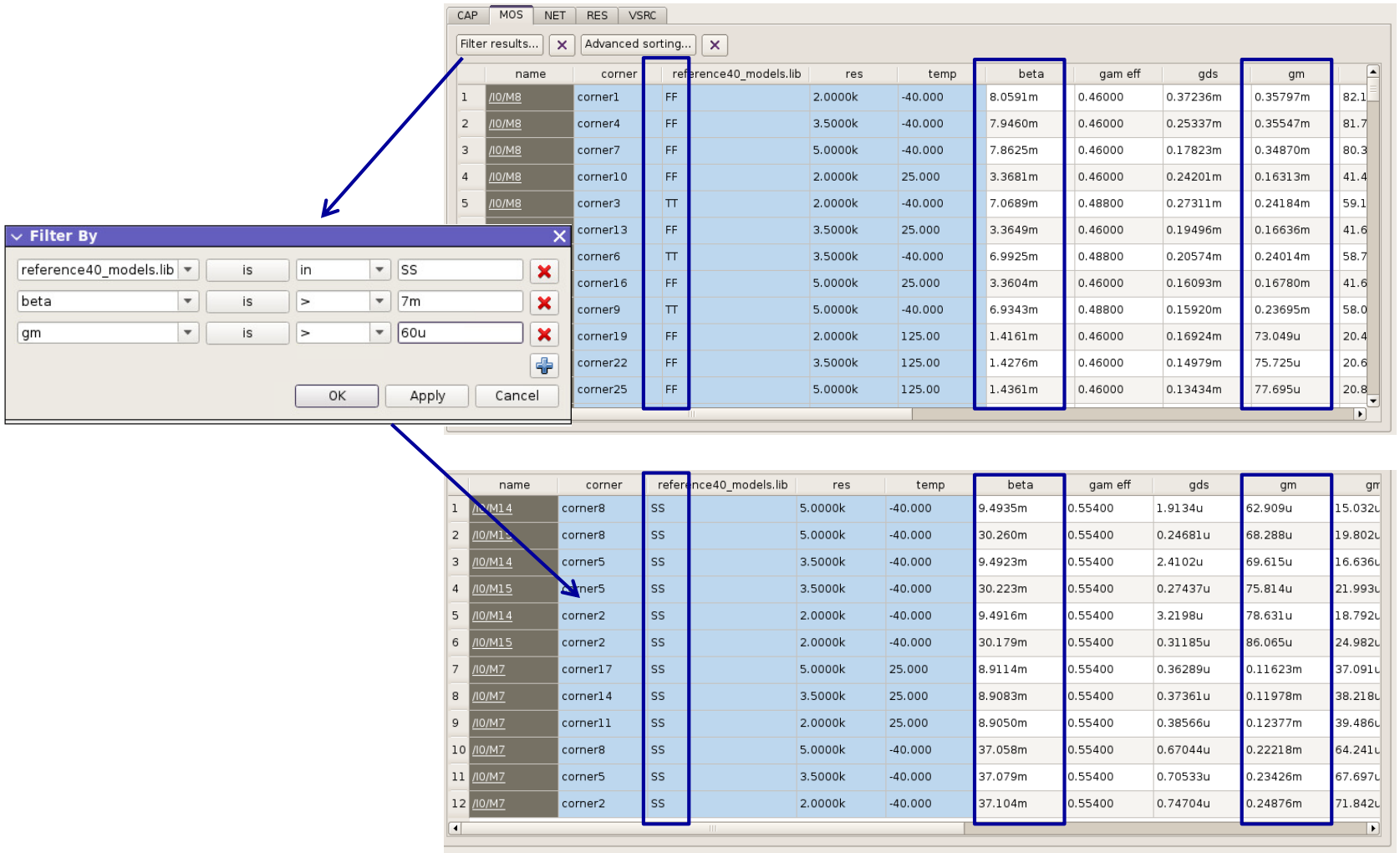
Operating Point Report

- **Filter DC OP results based on defined conditions**
- **Supported Conditions**
  - equal (=)
  - more (>)
  - less (<)
  - range
  - in



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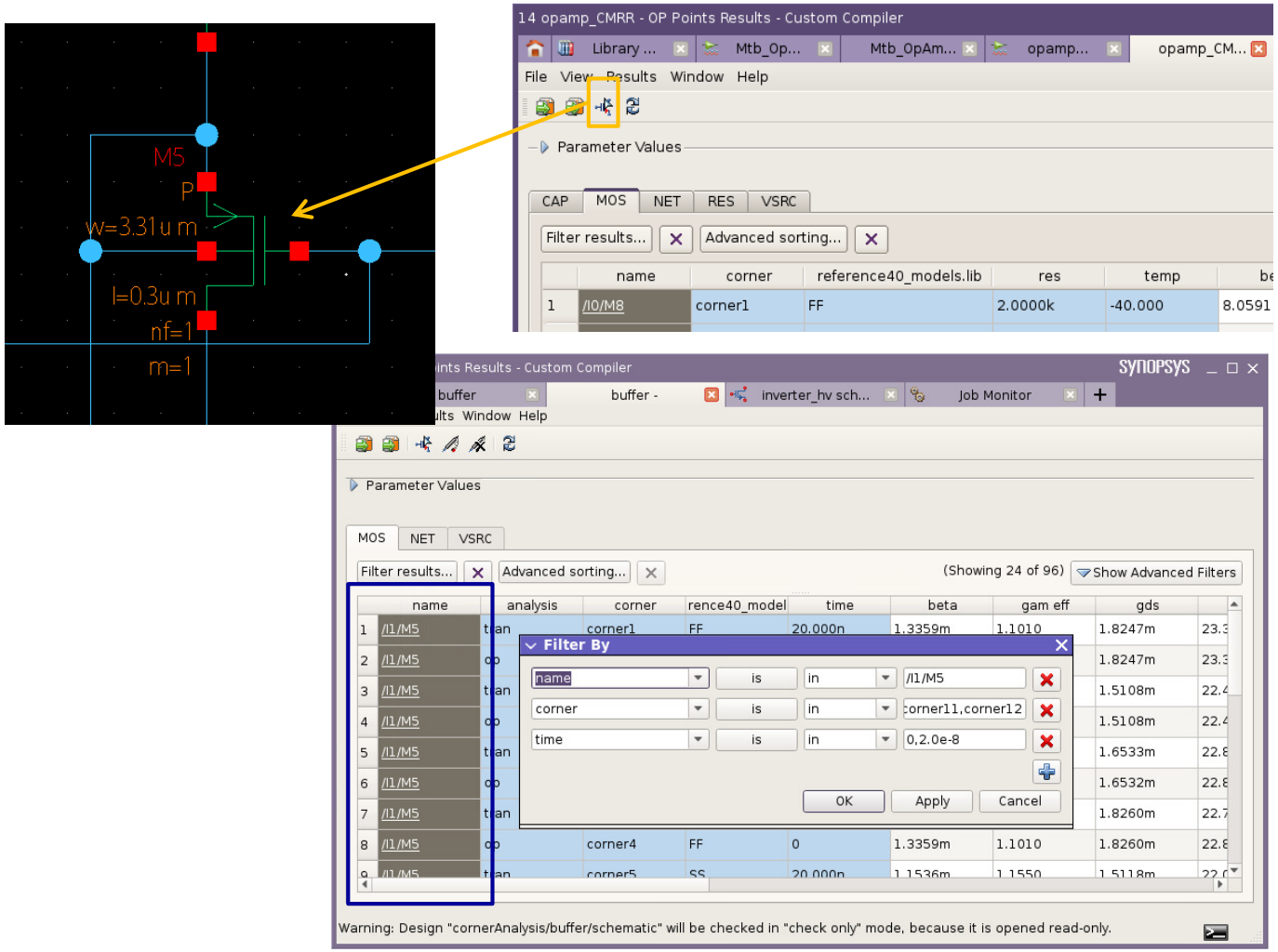
Operating Point Report

- Filter Operating Point information based on selected devices from Schematic Editor
- Click on devices to include them in OP Report
- Hold Ctrl and click to devices to remove them from selected devices
- Filter expression is created from selected devices



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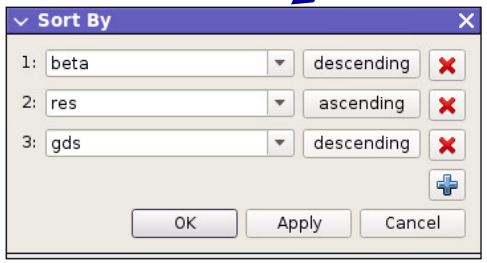
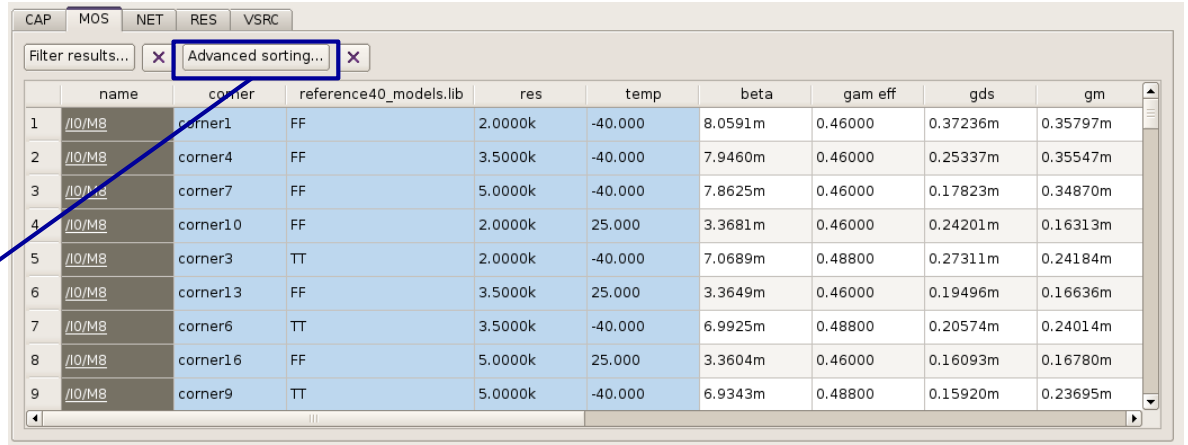
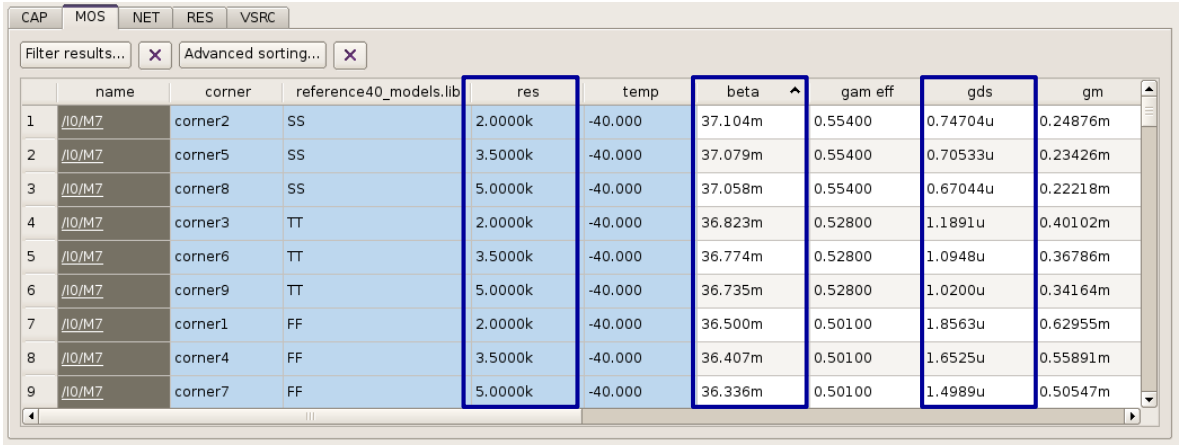
Operating Point Report

- **Sort DC OP results**
  - Ascending
  - Descending
- **Chain multiple parameter sorting**







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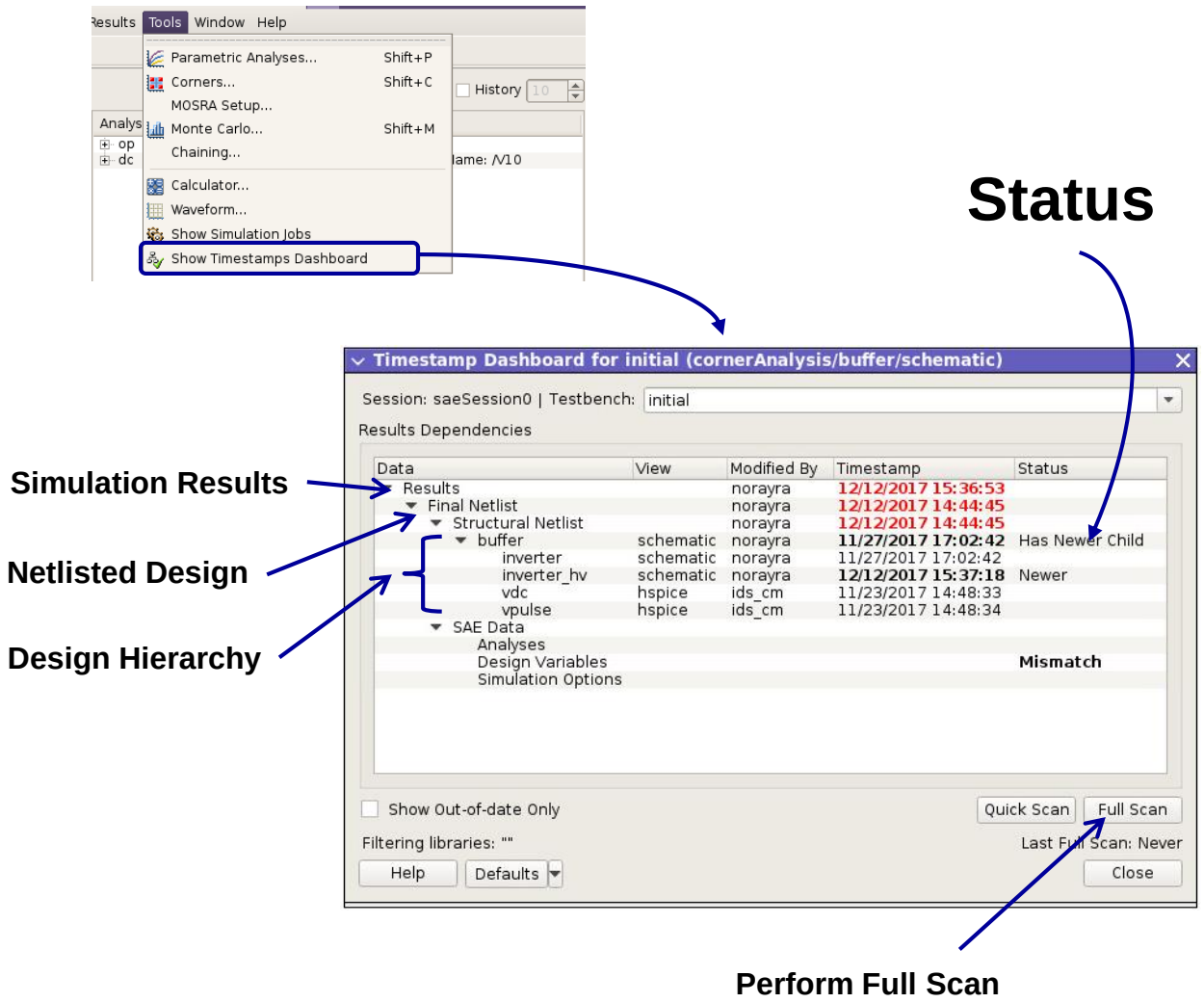
Timestamps Dashboard

- **Purpose**
  - Highlights if netlists or simulation results are out of date
- **Scan on demand Simulation Results, Netlist, Design timestamps and SAE setup**
- **Colorize outdated data**
- **Re-run netlisting and simulation from Context Sensitive Menu (CSM)**
  - Highlights rows as netlisting occurs
- **A preference can be set to ignore libraries**
  - Helps reduce the content that is tracked (PDK lib)

  `saTimestampDashboardFilterList`



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