

Custom Compiler Training

-SAE

1

Simulation Setup using SAE

Learning Objectives

In this lab, you will learn how to:

- Use the Custom Compiler Simulation and Analysis Environment (SAE) to set up a simulation, including non-simulator-specific and simulator-specific settings
- Netlist the testbench
- Simulate the testbench
- View and analyze waveforms using WaveView
- Save the simulation setup into the state
- Verify the Voltage-Controlled Oscillator (VCO) circuit design using HSPICE.

- Simulate the testbench
- View and analyze the waveforms using WaveView
- Save the simulation setup into the state

Lab Duration:
30 minutes

Before You Start

Make sure you have the following:

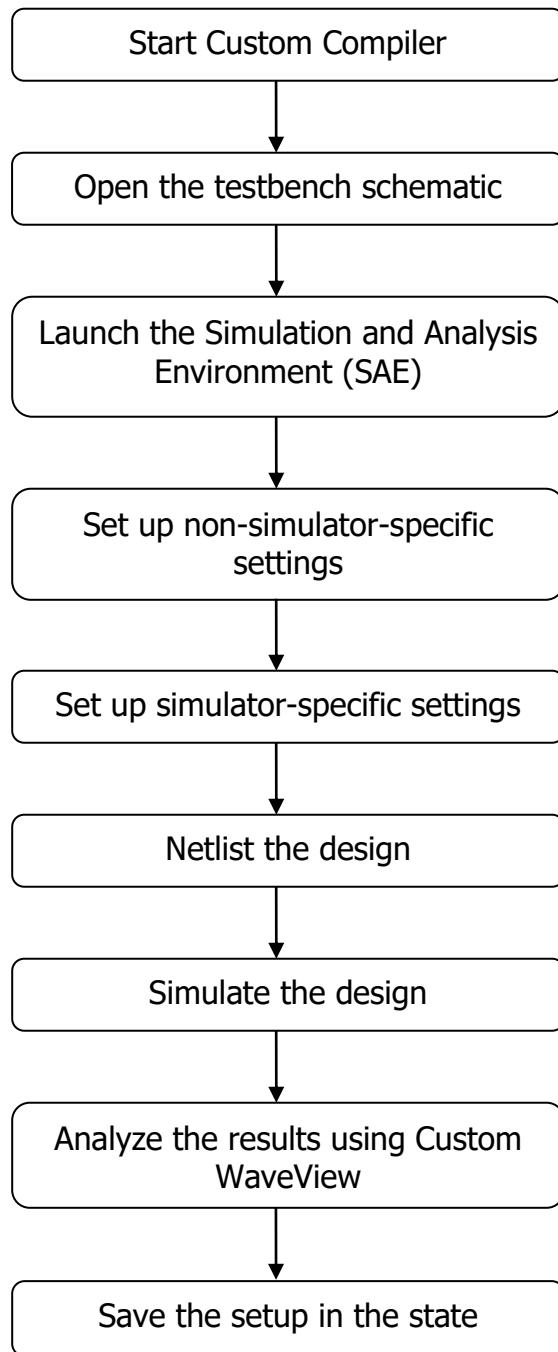
Item	Description	Location
HSPICE O-2018.09	Software	Installed on the server
Custom Explorer O-2018.09	Software	Installed on the server
SAE_DataSetup_Lab1: DemoPLL lib.defs	Lab data folder: OpenAccess design library Library definition file	The directory where you unpacked the lab data

Before doing the simulation setup, it is important to understand the use model of the commands that are required.

Refer to the *Custom Compiler Simulation and Environment User Guide* for the commands that are used in this lab.

Flow Overview

Lab 1 Tasks



Answers and Solutions

There is an *ANSWERS and SOLUTIONS* section at the end of this lab. Refer to this section often to verify your answers or to obtain help with the execution of some steps.

Instructions

Task 1. Start Custom Compiler

1. In the UNIX window, change the directory to *SAE_DataSetup_Simulation_Lab1*.
2. Start Custom Compiler from the UNIX prompt.

```
Unix% cd SAE_DataSetup_Simulation_Lab1  
Unix% custom_compiler &
```

Task 2. Open the Test Bench Circuit

1. From the design library *DemoPLL*, open the cellview: *vco_tb/schematic*.
2. The VCO testbench *vco_tb* cellview opens in a Schematic Editor window.
Note: This circuit is a Voltage-Controlled Oscillator (VCO). Several components in the design use design variables to specify their values.
3. Look at the two voltage source components to the left of the *vco* block. The voltage parameter values are set to *vdc*, *vtune*, *vtune2* design variables.

Task 3. Launch the Simulation and Analysis Environment

1. Invoke the Simulation and Analysis Environment using **Tools → SAE** from the Schematic Editor window.
Note: This opens the Simulation Analysis Environment (SAE) window, which comes with design *DemoPLL/vco_tb/schematic* pre-populated. Check this by choosing **Setup → Design**. The SAE window is divided into various sections to set up the simulation.

Task 4. Set up the Simulator and Run Directory

In this task, you will set up the simulator and run directory for storing the simulation results. The run directory is the directory where all the simulation results are stored for the specified simulator.

1. In the SAE window choose **Setup → Simulator** to open the **Simulator** dialog box.
2. Set the **Results Directory** to *./simulation*.

3. Make sure that Simulator is set to **HSPICE** and click **OK** to submit.

Note: If specified simulation directory doesn't exist, you will be prompted, if you want to create it.

Task 5. Set Up the Model File

In this task, you will setup the model file path to provide an input to the simulator.

Device models play an important role in predicting the behavior of the circuit during simulation. The device model parameters are generally shipped in a file (that is, a SPICE model file) from the foundry. The parameters differ from process to process and from foundry to foundry.

1. In the SAE window choose **Setup → Model Files** to open the **Model Files** dialog box.
2. Set up the **Include Path** of the model file *reference40_models.lib* using:

```
<path to PDK directory>/PDK/hspice/reference40_models.lib
```

Note: The *reference40_models.lib* file is provided with the PDK in the *hspice* directory.

3. Set the corner **Section** to **TT (typical corner)**.

Note: As you click on the **Section** field, a drop-down list appears listing all the available corners (FF, TT, SS ...) from the model file.

4. Click **OK**. This sets up the model file for simulation.

Note: Include other files by choosing **Setup → Include Files** to open the **Include Files** dialog.

Task 6. Set the Design Variables

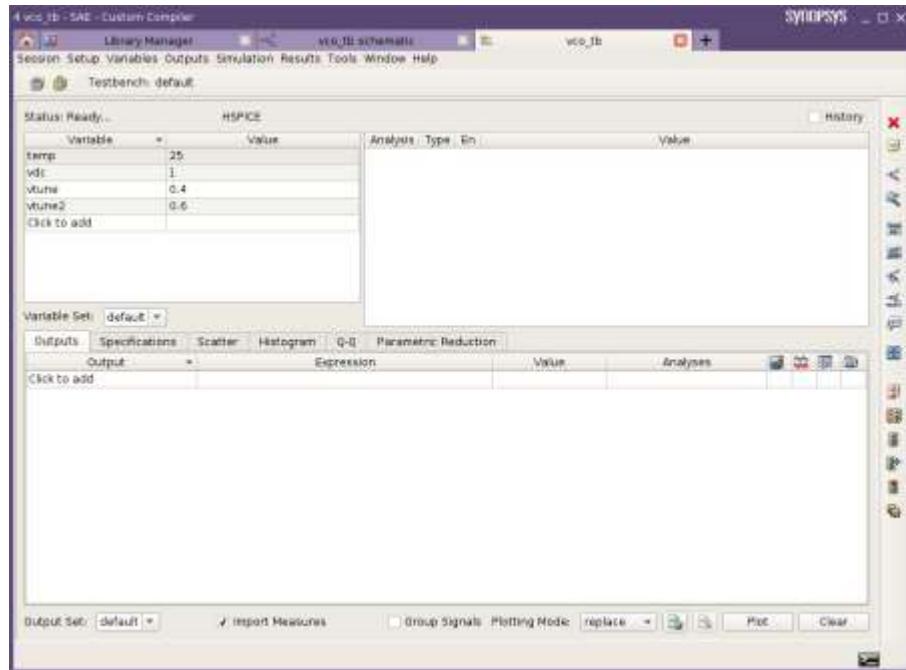
In this task, you will manage the design variables used in your design.

1. From the SAE main menu, choose **Variables → Copy From Design** to read the design variables from the design.
Design variables appear in the **Variable** section of the SAE main window.
2. Set the design variables to the following values:

Variable	Value
vdc	1

vtune	0 . 4
vtune2	0 . 6

3. The SAE window should look as follows:



Task 7. Setup the Analysis

In this task, you will set up the transient and operating point analyses to verify the circuit performance.

The next step is to specify the type of analysis to run on the circuit in order to verify its performance.

1. In the SAE window choose **Setup → Analyses** (or use the shortcut key **A**).
2. Set the **Analysis Type** *tran* (transient point) with following settings:
 - a. **Start Time:** 0
 - b. **Number of Intervals:** 1
 - c. **Time Step:** 0.1n
 - d. **Stop Time:** 50n
 - e. **Advanced Settings:** True

- i. **Method:** Temp Sweep
 - ii. **Temp Values:** (1n 25 50n 125)
 - iii. **Temp Step:** 10
- f. Enable:** True

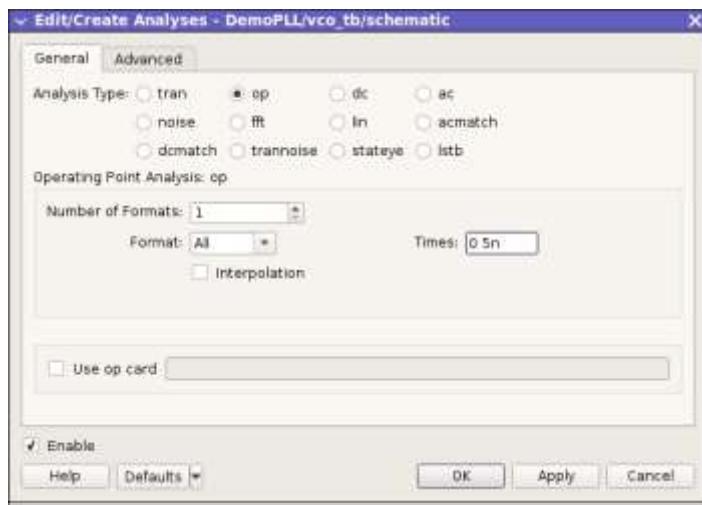


3. Apply the settings.

Question 1. What do you observe when you apply the settings?

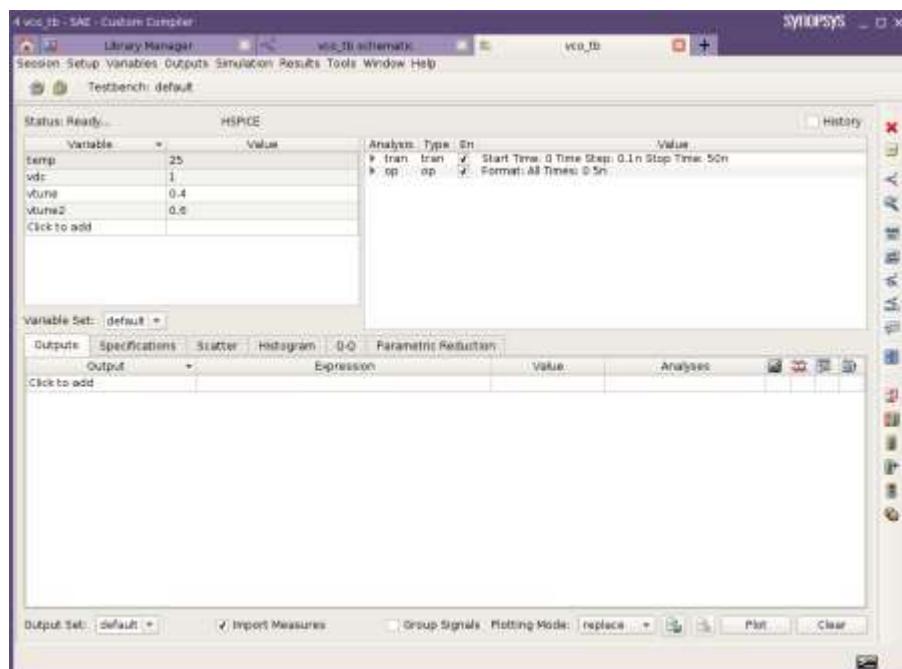
4. Set the **Analysis Type op** (operating point) with the following settings:

- a. **Number of Formats:** 1
- b. **Format:** All
- c. **Times:** 0 5n
- d. **Enable:** True



- Click **OK** to apply the settings.

Both analyses appear in the SAE main window in the **Analysis** section. The SAE window should look as follows:



Task 8. Set Up Outputs

In this task, you will set up the outputs to see the results after simulation.

- In the SAE window, choose **Outputs** → **Add from Design** (CTRL+P) to select the nets *LFIN* and *OUT*. You will be navigated to the *vco_tb* schematic view to

select the outputs from the VCO testbench. As you click on the nets in the design, they are added to the **Outputs** section of the SAE main window.

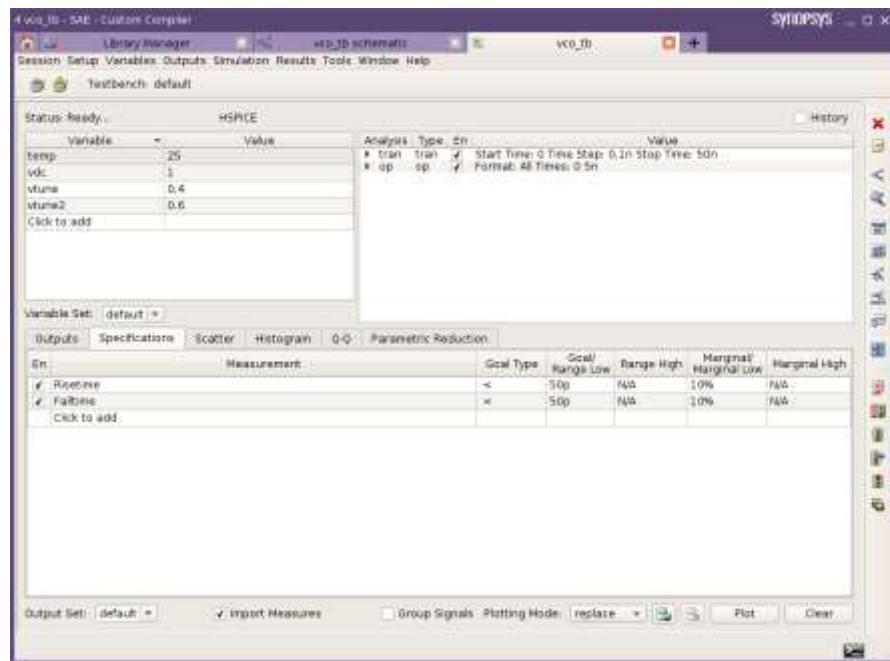
Question 2. Which command is invoked in the Schematic Editor?

.....

2. When you are done with net selection, press **Esc** to end the selection process.
3. Open the Results Analyzer using **Results →Analyzer** and switch to the **Calculator** tab.
4. Use the **Filter** field to find the **risetime** function quickly. Double-click on the risetime function in the search results.
5. Use the following settings for the risetime function:

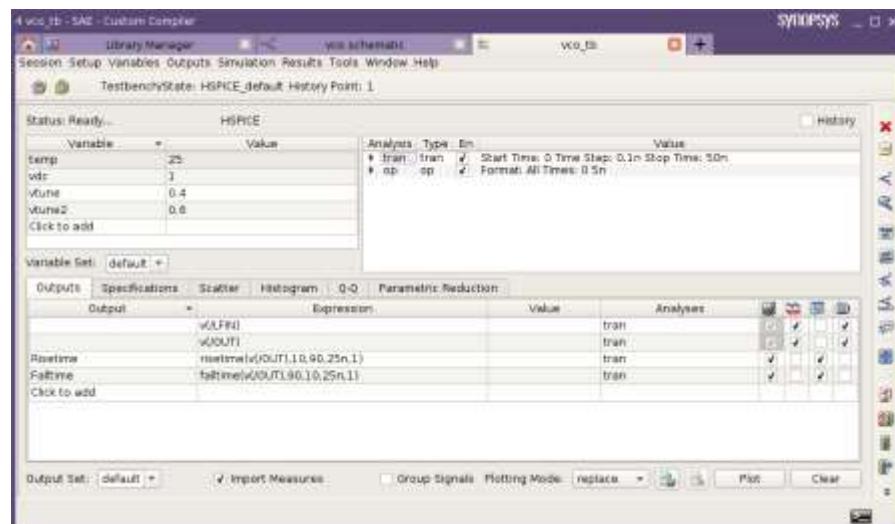
Arguments	Value
signal	V(/OUT)
low y level	10
high y level	90
x start	25n
percent	true (1)

6. Click the commit button  to create the expression.
7. Click the **Add to Outputs** button in the Results Analyzer to add the newly created expression to the **Outputs** tab of the SAE window.
8. In the **Outputs** tab of the SAE window, click in the Output column to open the text box and name the newly created expression **Risetime**.
9. Following the same steps, create an expression to measure output signal fall time and name it **Falltime**.
10. Switch to the **Specifications** tab and add specifications for the **Risetime** and **Falltime** output expressions to be less than 50p with marginal value of 10%.



11. Switch to the **Outputs** tab. In the Outputs table, check **Save Waveform Images** and uncheck **Show in Results Viewer** checkboxes for LFIN and OUT expressions.

The SAE window should look as follows:

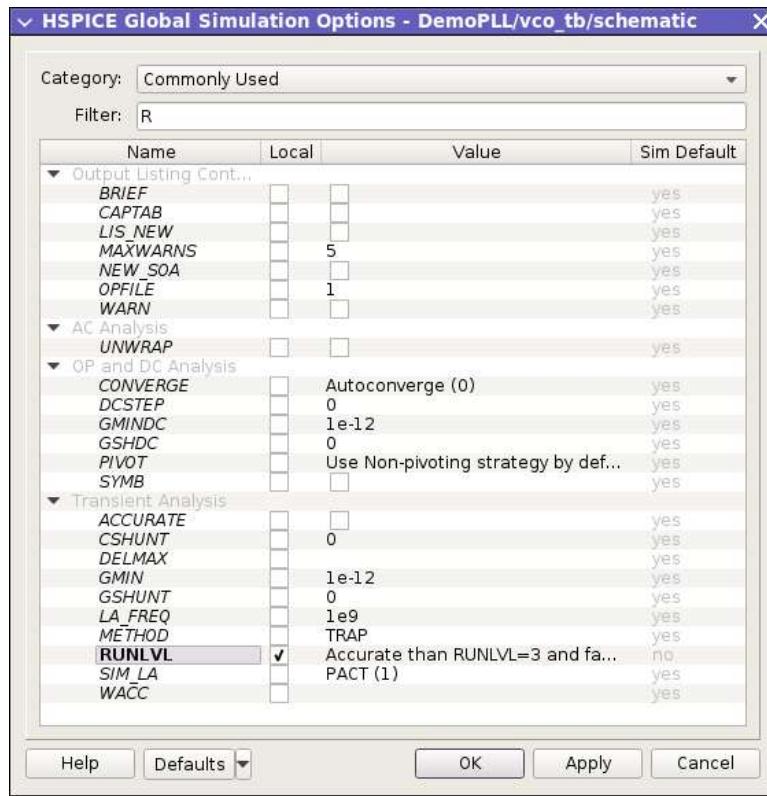


Task 9. Set Up Simulation Options

In this task you will set simulator options to control the simulation process.

1. In the SAE window, choose **Simulation → Options (O)** to open the **Simulation Options** dialog box.
2. Set the RUNLVL option to level 4.

The **HSPICE Global Simulation Options** dialog box should look as follows.



3. Click **OK** to apply settings.

Task 10. Set up Convergence Aids

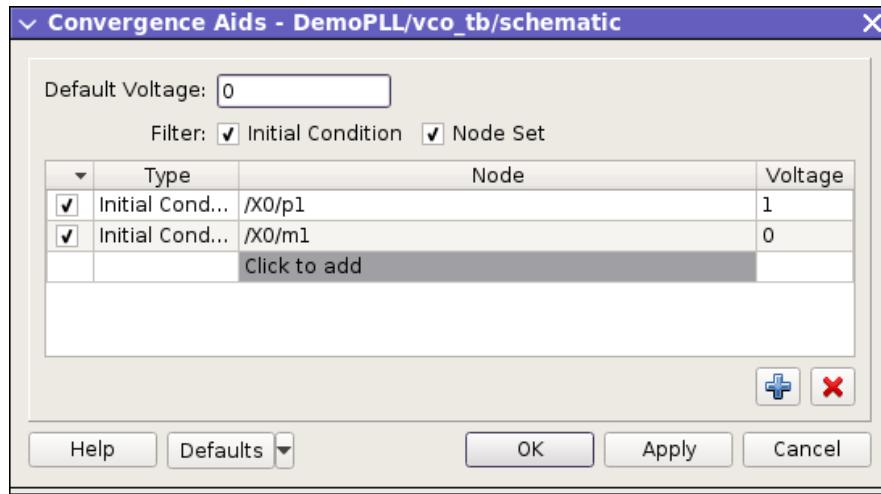
In this task, you will set up the convergence aids to help the simulator converge and provide correct results. Convergence aids are used to set initial conditions for selected circuit nodes.

1. In the SAE main window, choose **Setup → Convergence Aids** to open the Convergence Aids dialog box.
2. Click “**Click to add**”, and then click the Select in Design icon to select a node from the design.

The Schematic Editor opens so you can choose a net from the design.

3. Descend into the vco block and select the nets **p1** and **m1**. Press Esc to exit the command.

- For the net /X0/p1, set **Voltage** to 1. For the net /X0/m1, set **Voltage** to 0.



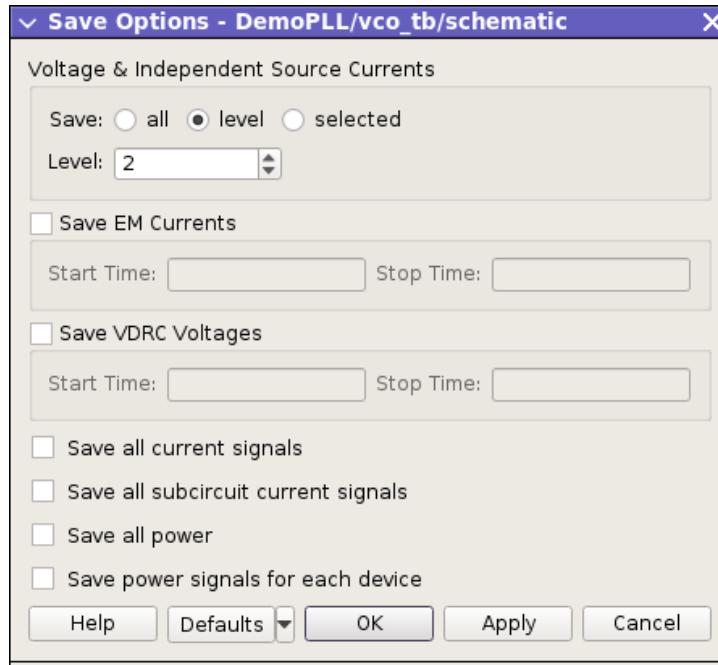
- Click OK to apply changes.

Task 11. Set Up Save Options

In this task you will set save options to control number of saving signals.

- In the SAE window, choose **Outputs → Save Options** to open the **Save Options** dialog box.
- Set the Level option to level 2.

The **Save Options** dialog box should look as follows.



- Click **OK** to apply settings.

Task 12. Netlist the Design

In this task, you will generate the netlist for the *vco_tb* schematic testbench.

The next step in the design cycle is to generate the final netlist of the circuit testbench. This netlist will be the input to the simulator. The simulation run will be used to verify the electrical performance and the functionality of the circuit.

1. In the SAE main window, choose **Simulation → Netlist → Create (N)** to generate the netlist.

The final netlist is created and opened in the Custom Compiler Text Viewer window.

Question 3. What is the default location and filename of the structural netlist and final netlist that were created?

2. Choose **File → Close Window** to Close the Custom Compiler Text Viewer.

Task 13. Simulate the Design

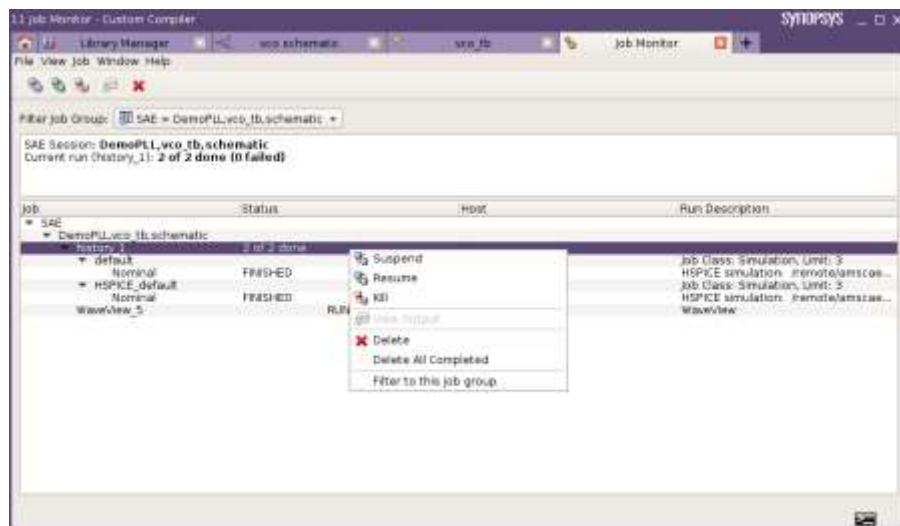
In this task, you will simulate the *vco_tb* circuit using the HSPICE simulator.

Once all of the inputs and outputs are defined in SAE, the simulation can be run.

1. In the SAE window launch **Save Options** dialog with **Outputs->Save Options** and set "all" value for Save option.
2. Choose **Simulation → Run** to start the simulation.

The HSPICE simulator is launched in the specified run directory (by default it is *~/simulation*).

3. The Job Monitor is launched to show the simulation progress.



Note that from CSM menu you can suspend/resume or kill the job, view simulation output log file.

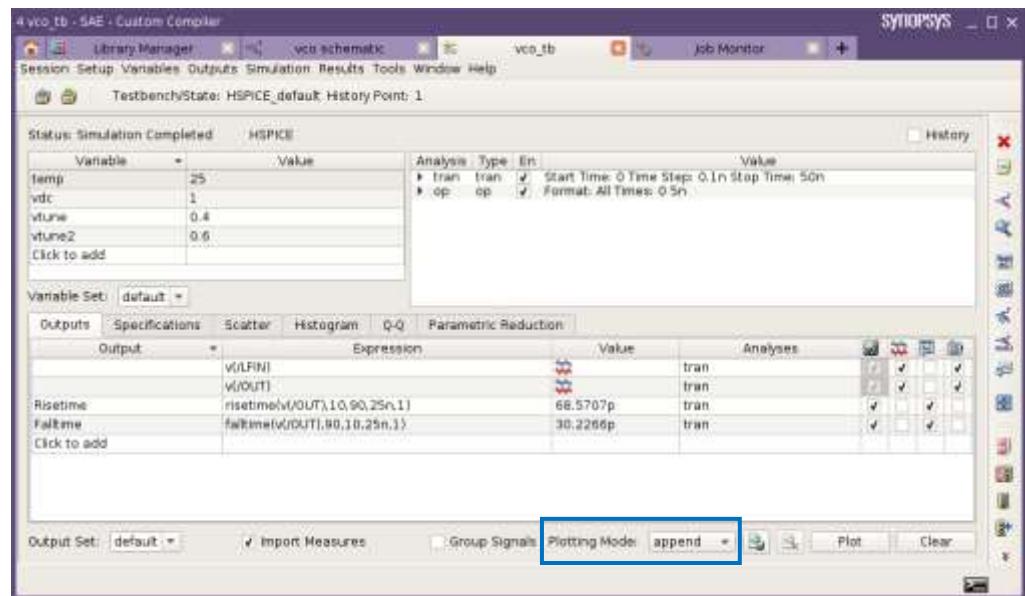
4. Observe that after the simulation has completed, the two output signals of the VCO circuit named OUT and LFIN are plotted automatically in WaveView.

Outputs appear in the outputs section of the SAE window. They can be signal waveforms, expressions that evaluate to a scalar number, or expressions that evaluate to a waveform.

Task 14. Probe Waveforms Using WaveView

After the simulation is complete, you can analyze and debug the results by probing other signals in WaveView.

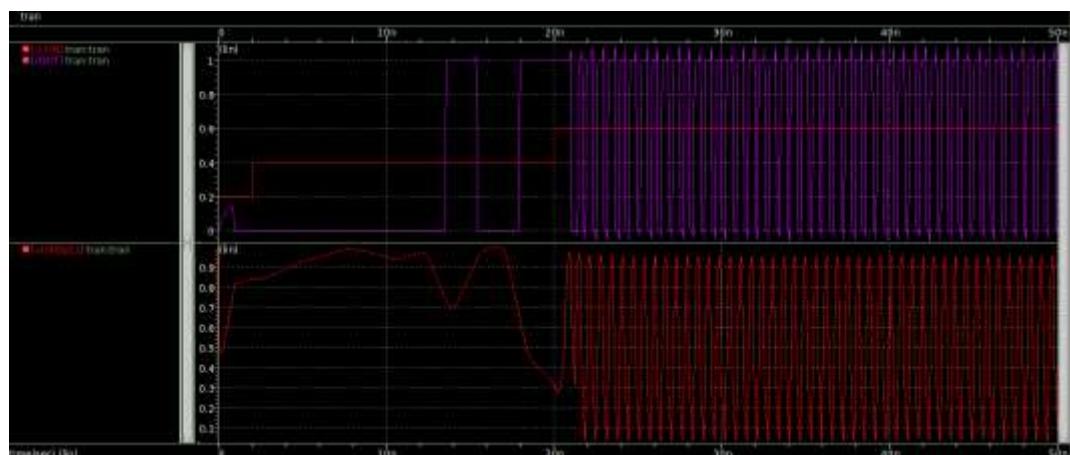
1. In the SAE main window, change the **Plotting Mode** to **append**.



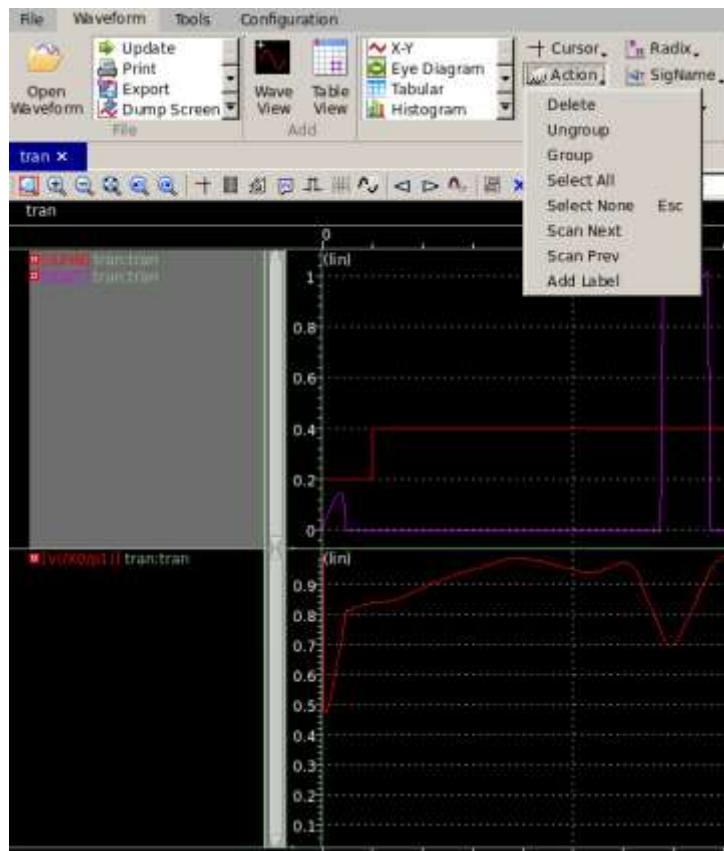
- Choose **Results → Plot Signal → Transient Signal** to plot the waveform of the amplifier output signal **p1** (at 1X hierarchy depth).

The transient voltage waveform at node **/X0/p1** is plotted and appended in the existing WaveView window.

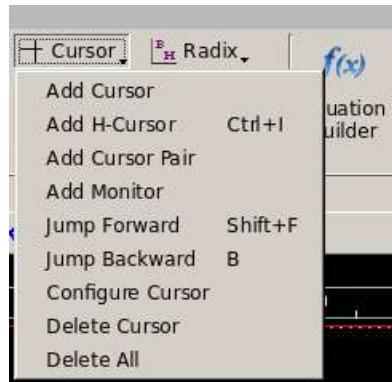
The WaveView window should look as follows:



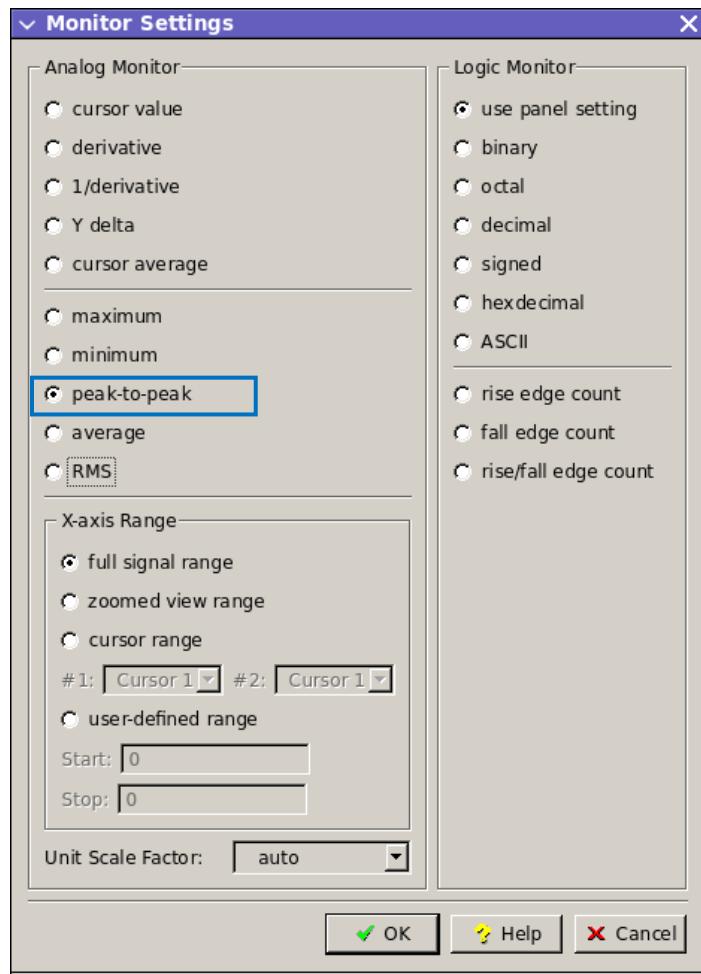
- Click on first pane and choose **Action→Ungroup** to ungroup signals



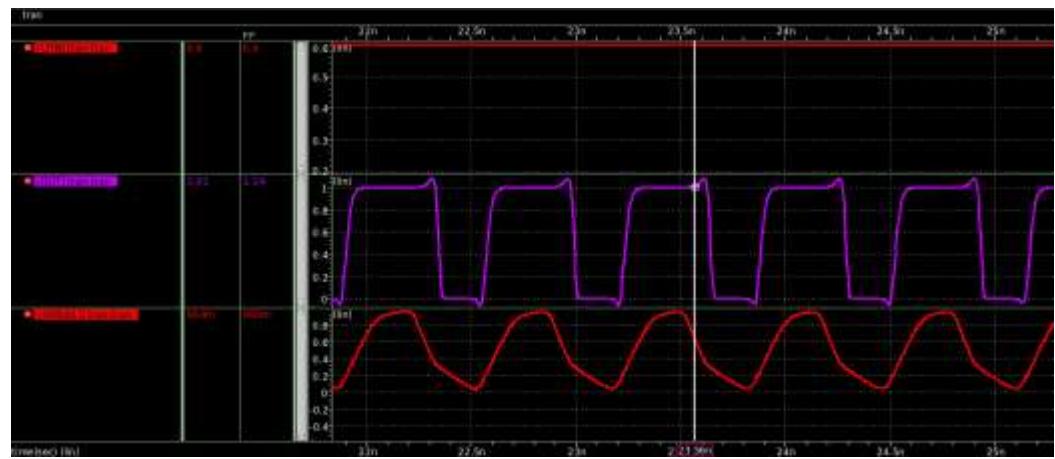
4. Zoom on the x-axis to view sections from 22n to 25n.
5. Choose **Cursor → Add Cursor** to add a cursor.



6. Choose **Cursor → Add Monitor** to add peak-to-peak monitors.



At this point, the WaveView window should look as follows:



- Choose **File → Exit** to close the WaveView window.

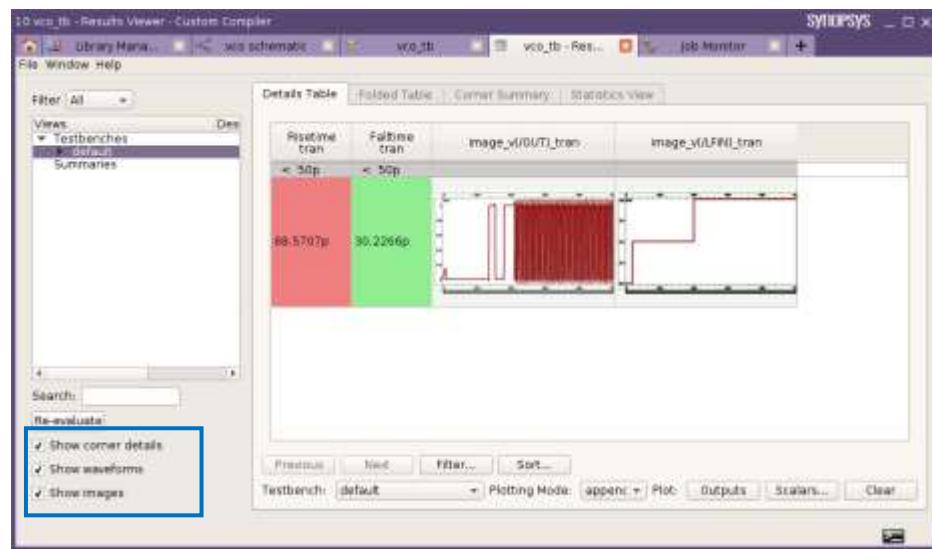
Task 15. View Results in the Results Viewer

In this task you will use the Results Viewer to view simulation results.

1. in SAE window choose **Results→Viewer** to open the Results Viewer.

The Results Viewer shows a summary for all measurements and the number of specification violations.

2. Click on the testbench **default** and check the **Show Images** checkbox.



3. Double-click an image thumbnail to open a larger image.
4. Close the Results Viewer.

Task 16. Back-Annotate the Results

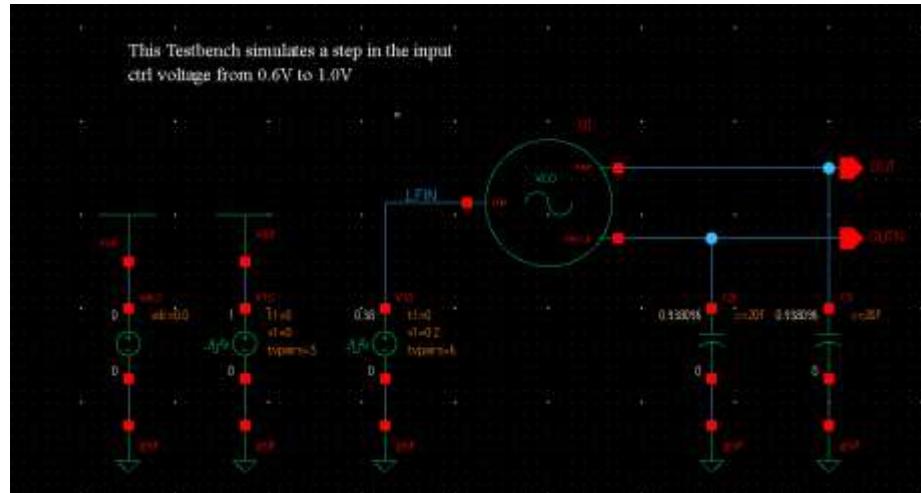
In this task, you will learn to back-annotate the results to the schematic.

1. From the SAE window, choose **Results → Annotate → Transient Node Voltages** to back-annotate the instantaneous transient node voltages onto the schematic.

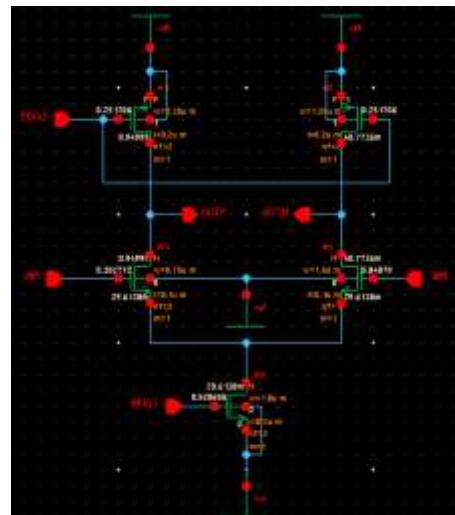
The **Backannotate Transient Node Voltage** dialog box opens, prompting you for the instant in time you wish to probe.

2. Set the **Time Point** to **35n** seconds and click **OK**.

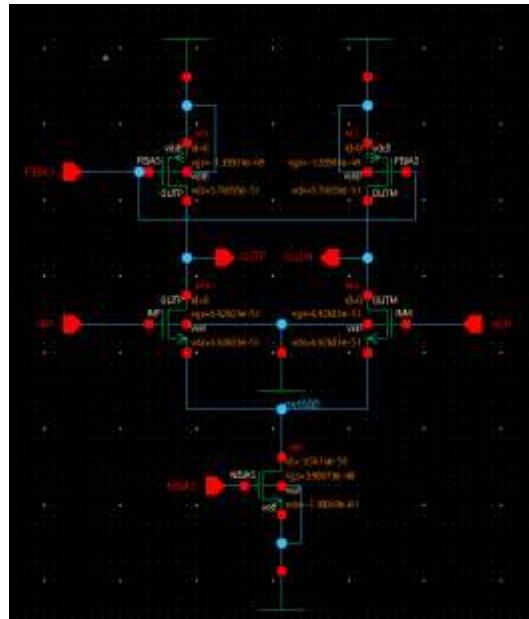
The instantaneous node voltages from the transient simulation at the time point **35n** are annotated onto the schematic. At this point, your Schematic Editor (SE) window should look as follows:



3. In the SE window, descend into the **vco** block and then into the **amp** block. The schematic for the **amp** block should look as follows:



4. Follow the same steps to back-annotate the DC Operating Point onto the schematic. At this point, the SE window should look as follows:



- Choose **Results** → **Annotate** → **Clear Annotations** to clear the annotation results using.

Task 17. Print the Results

In this task, you will print the DC operating points to a file to be further processed and analyzed.

- From the SAE window, choose **Results** → **Print** → **DC Operating Points** to print the DC operating point of the **pmos** instance **m1** in the amplifier block.
You will be prompted to select the instance in the schematic.
- As you click on the **m1** instance, the **DC Operating Points** dialog box opens with a table showing all of the DC operating information for the **m1** instance.
- Similarly, click on the other instances **m2**, **m3**, **m4**, **m5** and observe what happens.
- At this point, the **DC Operating Points** dialog box should look as follows:

	cgtot	vod	vth	cbtot	region	cgs	id
/X0/4/m1	13.2778f	-0.728415	-0.265530	2.72716f	2.0	1.05402f	0.142530m
/X0/4/m2	4.72454f	0.425048	-0.419190	4.62519f	0	0.983390f	11.1610z
/X0/4/m3	1.72206f	-0.427695	0.482179	2.40526f	0	0.623143f	1.34699n
/X0/4/m4	1.92251f	-0.459755	0.470229	2.70621f	0	0.560065f	-0.610423n

- Click **Export CSV** to save the DC operating points to a file with the name **amp_dc.txt**.
- Close the **DC Operating Points** dialog when finished.

7. In the UNIX terminal, open the file **amp_dc.txt** using a text editor, such as vim or emacs. Observe the contents of the file.

Task 18. Save the Simulation Setup as an SAE State

In this task, you will save the setup associated with the current session as an SAE state. This allows you to use this setup at a later time.

An SAE state is a collection of files that captures all settings in a testbench. Once states are named, a directory is also created with that name, in which the various files and settings are stored. Individual state files are saved in XML format and are named so that you can identify the type of information included in each file.

1. From SAE window, choose **Session → Save State** to save the state with the name *simulationSetup* into an OpenAccess database, (**Hint:** Set the **To** option to **OpenAccess**.)
2. Click the **OK** button to save the state.

By default, the **States Directory** is selected under the **To** options.

Question 4. What are the available categories during **Save State** and why?

Question 5. What do you see in Library Manager in *DemoPLL/vco_tb* cell after saving the state?

3. Choose **Session → Close** to close the SAE session.
4. Close the VCO testbench *vco_tb* schematic.

Congratulations!

You have successfully completed the simulation setup using SAE to verify the VCO design using HSPICE!

Answers and Solutions

Task 7. Set Up the Analysis

Question 1. What do you observe when you apply the settings?

- As you apply each setting, it appears in the SAE main window under the **Analysis** section.

Task 8. Set Up Outputs

Question 2. Which command is invoked in the Schematic Editor?

- The **Pick Object** command is invoked, which allows you to select the signals you want to plot.

Task 12. Netlist the Design

Question 3. What is the default location and filename of the structural netlist and final netlist that were created?

- Default location is
~/simulation/DemoPLL,vco_tb,schematic/history_1/simulation/HSPICE_default/HSPICE/nominal/netlist
- Structural netlist file name is netlist
- Final netlist file name is input.spi

Task 18. Save the Simulation Setup as an SAE State

Question 4. What are the available categories during **Save State** and why?

- There is a total of 23 categories, out of which only 8 are enabled. These are: **Analyses, Convergence Aids, Design Variables, Models, Mosra, Options, Outputs** and **Save Options**.
- Only these categories are enabled because the options for only these categories are set during the complete simulation setup.

Question 5. What do you see in Library Manager in *DemoPLL/vco_tb* cell after saving the state?

1. A new view, *simulationSetup*, appears under the *DemoPLL/vco_tb* cell.

2

2. Results Analyzer

Learning Objectives

In this lab, you will learn how to:

- Use the Results Analyzer to create your own expressions for measurement
- Measure the results of an Operational amplifier circuit to verify its small and large signal performance
- Post-process and analyze the results

Lab Duration:
30 minutes

Before You Start

Make sure you have the following:

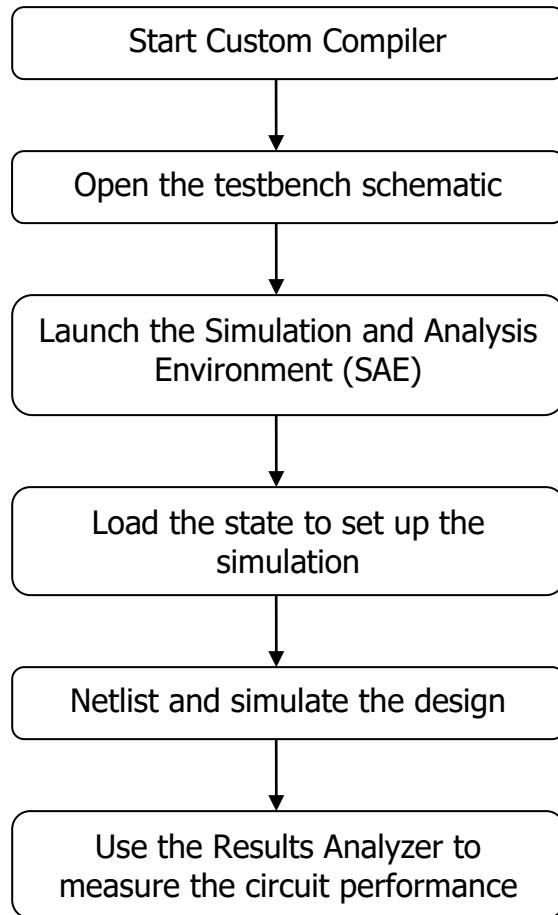
Item	Description	Location
HSPICE O-2018.09	Software	Installed on the server
Custom Explorer O-2018.09	Software	Installed on the server
SAE_ResultsAnalyses_Lab1: analogCircuits lib.defs	Lab data folder: OpenAccess design library, containing the test bench of an <i>Opamp</i> design for small signal analysis Library definition file	The directory where you unpacked the lab data

Before verifying the performance of the circuit, it is important to understand the use model of the commands that are required to verify it.

Refer to the *Custom Compiler Simulation and Environment User Guide* for the commands that are used in this lab.

Flow Overview

Lab 1 Tasks



Instructions

Task 19. Start Custom Compiler

2. In the UNIX window, change the directory to *SAE_ResultsAnalyses_Lab1*.
3. Start Custom Compiler from the UNIX prompt.

```
Unix% cd SAE_ResultsAnalyses_Simulation_Lab1  
Unix% custom_compiler &
```

Task 20. Open the Testbench Circuit

4. From the design library *analogCircuits*, open the cell view *Tb_Opamp/schematic*.

Note: The *Tb_Opamp* schematic cell view opens in a Schematic Editor window.

Task 21. Launch the Simulation and Analysis Environment

5. Invoke the Simulation and Analysis Environment using **Tools → SAE** from the Schematic Editor window.

Note: This opens the Simulation and Environment (SAE) window, which comes with the design *analogCircuits/Tb_Opamp/schematic* pre-populated.

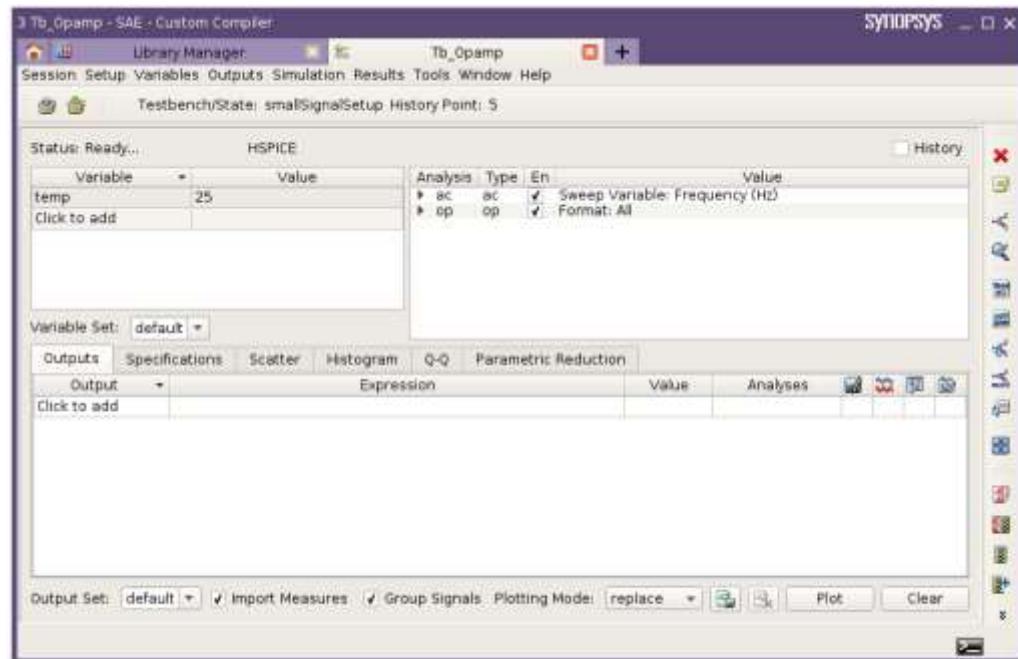
Task 22. Load the State

In this task, you will load the simulation setup for *Tb_Opamp*, where you will perform an AC analysis to verify the small signal performance of the circuit.

6. In the SAE window, choose **Session → Load State** to open the **Load State** dialog box. Choose the OpenAccess database and click **OK** to load the state *smallSignalSetup*.

Note: This loads all the categories which are saved during the time of saving the state.

7. The SAE window should look as follows:

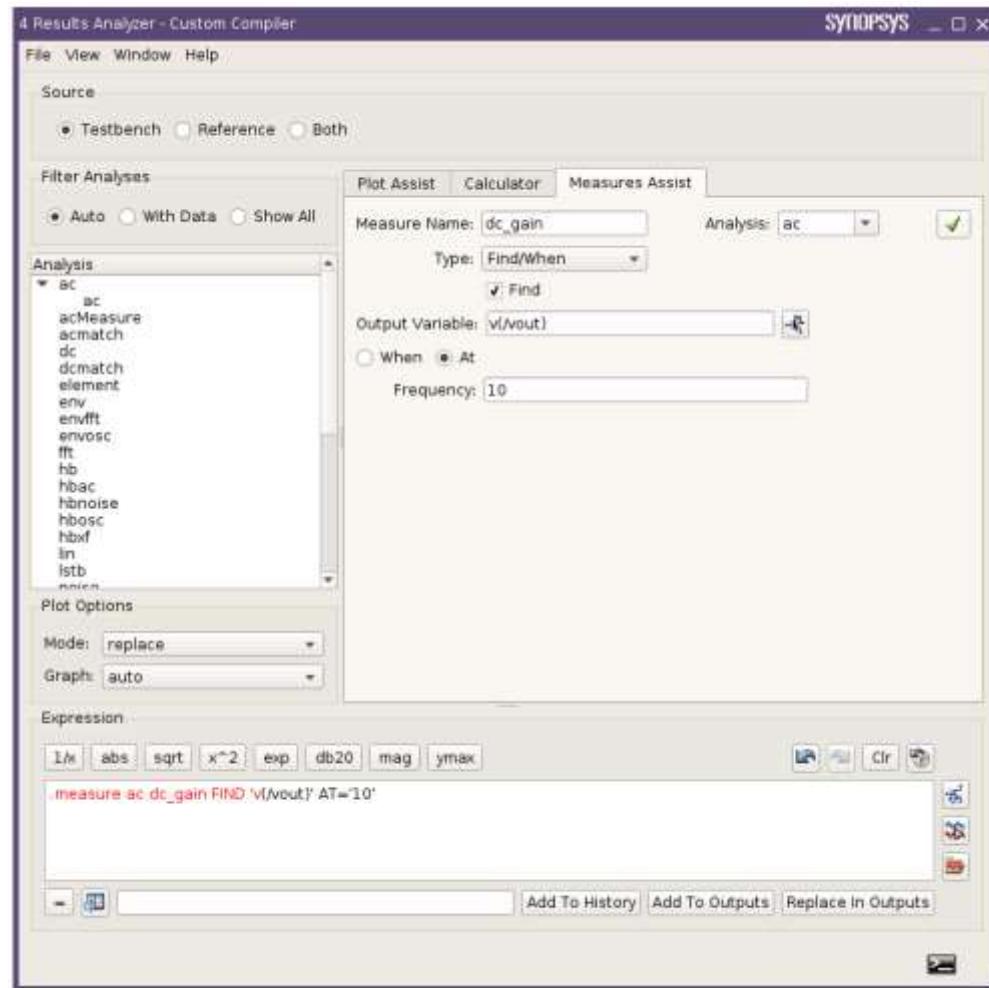


Task 23. Create HSPICE Measurements

In this task you will create HSPICE measure statements using the SAE Results Analyzer.

8. In the SAE window, choose **Results → Analyzer** to open the Results Analyzer dialog box.
9. Switch to the **Measures Assist** tab.
10. Type **dc_gain** as the **Measure Name**.
11. Select **ac** for **Analysis**.
12. Select **Find/When** for **Type**.
13. Click **Pick from Schematic** . The schematic view opens in Pick mode. Pick the net **vout**, which then populates the Output Variable in the Results Analyzer.
14. Choose **At** and type **10** for **Frequency**.
15. Click to create a measurement.

At this point Results Analyzer should look as follows:

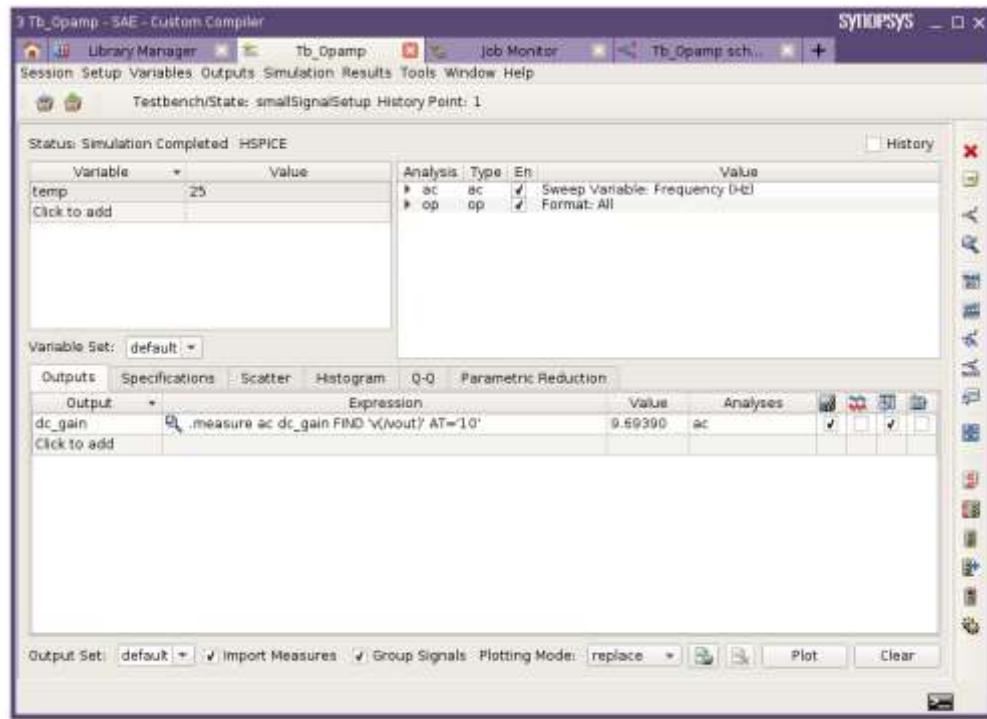


16. Click **Add to Outputs** to add the measurement to the SAE outputs pane.
17. Close the Results Analyzer.

Task 24. Netlist and Simulate the Design

In this task, you will netlist and simulate the *Opamp* schematic.

18. Choose **Simulation → Netlist and Run** to generate the netlist and simulate the design.
Note: The Job Monitor opens in a new tab so you can monitor the progress. If the simulation is failing, you can double-click on the job to open the Text Viewer and view the simulation log files.
19. After simulation you will see the measured value in the SAE **Outputs** tab.



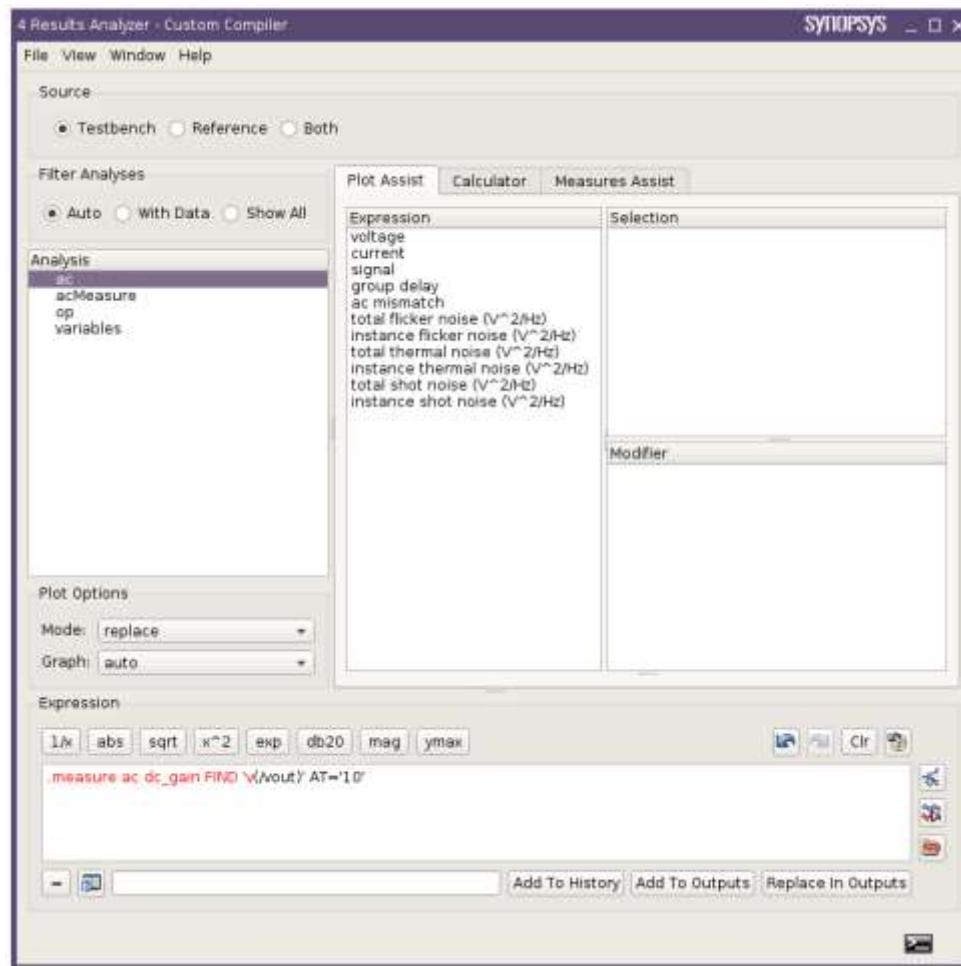
Task 25. Analyze Results using the Results Analyzer

Once the simulation is finished, the next step is to view the waveforms in the Waveform Viewer to analyze the results.

In this task, you will measure the results using the Results Analyzer to verify the small signal performance of the Opamp circuit. You will measure the following specifications for small signal analysis.

- Small-signal gain, Av
 - 3dB-Bandwidth, BW
 - Phase Margin, PM
- 20.** In the SAE window, choose **Results → Analyzer** to open the Results Analyzer.

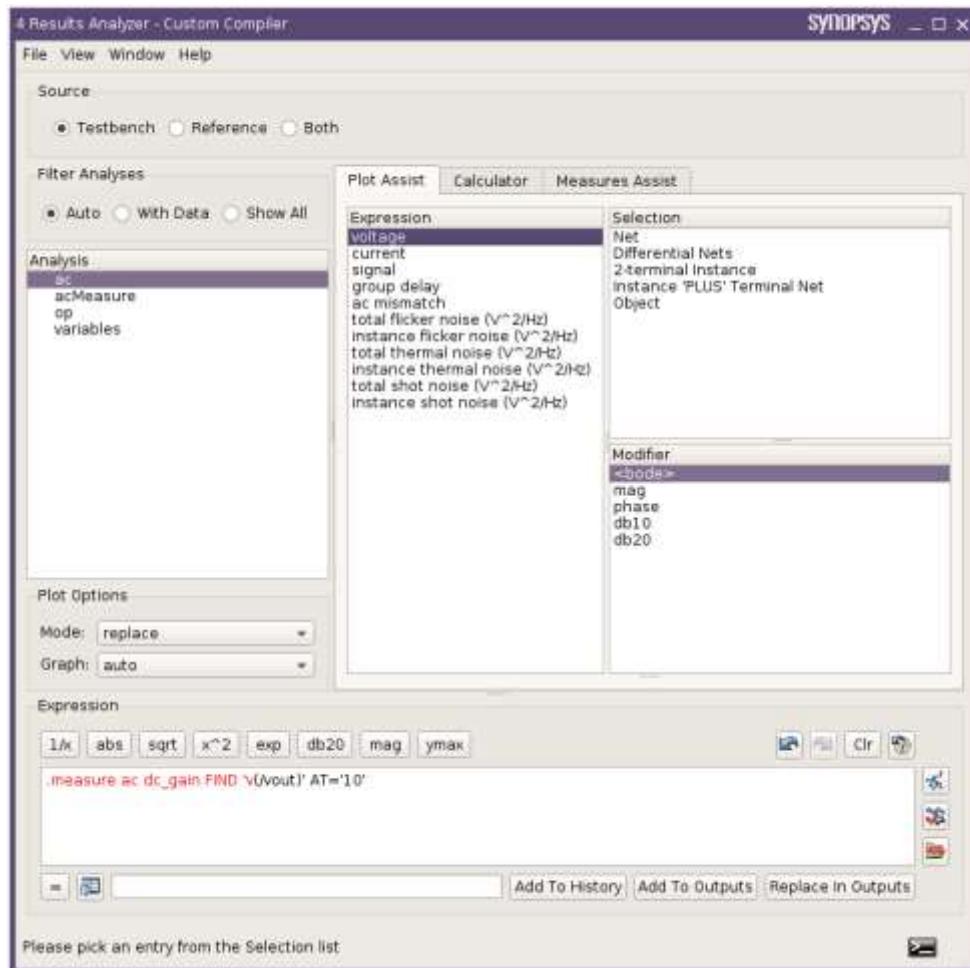
Note: Note that Filter Analyses setting is set to **Auto** by default, which shows only analyses with available data.



21. In the **Plot Assist** tab, select **voltage** for the **Expression**.

Note: When you select **voltage**, different options appear in the **Selection** and **Modifier** panes. In the **Modifier** pane, bode plot, <bode> is selected by default.

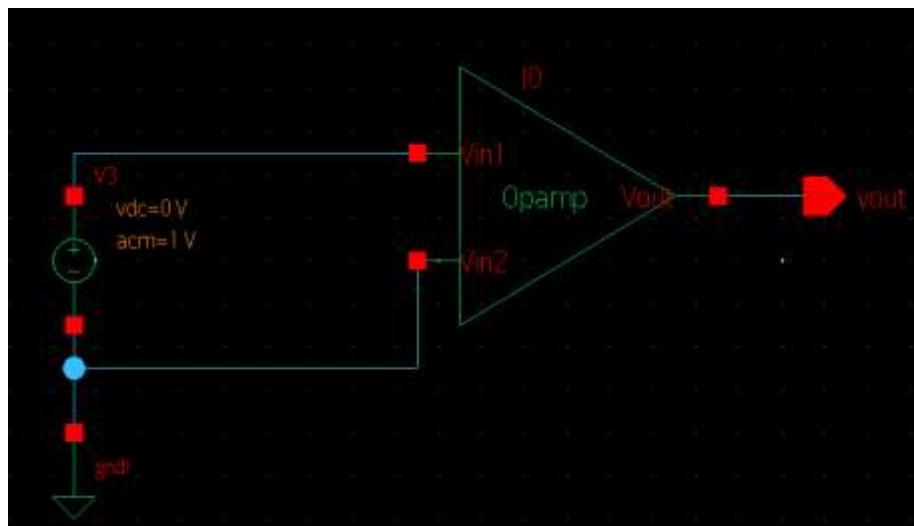
22. At this point, the Results Analyzer should look as follows:



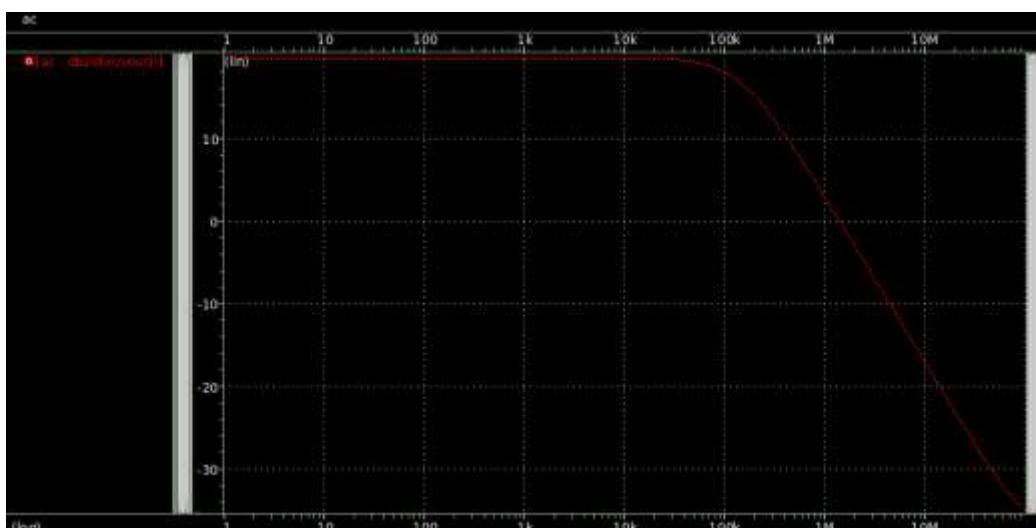
23. Double-click on **Net** for the **Selection**.

Note: This prompts you to select the net in the *TB_Opamp* schematic.

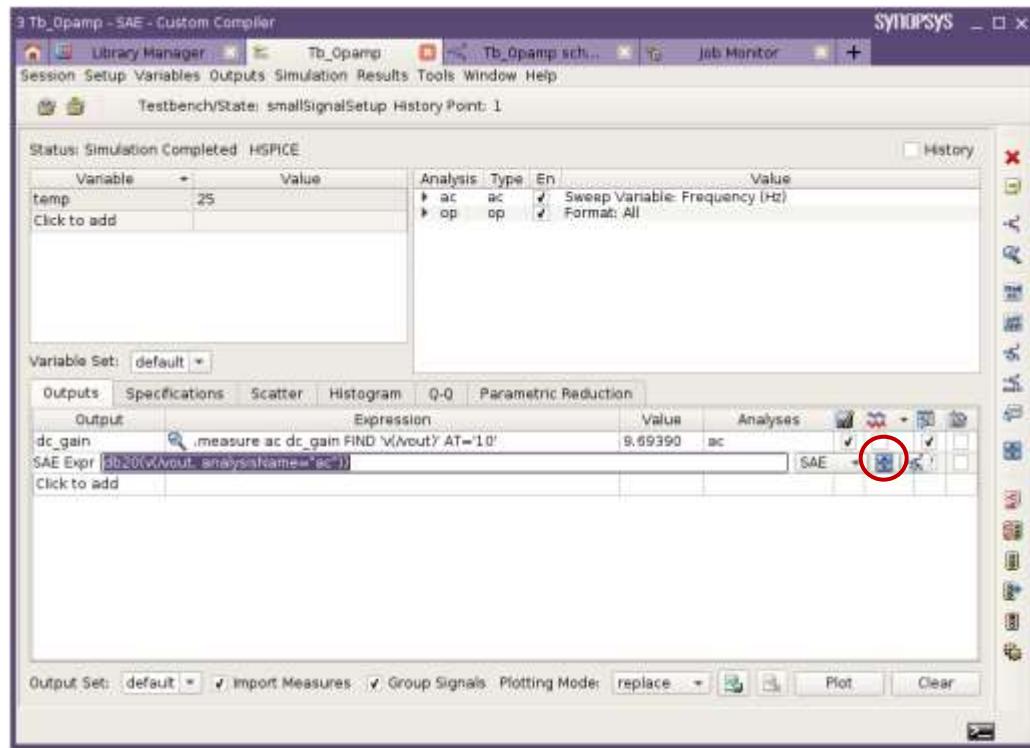
24. Select the net *vout* in the schematic and press Esc to exit the **Pick Object** command.



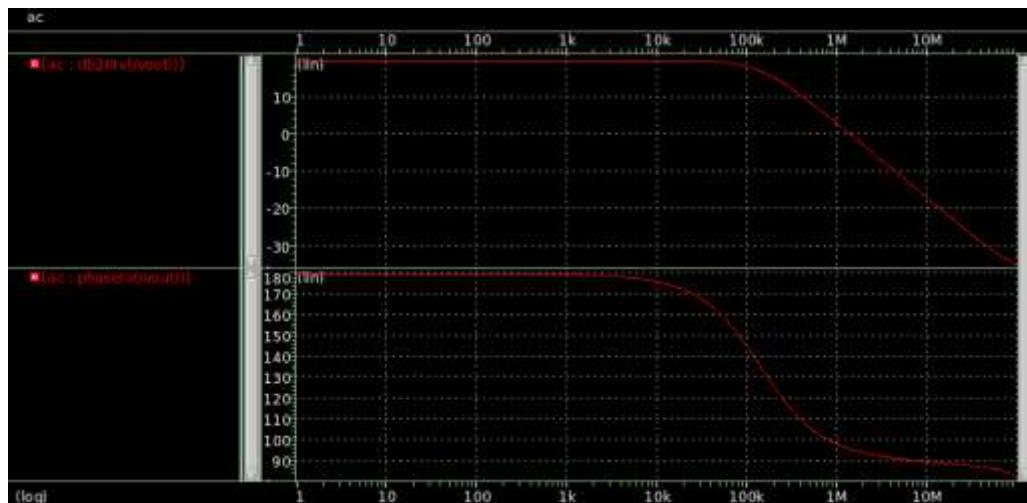
25. In the Results Analyzer dialog box, select **db20** in the **Modifier** pane. In the **Expression** section below the **Plot Assist** tab, the expression becomes $db20(v / v_{out})$.
26. Under the expression, click the $=$ button. This plots the magnitude plot in dB. The image should look as shown below.



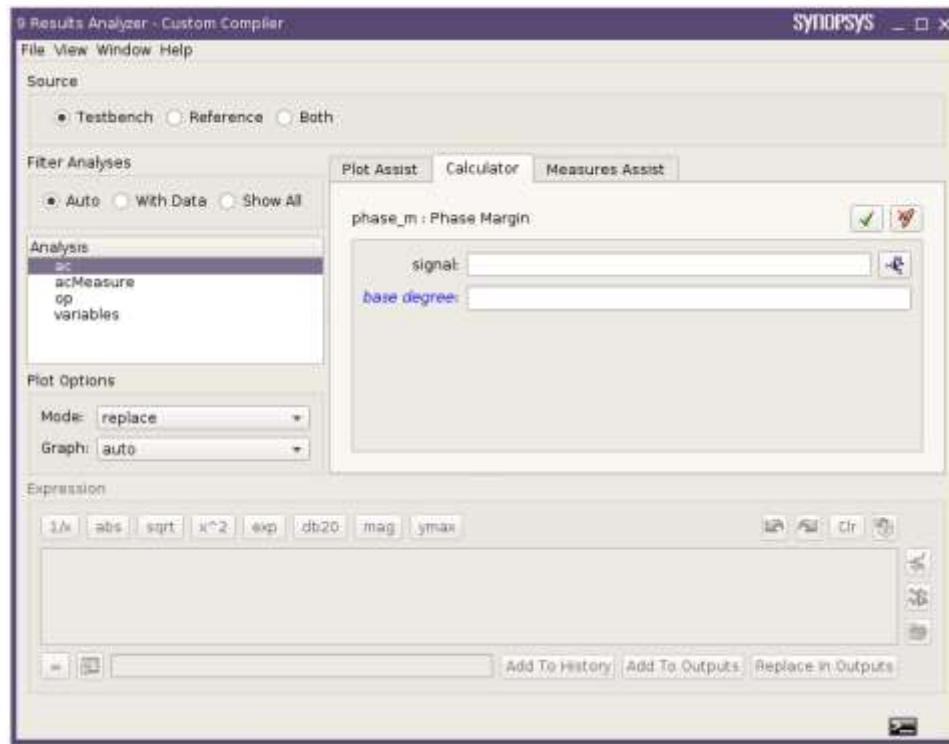
27. In the Results Analyzer, click **Add To Outputs**.
- Note:** This adds the expression in the **Outputs** tab of the SAE window.
28. In order to measure the gain, click in the db20 **Expression** cell in the **Outputs** tab to show the **Launch Calculator** icon. Click **Launch Calculator** to open the Calculator in the Results Analyzer dialog box.



29. In the Calculator find and double-click on **ymax** function, click the green check mark to apply the function to the new expression.
30. Click button.
31. In the Results Analyzer, click **Add To Outputs**.
32. Switch to **Plot Assist** tab.
33. To plot the phase, in the **Modifier** pane select **phase**, from Selection pane double click on **Net**. You will be prompted to select a net from schematic.
34. Select net **vout**. Phase will be plotted in WaveView.



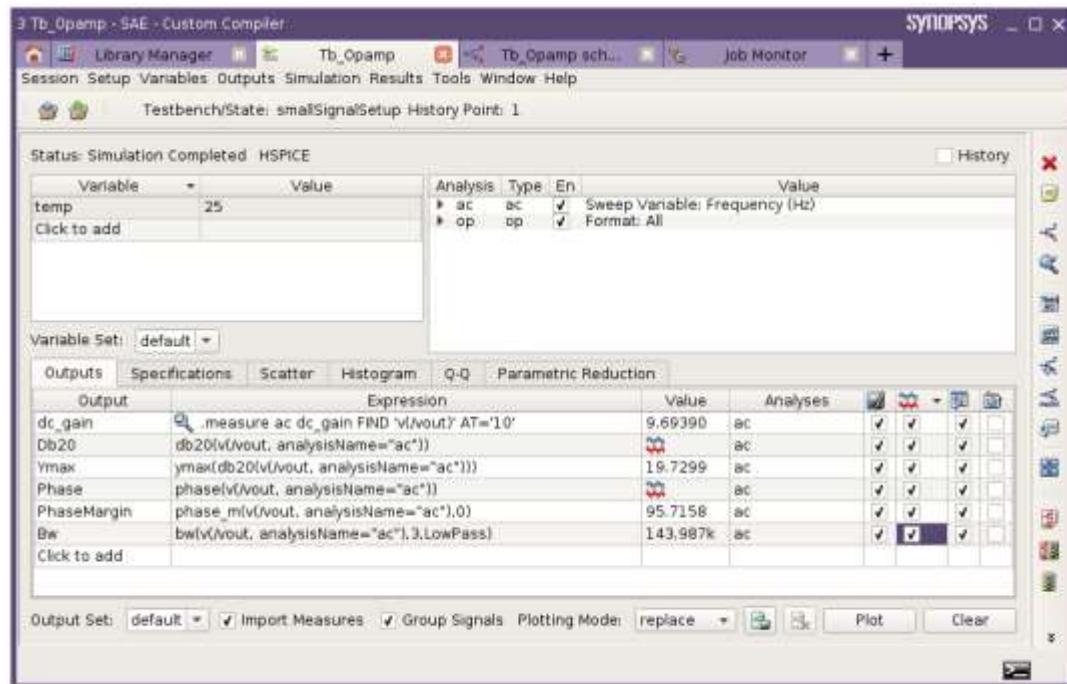
35. In the Results Analyzer, click **Add To Outputs**.
36. Click **Clr** to clear the expression in the **Expression** field in Results Analyzer dialog.
37. Switch to the **Calculator** tab. Now you will use the calculator to measure the phase margin and 3-db Bandwidth.,
38. Select the **Category** as **Measure**.
39. Double-click on the **phase_m** function.



40. Click the button next to the **signal** field.
Note: This will prompt you to pick the signal from the schematic.
41. Pick the output signal **vout** in the schematic.
42. Specify **0** for **base degree**.
43. Click the green check mark button.
Note: The phase margin expression is added to the **Expression** field.
44. Click button to measure the phase margin.
45. In the Results Analyzer, click **Add To Outputs**.
46. Follow steps from 21 to 25 and similarly measure the 3-db Bandwidth of the circuit.

Hint: From the calculator, use *bw* and set the **db bound** value as 3 and **band type** as LowPass.

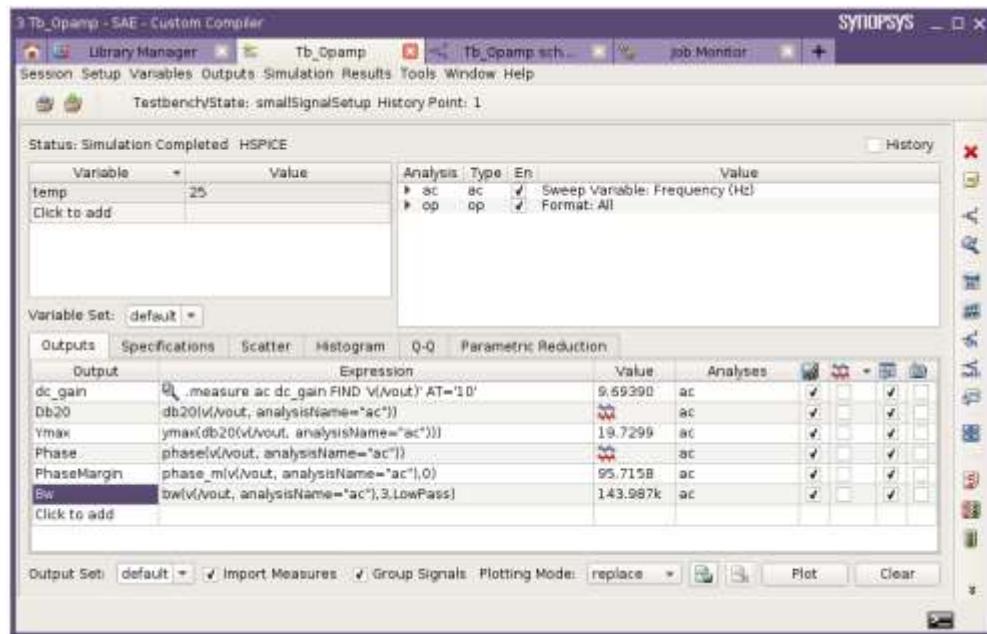
47. In the Results Analyzer, click **Add To Outputs**.
48. Close the Results Analyzer dialog box and WaveView.
49. Enable plotting for all expressions.
50. Choose **Simulation → Run** to run the simulation again.
51. The SAE main window should look like the following image after the simulation finishes. All the measurements are added to the output section, which can be saved and plotted at any point in time.



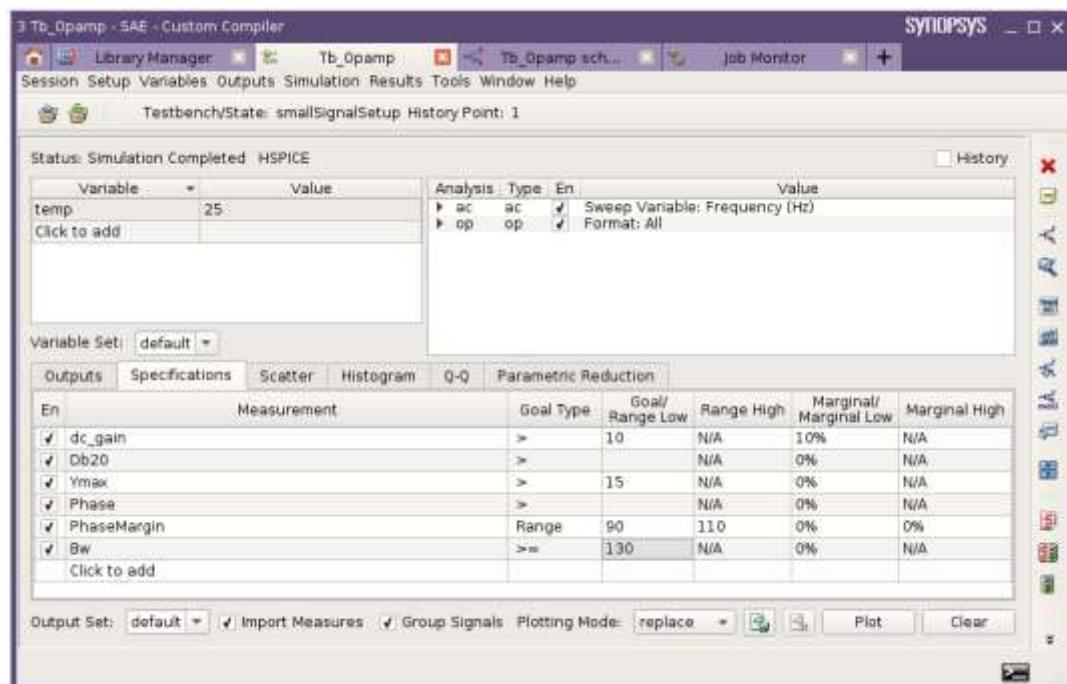
Task 26. Analyze Measurement Results

In this task you will analyze the measurement results, which were created in the previous task. You will set specifications on the measurement values and see their statuses.

52. In the main SAE window, specify names for the measurements that were configured in the previous task, as shown in the following screen capture.



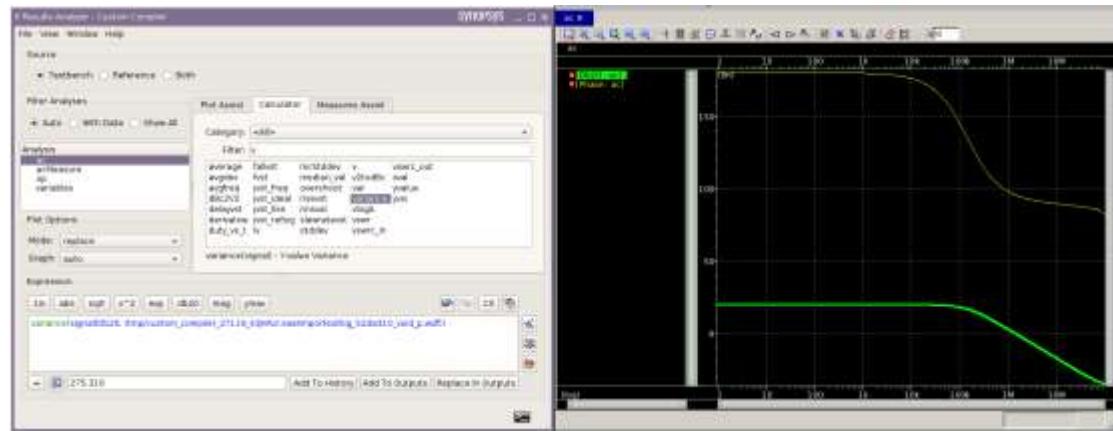
53. Switch to the **Specifications** tab in the SAE. All Results Analyzer measurements appear in this tab, and you have the option to specify goal and marginal values for the measurements.



Task 27. More Features in the Results Analyzer

In this section, you will become familiar with other features of the Results Analyzer that allow you to perform more advanced analyses on simulation results.

54. In the main SAE window, which was configured in the previous task, choose **Results → Analyzer** to open the Results Analyzer.
55. Click **Pick from Waveform Viewer** , which is located to the right of the **Expression** field in Results Analyzer dialog.
56. Select **DB20** signal from WaveView. Notice that the vout signal appears in the **Expression** field.



57. Select **variance** from calculator functions and measure the variance of the v(out) signal magnitude.
58. Click **Evaluate/Tabulate**  to see the **Variance** value in a separate window.

Note: **Pick from Signal Browser**  allows you to select the signal from the Waveform Viewer signal browser field.

Congratulations!

You have successfully analyzed the small-signal performance of an Opamp design using the Results Analyzer.

3

Parametric Analysis

Learning Objectives

The main goal of this lab is to familiarize you with the parametric analysis to optimize the circuit performance.

After completing this lab, you should be able to:

- Setup parametric analysis
- Run parametric analysis
- Analyze the results

Lab Duration:
20 minutes

Introduction

During this lab, you will use parametric analysis to analyze the Operational Amplifier design with varying set of parameters.

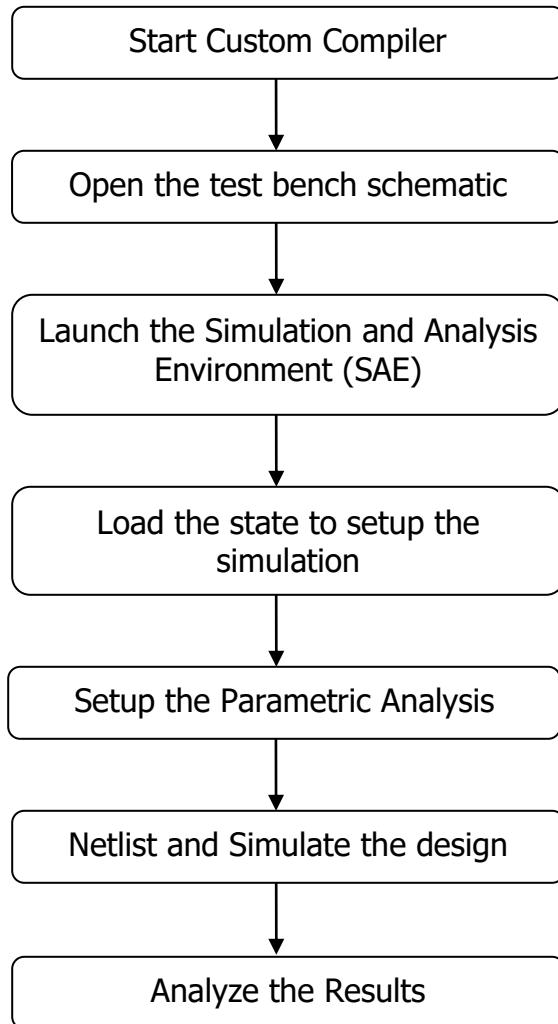
In this lab, you are provided with the *analogCircuits* OpenAccess database library and a *lib.defs* file. The *analogCircuits* library contains the Operational Amplifier testbench *TB_Opamp*. You will make use of this testbench to optimize the circuit performance. The *lib.defs* is the default library definition file that contains library name mapping to their physical location.

Before verifying the performance of the circuit, it is important to understand the use model of the commands that are required to verify it.

Please refer to the *Simulation and Environment User Guide* for the commands that are used in this lab.

Flow Overview

Lab 1 Tasks



File Locations

All files for this lab are located in the directory *SAE_ParametricAnalysis_Lab1*.

Directory Structure

SAE_ParametricAnalysis_Lab1

Current working directory

analogCircuits

OpenAccess Design library

Relevant Files

lib.defs

Library Definitions file

Answers & Solutions

There is an *ANSWERS / SOLUTIONS* section at the end of this lab. You are **encouraged** to refer to this section often to verify your answers, or to obtain help with the execution of some steps.

Tool Versions

Custom Compiler	O-2018.09-SP1
HSPICE	O-2018.09-SP1
Custom Explorer	O-2018.09-SP1

Instructions

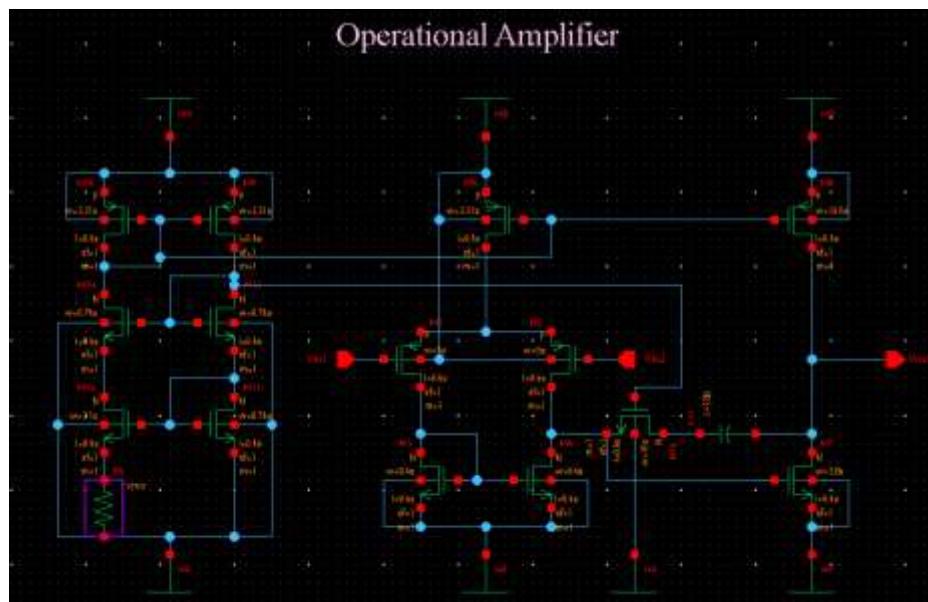
Task 28. Start Custom Compiler

59. In the UNIX terminal window change your current working directory to *SAE_ParametricAnalysis_Lab1*. This will be your working directory for this lab.
60. Start Custom Compiler from the UNIX prompt.

```
custom_compiler &
```

Task 29. Open the Test Bench Circuit

61. From the design library *analogCircuits*, open the schematic cell *Tb_Opamp* of the view name *schematic*.
- Note:** *TB_Opamp* cellView will be opened in a Schematic Editor window.
62. Descend into *I0* Opamp instance and notice the biasing *R6* resistor placed there. During the lab that biasing resistor value will be changed.



Task 30. Launching Simulation and Analysis Environment

63. Invoke the Simulation and Analysis Environment using **Tools → SAE**.
- Note:** This will open up the Simulation and Environment window which comes with design *analogCircuits/TB_Opamp/schematic* pre-populated.

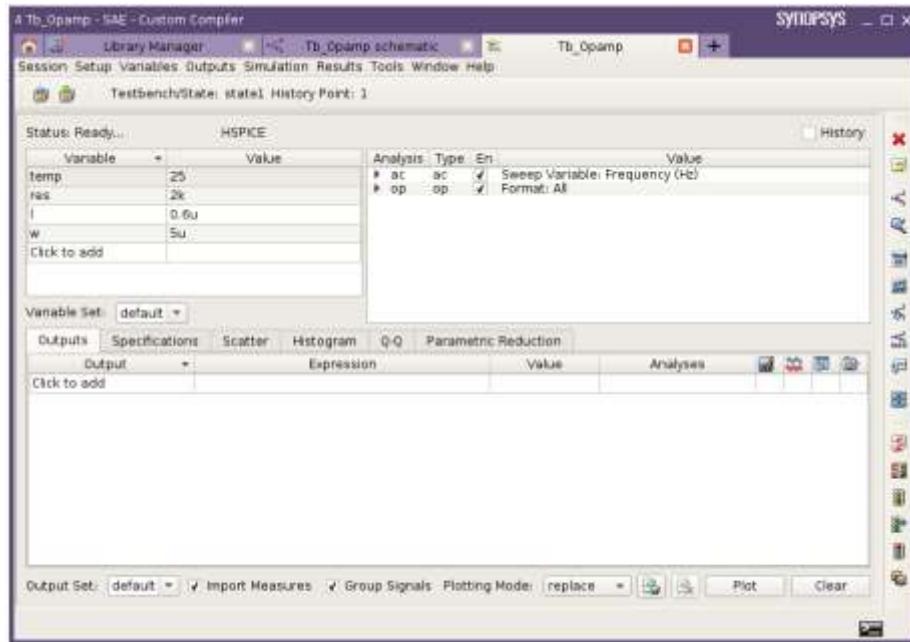
Task 31. Load the State

In this task, you will load the simulation setup for *TB_Opamp* where you will perform the *ac* analysis to verify the signal performance of Operational Amplifier.

64. Load the state *state1* from the OpenAccess database using **Session → Load State....**

Note: It will set up the analyses and model files for simulation.

65. SAE window should look like as shown in the image:



Note: Using **Setup → Model Files** make sure that model path is set up to

```
<path to PDK directory>/PDK/hspice/reference40_models.lib
```

Task 32. Setup the Parametric Analysis

In this task, you will setup the parametric analysis to optimize an Operational Amplifier circuit by varying the biasing resistor value and temperature.

66. Open the Parametric Analyses dialog using **Tools → Parametric Analyses....**
67. Click on **Add new sweep**  button

Note: Add New Sweep dialog will pop up, where you can choose to sweep single variable or to create a data driven sweep.

68. Select **Single Variable** for *Sweep Type* and choose variable **res** from *Variable Name* drop down menu.

69. Fill the form as follows:

a. Under **Range Details**:

i. Enable **Start/Stop**

ii. Set **Start: 2k**

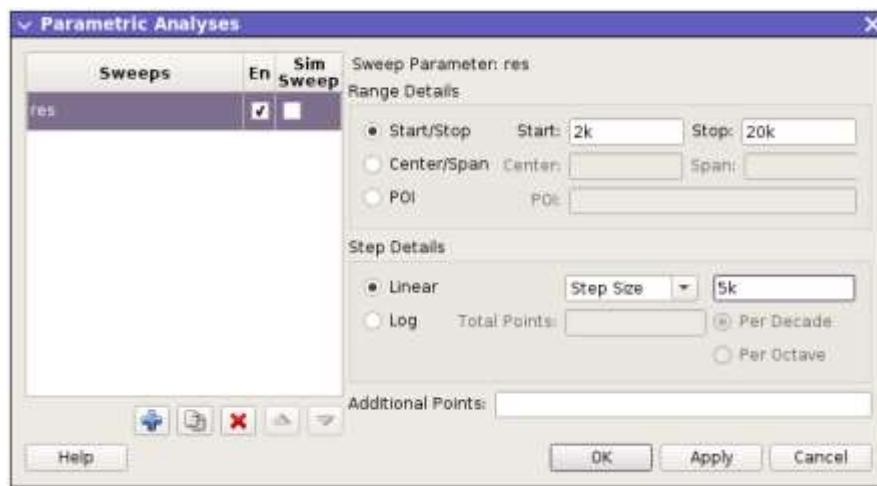
iii. Set **Stop: 20k**

b. Under **Step Details**:

i. Choose **Linear**

ii. Set **Step Size** value to **5k**

70. The Parametric Analyses window should look like as shown in the image:



71. Click **Apply** to add the configured parametric analyze.

72. Click on **Add new sweep** button to add new variable for sweep.

73. Select **Single Variable** for *Sweep Type* and choose variable **temp** from *Variable Name* drop down menu

74. Fill the form as follows:

a. Under **Range Details**:

i. Enable **Start/Stop**

ii. Set **Start: -40**

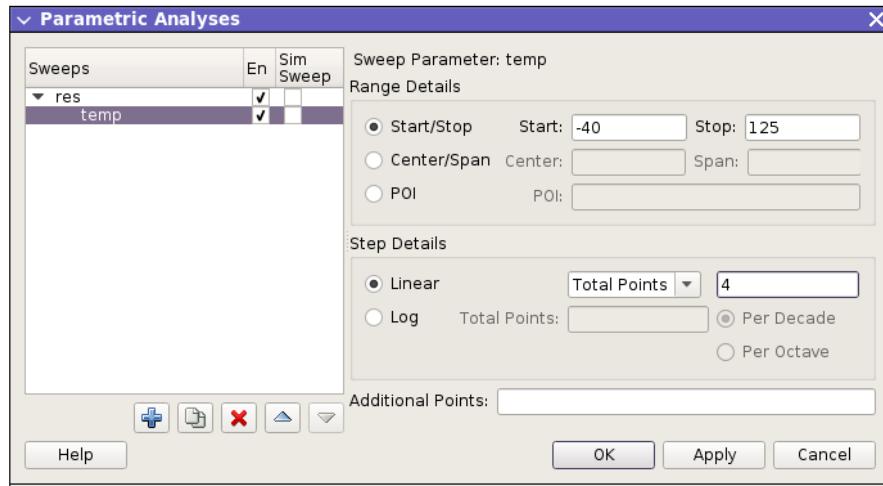
iii. Set **Stop: 125**

b. Under **Step Details**:

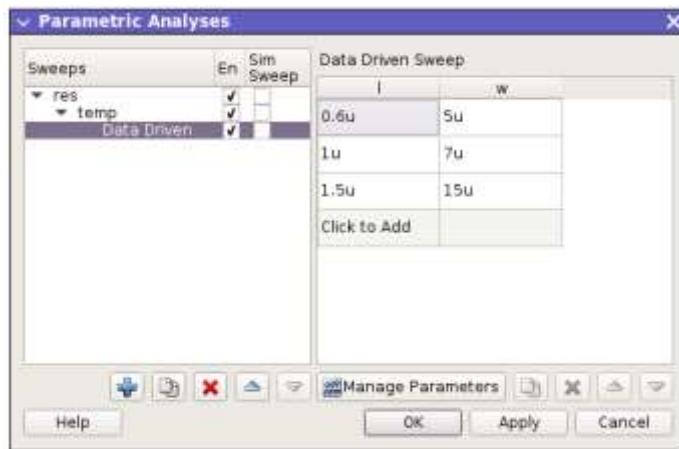
i. Choose **Total Points**

ii. Set Total Points value to 4

75. The Parametric Analyses window should look like as shown in the image:



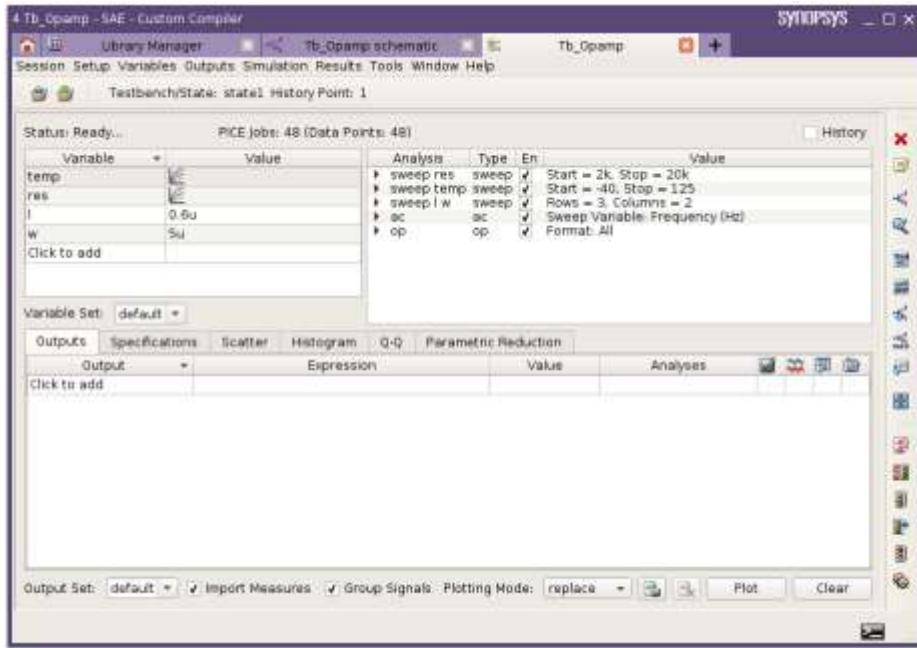
76. Click **Apply** to add the configured parametric analyze.
77. Click on **Add new sweep** button to add new variable for sweep.
78. Select **Data Driven** for *Sweep Type* and enable only w and l parameters.
79. Fill the table as follows.



80. Click **OK**. This will setup the parametric analysis for Operational Amplifier circuit.

Note: The parametric sweep appears in the main SAE window under analysis section.

81. SAE window should look like as shown in the image:



Task 33. Netlist and Simulate the Design

In this task, you will netlist and simulate the *TB_Opamp* schematic with varying biasing resistor values.

82. Generate the netlist and simulate the design using **Simulation → Netlist and Run**.
83. It opens up the **Job Monitor** to see the simulation progress.
84. Close the Custom Compiler Job Monitor.

Task 34. Setup Measurements for Parametric Analysis

In this task, you will measure the results using Results Analyzer to verify the small signal performance of the Opamp circuit. You will measure the following specifications for small signal analysis.

- Small-signal gain, Av
 - 3dB-Bandwidth, BW
 - Phase Margin, PM
85. From the SAE window, open the Results Analyzer using **Results → Analyzer...**
 86. Select the **ac** Analysis.

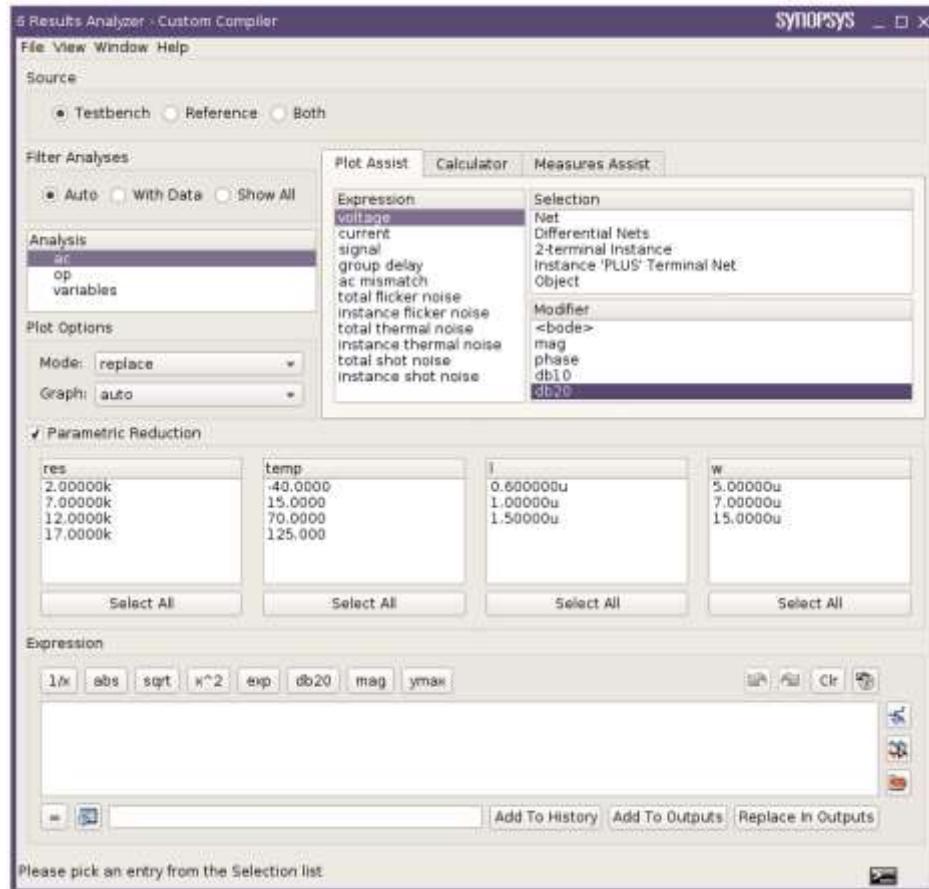
Note: Pay attention that all parameter sweep values are listed under **Parametric Reduction** filed.

87. Under the **Plot Assist** tab select the **Expression** as *voltage*.

Note: As you click on *voltage* different options get appeared in the **Selection** and **Modifier** section. In the Modifier section, bode plot <bode> is selected by default.

88. Select *Modifier* as *db20*.

89. At this point, Results Analyzer will look like as in the image.



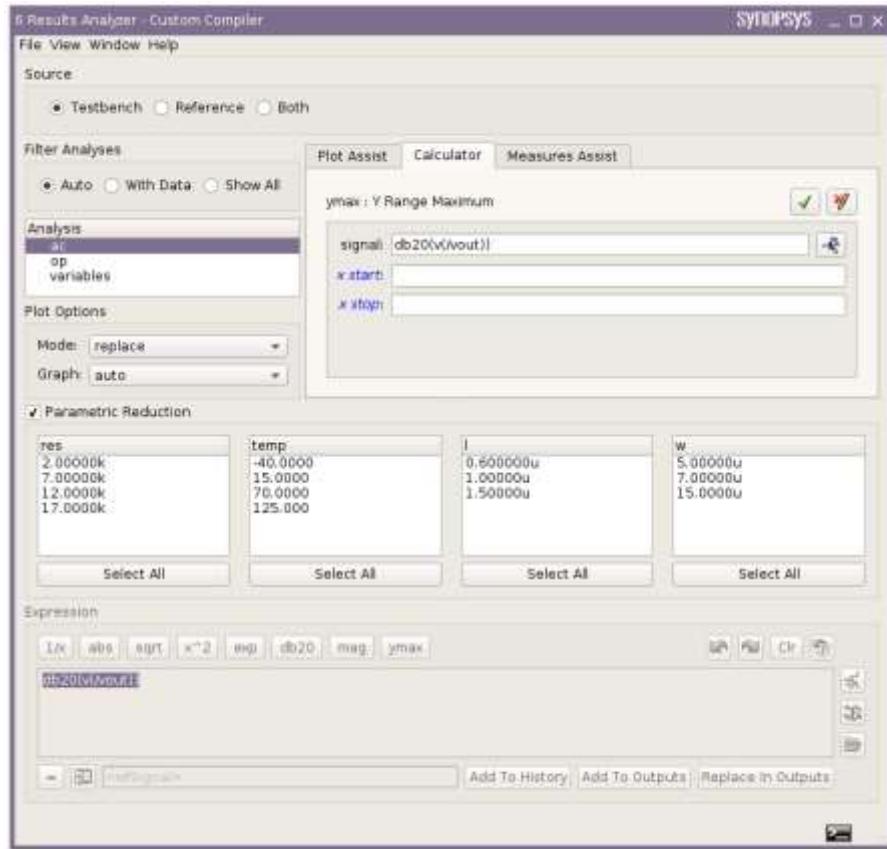
90. Now double click on the *Net* as **Selection**.

Note: This will prompt you to select the net in the *Tb_Opamp* schematic.

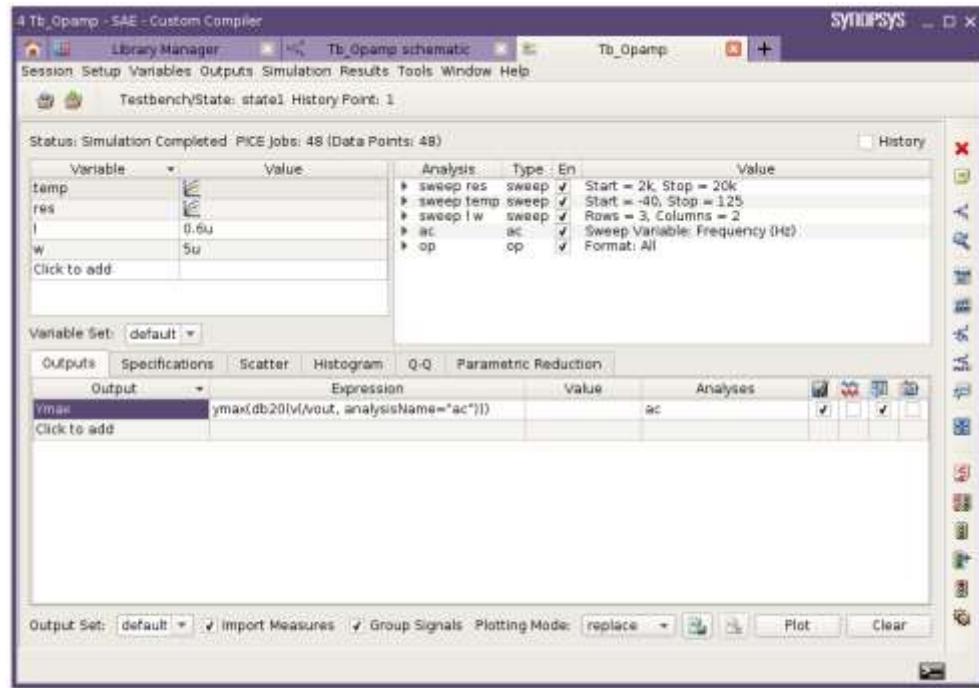
91. Select the net *vout* in the schematic and abort the **Pick Object** command.

Note: As you select the net, the expression *db20(v(/vout))* gets entered in the **Expression** section of the Analyze Results dialog and also the magnitude plot of the output signal *vout* gets plotted in WaveView.

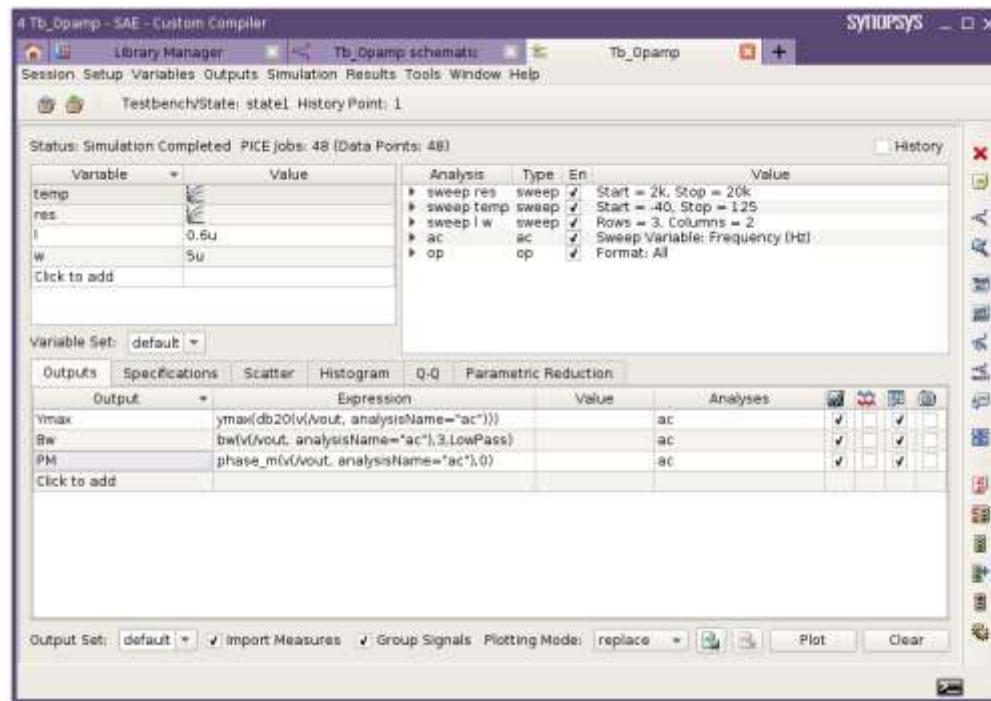
92. In order to measure the gain, double click on **ymax** from Calculator tab in Results Analyzer.



93. Press tick button to add the gain expression in RA.
 94. In the Results Analyzer, click on **Add To Outputs**.
- Note:** This will add the expression in the output section of the SAE window.
95. Make sure that $ymax(db20(v/vout))$ expression was added in SAE window. Assign Output name to that expression as Ymax.
 96. SAE window should look like as shown in the image:



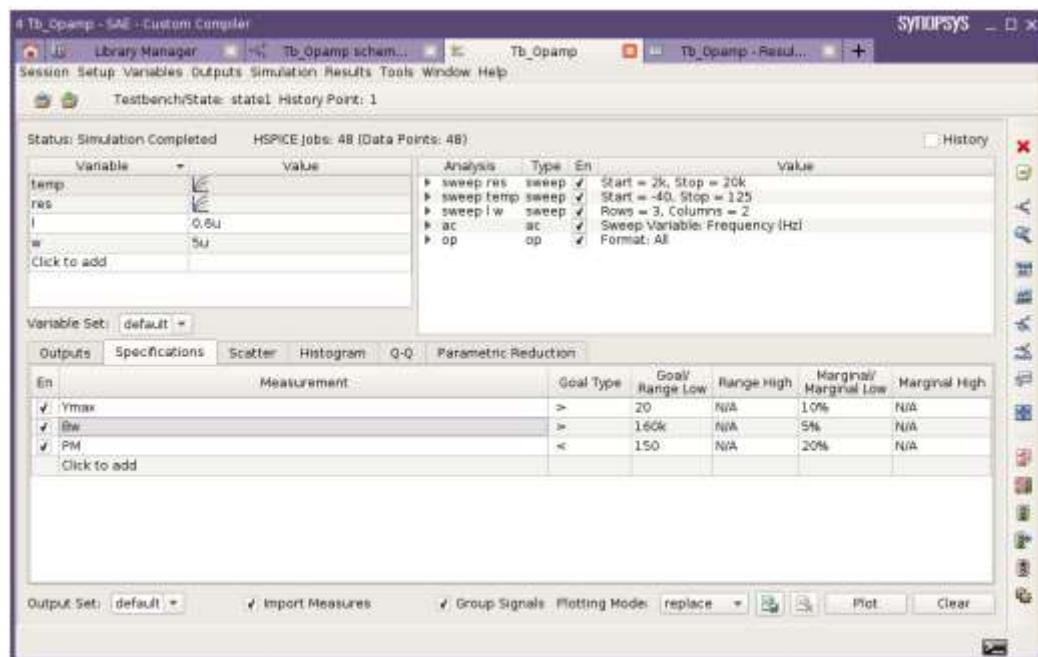
97. Using the similar steps, add *bw* and *phase_m* measures to SAE. Specify those measure names as it is shown in the below screenshot.



Task 35. Setup measurements specifications for Parametric Analysis

In this task, you will setup specifications on the measures, which were configured in the previous task

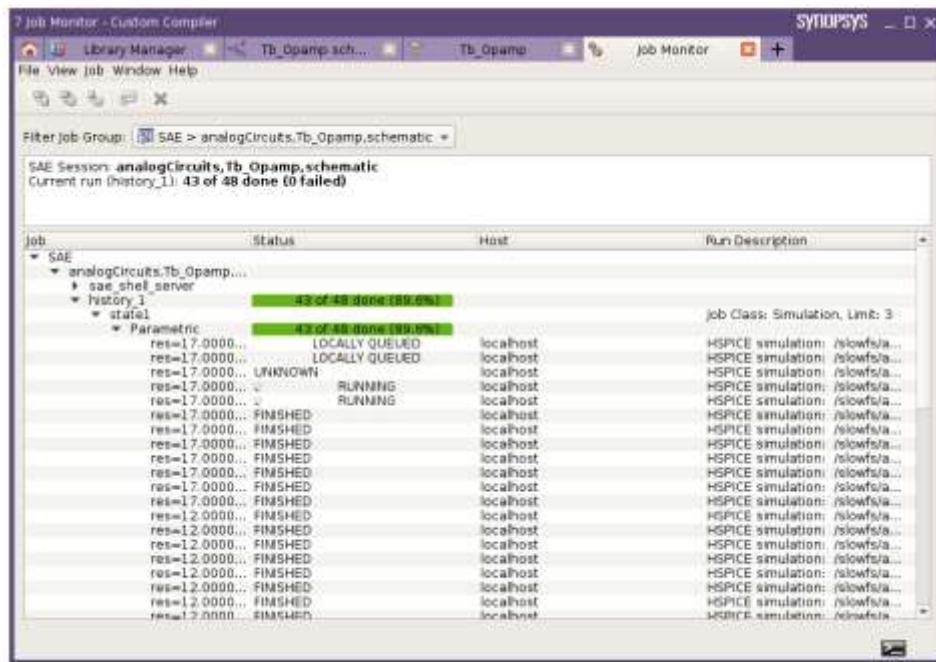
98. From the SAE window, click the *Specifications* tab. You will see that all measures are automatically added in this tab.
99. Click on Goal field for Ymax measure and select *Greater Than* expression
100. Specify 20 as Goal value and 10% as Marginal value.
101. The same way set the specifications on the remaining measurements as it is shown in the below screenshot



Task 36. Netlist and Simulate the Design

In this task, you will netlist and simulate the *TB_Opamp* schematic with varying biasing resistor values.

102. Generate the netlist and simulate the design using **Simulation → Netlist and Run**.
103. It opens up the Custom Compiler Job Monitor window.

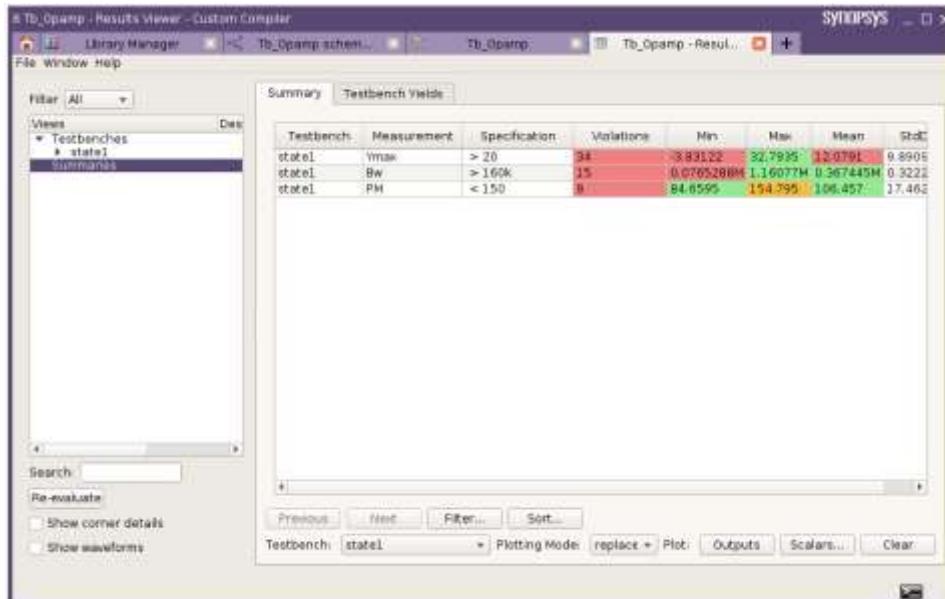


104. Close the Custom Compiler Job Monitor window.

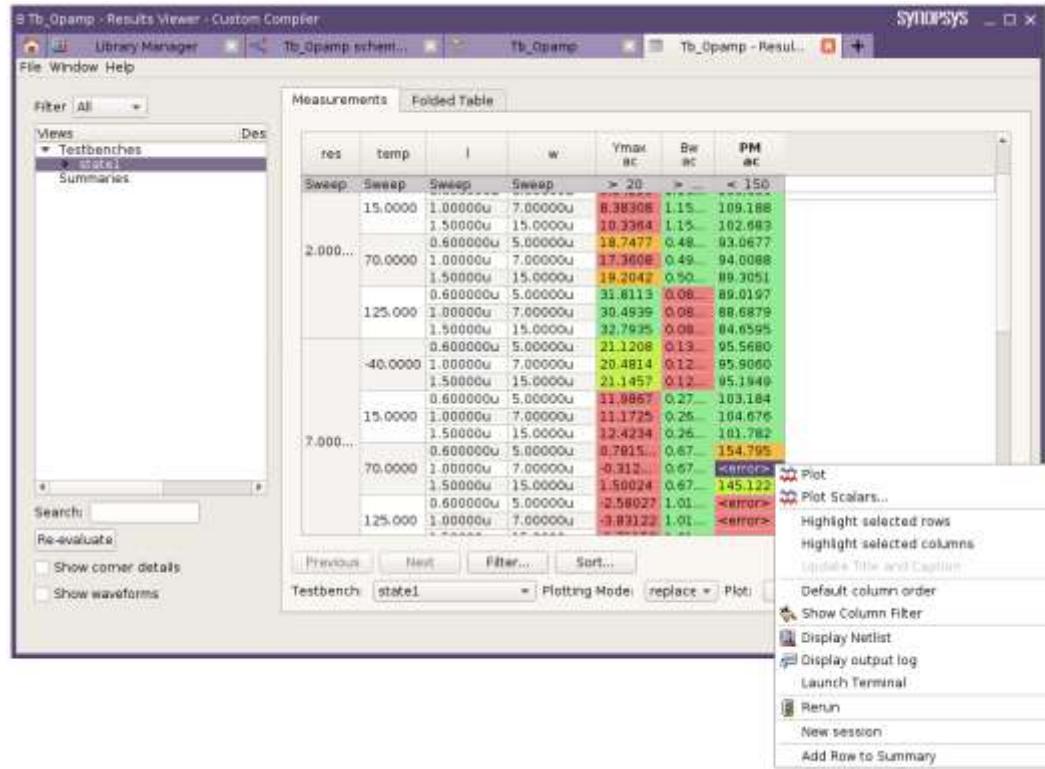
Task 37. Results Debugging

In this task you will analyze the results of corner analyses by using Results Viewer.

To see the status of your measurements for all swept parameters, invoke **Results → Results Viewer...** from SAE main window.



105. Select “state1” testbench from Views pane.
106. In this view all measurements are shown for each parameter sweep values.
107. As it can be seen from the *Results Viewer* dialog screenshot, the measurements are automatically get colored showing which of them met the goal, which not and which are in the marginal value range (colored in gradient).
108. There are some iterations, where PM measurement failed to evaluate. They have <error> as value. Select one of those empty fields, say for *res*=7k and *temp*=125, and bring up the context sensitive menu using your right mouse button. Observe the options which are available in the given CSM menu.
109. Select “New Session” from the CSM menu.

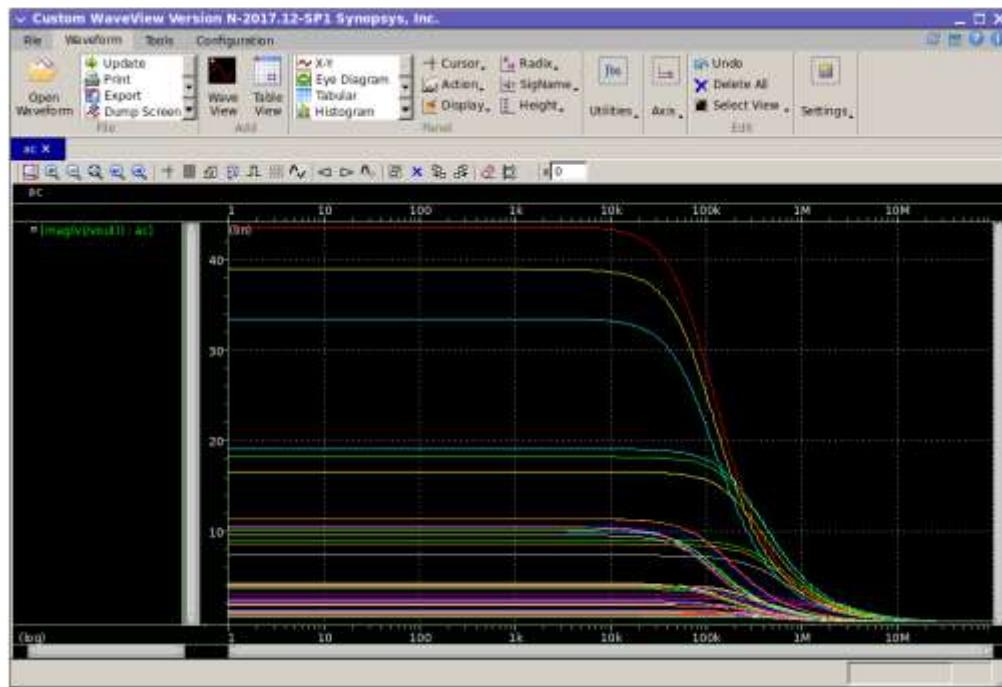


110. Observe new SAE state will be created, which contains all parameters set to same value as they are for the exact iteration. Using that SAE session, you can re-run that iteration and understand the reason of measurement failure.
 111. Close the SAE session opened in previous step and go back to Results Viewer. From CSM menu for <error> value for PM measurement select Plot
- Note:** The whole reason of PM fail is that the *v(out)* gain is below 0db.
112. From the CSM observe that you have capability to rerun the simulation, plot, view netlist and simulation log file.

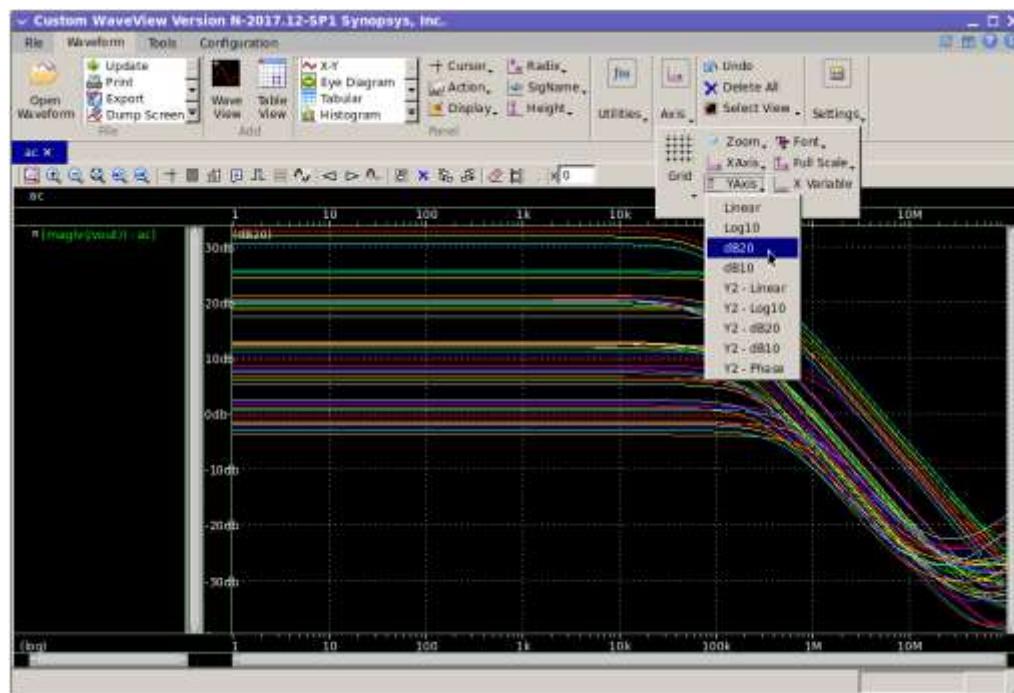
Task 38. Plotting and Analyzing Results in WaveView

In this task, you will plot and analyze the voltage gain of an Operational Amplifier for different biasing resistor values.

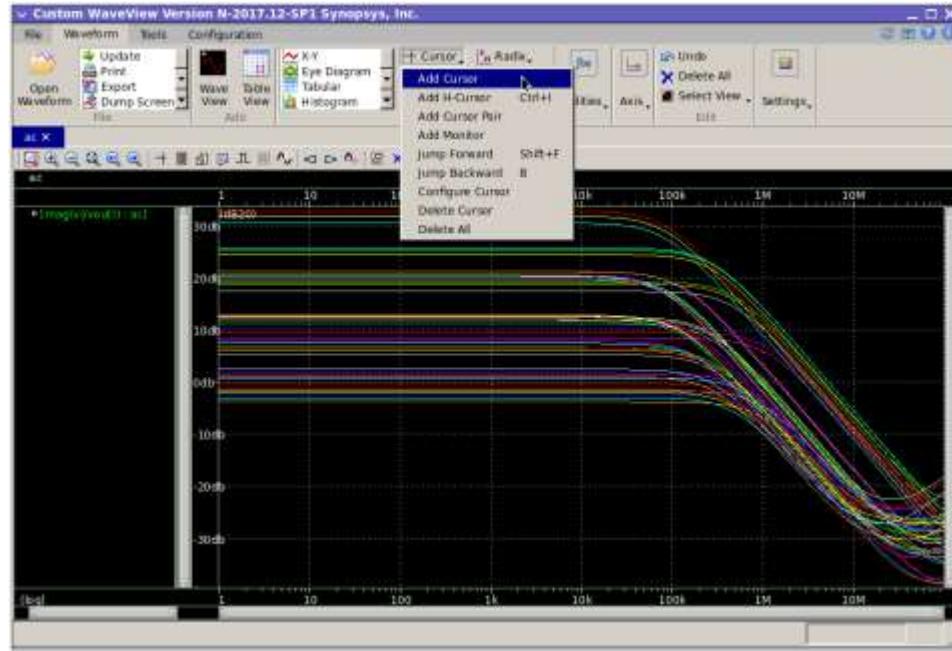
- 113.** Plot the ac magnitude of the output signal *vout* using **Results → Plot Signal → AC Magnitude** and select **vout** signal from the design.



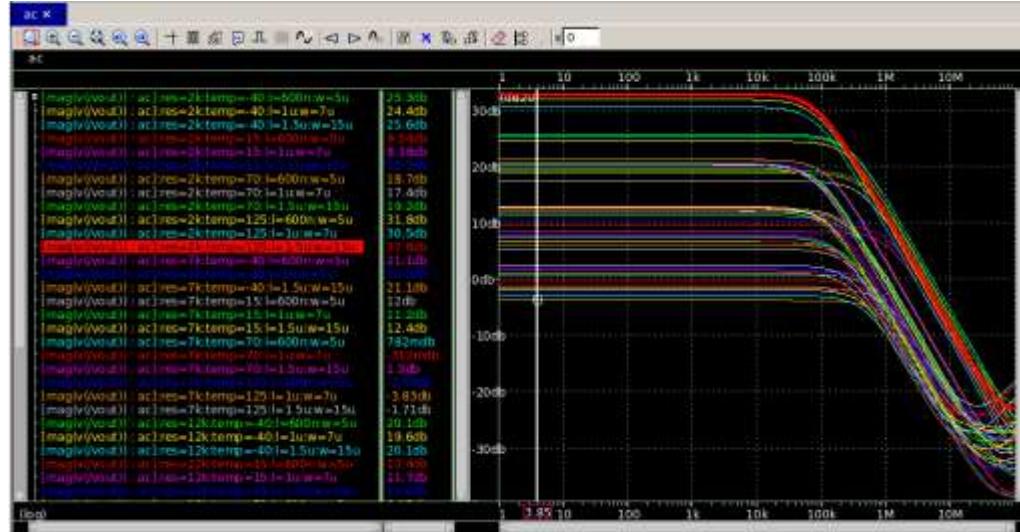
- 114.** Set the y-axis to a log scale in WaveView using **Axes → Y-Axis Type → dB20**.



115. Measure the gain by adding the measurement cursor using **Cursor → Add Cursor**.



116. The waveform will look like as shown in the image.



117. From the waveform, you can easily make out that the maximum gain is of 32.8 dB for biasing resistor $res = 2k$, $temp = 125$, $l = 1.5\mu$ and $w = 15\mu$. This is one of the ways you can optimize your circuit.

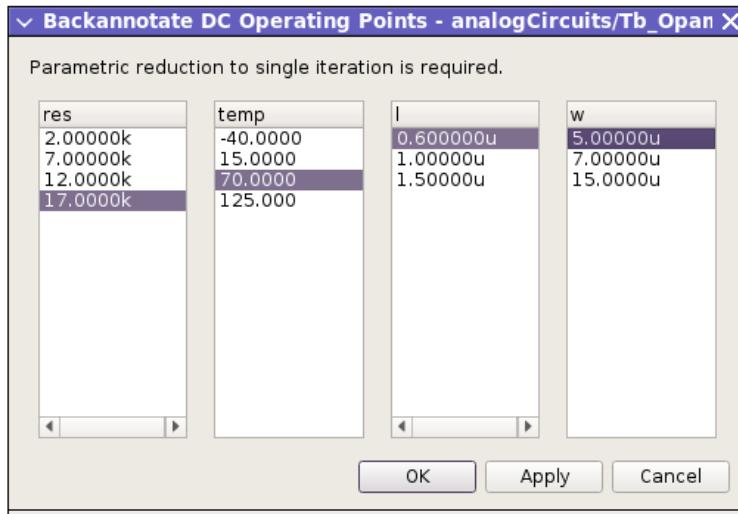
Task 39. Back-annotating Results

In this task, you will learn how to back-annotate the results to the schematic for the biasing resistor $res = 17k$, $temp = 70$, $l=0.6\mu$ and $w=5\mu$.

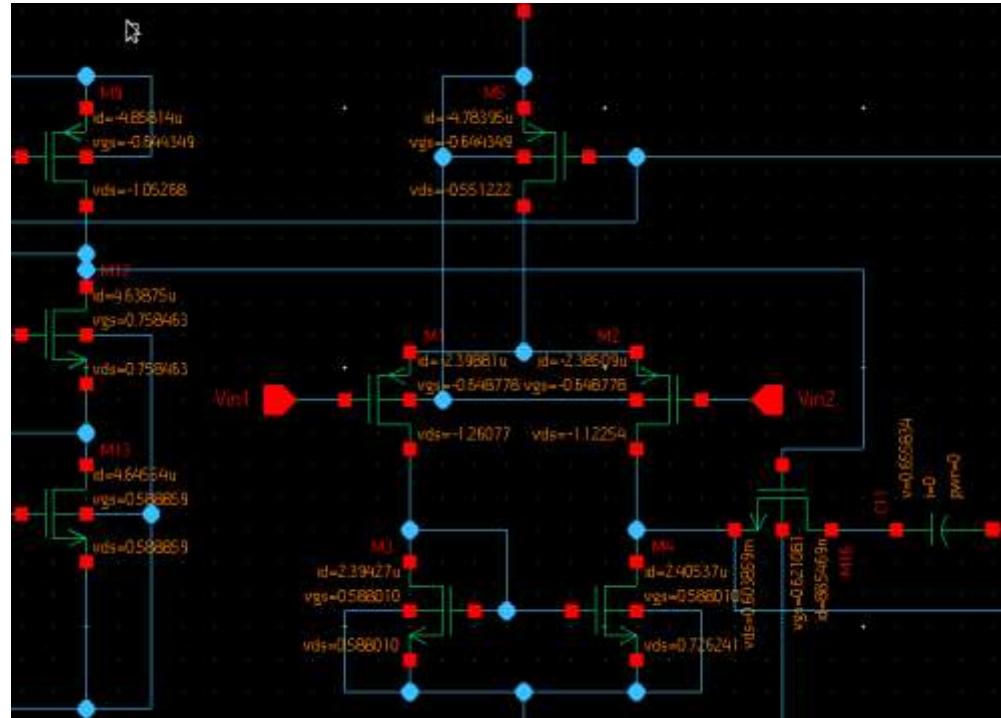
- 118.** From the SAE window back-annotate the DC operating point using **Results → Annotate → DC Operating Point**

Note: This will bring up the **Backannotate DC Operating Points** dialog.

- 119.** Select the entry **res** as $17k$, $temp = 70$, $l=0.6$ and $w=5u$. Click OK.



- 120.** Descend one level down the hierarchy from testbench schematic into opamp and you will see the DC Operating Point of the devices corresponding to resistor value $res=17k$, $temp=70$. The annotated data will look like as shown in the image.



Task 40. Printing Results

In this task, you will print out the DC Operating points of the devices for the analysis purpose.

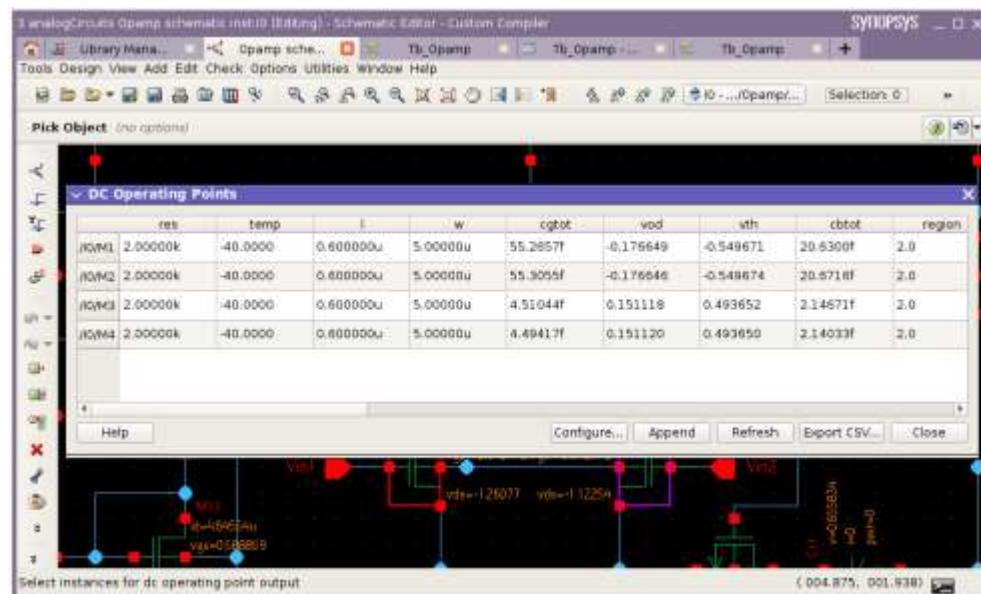
121. From the SAE window, print the DC Operating points of the differential input PMOS transistors M1 and M2 using **Results → Print → DC Operating Points**.

Note: This will bring up the Print DC Operating Point dialog.

122. Select desired conditions for sweep parameters and click OK.

Note: You will prompt to pick the object in the schematic.

123. As you click on the instance M1 and M2, DC Operating Points form will come up with the operating point information corresponding to resistor value $res=2k$, $temp=-40$, $I=0.6u$ and $w=5u$.



124. Close the DC Operating points form.

125. Close all windows.

Congratulations!

You have successfully performed parametric analysis to optimize your circuit using Simulation and Analysis Environment (SAE).

4

Corners Analysis

Learning Objectives

The main goal of this lab is to use the Corners Analysis Tool in SAE for setting up, simulating and reviewing results.

After completing this lab, you should be able to:

- Setup Corners Analysis
- Modify necessary parameters
- Simulate and analyze Corners results

Lab Duration:
30 minutes

Introduction

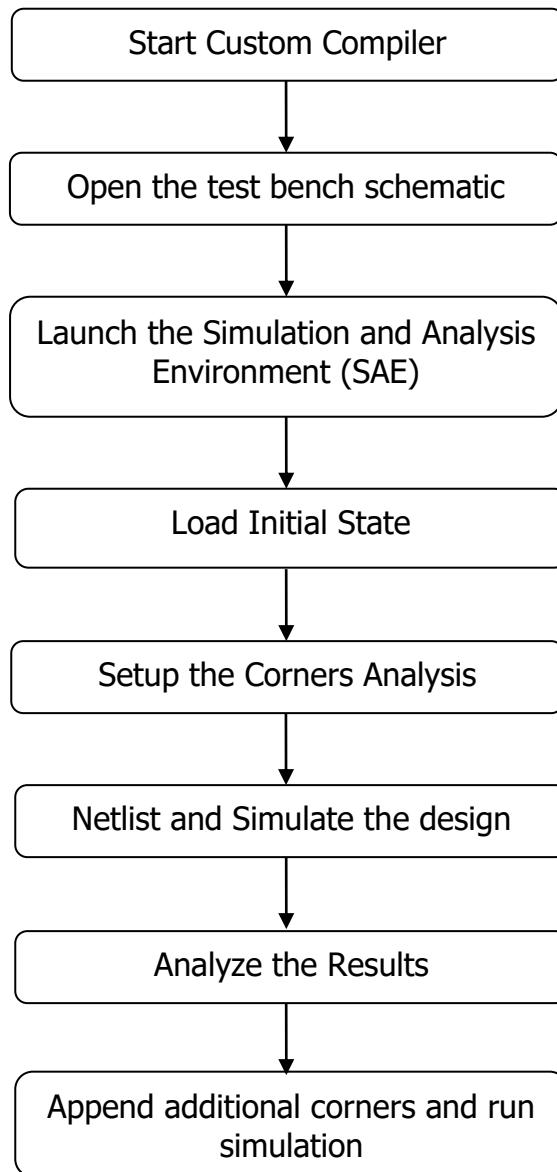
During this lab you will setup Corners Analysis by modifying design parameters, as well as simulate the design and observe simulation results.

In this lab, you are provided with the OpenAccess database library necessary for Corners Analysis and a *lib.defs* file. The *cornerAnalysis* library contains Opamp cell and the testbench for simulation. The *lib.defs* is the default library definition file that contains library name mapping to their physical location.

Please refer to the *Simulation and Environment User Guide* for the commands that are used in this lab.

Flow Overview

Lab 1 Tasks



File Locations

All files for this lab are located in the directory *SAE_CornerAnalysis_Lab1*.

Directory Structure

SAE_CornerAnalysis_Lab1	Current working directory
cornerAnalysis	OpenAccess Design library
lib.defs	Library Definitions file
models	Folder containing model files

Relevant Files

.../PDK/	PDK directory
----------	---------------

Tool Versions

HSPICE	O-2018.09
WaveView	O-2018.09

Instructions

Task 41. Start Custom Compiler

126. In the UNIX terminal window, change your current working directory to *SAE_CornerAnalysis*. This will be your working directory for this lab.
127. Start Custom Compiler from the UNIX prompt.

```
custom_compiler &
```

Task 42. Open the Test Bench Circuit

128. From the design library *cornerAnalysis*, open the schematic cell *Opamp_OpenLoop* of the view name *schematic*.

Note: *Opamp_OpenLoop* cellView will be opened in a Schematic Editor window.

Task 43. Launching Simulation and Analysis Environment

129. From schematic window invoke the Simulation and Analysis Environment using **Tools → SAE**.

Note: This will open up the Simulation and Environment window which comes with design *cornerAnalysis / Opamp_OpenLoop / schematic* pre-populated.

Task 44. Load the State

In this task, you will load the simulation setup for *Opamp_OpenLoop* where you will perform Loop Stability analysis to verify the signal performance of the Opamp.

130. Load the state *OpenLoopMeasure* from SAE window using **Session → Load State...** or use **L** bind key.

Note: This will load simulation setup for transient analysis and setup outputs for measurements.

131. Switch the **From** section to *Open Access* and press **OK** button to load the state.

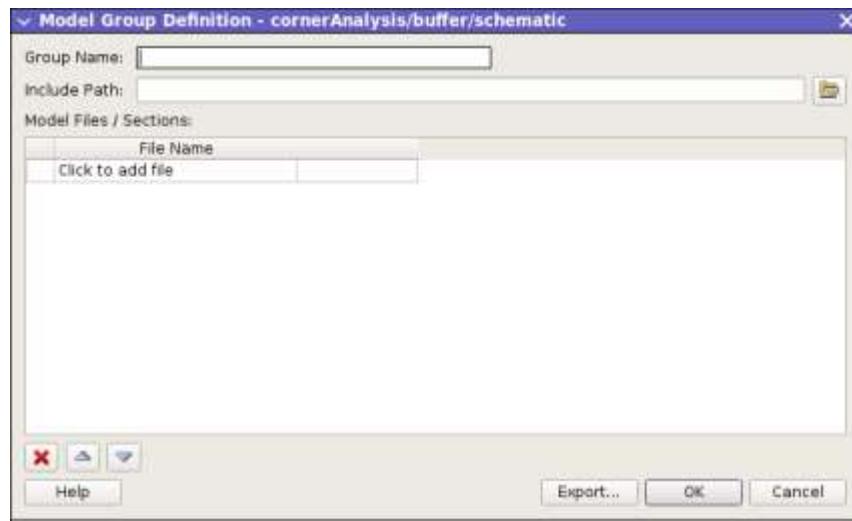
Task 45. Create model group

In this task you will create model group, combining low and high voltage devices.

132. Open **Model Files** dialog using **Setup → Model Files...** or **M** bindkey from SAE window.

133. Click on **Click to create definition** filed in Model Files dialog, under Model Group section.

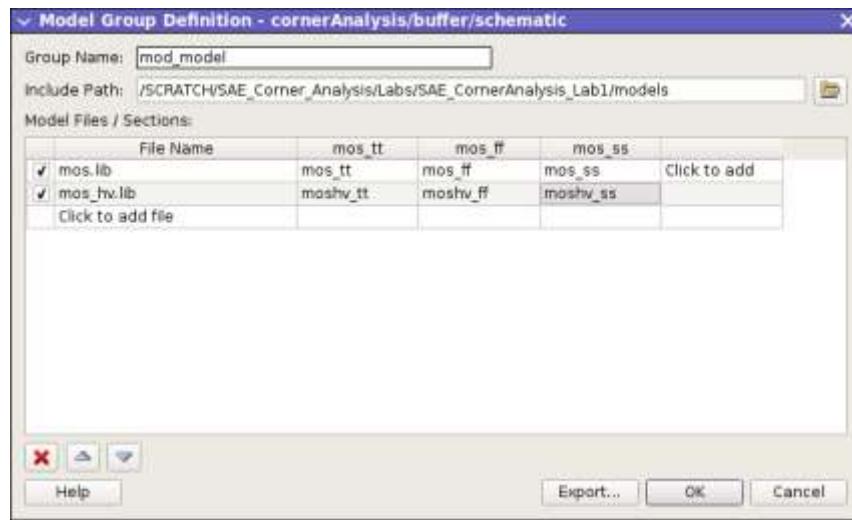
Note: **Model Group Definition** dialog will pop up.



134. Specify **mos_model** for **Group Name**
135. For **Include Path** browse to *models* directory inside *SAE_CornerAnalysis_Lab1* directory and click Choose.
136. Click on **Click to add file** and select mos.lib and mos_hv.lib files.
137. Click on **Click to add**, right after model file name and select model corner.

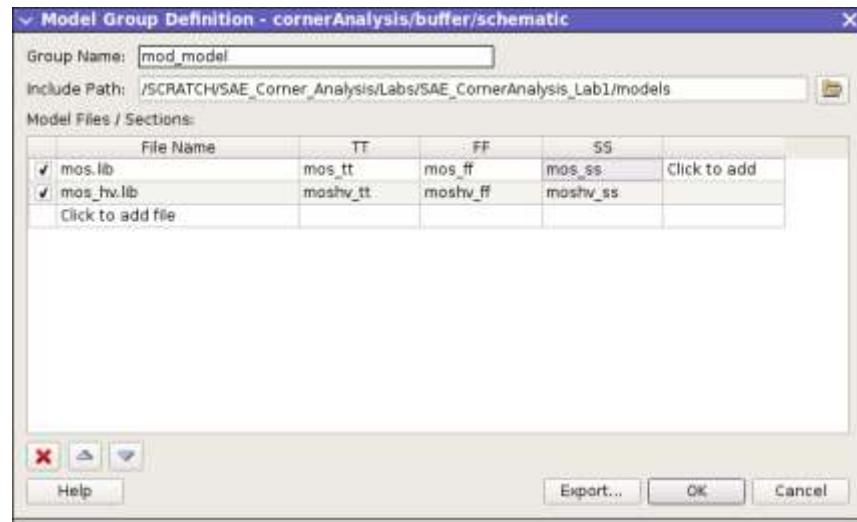
Note: This will create model section for entire model group.

138. Combime same sections for low and high voltage mos libraries together.

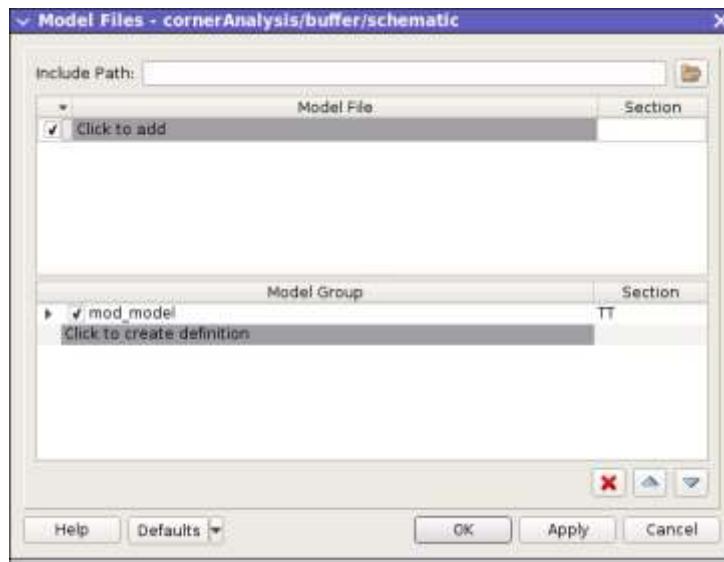


Note: Sections for model group will get names automatically, which will be the name of the section, which is selected first.

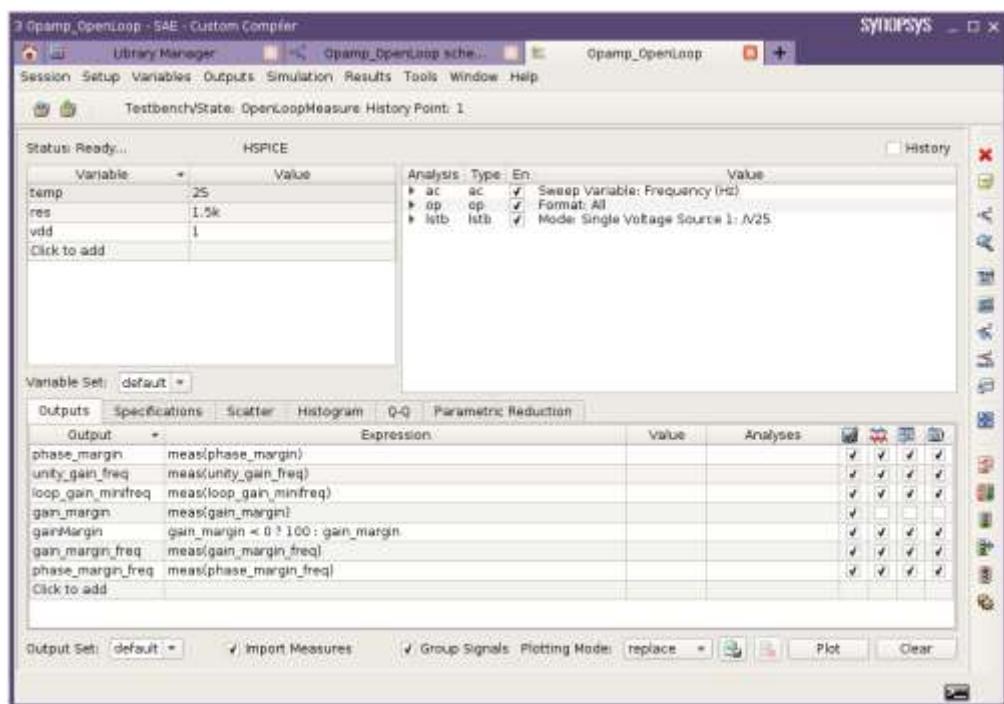
- 139.** Rename model group sections to be TT, FF and SS. Right click on the column header and select Rename Section...



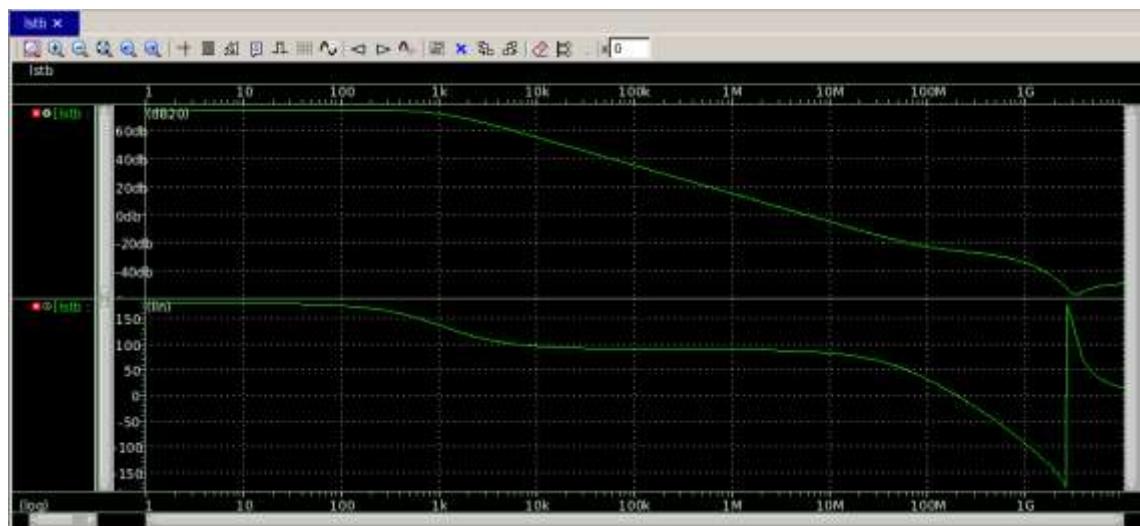
- 140.** Click **OK** in Model Group Definition dialog to close it. Model Files dialog should look like as shown in the image below.



- 141.** Click **OK** in Model Files dialog to close it. SAE window should look like as shown in the image below



142. From the SAE window run netlist and simulation sequentially using **Simulation > Netlist and Run** or use **Ctrl+R** bind key.
143. Observe the simulation results in **Custom WaveView** using **Results > Plot Signal > Loop Gain Magnitude and Phase**.



144. Close the **Custom Wave View** window.

Task 46. Setup the Corners Analysis

In this task, you will setup the Corners analysis by varying model corners, *res* and *vdd* design parameters.

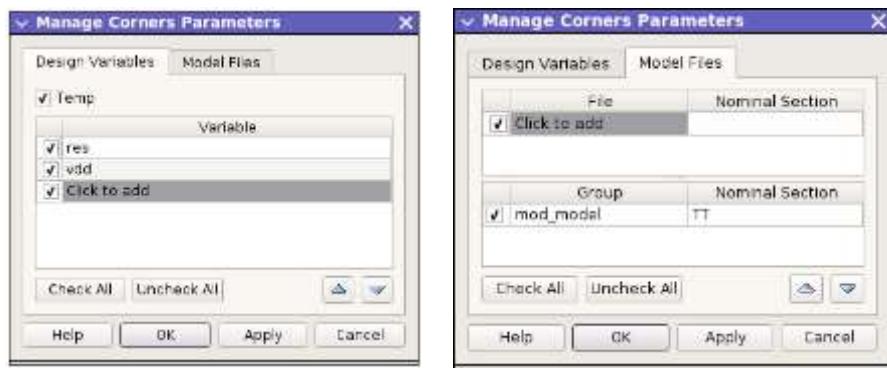
145. From SAE window open the Corners Setup dialog using **Tools → Corners ...**

146. Click the “*Add Design Variables...*” button to add corner parameters

Note: The “Manage Corners Parameters” dialog appears.

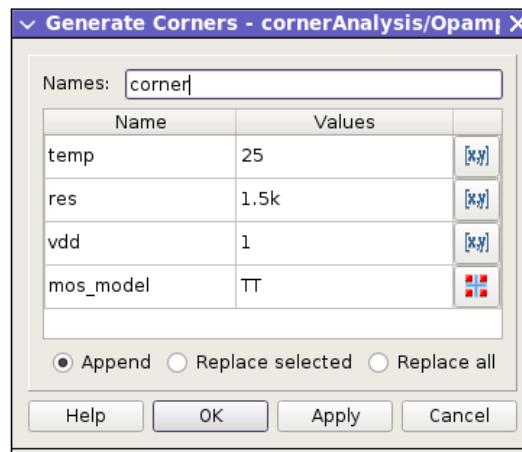
147. Enable *res* and *vdd* parameters.

148. Switch to Model Files tab and enable *mos_model* corner group.



149. Click OK.

150. Click “*Generate Corners...*” to define simulation corners. The “*Generate Corners*” dialog appears like the below screenshot.

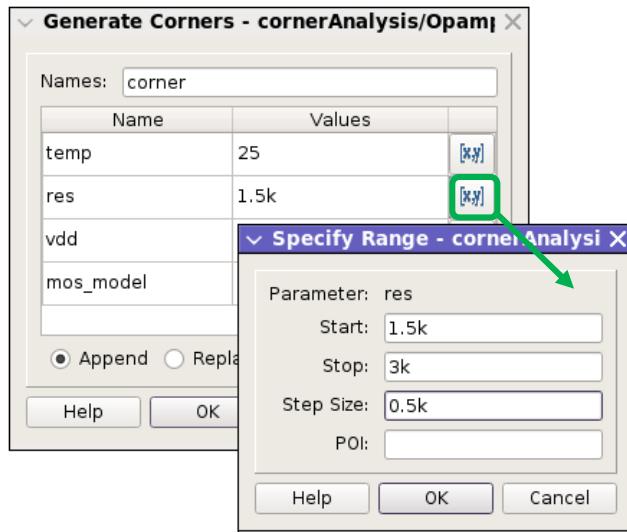


151. Click on “Specify range” button in front of *res* parameter and specify range of *res* variable with values shown in table below:

Start	1.5k
Stop	3k

Step	0.5k
------	------

152. The “Specify Range” dialog should look like the below image.



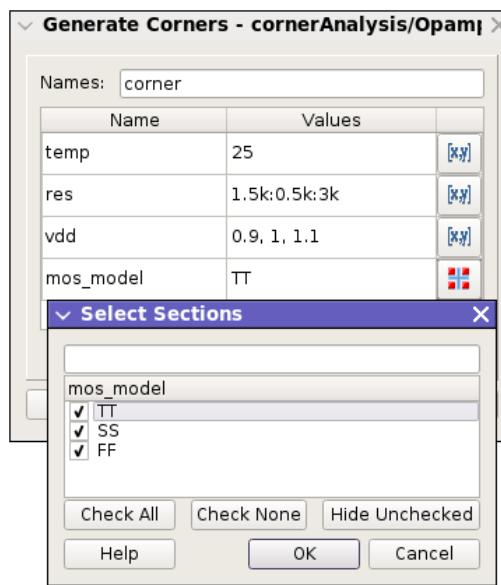
153. Click OK to close the “Specify Range” dialog.

154. The same way specify range of “vdd” variable with values shown in table below:

Note: Delete “Start” value

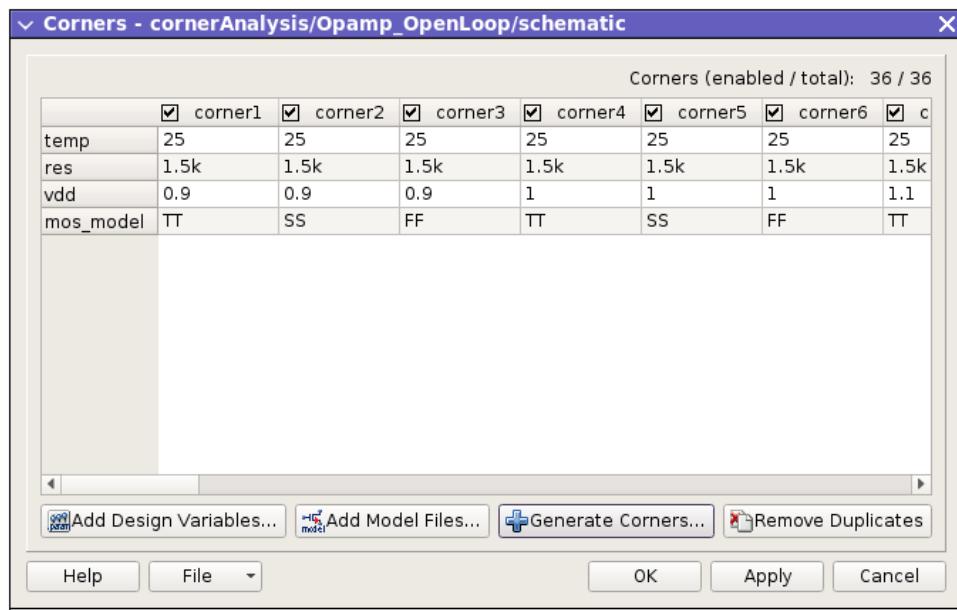
POI	0.9, 1, 1.1
-----	-------------

155. Click on “Specify Sections” button in front of mos_model entry and enable TT, FF and SS sections.



156. Click **OK** in the “Generate Corners” dialog.

Note: All possible corners appear in the “Corners Setup” dialog as shown in the image:



157. Click OK to close the “Corners Setup” dialog.

Note: The Corners analysis will appear in the Analysis field of SAE main window.

Task 47. Setup the Corners Groups

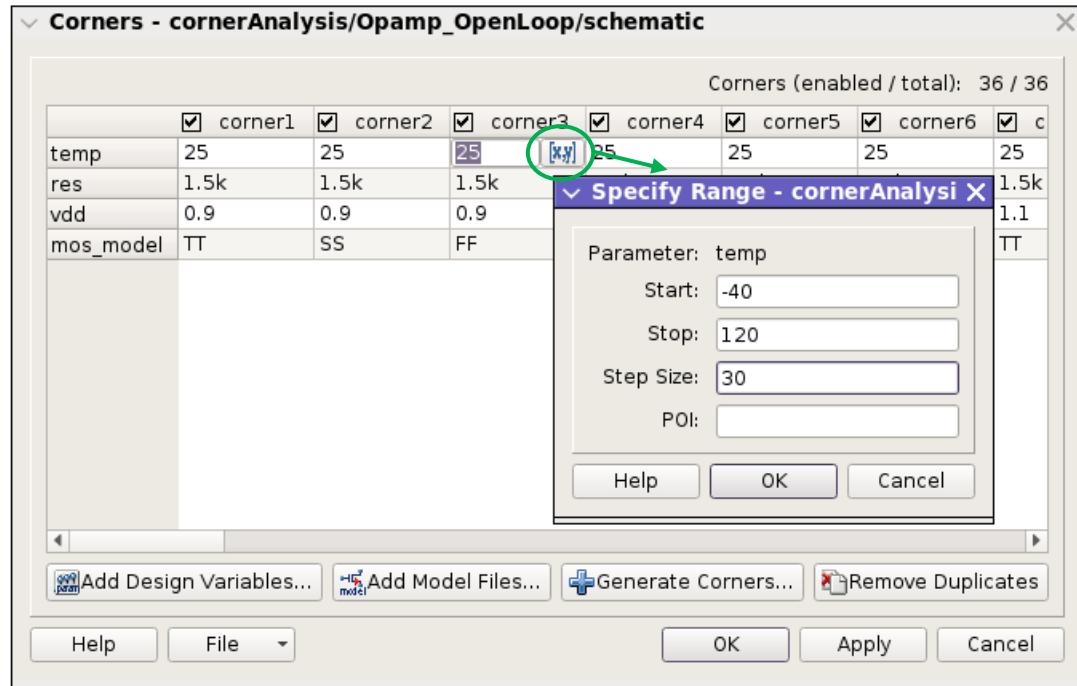
In this task, you will setup the Corners group by varying the design *temp* parameter. Instead of using the corner generator (Tools > Corners Setup > Generate Corners> to create each corner user can now directly create corners in the Corners Setup dialog. Multiple values can be specified for a parameter and represented as a corner group which is a more compact form for viewing and later editing corners. The values can be specified using both ranges and individual Points of Interest.

158. From SAE window open the **Corners Setup** dialog using **Tools → Corners....**

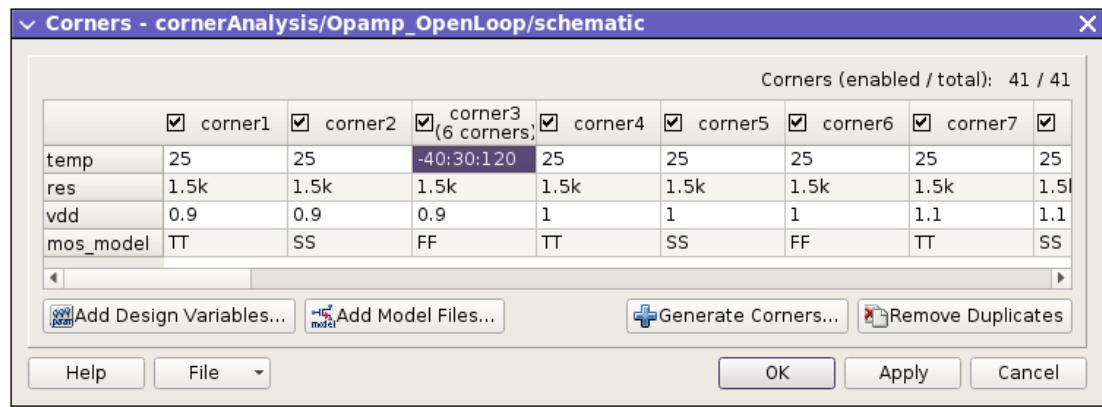
159. Click on *temp* variable in the corner names *corner3*

160. Press on “Edit Corner Value” icon to open range specification dialog.

161. Specify the new corners for *temp* variable as it is shown in the below screenshot



162. Click OK to close the “Specify Range” dialog.
163. The “Corners Setup” dialog looks like the below image at this point



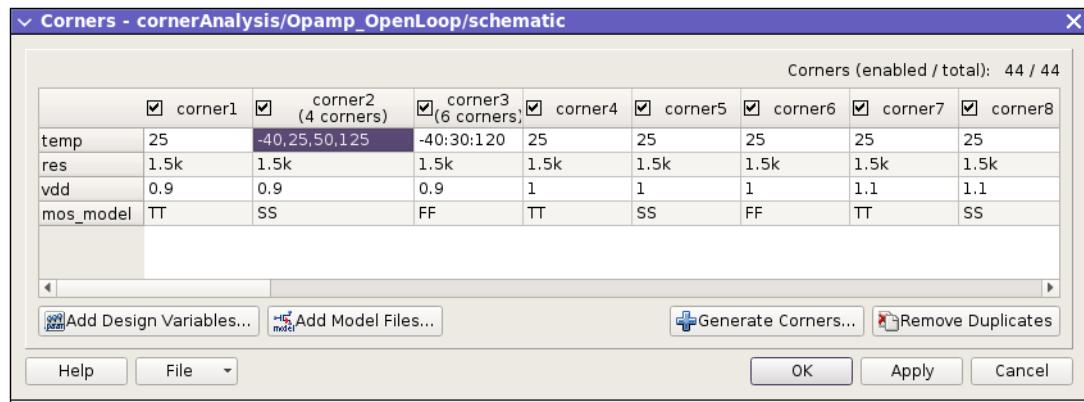
Note: Pay attention to the created *corner3* corner, as it can be seen the *temp* variable sweep values are grouped in one place to let user have better understanding about the sweep range

164. The corners can be specified directly in “Corners Setup” dialog, by writing comma separate values.

Specify the comma separated “*temp*” variable values for *corner2* as shown in table below:

temp	-40, 25, 50, 125
------	------------------

165. The “Corners Setup” dialog looks like the below image at this point

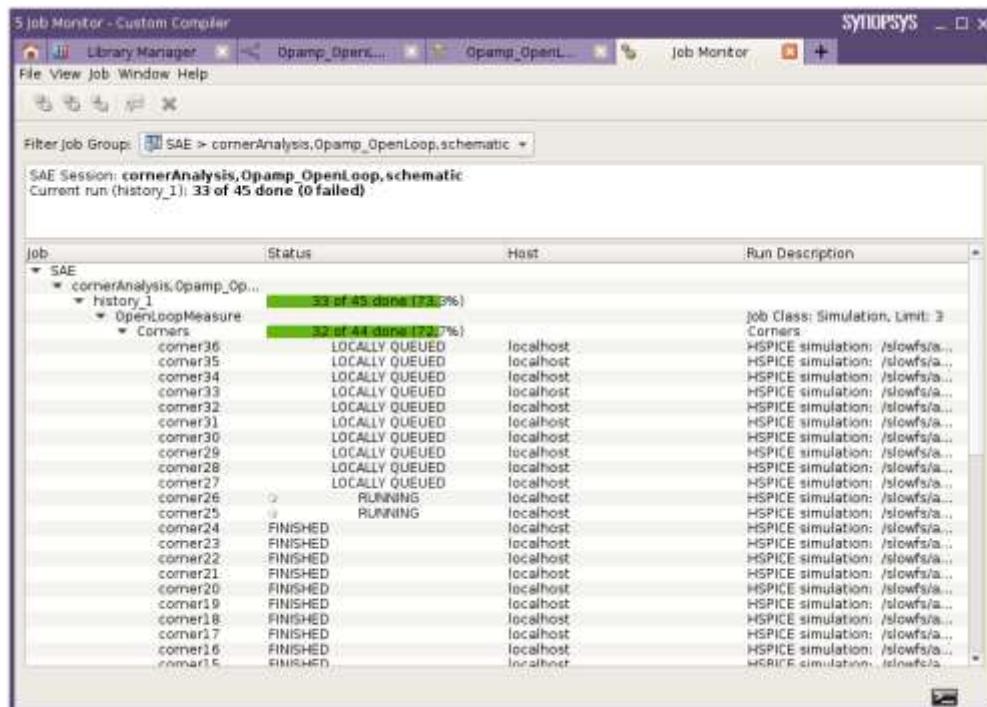


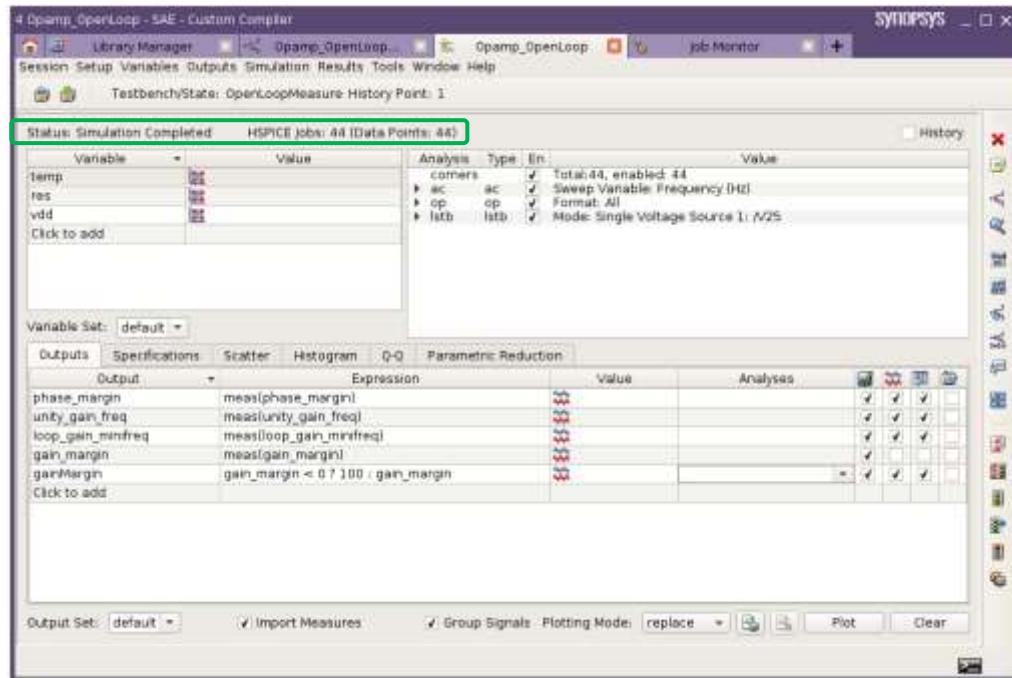
166. Click OK to close the “Corners Setup” dialog.

Task 48. Netlist and Simulate the Design

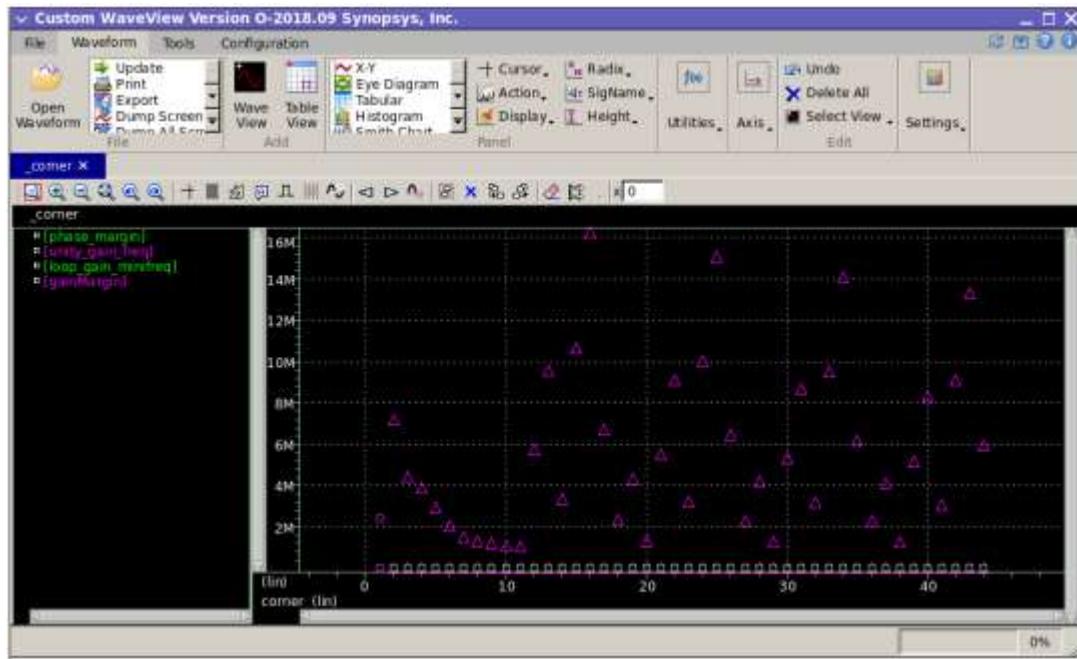
In this task, you will netlist and simulate the *Opamp_OpenLoop* schematic with varying *res* and *vdd* parameters.

167. Generate the netlist and simulate the design using **Simulation → Netlist and Run** command from SAE window or use **Ctrl+R** bind key.
 168. This opens up the Job Monitor in new tab.





169. After the simulation finishes the specified outputs will be evaluated and plotted in Custom WaveView as shown on the picture below.

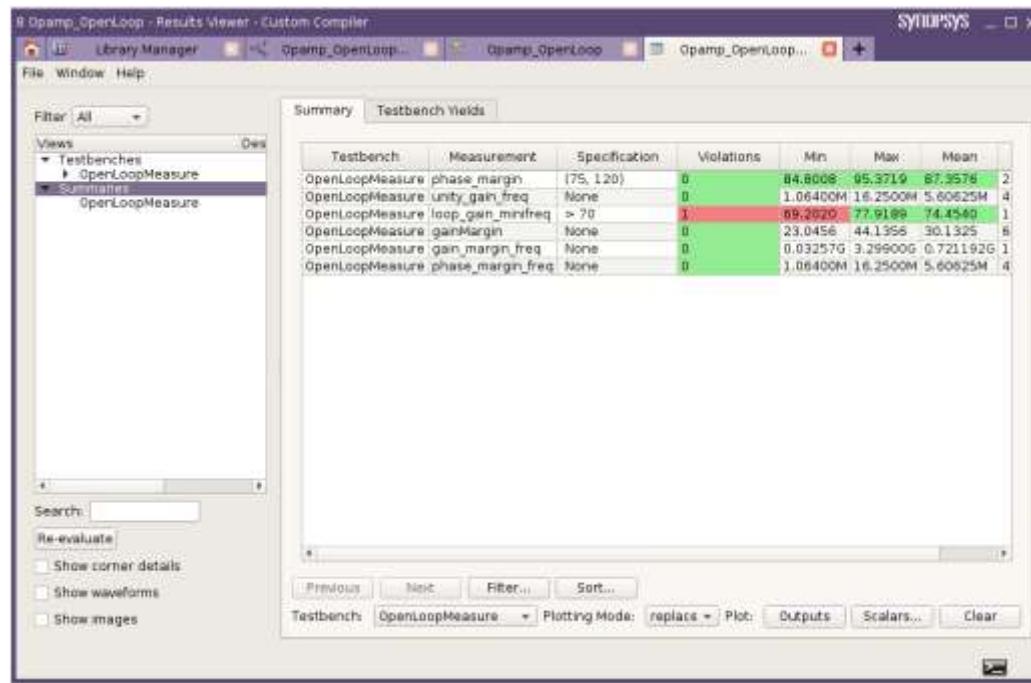


170. Close the **Custom Wave View** window.

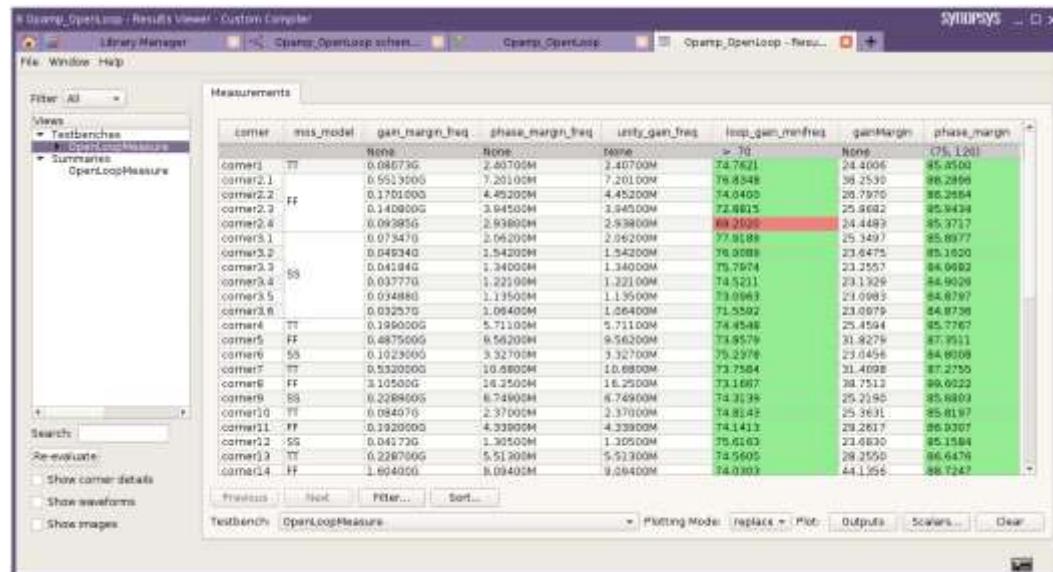
Task 49. Results debugging

In this task you will analyze the results of corner analyses using Results Viewer.

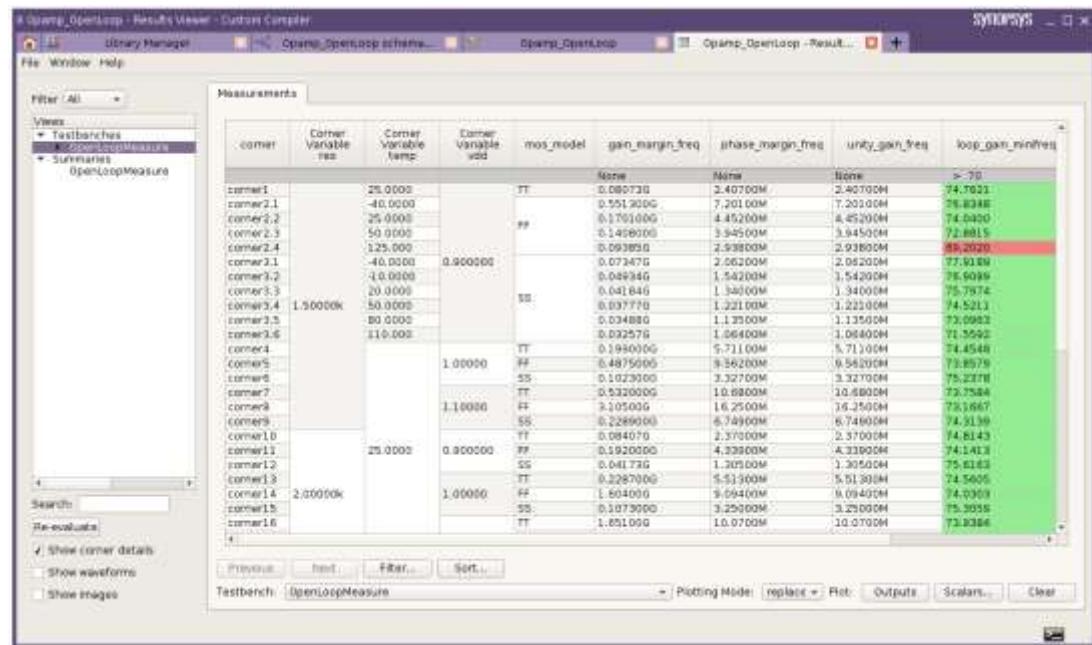
171. To see the status of your measurements for all corners, invoke **Results → Viewer...** from SAE main window.



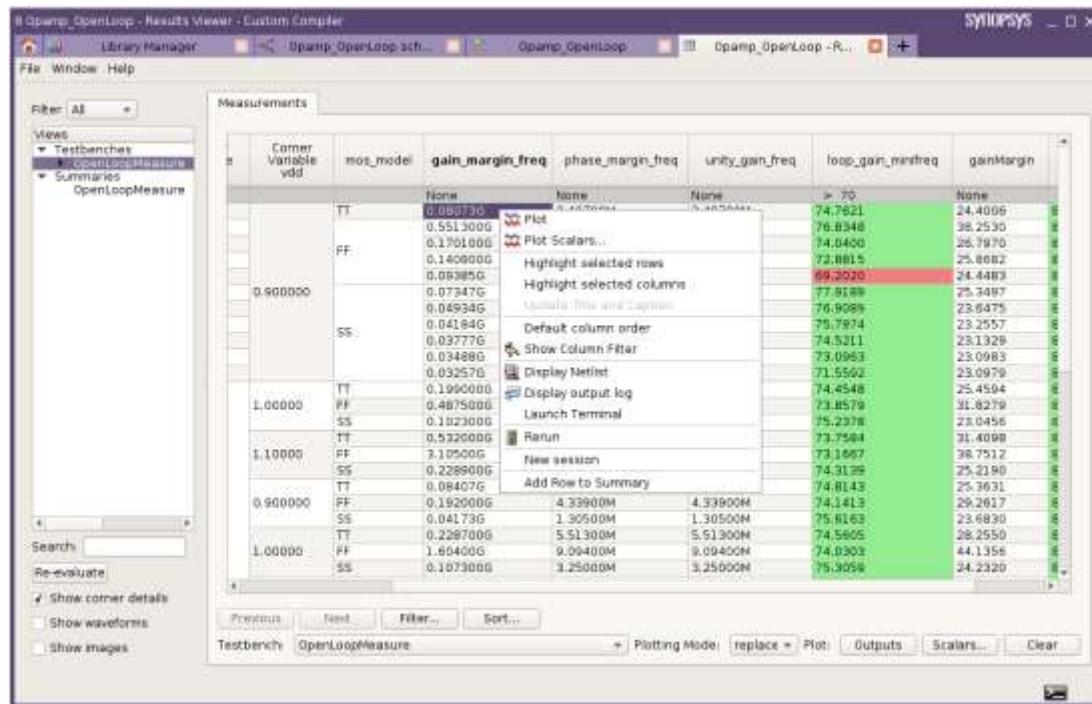
172. Click on testbench **OpenLoopMeasure** and expand tree under that testbench. Observe the results as shown in the picture below.



173. Enable **Show corner details**.



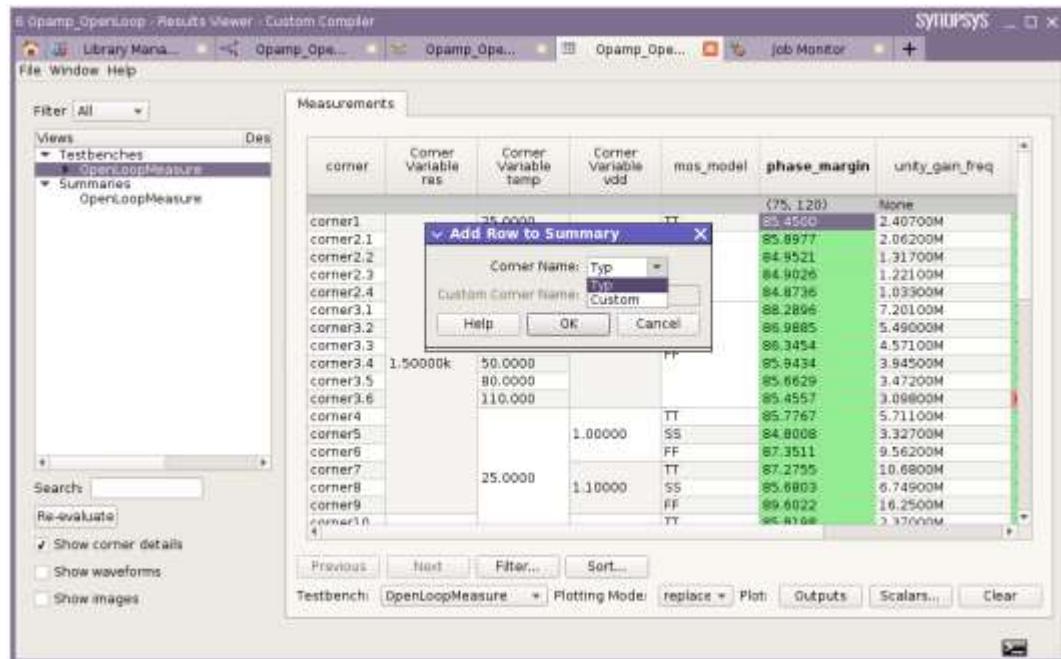
174. Select a particular value, say from *corner1* gain_margin_freq measurement value, and bring up the context sensitive menu using your right mouse button. Observe the options which are available in the given CSM menu.



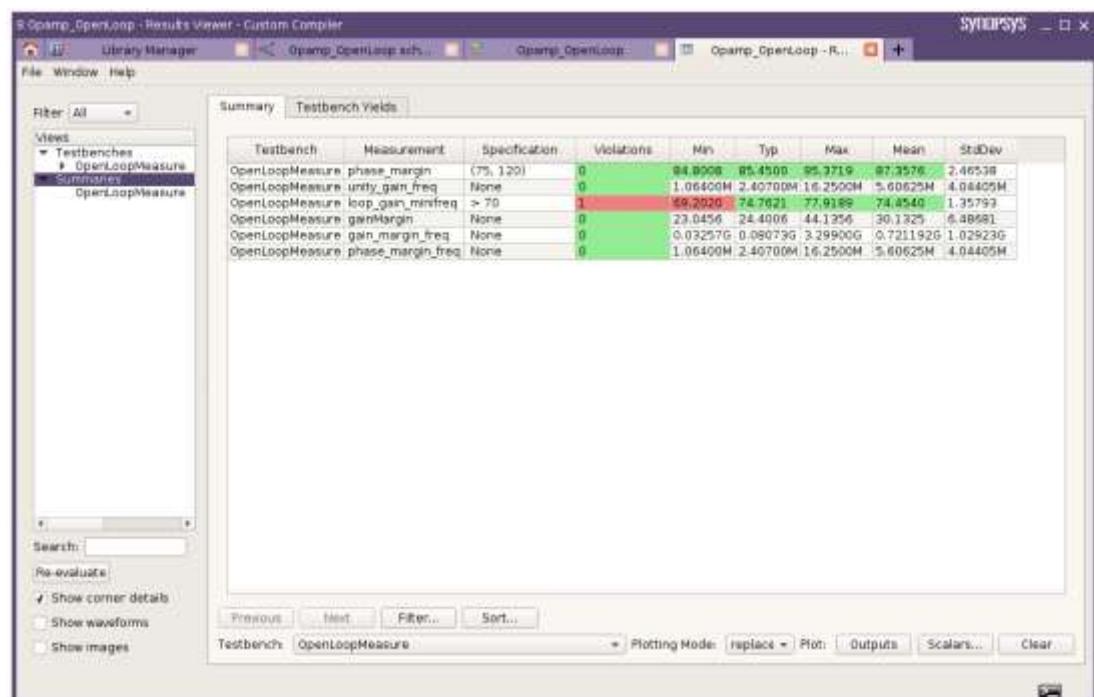
175. Select “New Session” from the CSM menu. Observe new SAE state created, which contains all parameters set with same value as for the selected corner.

176. Close new created SAE window.

177. From the CSM observe that you have capability to **Plot** input signals for that measurement, **Display Netlist** and **Output Log** file.
178. From the CSM choose **Add Row to Summary**. It will add selected row to summary table with selected or provided column name.



179. Choose **Typ** and click OK.
180. Click on Summaries in Views pane and observe that **Typ** row is added in the middle of Min and Max columns.

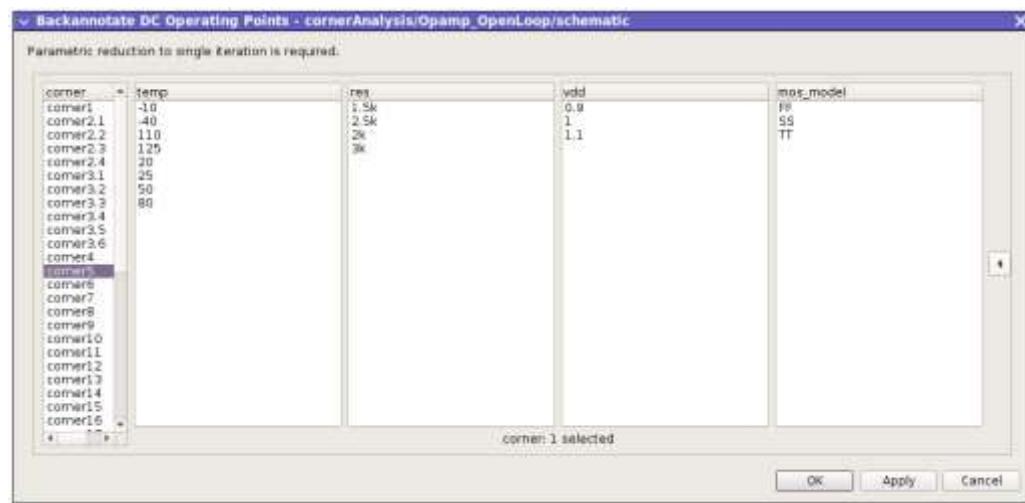


181. Close Custom Compiler Result Viewer window.

Task 50. Back-annotating Results

In this task, you will learn how to back-annotate the results to the schematic.

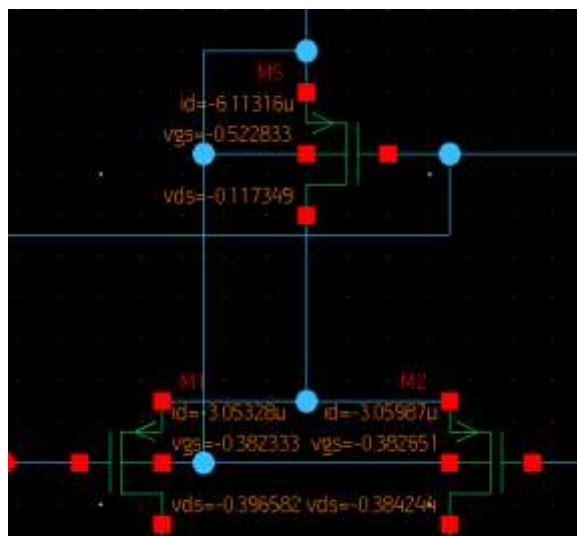
182. From the SAE window back-annotate the DC operating point using **Results → Annotate → DC Operating Point**
183. This will bring up the Backannotate DC Operating Point dialog.



Note:

You can select either by clicking on corner name or by selecting parameter conditions. You can hide parameter conditions using arrow at the right side of the dialog.

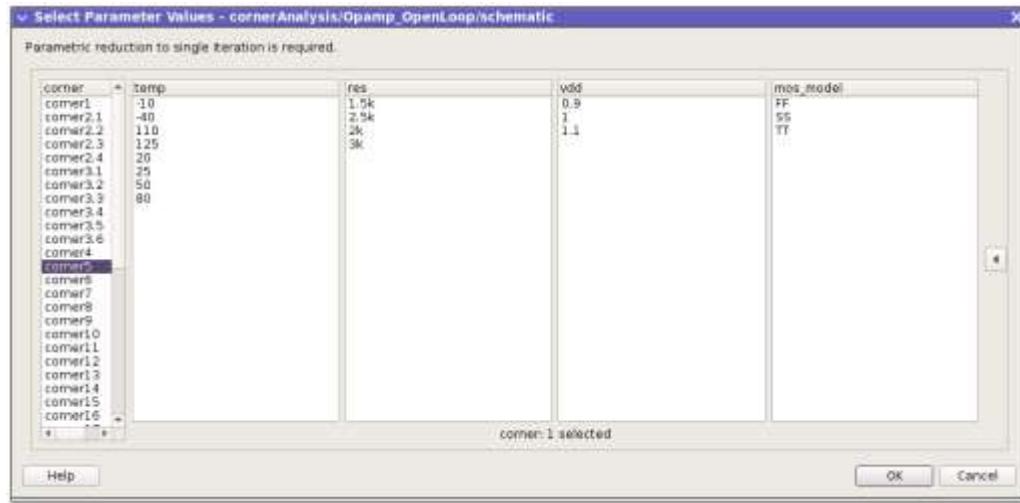
184. Select *corner5* and click OK.
185. Descend one level down the hierarchy in the schematic and you will see the DC Operating Point of the devices corresponding to the corner5.



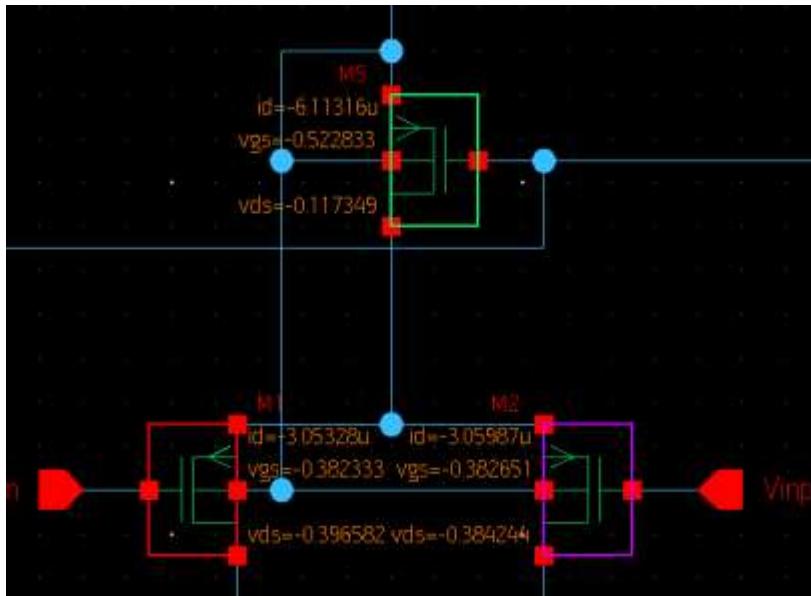
Task 51. Printing Results

In this task, you will print out the DC Operating points of the devices for the analysis purpose.

186. From the SAE window, print the DC Operating points using **Results → Print → DC Operating Points**.
187. This will bring up the Print DC Operating Point dialog.



188. Select *corner5* from the Corners Analysis and click OK.
189. You will be prompted to pick the object in the schematic.



190. As you click on the instance M1, M2 and M5 from I0, DC Operating Points form will come up with the operating point information corresponding to 5th corner.

	temp	res	vdd	mos_model	Corner	cgtot	vod	vth
/Q/M1	25	1.5k	1	FF	corner5	6.69210f	28.5640m	-0.410897
/Q/M2	25	1.5k	1	FF	corner5	6.72073f	28.3859m	-0.411036
/Q/M5	25	1.5k	1	FF	corner5	18.8563f	-0.134867	-0.387957

191. Press **Configure...** button in that dialog and notice that you can change the corner there.
192. Close the DC Operating points form.

Task 52. Viewing Operating Points Report

Also you can print DC operating point results as shown in previous task, there is a better and more powerful way to analyze the results.

193. From the SAE window, launch **OP Points Results** using **Results → Print → Operating Point Report**.

Note: It is possible to choose, if OP Point Results is opened in a tab or in a new window. Preference to control that behaviour is **saOpPointsOpensIn**, which accepts values as “tab” and “window”. By default, it comes up in a new tab.

corner	temp	res	vdd	mos_model
corner1	-10	1.5k	0.9	FF
corner2.1	-40	2.5k	1	SS
corner2.2	110	2k	1.1	TT
corner2.3	125	3k		
corner2.4	20			
corner2.5	25			
corner3.1	50			
corner3.2	80			
corner3.3				
corner3.4				
corner3.5				
corner3.6				
corner4				
corner5				
corner6				
corner7				
corner8				
corner9				
corner10				
corner11				
corner12				
corner13				
corner14				
corner15				
corner16				
corner17				

194. Choose corner condition to view OP results. Select corner1 for corner.
195. Click **View Results**.

The screenshot shows the Synopsys Custom Compiler interface with the title bar "15 Opamp_OpenLoop · OP Points Results - Custom Compiler". The menu bar includes File, View, Results, Window, Help. The toolbar has icons for Home, Library Manager, Open, Save, and others. The main window has tabs for CAPACITORS, MOS, NET, RESISTORS, and VSRC. The MOS tab is active, showing a table with 13 rows of data. The columns are: name, analysis, corner, mos_model, res, temp, time, vdd, beta, and cbtot. The data rows show various device names like ADMM1 through ADMM8, analysis type (op), corner (corner1 or corner2), and various parameter values.

Note, that there are separate tabs to show MOS devices, nets and voltage sources. If you have other devices like resistors and capacitors, they also will be shown in separate tabs.

196. Switched to MOS tab to view operating point results for MOSFETs.
Leave only columns, in which you are interested, by hiding other ones.
197. Right click on column header and choose **Show/Hide Columns...**
198. Select corner conditions and desired OP parameters to show/hide.

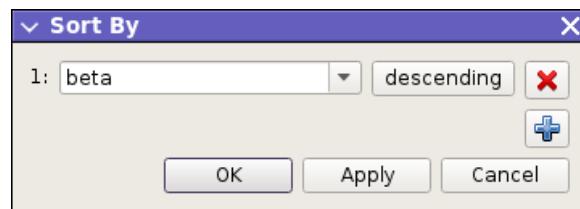
The screenshot shows the "Show/Hide Columns" dialog box over the OP Points Results table. The dialog lists numerous parameters with checkboxes: Select All, name, analysis, corner, mos_model, res, temp, time, vdd, beta, cbtot, cibot, cdibot, cgd, cgs, cgrat, cxtot, gam_eff, gds, gm, gmb, ibd, ibs, id, region, vbs, vds, vdsat, vgs, vod, vth. The checkboxes for time, vdd, beta, and cbtot are checked. The background table shows the same 13 rows of OP point data as the previous screenshot.

199. Click OK

name	analysis	corner	res_model	res	temp	vdd	beta	gm/eff	gds	gm
1 R1	op	corner1	TT	1.5000k	25.000	0.80000	1.0370m	0.48800	0.25123u	15.460u
2 R2	op	corner1	TT	1.5000k	25.000	0.80000	0.56784m	0.48800	0.12487u	31.764u
3 R3	op	corner1	TT	1.5000k	25.000	0.80000	1.6798m	0.52800	0.4211n	10.479u
4 R4	op	corner1	TT	1.5000k	25.000	0.80000	1.9124m	0.52900	0.1011n	10.380u
5 R5	op	corner1	TT	1.5000k	25.000	0.80000	1.6869m	0.52800	2.4828u	34.211u
6 R6	op	corner1	TT	1.5000k	25.000	0.80000	7.8736m	0.52800	0.15948u	38.507u
7 R7	op	corner1	TT	1.5000k	25.000	0.80000	3.0364m	0.48800	0.25363u	15.498u
8 R8	op	corner1	TT	1.5000k	25.000	0.80000	0.98709m	0.52800	48.624n	13.491u
9 R9	op	corner1	TT	1.5000k	25.000	0.80000	0.98709m	0.52800	48.000n	13.445u
10 R10	op	corner1	TT	1.5000k	25.000	0.80000	0.58765m	0.48800	13.482u	19.523u
11 R11	op	corner1	TT	1.5000k	25.000	0.80000	0.55711m	0.52800	0.61426u	0.17582m
12 R12	op	corner1	TT	1.5000k	25.000	0.80000	2.8373m	0.48800	0.67294u	0.15802m

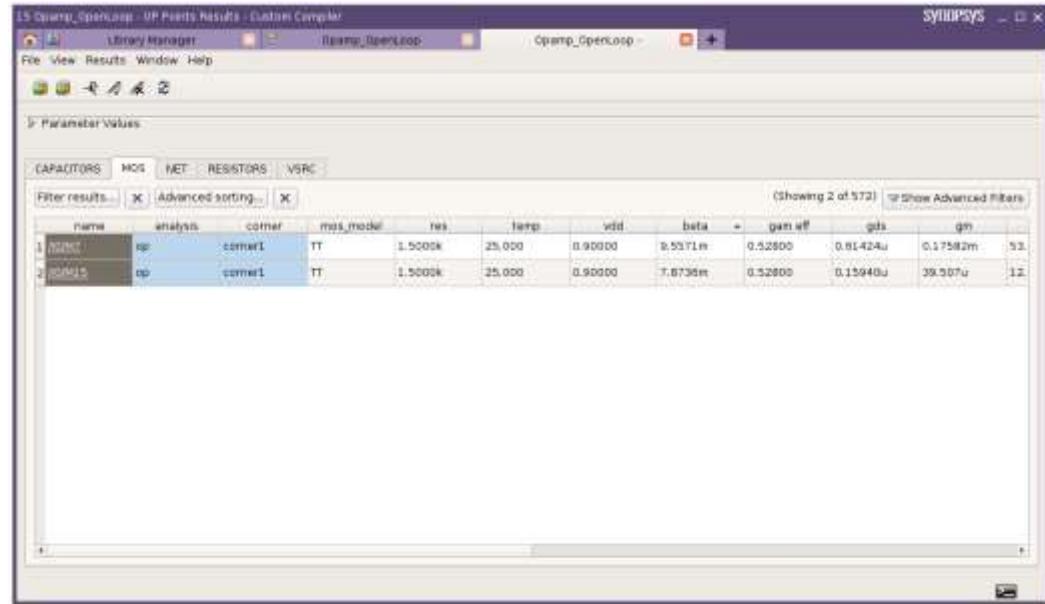
200. Sort results using parameter beta. Click on **Advanced sorting...**

- 201. Click on button to add sorting rule.
- 202. Click on **ascending** button to change it to **descending**, choose parameter *beta* and click OK.



203. Filter results using parameter beta. Click on **Filter results...**

- 204. Click on button to add filtering rule.
- 205. Choose parameter *beta* and specify it to be greater than 5m
- 206. Click OK

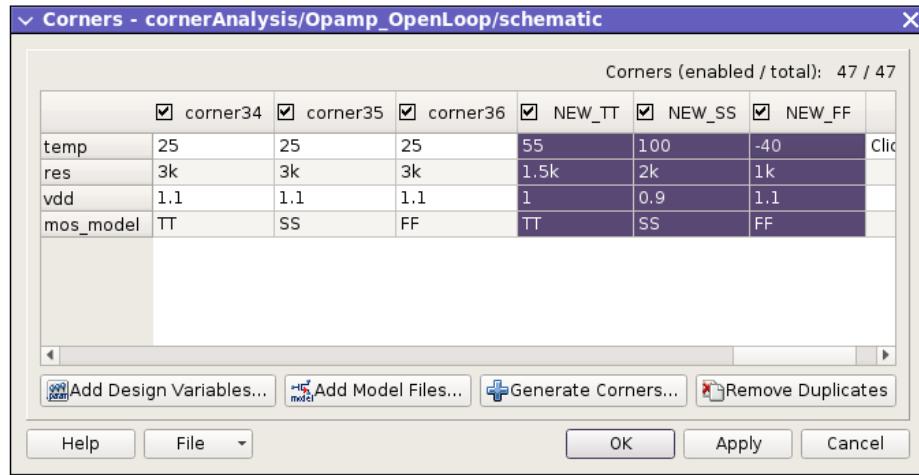


207. Close OP Point Results window.

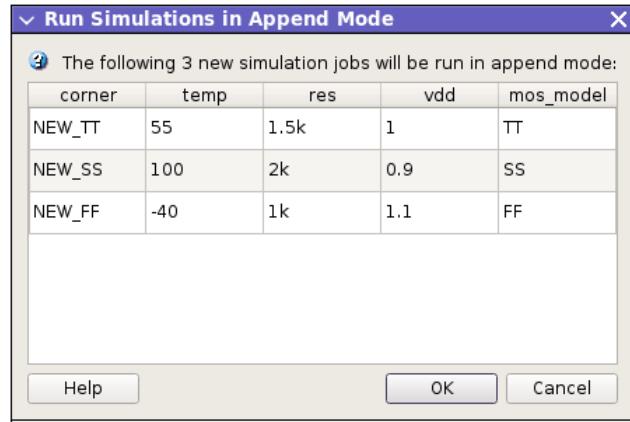
Task 53. Append new corners

In this task you will add more corners to already run results.

208. Add new additional corners to corners setup. Use **Tools > Corners** and add NEW_TT, NEW_SS and NEW_FF corners.

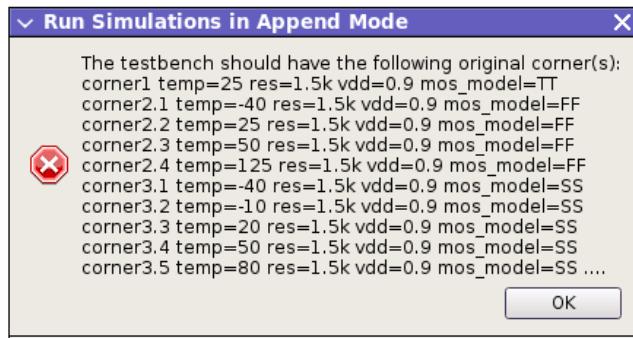


209. Click OK to accept changes and close the dialog.
210. From SAE main window press Run+ button . Pop up will show which corners will be run in append mode.

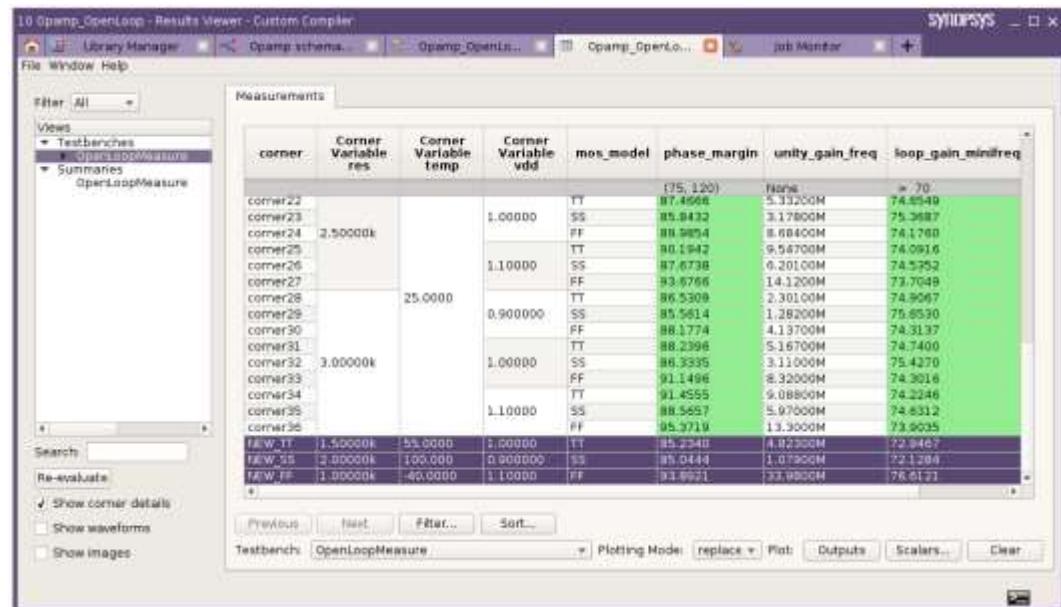


Note:

In order to use simulation append mode (Run +), you should not change original corner/sweep setup. For example, disable some corners in your original corners setup and you will get following message



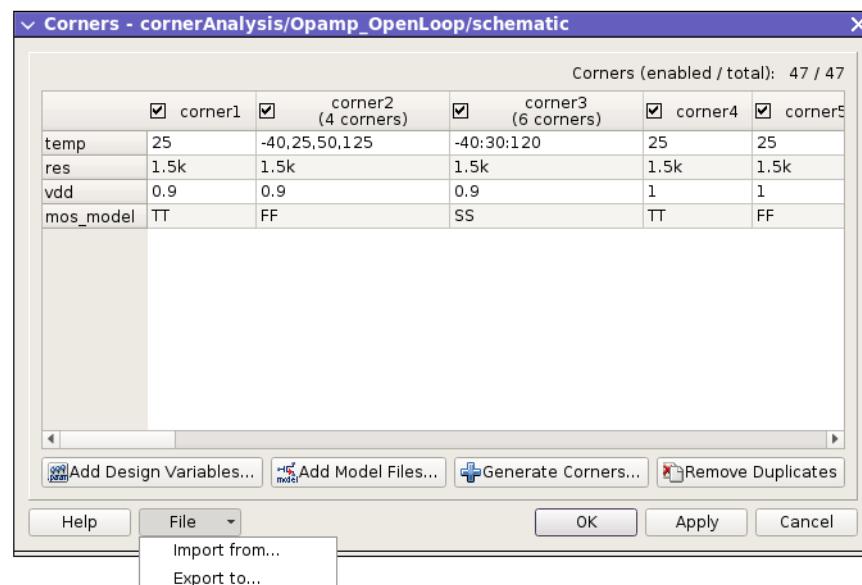
211. Press OK to launch the jobs.
212. After simulations are completed, open Results Viewer using **Results > Viewer...**
213. Scroll results table till the end and notice new corners are appended to the results.

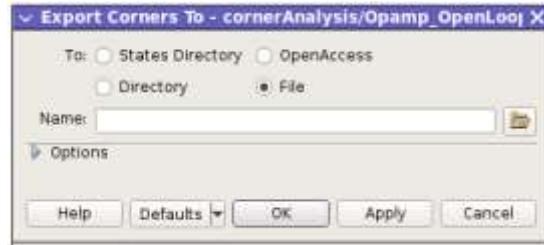


Task 54. Exporting Corners to a File

In this task you will export generated corners to the file. That file can be used to import corners to some other SAE session later if needed.

214. Open Corners dialog using Tools > Corners...
215. Click on File button and click on Export to... item.





216. Specify file name and press **OK** button.

Congratulations!

You have successfully performed Corners analysis to optimize your circuit using SAE.

5

Monte Carlo Analysis

Learning Objectives

The main goal of this lab is to familiarize you with the Monte Carlo analysis to see the effects of process variations on circuit performance.

After completing this lab, you should be able to:

- Perform Monte Carlo analysis
- Analyze the results

Lab Duration:
30 minutes

Introduction

During this lab, you will use the Monte Carlo analysis to analyze the opamp design with varying threshold voltage ($vth0$) of transistors.

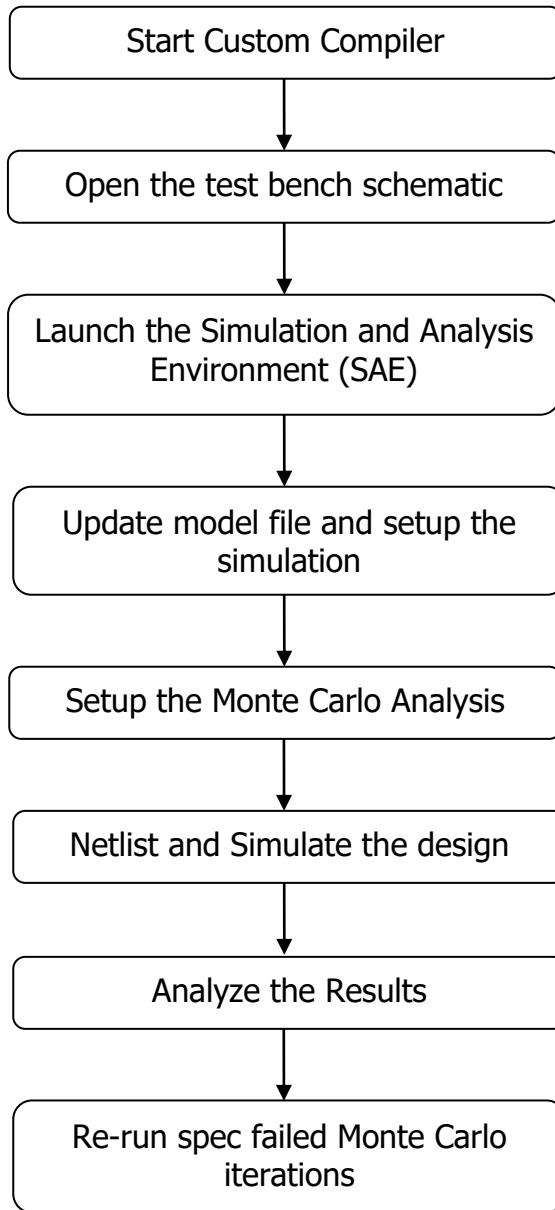
In this lab, you are provided with the *MonteCarlo* OpenAccess database library and a *lib.defs* file. The *MonteCarlo* library contains the opamp testbench Opamp_OpenLoop. The *lib.defs* is the default library definition file that contains library name mapping to their physical location.

Before verifying the performance of the circuit, it is important to understand the use model of the commands that are required to verify it.

Please refer to the *Simulation and Environment User Guide* for the commands that are used in this lab.

Flow Overview

Lab 1 Tasks



File Locations

All files for this lab are located in the directory `SAE_MonteCarlo_Lab1`.

Directory Structure

<code>SAE_MonteCarlo_Lab1</code>	Current working directory
<code>MonteCarlo</code>	OpenAccess Design library
<code>lib.defs</code>	Library Definitions file

Answers & Solutions

There is an *ANSWERS / SOLUTIONS* section at the end of this lab. You are **encouraged** to refer to this section often to verify your answers, or to obtain help with the execution of some steps.

Tool Versions

Custom Compiler	O-2018.09-SP1
HSPICE	O-2018.09-SP1
Custom Explorer	O-2018.09-SP1

Instructions

Task 55. Start Custom Compiler

217. In the UNIX terminal window change your current working directory to *SAE_MonteCarlo_Lab1*. This will be your working directory for this lab.
218. Start Custom Compiler from the UNIX prompt.

```
custom_compiler &
```

Task 56. Open the Test Bench Circuit

219. From the design library *MonteCarlo*, open the schematic cell *Opamp_OpenLoop* of the view name *schematic*.

Note: *Opamp_OpenLoop* cellView will be opened in a Schematic Editor window.

Task 57. Launching Simulation and Analysis Environment

220. Invoke the Simulation and Analysis Environment using **Tools → SAE**.

Note: This will open up the Simulation and Environment window which comes with design *MonteCarlo/Opamp_OpenLoop/schematic* pre-populated.

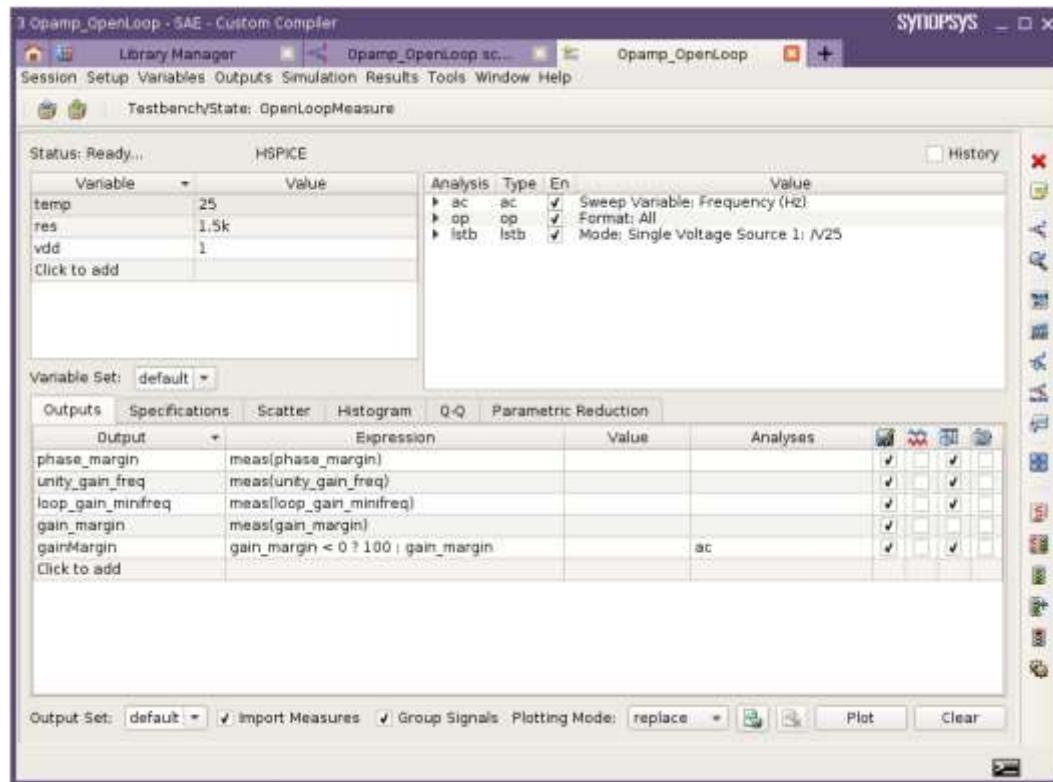
Task 58. Load the State

In this task, you will load the simulation setup for *Opamp_OpenLoop* where you will perform the Monte Carlo analysis to verify the signal performance of the opamp.

221. From SAE window, load the state *OpenLoopMeasure* from the OpenAccess database using **Session → Load State....**

Note: This will load simulation setup for tran and op analyses, will set correct model file and setup outputs for measurements.

222. SAE window should look like as shown in the image:



223. Switch to **Specifications** tab and observe spec limits for **phase_margin** and **loop_gain_minifreq**.

Output	Expression	Value	Analyses
phase_margin	meas(phase_margin)		ac
unity_gain_freq	meas(unity_gain_freq)		ac
loop_gain_minfreq	meas(loop_gain_minfreq)		ac
gain_margin	meas(gain_margin)		ac
gainMargin	gain_margin < 0 ? 100 : gain_margin		ac
Click to add			

Task 59. Setup the Monte Carlo Analysis

In this task, you will setup the Monte Carlo analysis by varying the transistor threshold voltage, v_{th0} .

224. From the UNIX console open the model file $../PDK/hspice/variations.lib$ with your favorite text editor.

Note: This will open model file used during simulation

225. Observe the Variation Block, which was added in the model file:

.Variation

.Global_Variation

Nmos N vth0=0.07

Pmos P vth0=0.06

.End_Global_Variation

.End_Variation

Note: In the example, the normal absolute variation on the threshold parameter vth0 is specified (sigma of 70mV or 60mV). For more information about Variation Block please refer to HSPICE User Guide: Simulation and Analysis.

226. From SAE window open the Monte Carlo Analyses dialog using **Tools → Monte Carlo**

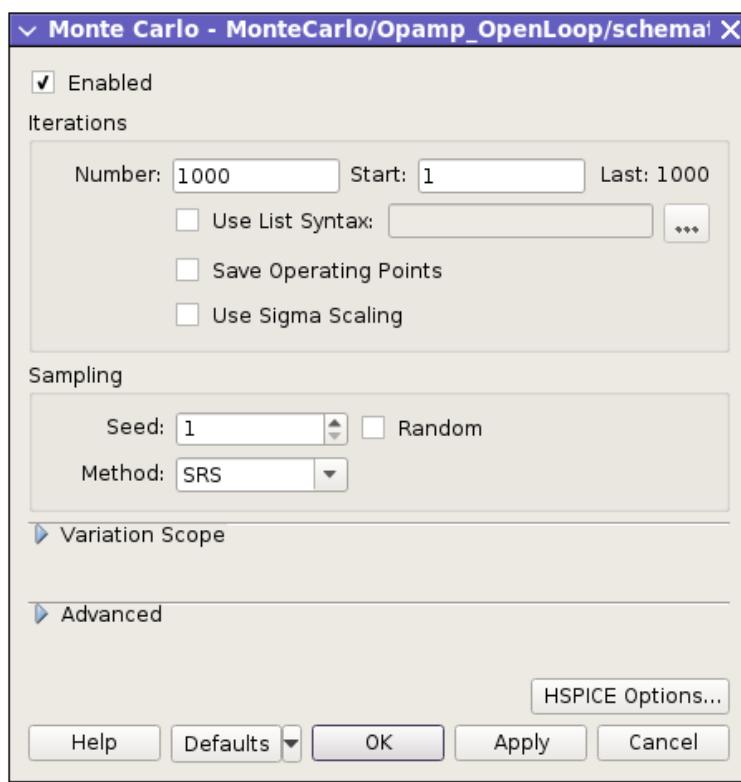
227. Fill the form as follows:

a. Iterations:

i. Number: 1000

ii. Starting: 1

228. Check **Enabled** button in the dialog to enable Monte Carlo analyze.



229. Click **OK**. This will setup the Monte Carlo analysis for Opamp_OpenLoop circuit.

Note: The Monte Carlo analysis appears in the main SAE window under the analysis section.

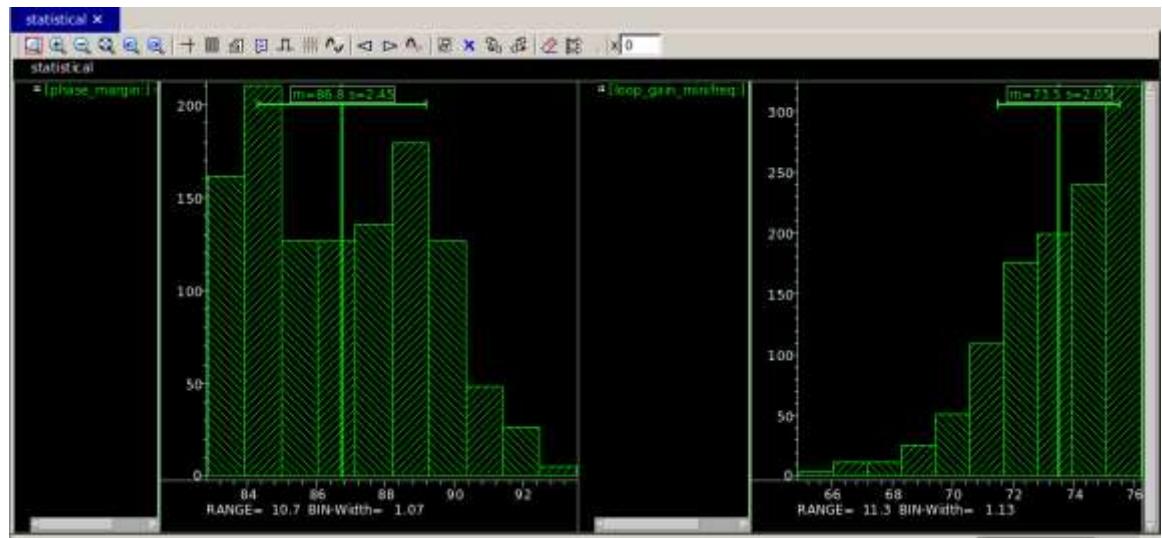
Task 60. Netlist and Simulate the Design

In this task, you will netlist and simulate the *Opamp_OpenLoop* schematic with varying *vth0* parameter.

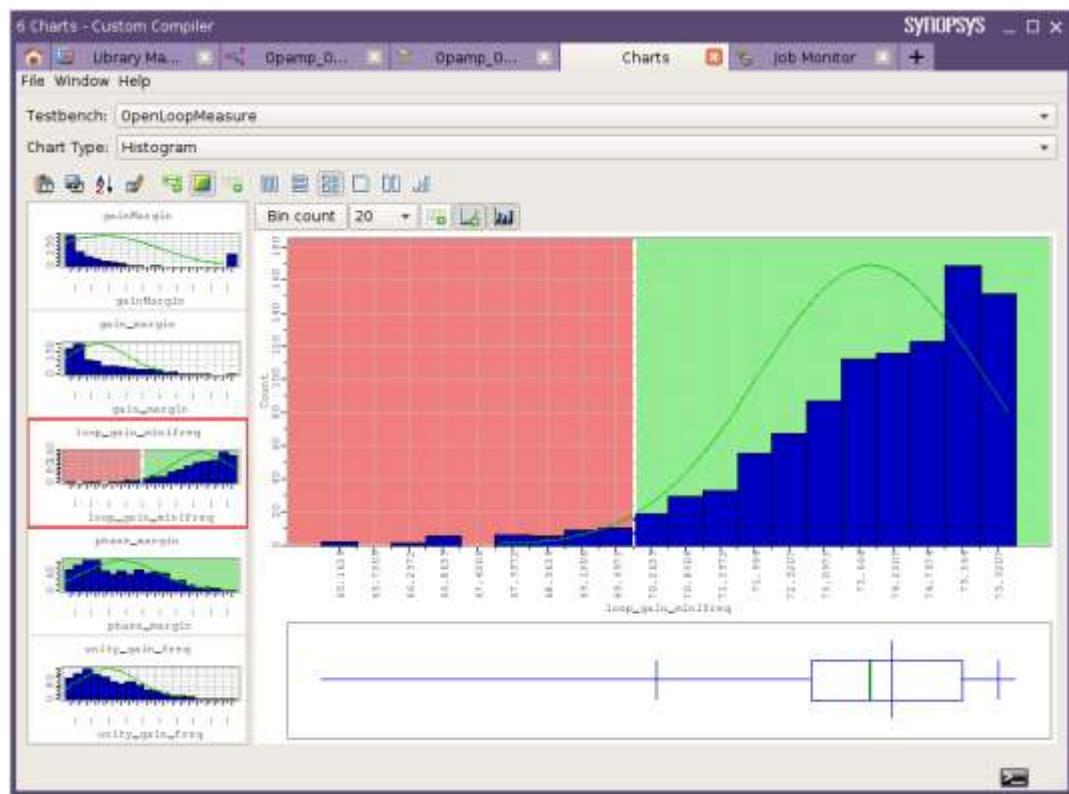
230. From SAE window, generate the netlist and simulate the design using **Simulation → Netlist and Run**.

Note: After the simulation finishes the specified outputs will be evaluated and plotted in WaveView. WaveView will statistical histograms for selected measurements.

231. Observe the **statistical** tab in WaveView window. Check the histograms and the mean values of **phase_margin** and **loop_gain_minifreq**.

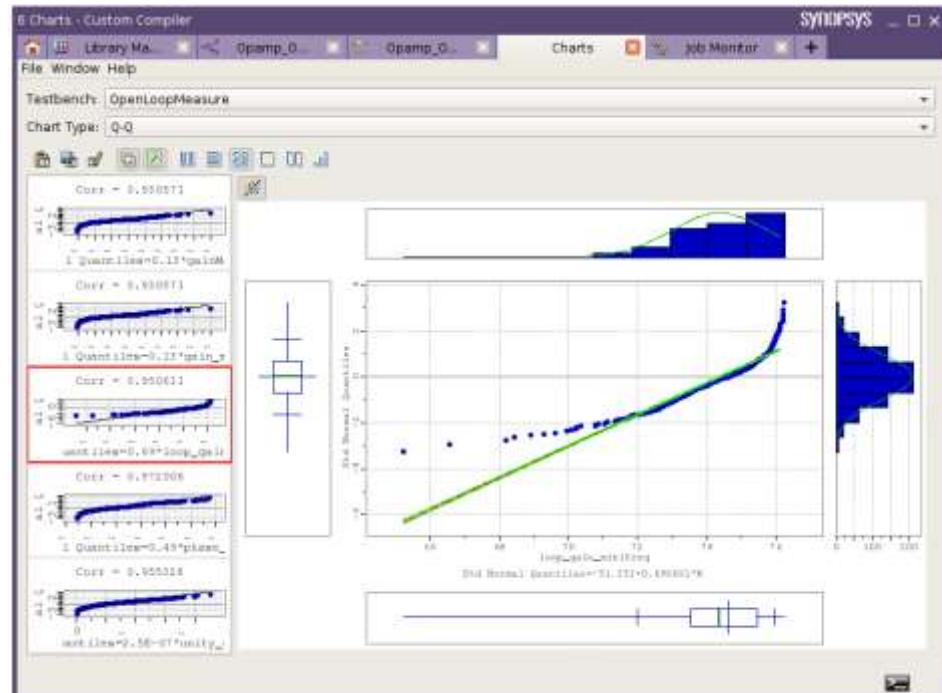


232. Histograms can be also viewed using Charts. To open Charts use **Results → Charts...** and select *Histogram* for **Chart Type**.



Measurements values inside green are in specification, and values inside the red region are values violating given specification.

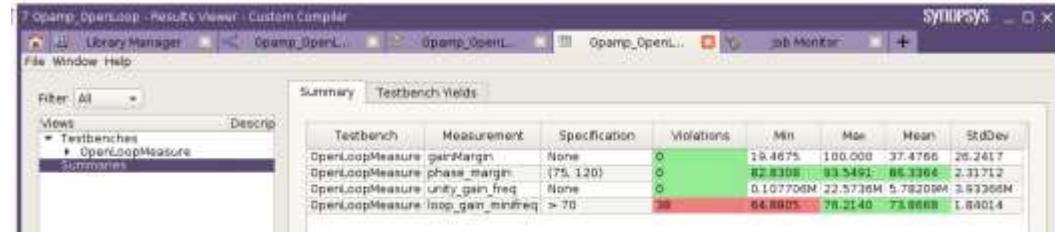
233. Switch **Chart Type** to Q-Q and observe them. The quantile-quantile (Q-Q) plot is a graphical technique for determining if two data sets come from populations with a common distribution.



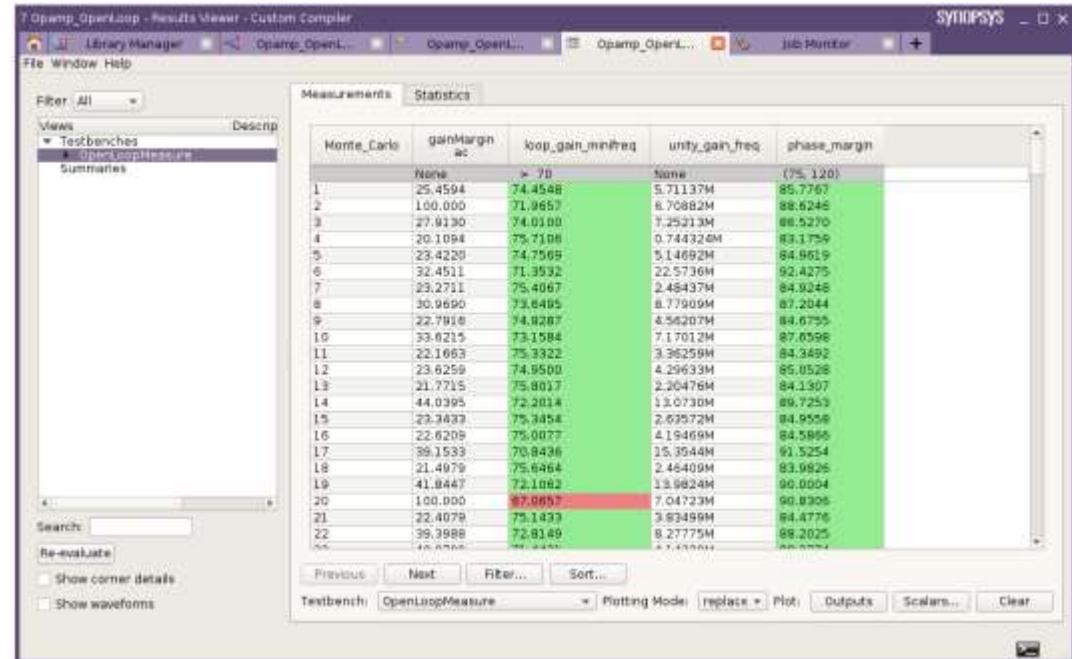
For true Gaussian distribution all data points are approximately on the same straight line.

234. Close the Charts window.
235. To see the measurements results for each iteration click on **Results → Viewer...** from SAE main window.

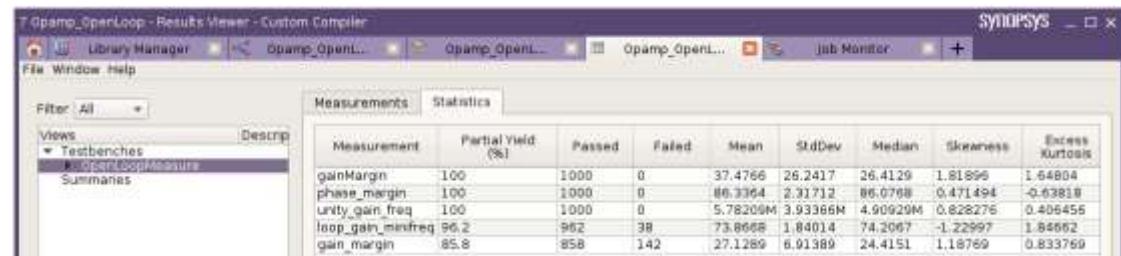
Observe that 38 iterations are failing for loop gain.



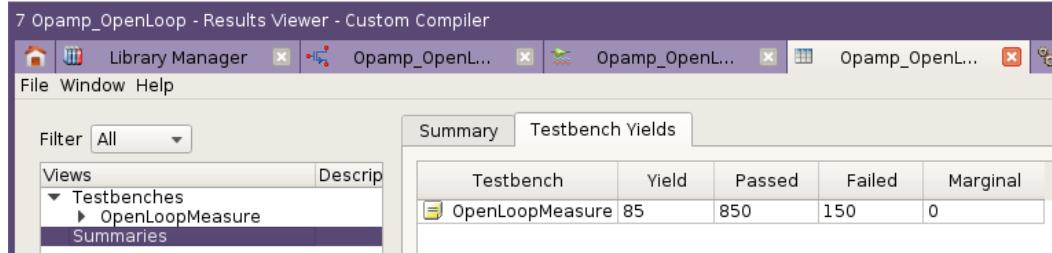
236. Click on testbench **OpenLoopMeasure** to see the results for each Monte Carlo iteration.



237. Click on the Statistics Tab in the RV, and observe the various statistical quantities, like partial yield, mean, sigma, skewness, excess kurtosis, etc.



- 238.** Click on the **Summaries** entry in the tree on the left, and observe the statistical summary data including overall yield.



- 239.** Close Results Viewer.

Task 61. Adjusting the Circuit and Running Failed Iterations

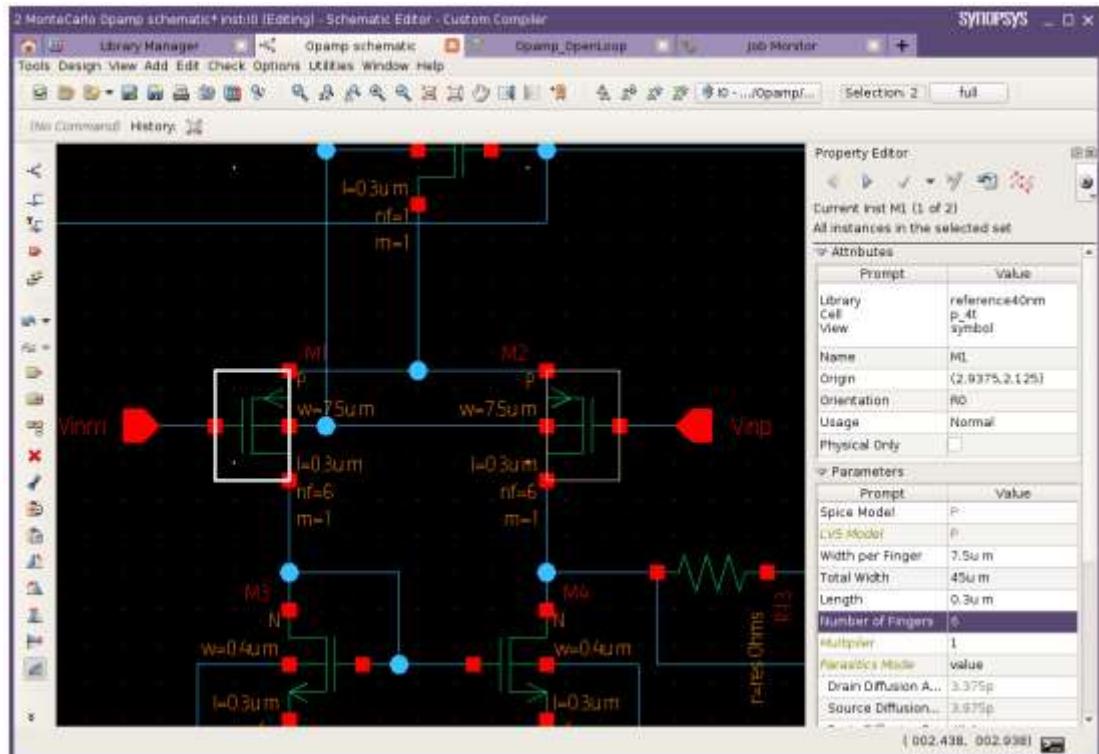
In this task you will fix loop gain violations, by adjusting the circuit and running only failed Monte Carlo iterations.

- 240.** Open design schematic and change adjust M1 and M2 device sizes as follows:

w=7.5u

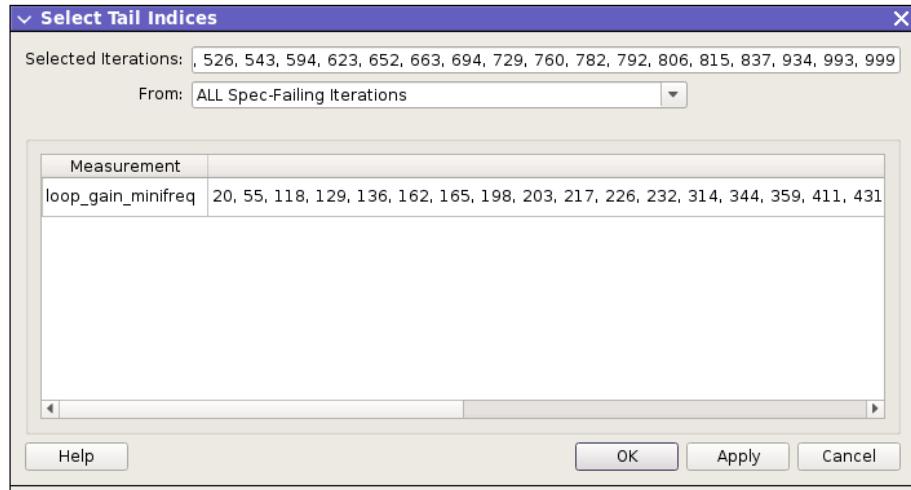
l=0.3u

nf=6

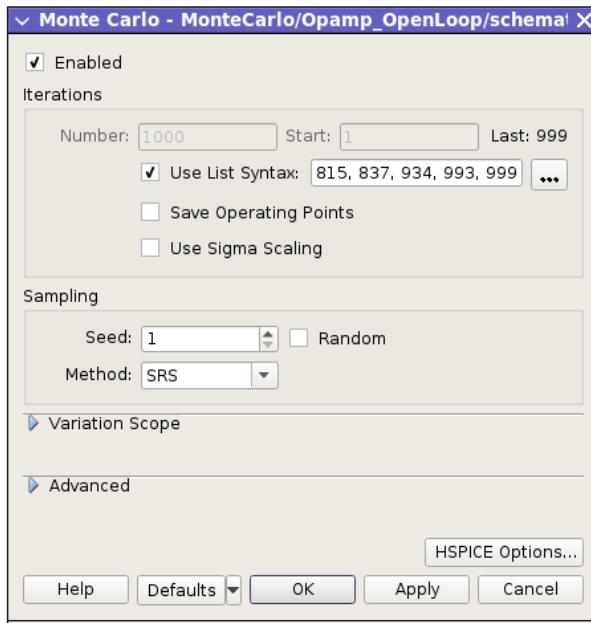


- 241.** Check and Save the design.

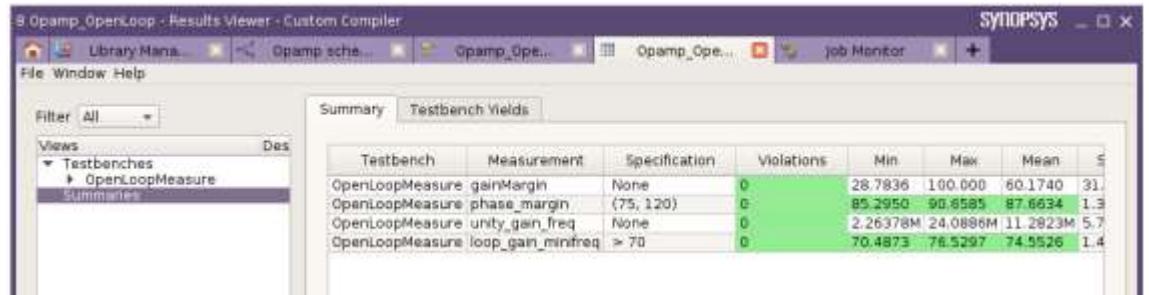
242. Open Monte Carlo setup dialog from **Tools > Monte Carlo ...**
243. Check **Use List Syntax** checkbox and press **...** button to invoke the ‘Select Tail Indices’ dialog.



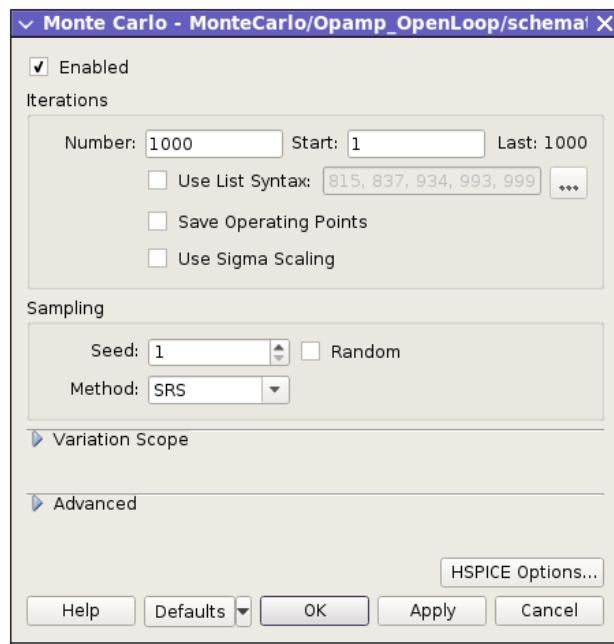
244. Expand **From** drop down menu and observe available choices. Leave it to stay **All Spec-failing iterations**.
245. Press OK. Monte Carlo setup dialog should look like image below:



246. Press OK.
247. Netlist and run simulation using **Simulation > Netlist and Run**.
248. Observe results using **Results → Viewer...** Note that there are no failures for loop gain measurement.

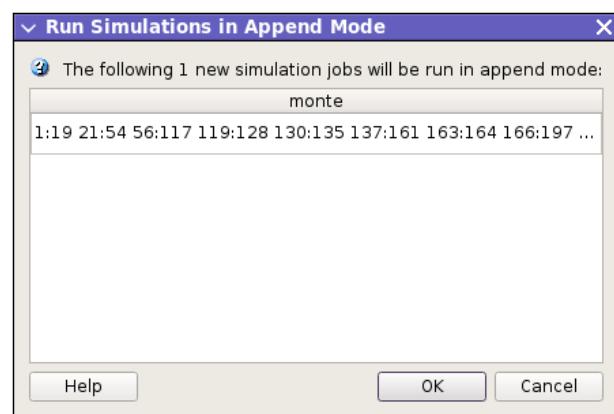


249. Now, as you fixed the circuit, you need to run whole set of Monte Carlo to confirm the fix.
250. Disable Use List Syntax and run 1000 iteration of Monte Carlo.

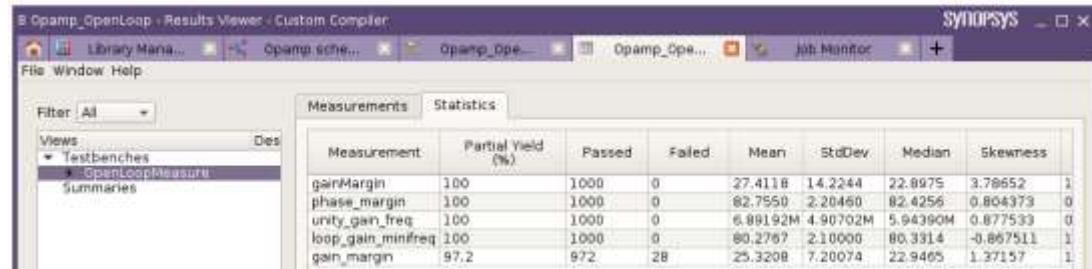


251. Hit Run+ button  to sun simulation in Append Mode. Previously run Monte Carlo iterations will be skipped.

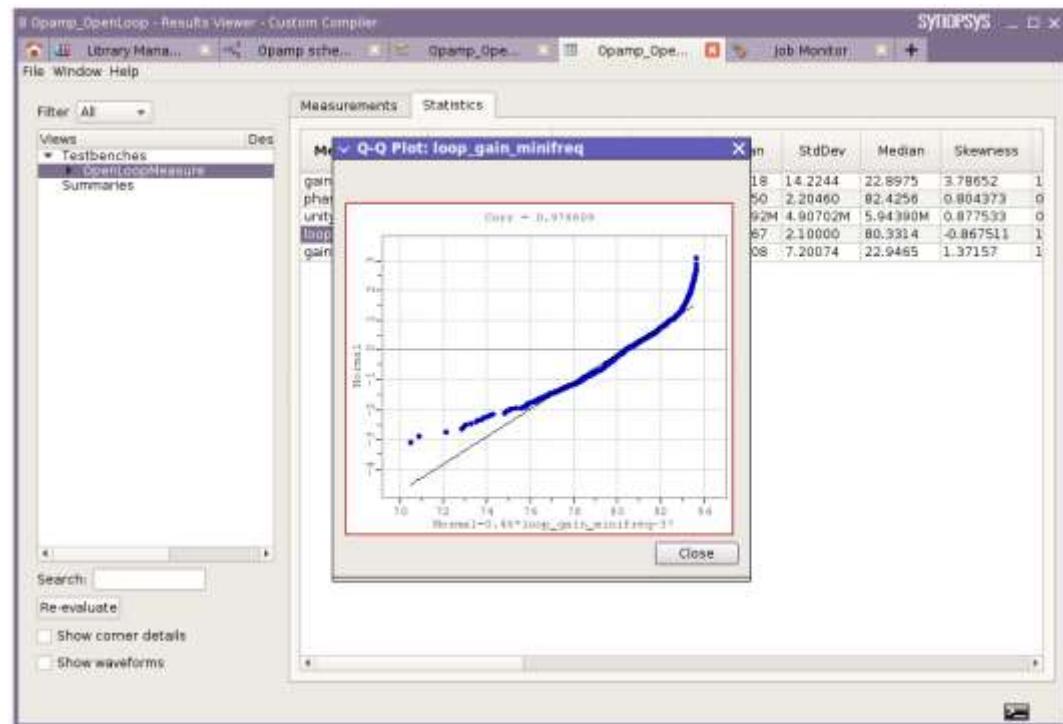
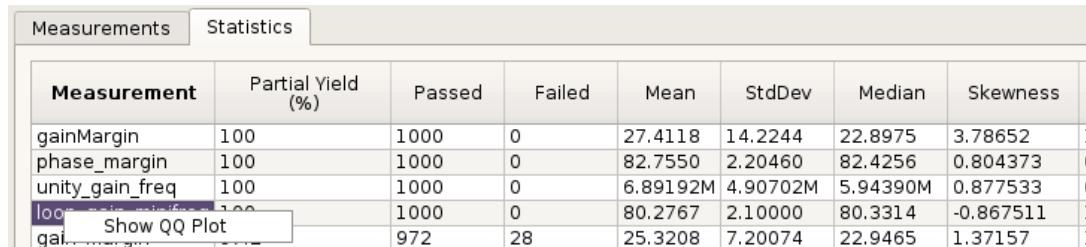
Dialog showing new iterations to be run will pop up.



252. Click OK to start simulations.
253. Open Results Viewer and observe statistical data for the measurements. You get 100% of yield for loop gain measurement for all 1000 Monte Carlo iterations.



254. Observe Q-Q plots after fixing the circuit. Right mouse button click on the measurement name in Statistics tab and click on **Show QQ Plot**.

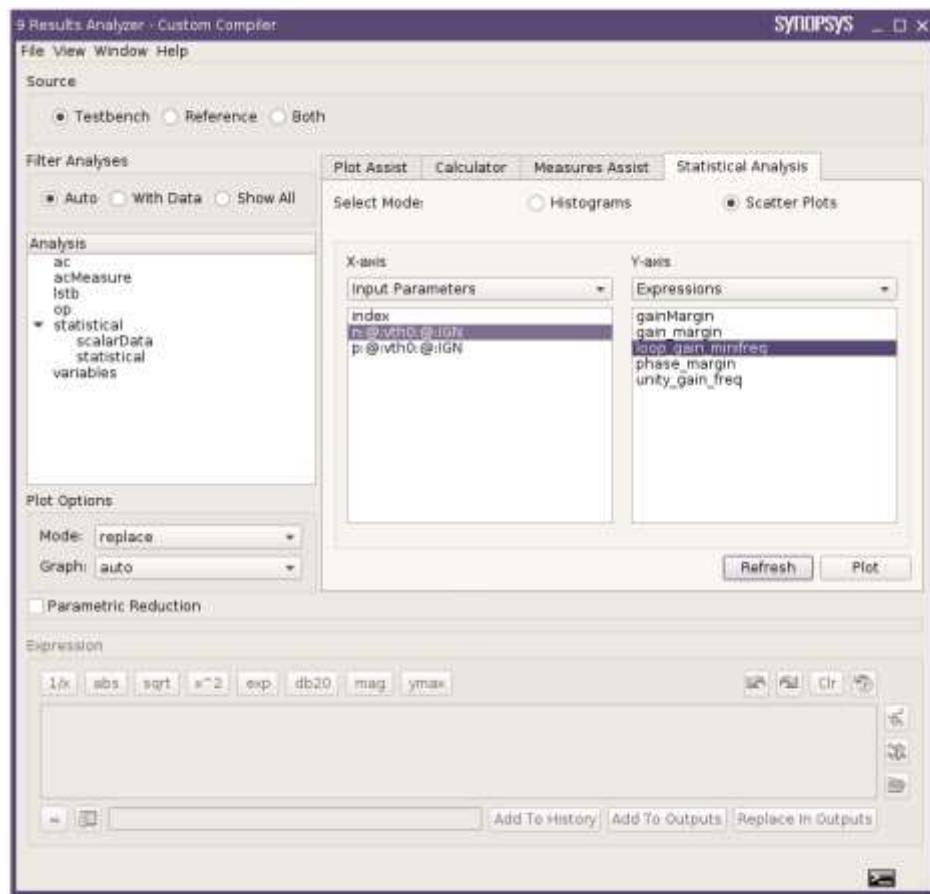


255. Close Q-Q Plot and Results Viewer windows.

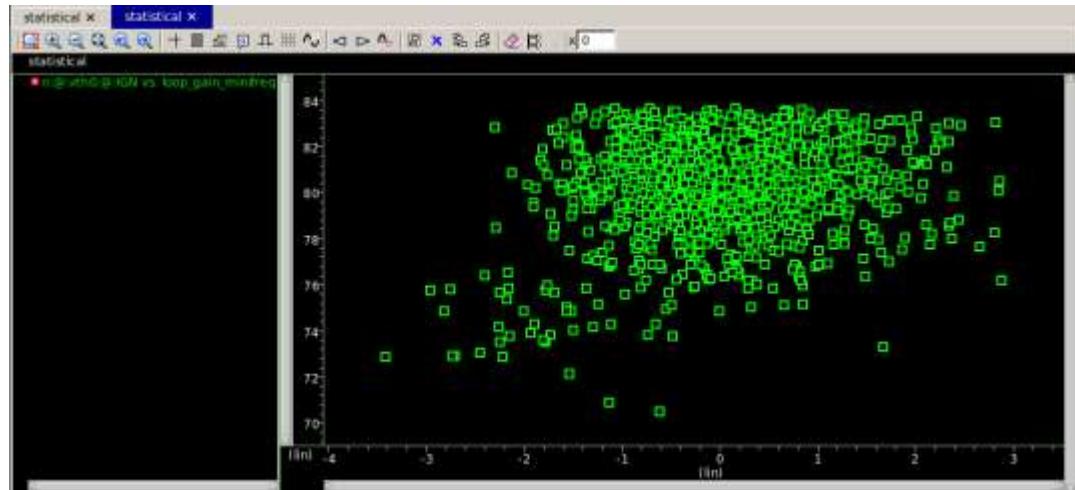
Task 62. Working with Results Analyzer

In this task you will debug Monte Carlo results using Results Analyzer.

256. From the SAE window open Results Analyzer by selecting **Results → Analyzer...**
257. In the opened Results Analyzer dialog select **Statistical Analysis** tab. Note that you can plot Histograms and Scatter Plots from Results Analyzer.
258. Select **Scatter Plots**. For X axis choose **Input Parameters** from drop down menu. You will see all parameters which are varied during Monte Carlo analysis.
259. Select **n:@:vth0:@:IGN** from Input parameters for X-axis and **loop_gain_minifreq** for Y-axis.



260. Press Plot button. This will plot scatter chart, where you can observe how opamp **loop_gain_minifreq** measurement is dependent from nmos device threshold voltage variation.



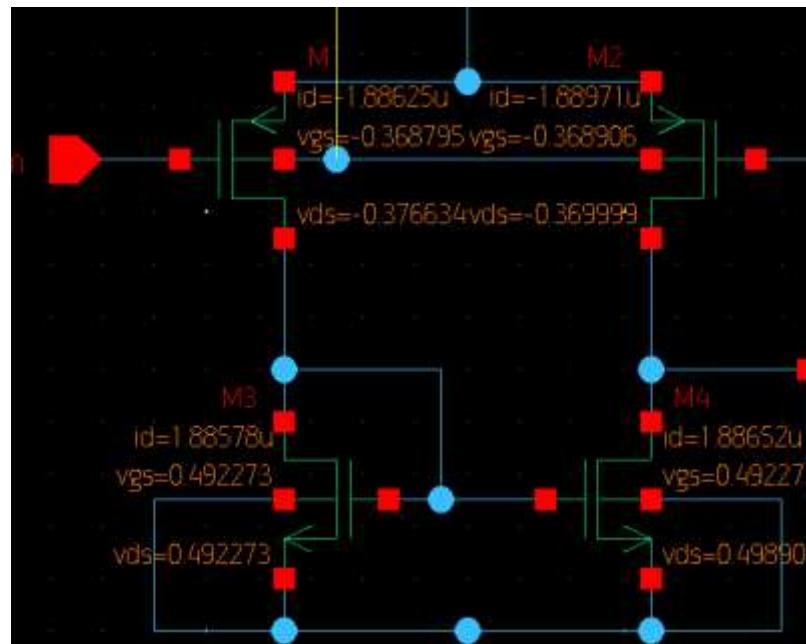
Task 63. Back-annotating Results

In this task, you will learn to back-annotate the results to the schematic.

261. From the SAE window back-annotate the DC operating point using **Results → Annotate → DC Operating Point**

Note: This will bring up the Backannotate DC Operating Point dialog.

262. Select the Monte Carlo iteration number 5 and click OK.
263. Descend one level down the hierarchy in the schematic and you will see the DC Operating Point of the devices corresponding to the 5th iteration of the Monte Carlo Analysis. The annotated data will look as shown in the image below.



Task 64. Printing Results

In this task, you will print out the DC Operating points of the devices for analysis purposes.

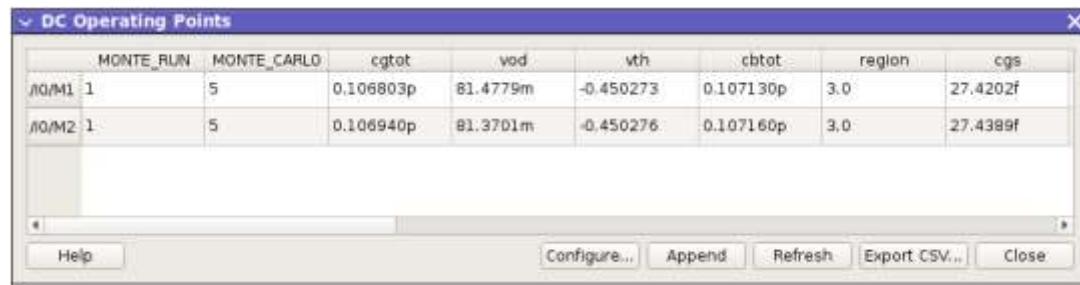
264. From the SAE window, print the DC Operating points using **Results → Print → DC Operating Points**.

Note: This will bring up the Print DC Operating Point dialog.

265. Select the 5th iteration of the Monte Carlo analysis and click OK.

Note: You will prompt to pick the object in the schematic.

266. As you click on the instance M1 and M2 inside the X0 opamp cell, the DC Operating Points form will come up with the operating point information corresponding to the 5th iteration of Monte Carlo analysis.



MONTE_RUN	MONTE_CARLO	cgtot	vod	vth	cbtot	region	cgs
/I0/M1	1	5	0.106803p	81.4779m	-0.450273	0.107130p	3.0
/I0/M2	1	5	0.106940p	81.3701m	-0.450276	0.107160p	3.0

267. Pressing the **Configure** button you can modify the MC iteration number.

268. **Cancel** the DC Operating points form.

269. Close all windows.

Congratulations!

You have successfully performed Monte Carlo analysis to optimize your circuit using SAE

6

HSPICE-HF Simulation Setup

Learning Objectives

The main goal of this lab is to use the Simulation and Analysis Environment in Custom Compiler to netlist and simulate the design using HSPICE-HF and post-process the results using Custom WaveView.

After completing this lab, you should be able to:

- Learn a simple LNA circuit
- Load the state for simulation setup
- Netlist the design
- Simulate the design
- View waveforms using Custom WaveView
- AC gain
 - NF
- Non-linearity: Compression, IP2, IP3

Lab Duration:
15 minutes

Lab 3

Introduction

During this lab, you will setup simulation, generate netlist and simulate the *BTlna_tb* design test bench using HSPICE-HF and verify the results in the waveform tool - Custom WaveView.

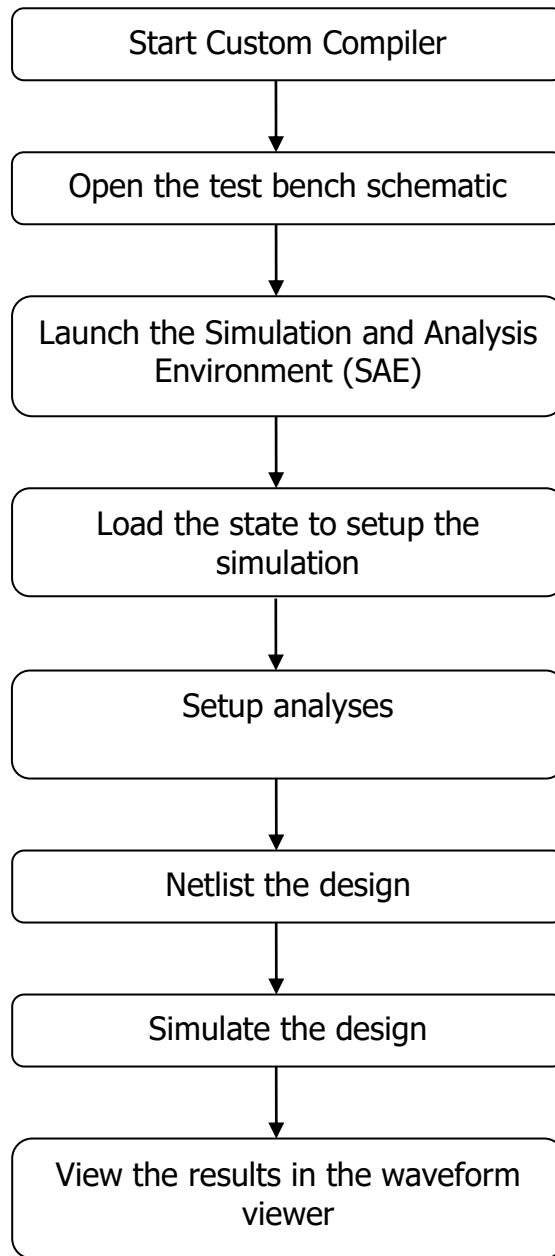
In this lab, you are provided with the *RFLibrary* OpenAccess database library and a *lib.defs* file. The *RFLibrary* library contains the test bench of *BTlna_tb* design. You will make use of this test bench to generate the netlist and simulate your design. The *lib.defs* is the default library definition file that contains library name mapping to their physical location.

Before verifying the performance of the circuit, it is important to understand the use model of the commands that are required to verify it.

Please refer to the *Simulation and Environment User Guide* for the commands that are used in this lab.

Flow Overview

Lab 1 Tasks



Lab 3

File Locations

All files for this lab are located in the directory *SAE_HSPICERF_Lab1*.

Directory Structure

SAE_HSPICEHF_Lab1	Current working directory
RFLibrary	OpenAccess Design library
lib.defs	Library Definitions file

Answers & Solutions

There is an *ANSWERS / SOLUTIONS* section at the end of this lab. You are **encouraged** to refer to this section often to verify your answers, or to obtain help with the execution of some steps.

Tool Versions

HSPICE O-2018.09-SP1

Custom WaveView O-2018.09-SP1

Lab 3

Instructions

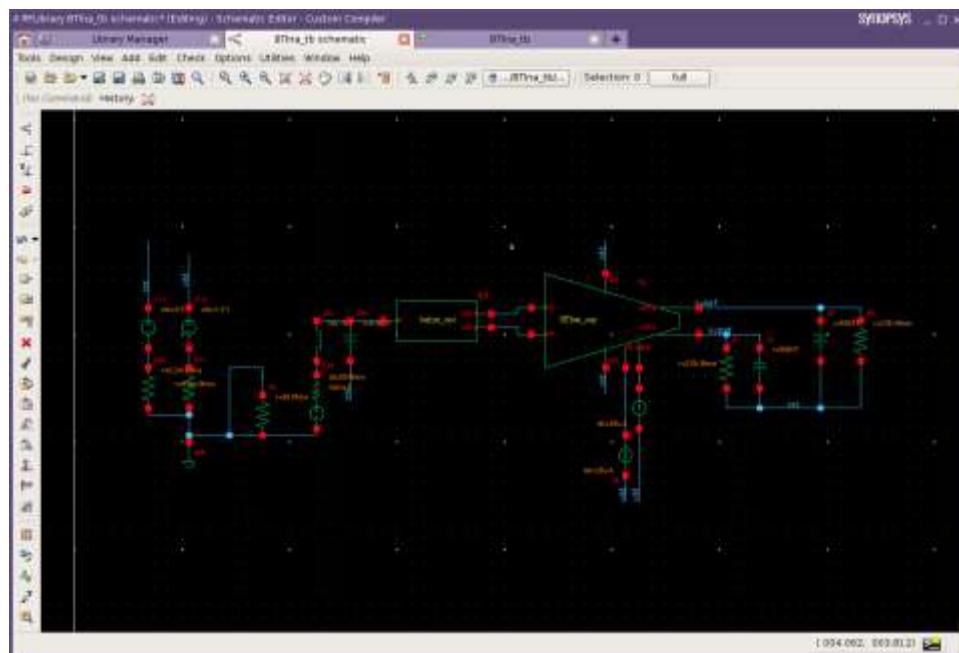
Task 65. Start Custom Compiler

270. In the Unix terminal window change your current working directory to *SAE_HSPICEHF_Lab1*. This will be your working directory for this lab.
271. Start Custom Compiler from the UNIX prompt.

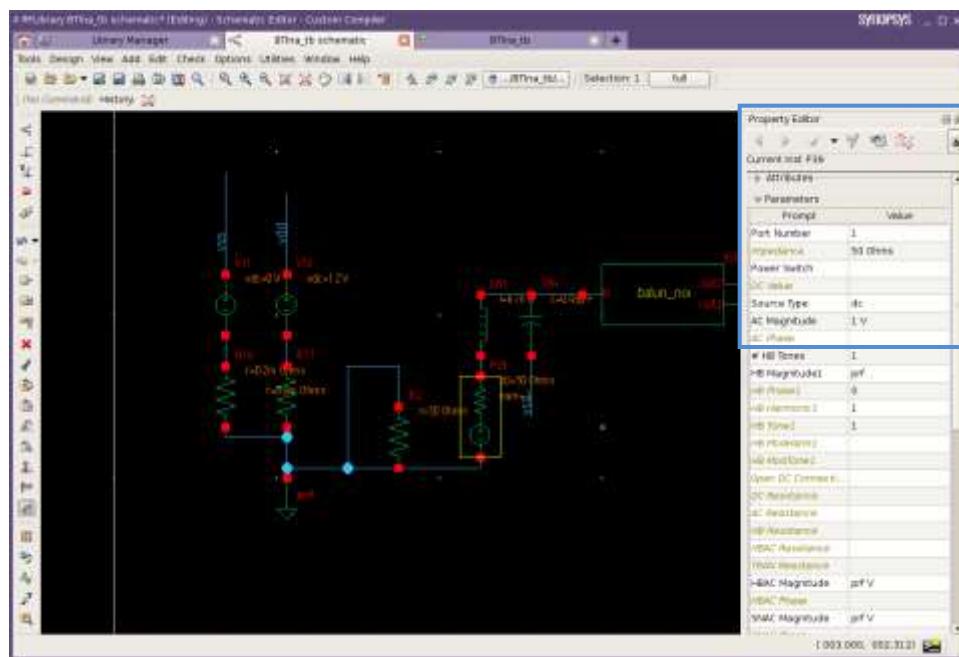
```
custom_compiler &
```

Task 66. Open the Test Bench Circuit

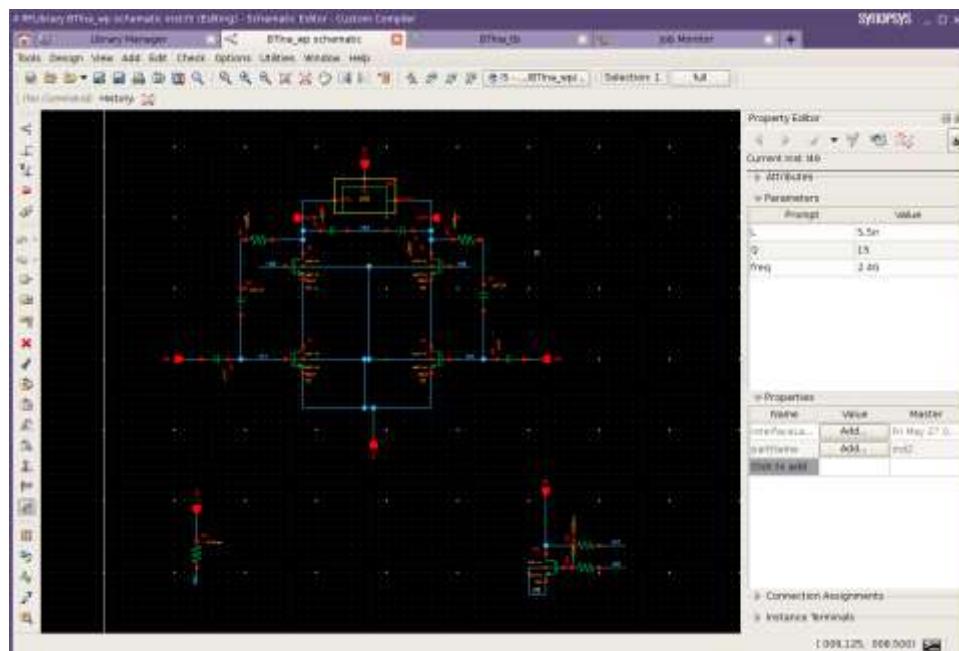
272. From the design library *RFLibrary*, open the *schematic* view of *BTlna_tb* cell. The design will be open in the Schematic Editor window, as shown in the picture below.



273. In the design window select instance P39 (port symbol) and bring out the Property Editor by typing "q" key. In the Property Editor window on the right, verify that
 - a. Power Switch property is blank,
 - b. "Source Type" is set to "dc",
 - c. AC magnitude is set to "1V".



274. Double-click the *BTlna_wp* cell in the schematic design to descend into the *BTlna_wp* circuit.



It's a common-source differential amplifier with resistive feedback input matching and LC tank tuning.

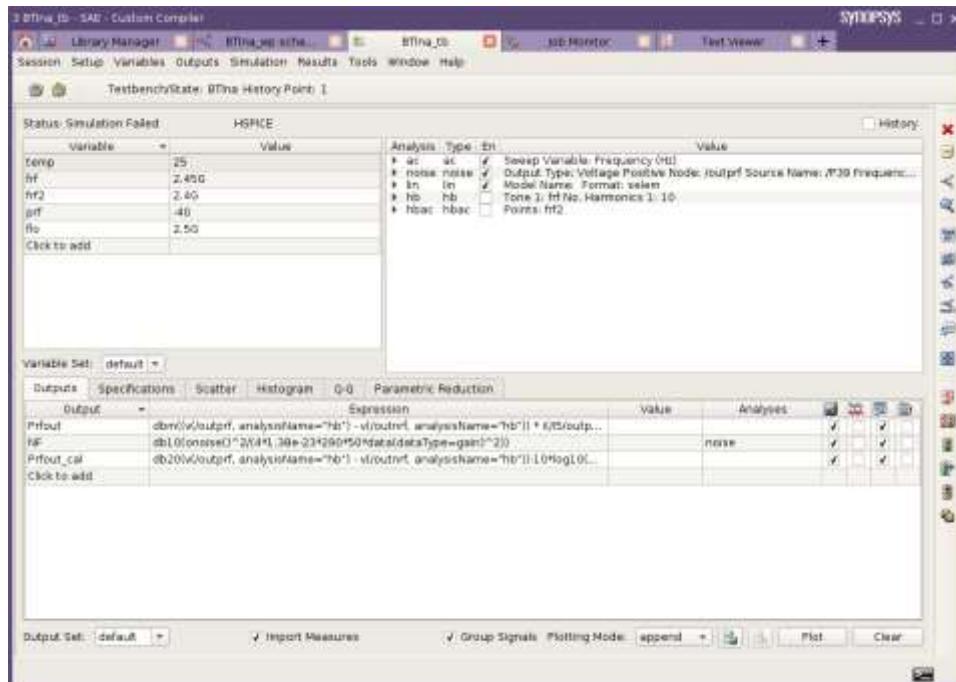
Lab 3

Task 67. Launching Simulation and Analysis Environment

275. Invoke the Simulation and Analysis Environment using **Tools → SAE**.
276. From SAE window load the state *BTlna* from the OpenAccess database using **Session → Load State....**

Note: This will load all the categories which are part of already existing state.

277. SAE window should look like as shown in the image:



Note: Notice in the Outputs window one can define math functions to print/plot signals, i.e. $NF = db10(onoise()^2/(4*1.38e-23*290*50*data(dataType=gain)^2))$

Task 68. Setting Up the Model File

Device models play an important role in predicting the behavior of the circuit during simulation. The device model parameters are generally shipped in a file (that is, SPICE model file) from the foundry. The parameters differ from process to process and from foundry to foundry.

In this task, you will setup the model file path to provide an input to the simulator.

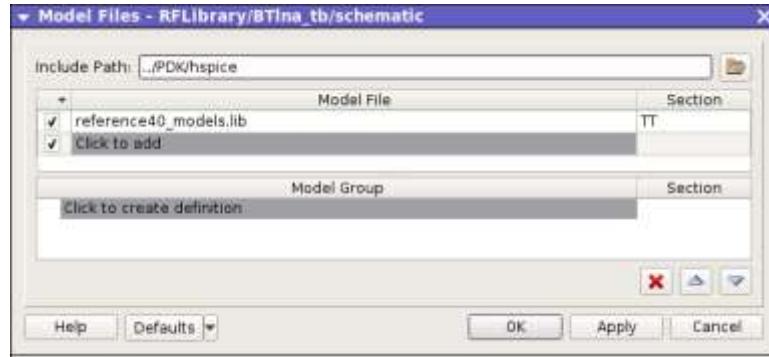
278. From SAE window set up the path of the model file *reference40_models.lib* using **Setup → Model Files...**

```
<path to PDK directory>/PDK/hspice/reference40_models.lib
```

Note: *reference40_models.lib* is provided with the PDK under *hspice* directory.

279. Set the corner Section to *TT* (*typical corner*).

Note: As you click on the section field, drop down list will appear which lists all the available corners (FF, TT, SS ...) from the model file.



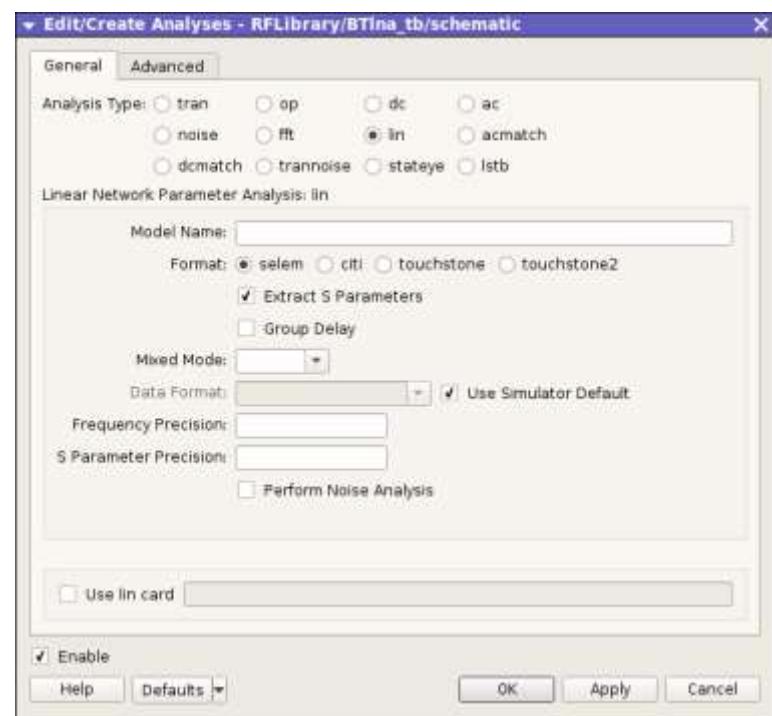
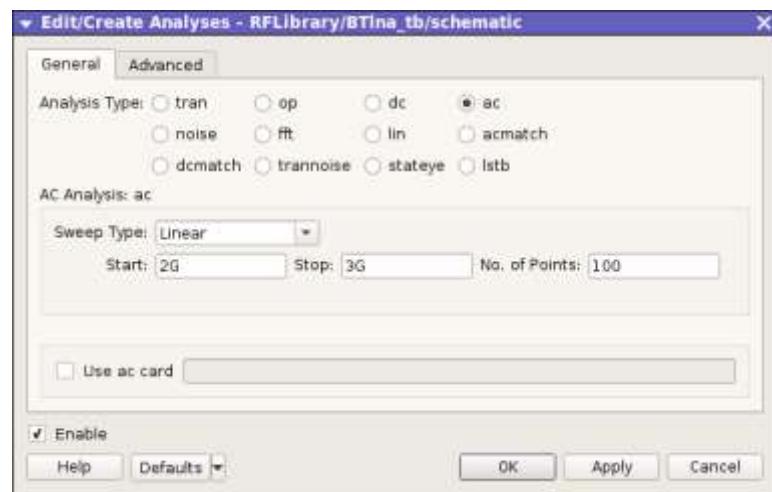
280. Click **OK**. This will setup the model file for simulation.

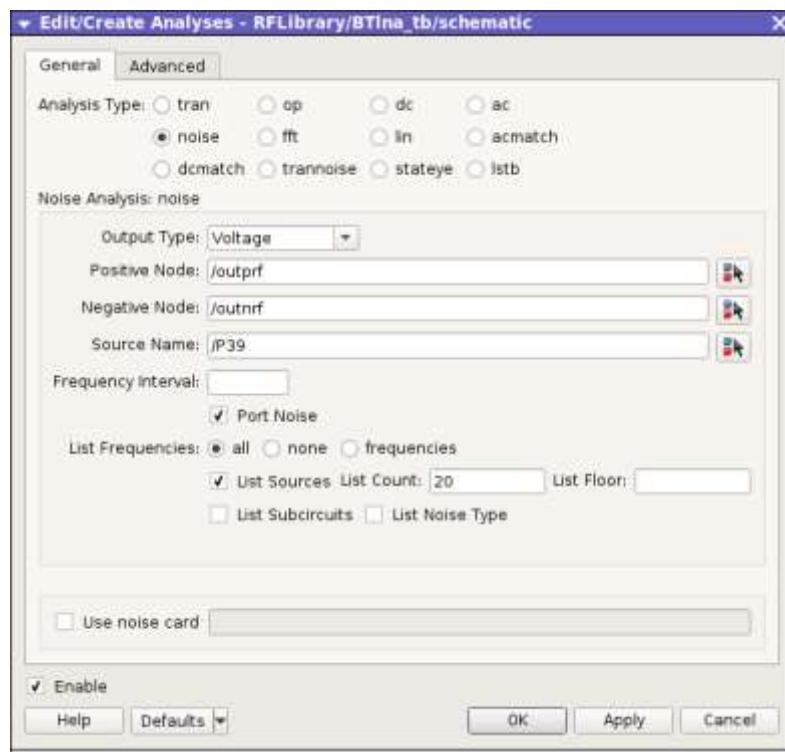
Task 69. Setup Simulation Analyses

In this task, you will set up AC/LIN/NOISE analyses to check the impedance matching, AC gain, and Noise Figure of the LNA circuit.

281. From SAE window launch Edit/Create Analyses dialog by invoking **Setup → Analyses....**
282. Open analyses in the SAE and check AC, LIN, and NOISE analyses settings. They should be as shown in the images below

Lab 3





- 283.** Click OK to setup the analysis.

Task 70. Netlist the Design and Simulate

The next step in the design cycle is to netlist the test circuit which will be the input for the simulation tools to verify the electrical performance and the functionality of the circuit.

In this task, you will generate the netlist of the *TBIna_tb* schematic.

- 284.** From SAE window, generate the netlist using **Simulation → Netlist → Create (N)**.

Note: It opens up the generated final netlist in the Custom Compiler Text Viewer window.

- 285.** Close the Custom Compiler Text Viewer by using **File → Close Window**.

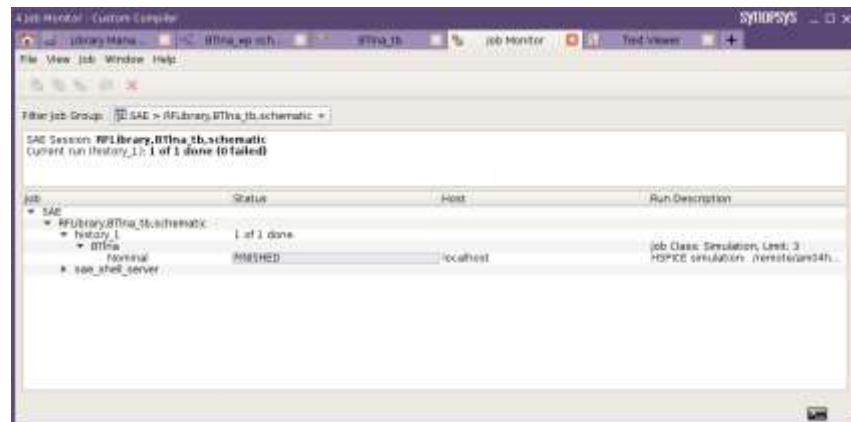
- 286.** From SAE window start the simulation using **Simulation → Run**

Note: The HSPICE simulator will be launched in the specified run directory (in this case: *./simulation*) and will simulate the design.

Note: By default, it opens up the simulation log in the Custom Compiler Text Viewer window.

Lab 3

287. You can observe the status of simulation on the *job monitor* window as shown in the image.

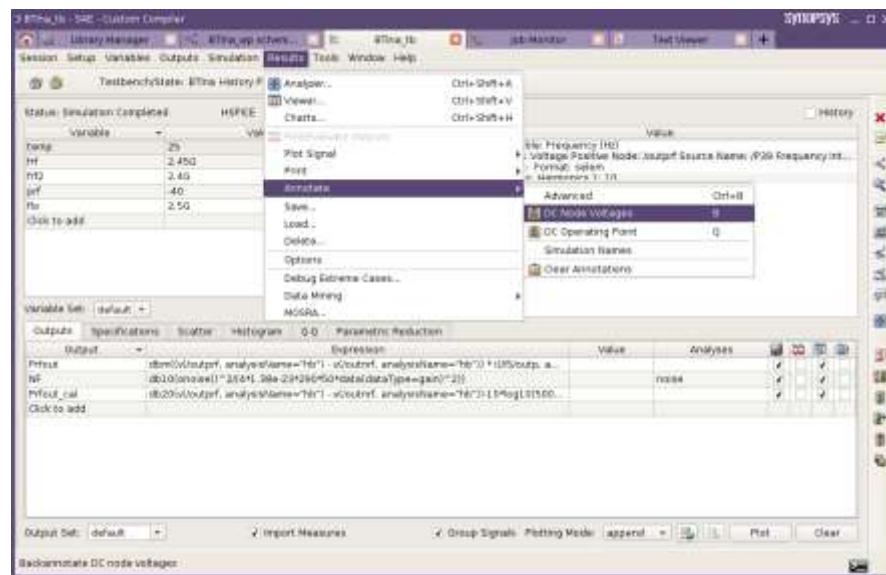


288. Once the simulation is finished, the result is ready to be probed.

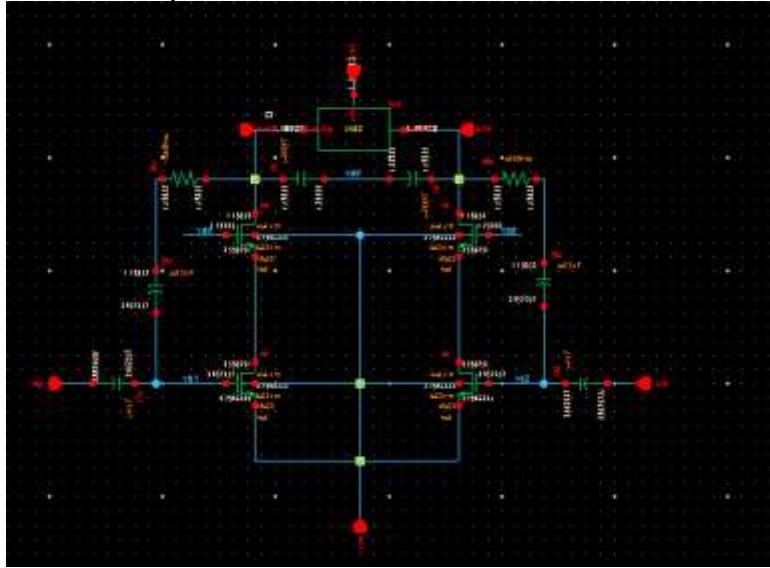
Task 71. Back Annotate the Simulation Results

In this task, you will learn to back annotate the results on to the schematic

289. From the SAE window back-annotate the DC node voltages using **Results → Annotate→ DC Node Voltages**



The DC node voltages will get annotated. Please observe node voltage annotations, picture below shows annotation of “BTlna” schematic design.



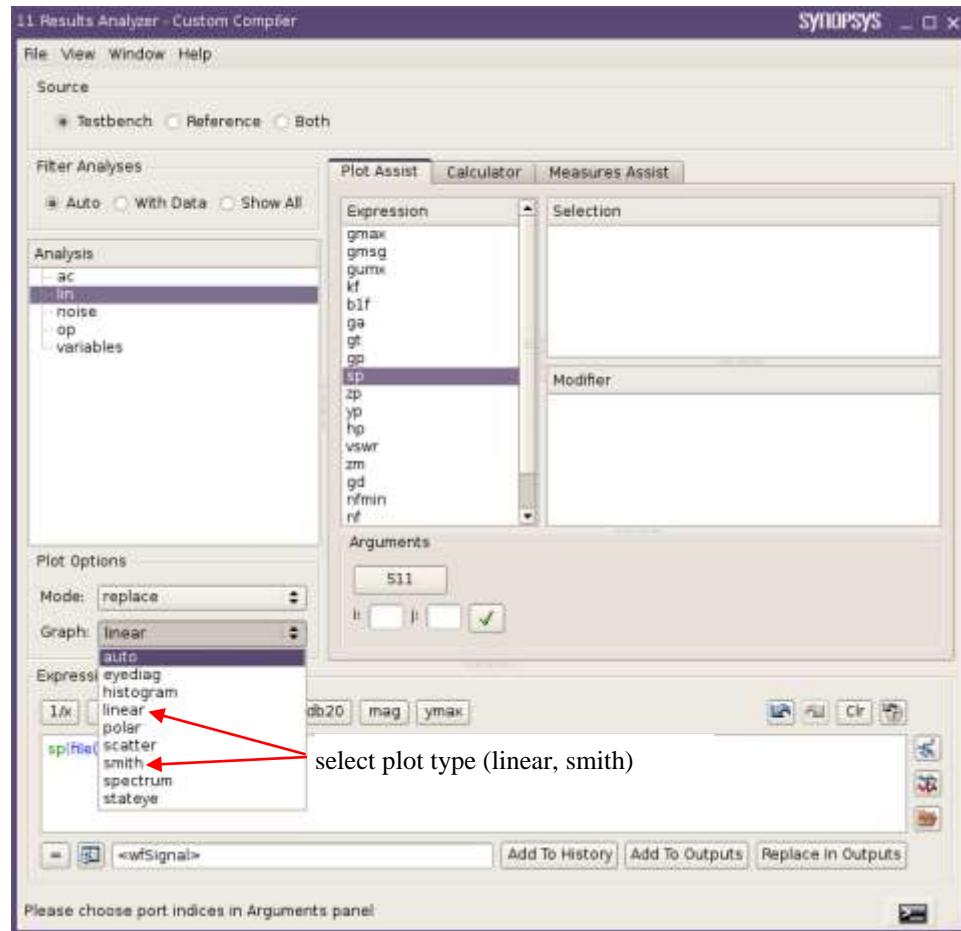
- 290.** Clear the annotation results using **Results → Annotate → Clear Annotations**.

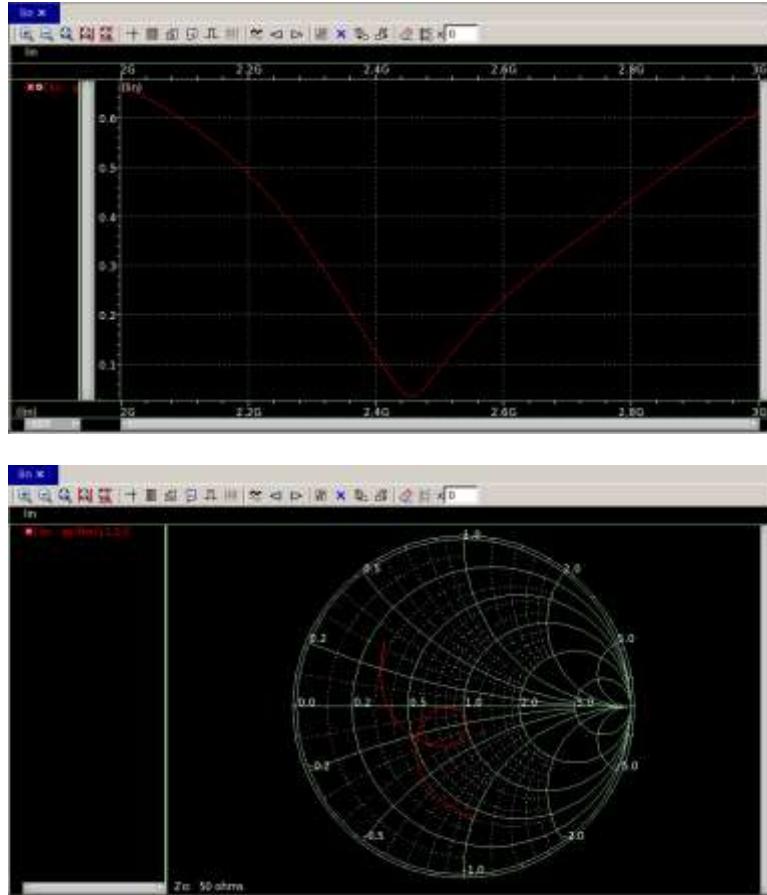
Lab 3

Task 72. Plotting Waveforms in Custom WaveView

After the simulation, the next step is to view and analyze the results in the waveform viewer.

291. Invoke Results Analyzer from SAE→Results→Analyzer.
292. First, let's look at the LIN analysis results. Go to analysis lin→sp, choose Linear (or Smith) from Graph dropdown menu, and then click S11 button, the S11 chart is shown below

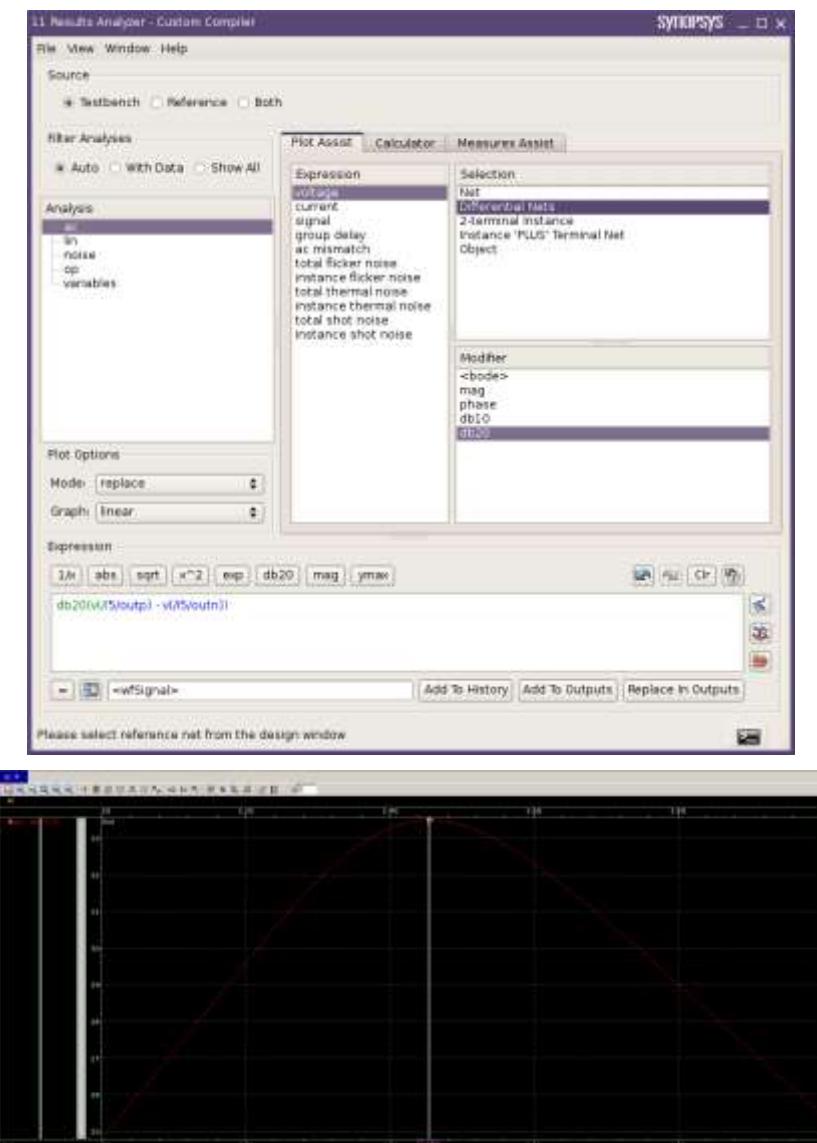




For wireless receivers, the antenna has a 50Ω impedance. To transmit maximum power from antenna to the receiver, matching the input impedance is essential. Smith Chart allows to analyse the passband (2.4-2.5GHz) power and tune matching circuits.

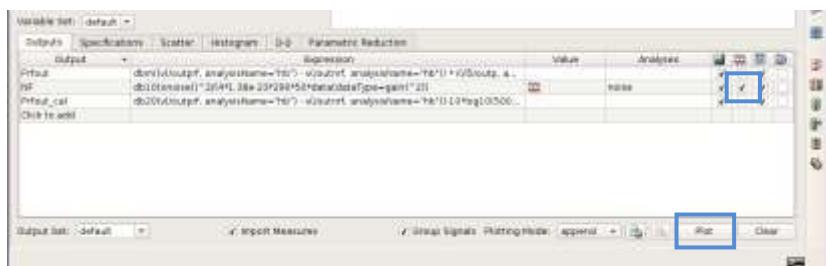
293. Next, we look at the AC gain. In the Results Analyser window select ac → Voltage → Differential Nets to plot AC gain plot. Use dB20 modifier for voltage, and probe the differential outputs in the LNS schematic design. This.

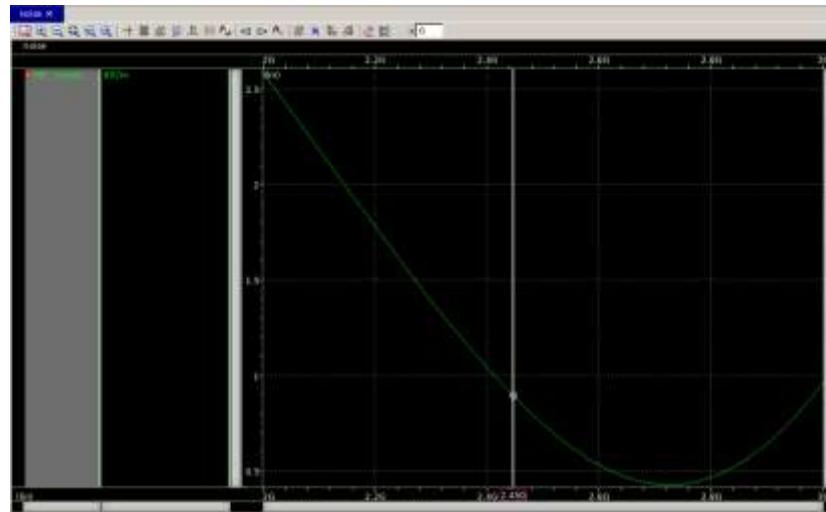
Lab 3



As you can see, the LNA has a gain of 33.5dB and the output LC tank tuned the circuit to the passband 2.4-2.5GHz

294. Now let us plot noise analysys results. For noise, we create an expression for noise figure in RA expression window and save in SAE Outputs table. In SAE Outputs table select the NF expression and click the Plot button ans shown in the pictures below.

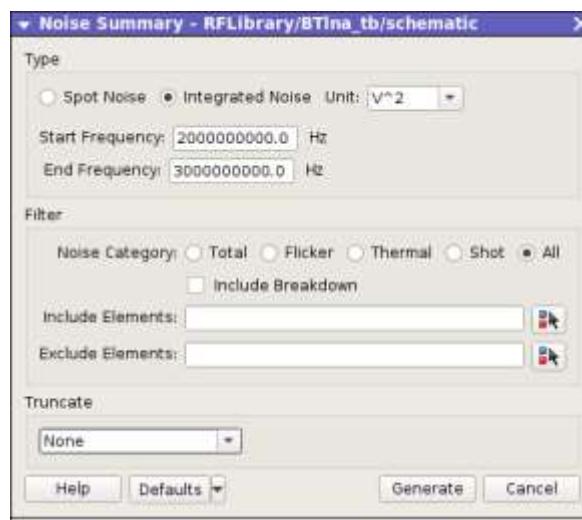




Task 73. Printing Noise Summary Report

In this task, you will print out the Noise Summary Report to further debug the circuit.

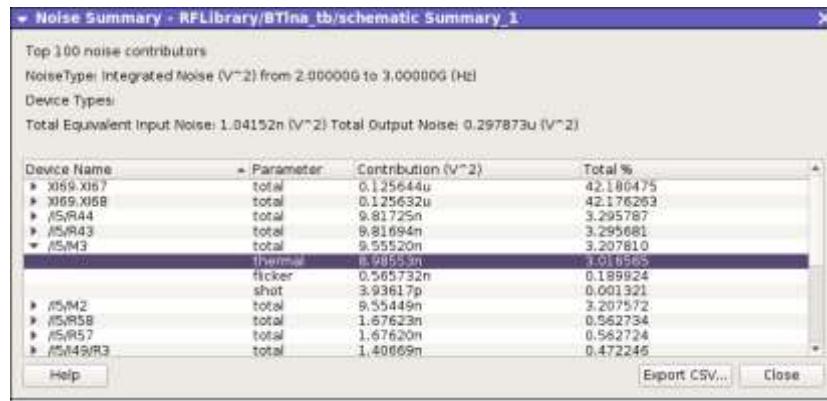
- 295.** From the SAE window, print the Noise Summary Report using **Results → Print → Noise Summary**. This will lunch **Noise Summary** dialog. Chose the following setting ins the dialog and click **Generate** button
- Type: **Integrated Noise**
 - Unit: **V^2**
 - Start Frequency: **2GHz**
 - End Frequency: **3GHz**
 - Noise category: **All**



The resulting report is generating. A list of all the devices noise contribution is sorted according to their ranking. Click on one of the transistors and expand the list of noise

Lab 3

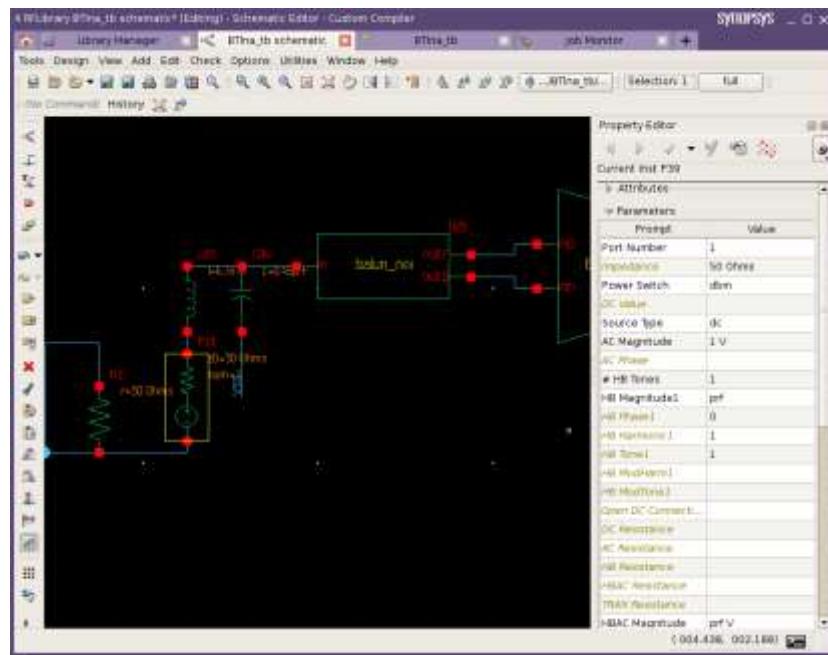
contribution from this transistor. It is also grouped by the types of the noise (thermal, shot, flicker, etc.).



Task 74. Large signal non-linear simulations

In this task, you will learn how to set up large signal non-linear simulations, and learn to find 1dB compression, IP2/IP3, etc. viewer.

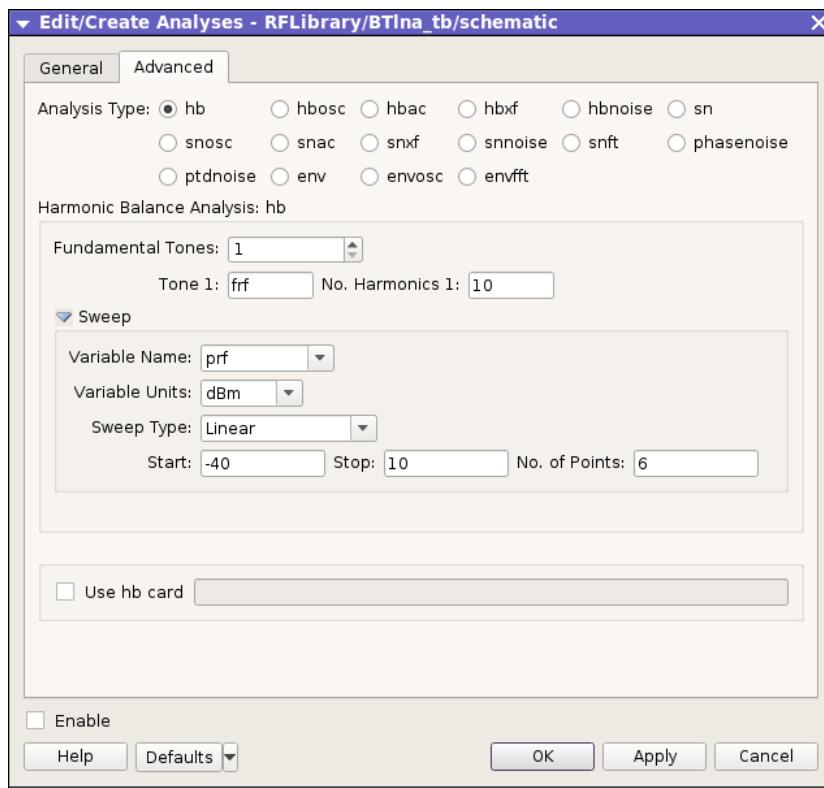
- 296.** Now we will perform single-tone HB analysis to find 1dB compression. In *BTlna_tb* schematic, bring out the Property Editor, select the P39 power switch and check its following properties and save the design:
- Change Power Switch to "dbm"
 - Set # HB Tones to "1"
 - Set HB Magenitude1 to "prf"
 - Set HB Phase1 to 0
 - HB Harmonic1 to 1
 - HB Tone 1 to 1



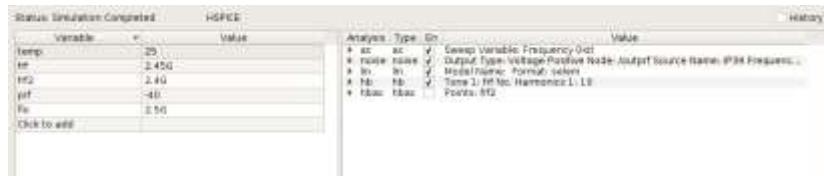
297. Go to SAE window, select **Setup** → **Analyses**, select the **Advanced** tab, choose **hb** setup form and set the following setting and check **Enable** switch as shown in the picture below:

- Set Fundamental Tones:1
- Tone 1 field: "frf"
- Set No. Harmonics 1: 10
- Expand Sweep and enter Variable Name: "prf"
- Select Variable Units: dBm
- Sweep Type: Linear
- Start: -40, Stop: 10, No of Points: 6

Lab 3

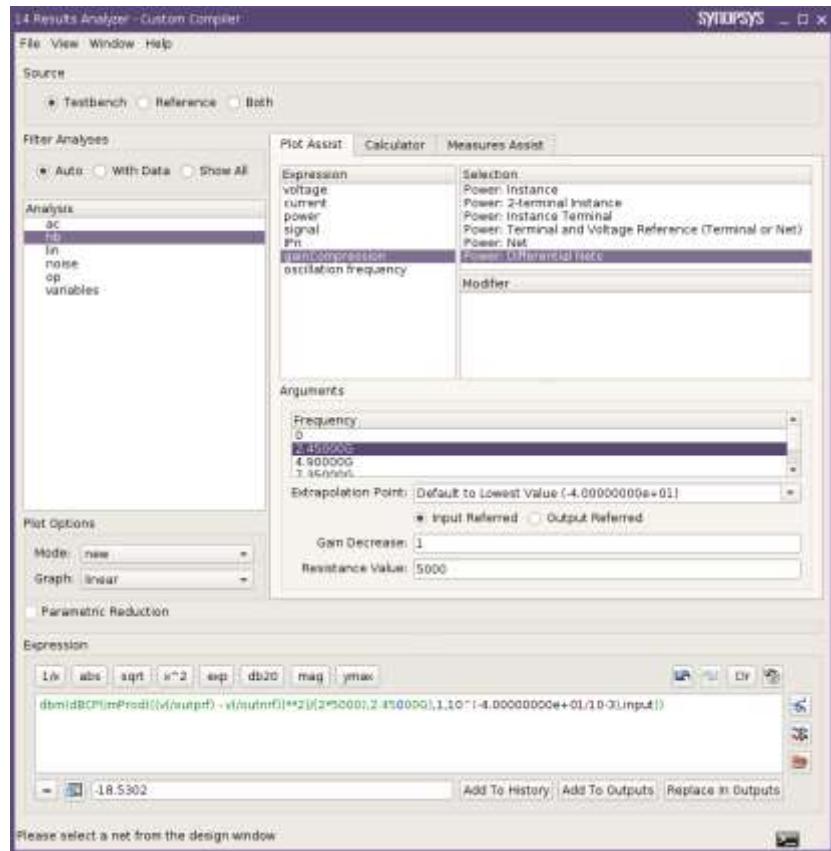


298. In the SAE Variable window check to make sure $frf=2.45G$, $prf=-40$, enable the **hb** analysis and run **Simulation→Netlist and Simulate**.

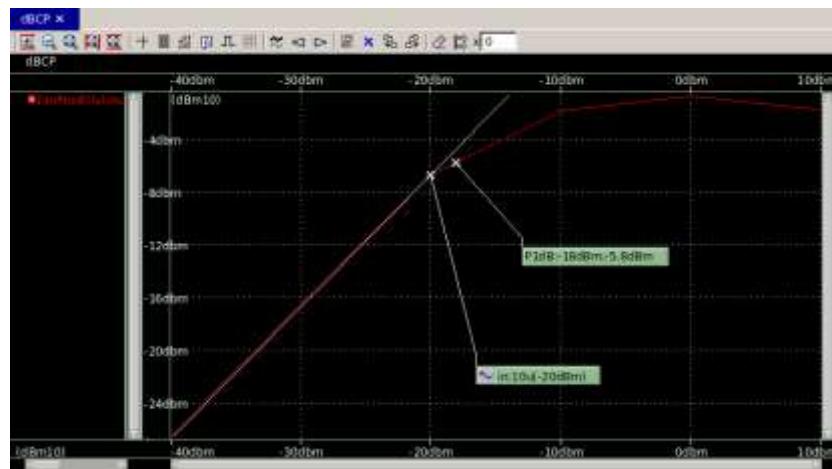


299. After simulation is finished, open the Results Analyzer.

- a. Choose **hb** in Analysis pane
- b. Select **gainCompression** in Expression Window
- c. Select **2.45G** in Frequency
- d. Extrapolation Point = **-40**
- e. Select **Input Referred**
- f. Enter 1 for Gain Decrease
- g. Enter 5000 as the Resistance Value.
- h. Double click Power: Differential Nets to choose BTlna_wp instance outputs (outp and outn)



300. In opened waveform the input 1dB compression point is calculated as $P_{1dB}=-18.5dBm$.



Close the Custom WaveView window using **File → Exit**.

Lab 3

Task 75. Two-tone HB analysis

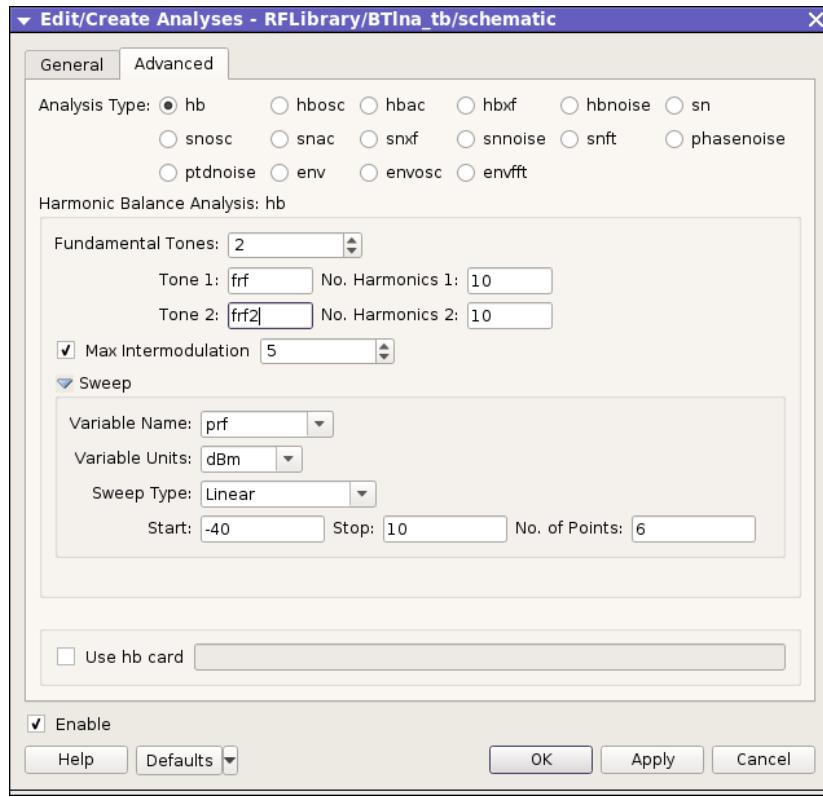
In this task, you will learn how to perform two-tone HB analysis to find IP3.

301. Open *BTlna_tb* schematic, bring out the Property Editor and select P39 port element. In Property Editor set the following properties

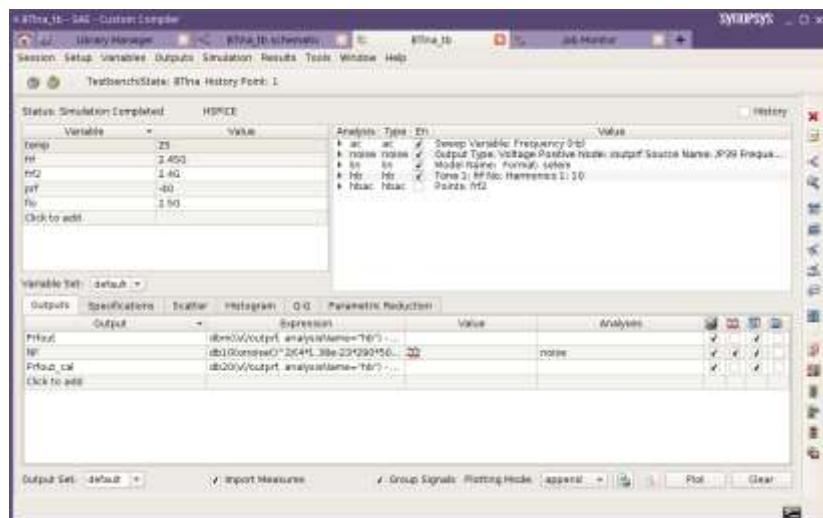
- a. # HB Tones: 2
- b. HB Magenitude2 to prf
- c. HB Pahse2: 0
- d. HB Harmonic2: 1
- e. HB Tone 1: 1
- f. HB Tone 2: 2



302. Go to SAE window, select **Setup**→**Analyses**, select the Advanced tab; Choose **hb** setup form.
303. In the open dialog set the following **hb** analysis settings as shown in the picture below:
- a. Fundamental Tones: 2
 - b. In Tone 2 field enter frf2
 - c. Keep the rest the same

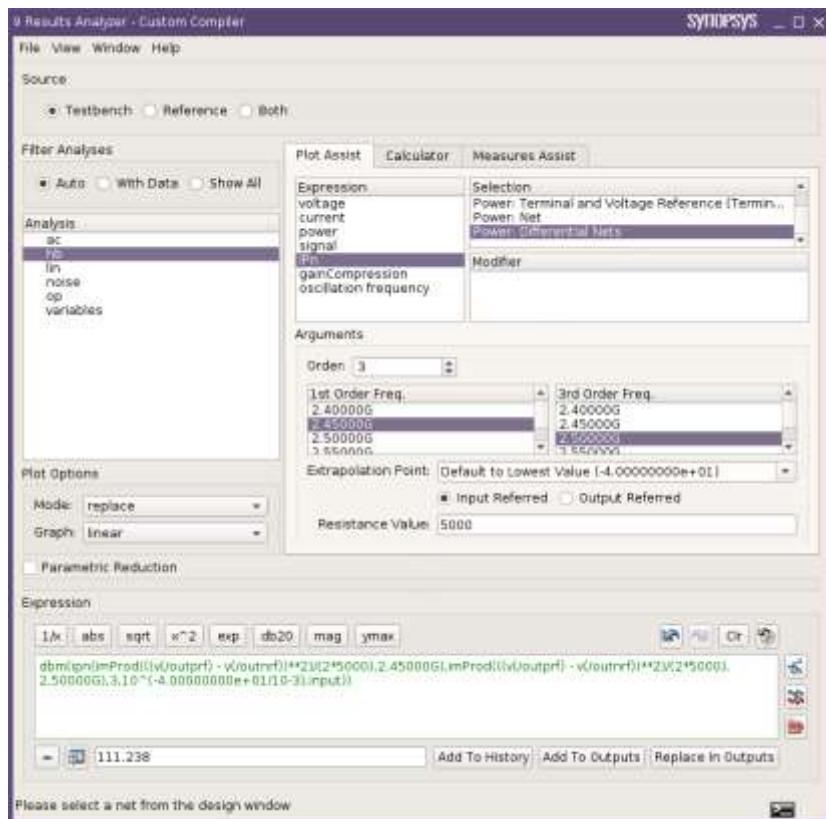


304. In the **Edit/Create Analyses** dialog click **OK** button to save the setting and close the dialog.
305. In the SAE Variable window check to make sure $\text{frf}=2.45\text{G}$, $\text{frf2}=2.4\text{G}$, $\text{prf}=-40$, all required analyses are enabled, as shown in the picture below, and start simulation with **Simulation**→**Netlist and Simulate**.

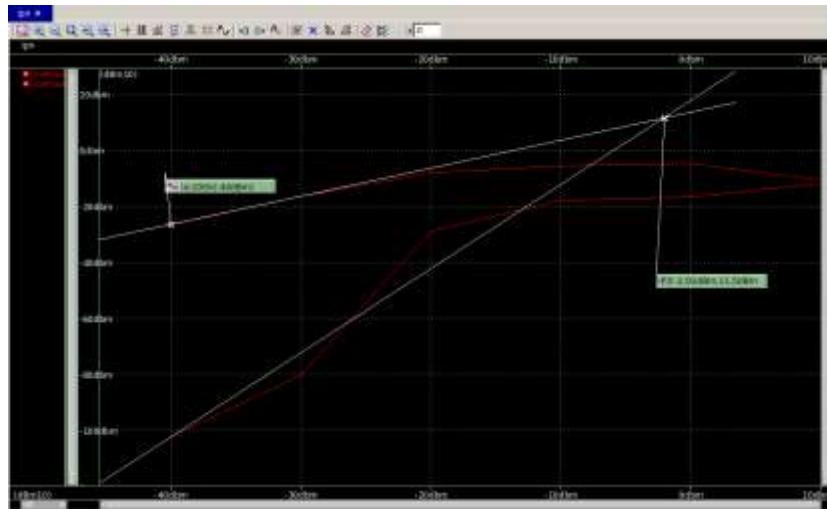


Lab 3

306. After simulation is finished, open the Results Analyzer dialog by **Results → Analyzer**. In **Results Analyzer** dialog select the following measurement settings:



- a. Analysis: hb
- b. Expression: IPn
- c. Order: 3
- d. In 1st Order Freq: 2.45G
- e. Choose 2.5G in 3rd Order Freq
- f. Extrapolation Point: -40.
- g. Select **Input Referred**
- h. **Resistance Value: 5000**
- i. Double click on Power: Differential Nets to choose the BTlna_wp instance outputs (outp and outn). This lunches Custom WaveView with input-referred IP3 calculation results

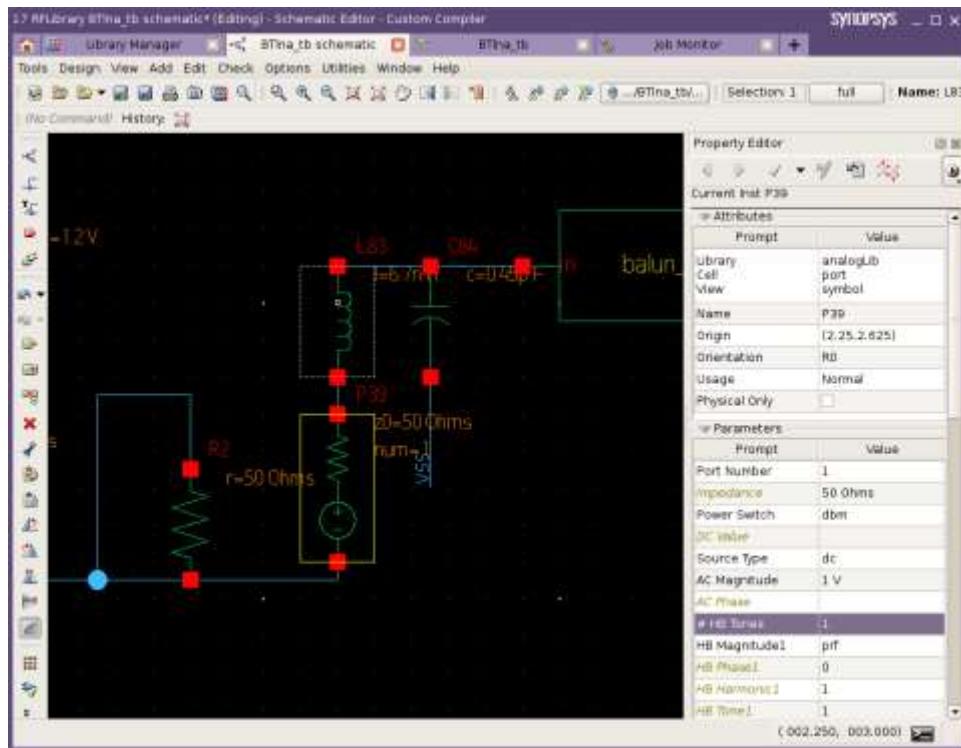


Task 76. Single-Ton HB/HBAC Analysis

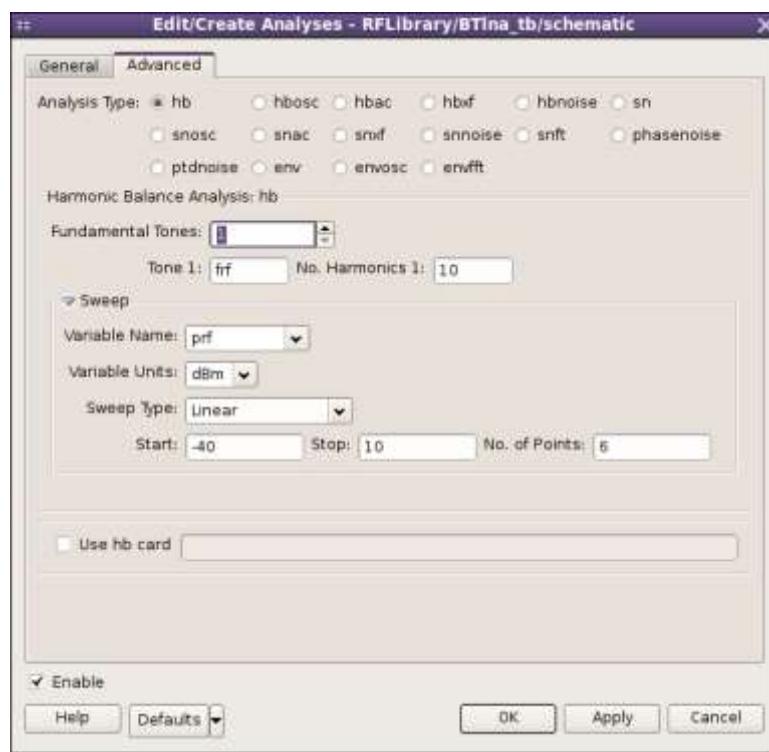
IP2/IP3 can be also obtained by a combination of a single-tone HB analysis with a HBAC analysis. In this case, a single tone large signal compressed the circuit into non-linear behavior and it can be characterized by a small signal analysis performed by HBAC. It requires significantly less computation time than multi-tone HB analysis with complicated or post-layout circuits.

307. Go to *BTlna_tb* schematic, bring out the Property Editor. In the schematic select P39 port element and set its # **HB Tones** property to 1. in Property Editor

Lab 3

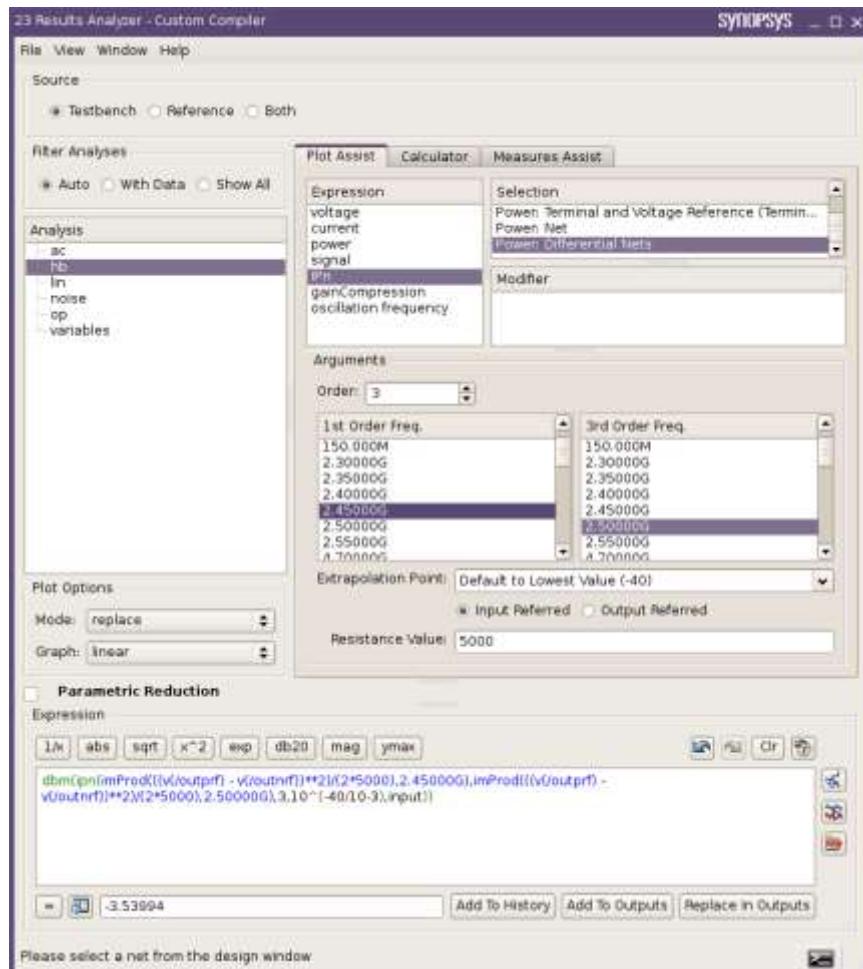


308. Launch SAE Edit/Create Analyses dialog with double-click the **hb** analysis in SAE Window Analysis table. Choose Fundamental Tones back to 1 and click OK button.



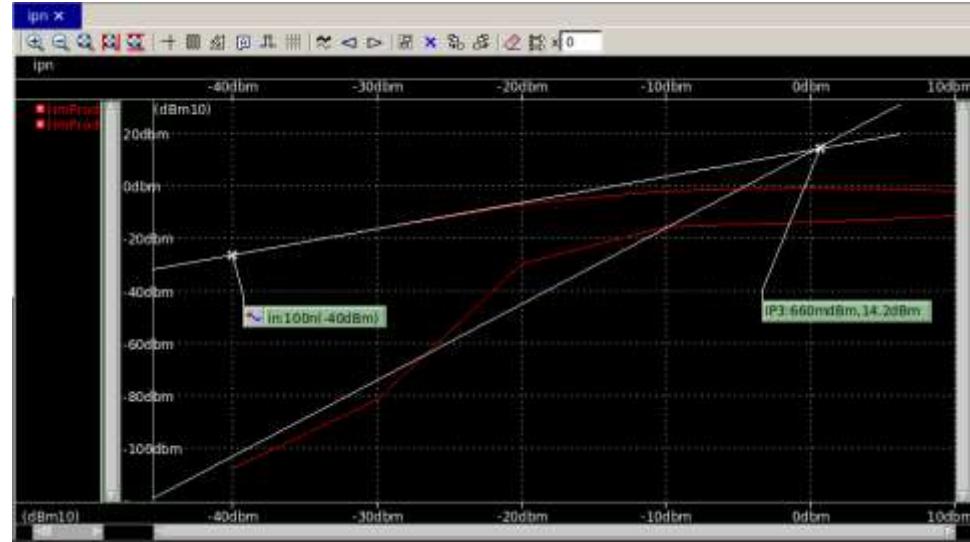
309. Start simulation with Simulation→Netlist and Simulate.

When the simulation is finished, open the Results Analyzer. As in **Task 11**, select the following measurement settings:



- Analysis: hb
- Expression: IPn
- Order: 3
- In 1st Order Freq: 2.45G
- Choose 2.5G in 3rd Order Freq
- Extrapolation Point: -40.**
- Select **Input Referred**
- Resistance Value: 5000**
- Double click on Power: Differential Nets to choose the BTlna_wp instance outputs (outp and outn). This lunches Custom WaveView with input-referred IP3 calculation results

Lab 3



Congratulations!

You have successfully verified the *BTlna_tb* design in the Simulation and Analysis Environment using HSPICE HF!

7

VCS-AMS Simulation Setup

Learning Objectives

The main goal of this lab is to use the Simulation and Analysis Environment in Custom Compiler to netlist and simulate your mixed-signal design using VCS-AMS and post-process the results using Custom WaveView.

After completing this lab, you should be able to:

- Launch the Simulation and Analysis Environment
- Set up the non-simulator specific settings
- Set up the simulator specific settings
- Netlist the mixed-signal design
- Simulate the design using both batch and GUI modes
- View waveforms using Custom WaveView

Lab Duration:
45 minutes

Introduction

During this lab, you will generate netlist and simulate the *wrapper* mixed-signal design test bench using VCS-AMS and verify the results in the waveform tool – Custom WaveView.

In this lab, you are provided with the *sram*, *Bist* and *MixedSimulation* OpenAccess database libraries and a *lib.defs* file. The *sram* library contains the schematic design of memory cell, *Bist* library contains the synthesized verilog netlist of memory Built-In Self-Test (BIST) module, *MixedSimulation* library contains the top level test-bench of mixed-signal design which will be simulated. The *lib.defs* is the default library definition file that contains library name mapping to the physical location of the libraries.

Please refer to the *Simulation and Environment User Guide* for the commands that are used in this lab.

Design Specifications

Embedded memories often represent a die's largest contributor to yield loss, because of very large area and density of these regular circuits. A successful memory test strategy must be used to assure the memory correct functionality in the chip. In the great majority of cases, embedded memories today are tested with Built-In Self-Test (BIST). BIST is techniques of designing additional digital hardware into integrated circuits to allow them to perform self-testing. This makes the electrical testing of a chip easier, faster, more efficient, and less costly. BIST consists of an on-chip engine, placed next to each embedded memory which writes algorithmically generated patterns to the memory and then reads these patterns back to discover defects.

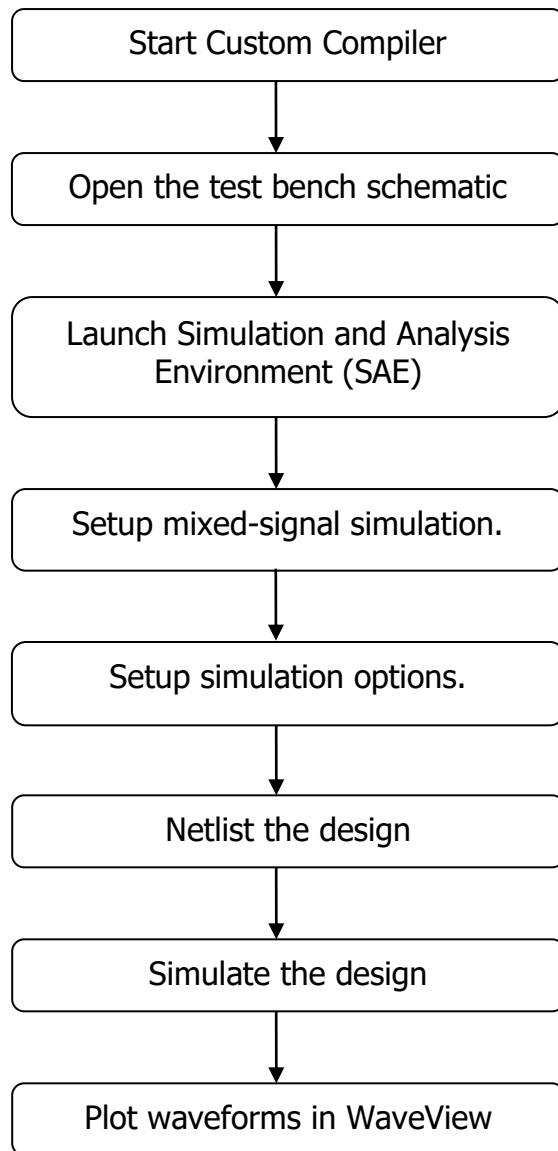
The main drawbacks of designing such type of mixed signal circuitries is the BIST module is digital circuit, and memory, which it will test, is analog circuit. While in separate, digital, and analog can work correctly but together they will not always work. This brings to drastically increase in design and verification time of such architectures.

Prior to running a mixed-signal simulation, designers have to design each module separately, test each of the digital and analog blocks, and run their pure digital and analog flows. Only after that they could run mixed-signal simulations to be sure that mixed-signal architecture is working. And if the simulation fails, they have to run the full flow again.

In this lab the memory circuit and its BIST engine will be simulated in the design phase, the simulation waves will be debugged by WaveView tool.

Flow Overview

Lab 1 Tasks



File Locations

All files for this lab are located in the directory *SAE_VCS_AMS_Lab1*.

Directory Structure

SAE_VCS_AMS_Lab1	Current working directory
sram	OpenAccess memory design library
Bist	Imported BIST module OpenAccess library
MixedSimulation	OpenAccess library where the top level mixed signal design is located, with its test-bench.
lib.defs	Library Definitions file

Relevant Files

bist_engine.sdf	File containing timing info
rmapAD.init	Resistance map file which will be used during the co-simulation

Answers & Solutions

There is an *ANSWERS / SOLUTIONS* section at the end of this lab. You are **encouraged** to refer to this section often to verify your answers, or to obtain help with the execution of some steps.

Tool Versions

CustomSim	O-2018.09
VCS-MX	O-2018.09
Custom WaveView	O-2018.09
Verdi	N-2017.12-SP1 or later

Instructions

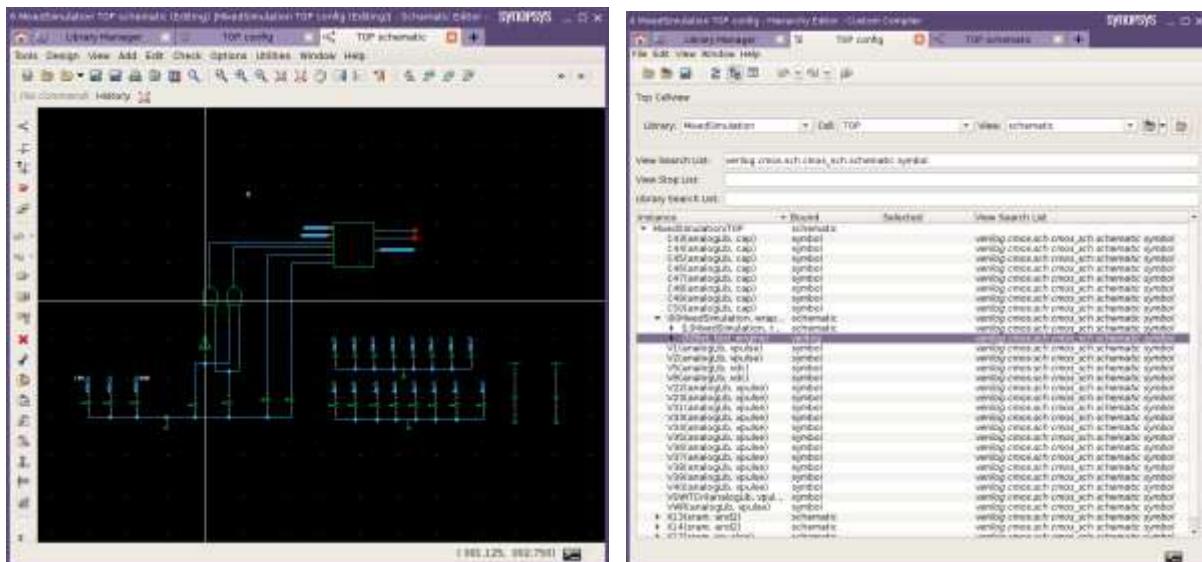
Task 77. Start Custom Compiler

310. In the UNIX terminal window change your current working directory to `SAE_VCS_AMS_Lab1`. This will be your working directory for this lab.
311. Start Custom Compiler from the UNIX prompt.

```
custom_compiler &
```

Task 78. Open the Test Bench Circuit

312. From library manager select config view of *TOP* cell from *MixedSimulation* library open *Design and Config*.
313. In Hierarchy Editor window expand I0 instance tree and make sure that instance *I3(Bist, bist_engine)* is bound to its *verilog* view, as it is shown in the image:



Note:

Memory and BIST engine top level testbench *TOP* cellView will be opened in a Schematic Editor, window together with hierarchy editor.

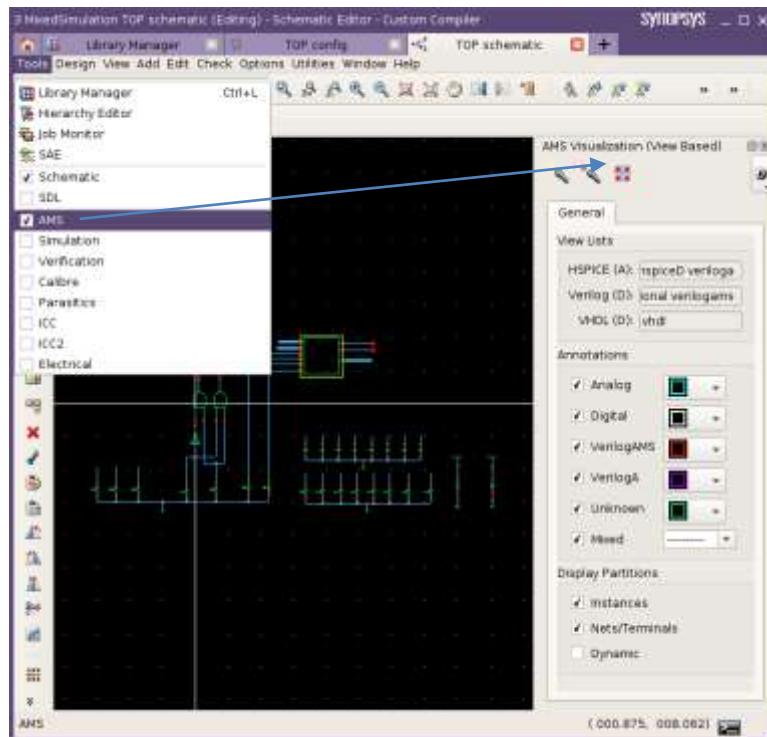
Note:

Using Hierarchy Editor, user can control the whole hierarchy of the mixed design, choose each instance switched master. For more information about working with Hierarchy Editor please refer to Custom Compiler **Hierarchy Configuration** training.

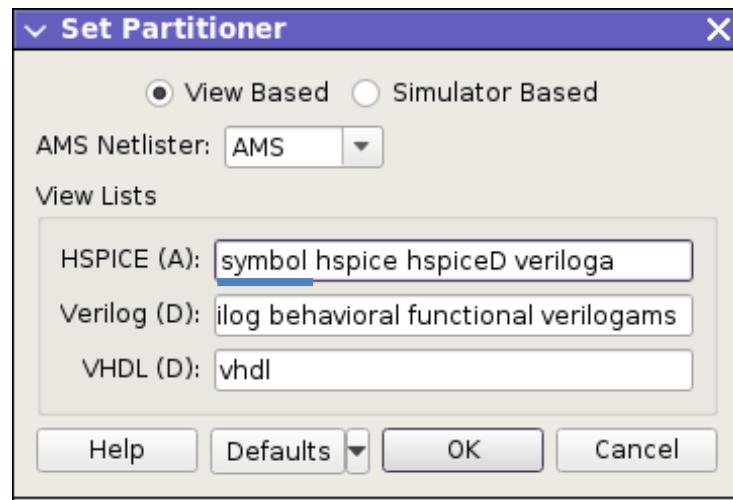
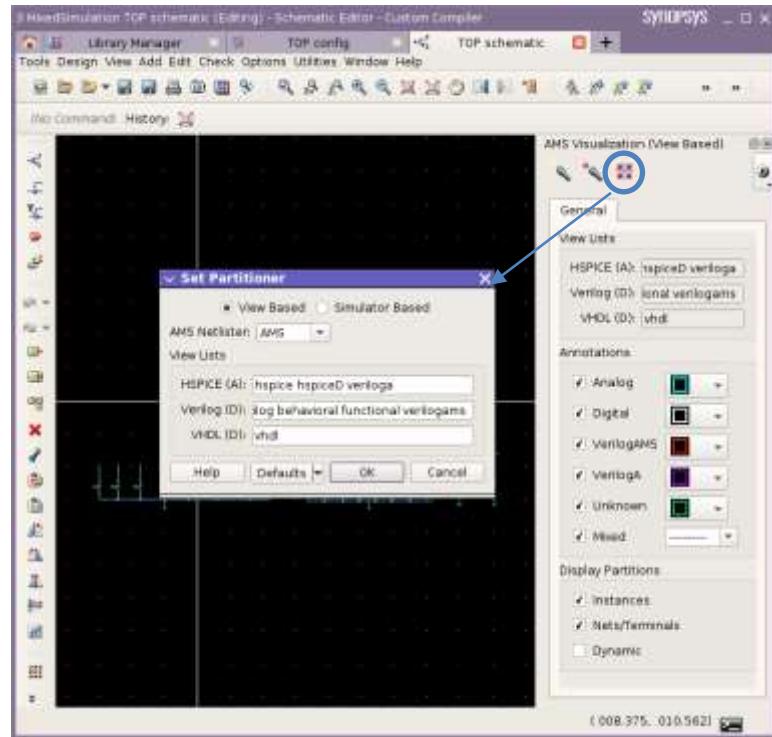
Task 79. Visualize AMS Partitioning

In this task you will use visualize partitioning mechanism in Custom Compiler, for visualization of mixed design digital and analog parts. The visualization mechanism allows to control AMS netlister bindings, different domains colorings.

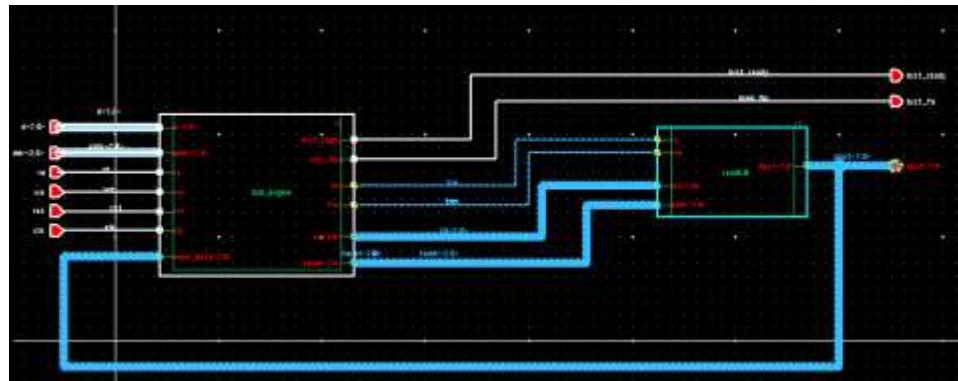
314. From Schematic editor window open AMS Visualization Assistant window by choosing **Tools → AMS**



315. In the opened assistant window user can control the View search list of AMS netlister, choose the colorings of various domains.
316. Click on to open "Set Partitioner" dialog. In This dialog add *symbol* view name in *HSPICE View List*. This will tell the Custom Compiler to treat *symbol* views as analog blocks.



317. Click **OK** to apply the settings and close the dialog.
318. After closing the dialog pay attention that in Schematic Editor blocks coloring was added showing each domain in its color. Descend into *wrapper (I0)* instance. It should look like as the image below



Here user can clearly see which block is digital, which is analog and which is mixed domain block.

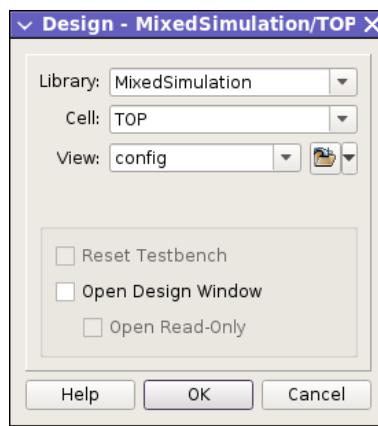
319. Now hide the AMS partitioning through the lab by pressing "**Hide partition visualization**" . This makes schematic design clean to easily find probes and wire names.



Task 80. Launching Simulation and Analysis Environment

In this task you will launch Simulation and Analysis Environment (SAE).

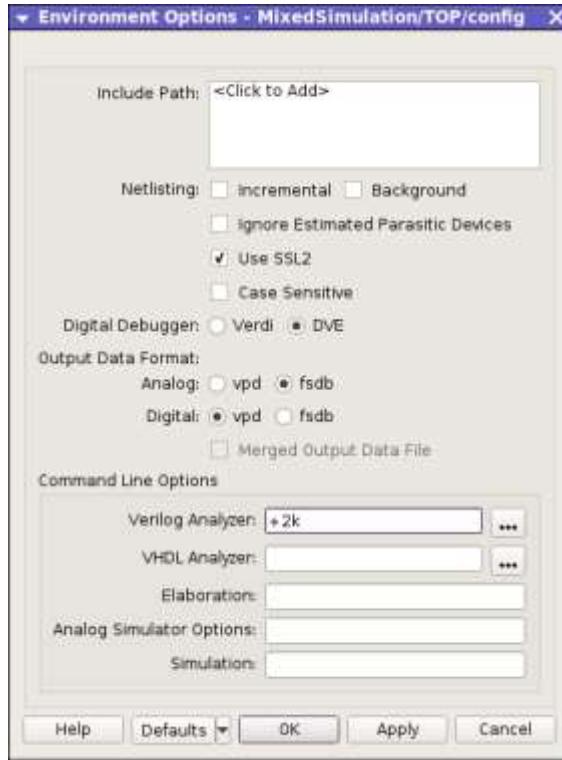
320. Invoke the Simulation and Analysis Environment using **Tools → SAE** from schematic window.
321. In the SAE window set the design to *MixedSimulation/TOP/config* with **Setup→Design**.



Task 81. Setup mixed-signal simulation

In this task, you will set up the mixed-signal simulator, which will run VCS-AMS mixed-signal simulation.

- 322.** From SAE window invoke the Simulation Setup using **Setup → Simulator...** and set the Simulator as **VCS AMS**, set the Results Directory to **./simulation**. Click OK and make sure that new simulation directory is created.
- 323.** Choose **Setup → Environment Options....** Users have the capability to specify compilation, elaboration and simulation related options in that dialog. Specify **v2k** option as Verilog files compilation option, by entering **+v2k** in Verilog Analyzer field.



Question 6. How can users specify VCS compilation, elaboration or simulation options?

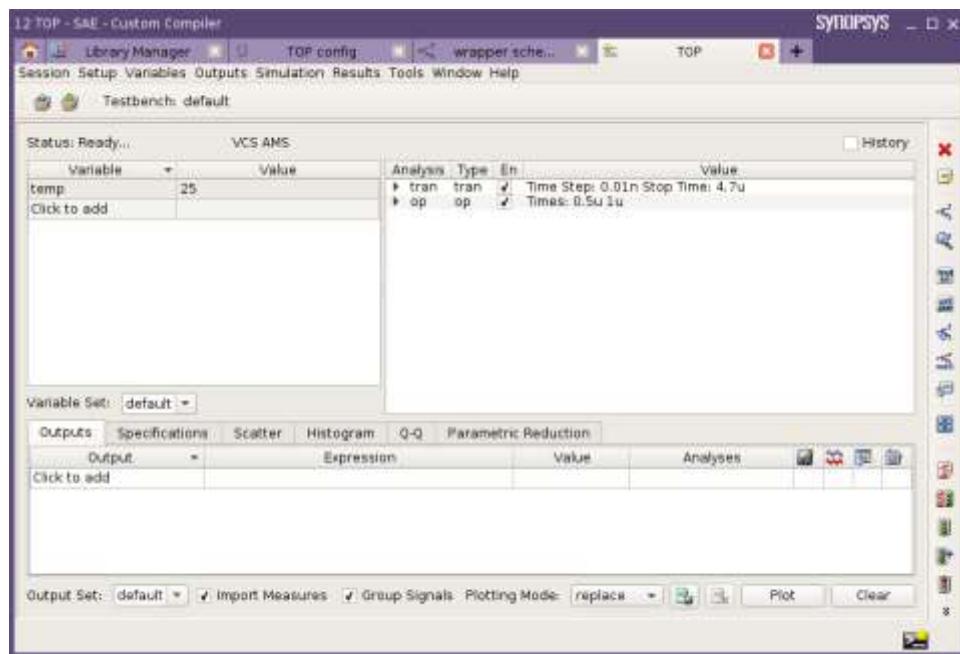
- 324.** Click **OK** to close the dialog.
- 325.** Set the transient analysis *tran* using **Setup → Analyses...** with following settings:
- Time Step:** 0.01n
 - Stop Time:** 4.7u
 - Enable:** True
- 326.** Click **Apply** button to save the setting.
- 327.** Set the operating point analysis *op* with the following setting:
- Times:** 0.5u 1u
 - Enable:** True
- 328.** Click **OK** to apply the settings.

Note: Both analyses will appear on the SAE main window under the Analysis section.

Note: Model files are being set from PDK. However user can also, set/verify the path of the model file by **Setup → Model Files....** Following model file should be specified

```
<path to Labs directory>/PDK/hspice/reference40_models.lib TT
```

329. SAE window should look like as shown in the image



Task 82. Setup digital timing (SDF) files

In this task you will specify the SDF back-annotation file to be used during simulation. The Standard Delay Format (SDF) is an IEEE standard for the representation and interpretation of timing data for use at any stage of an electronic design process. It has usually two sections: one for interconnect delays and the other for cell delays.

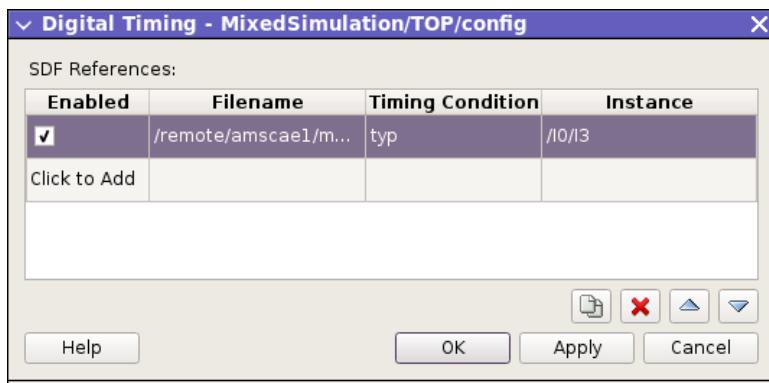
330. From SAE window set up the path of the digital timing file/s using **Setup → Digital Timing...** dialog to next file:

```
./bist_engine.sdf
```

There are three conditions in **Timing Condition** field that user can choose: typical, minimal and maximal. Specify that field as *typ*, and select the *bist_engine* (/I0/I3) instance as **LCV**.

Note: This dialog allows specifying the SDF files, which contain timing info of the scheme, and use the timing data of those files during simulation.

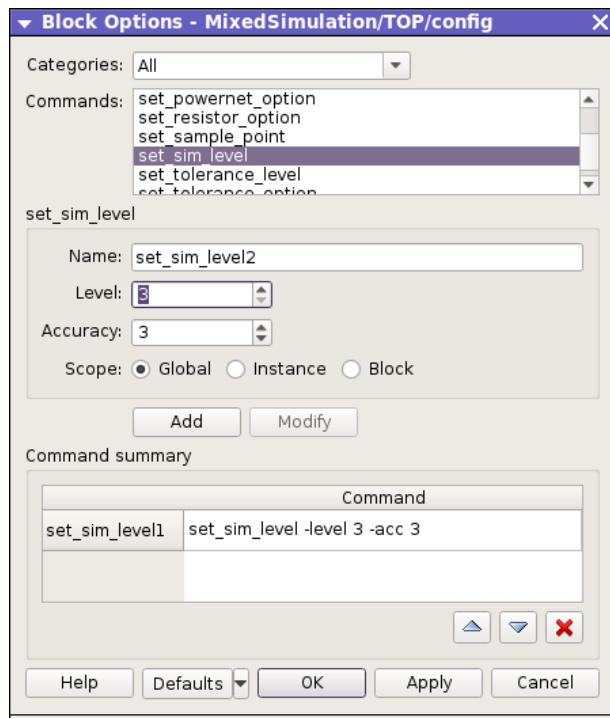
Fill the fields of that dialog as shown in the below screenshot and click **OK** button:



Task 83. Setup simulation options

In this task, you will setup options to control the mixed-signal simulation. Generally, those options are divided into following parts: options for controlling CustomSim simulator, options for controlling VCS simulator and options for controlling mixed-signal translations.

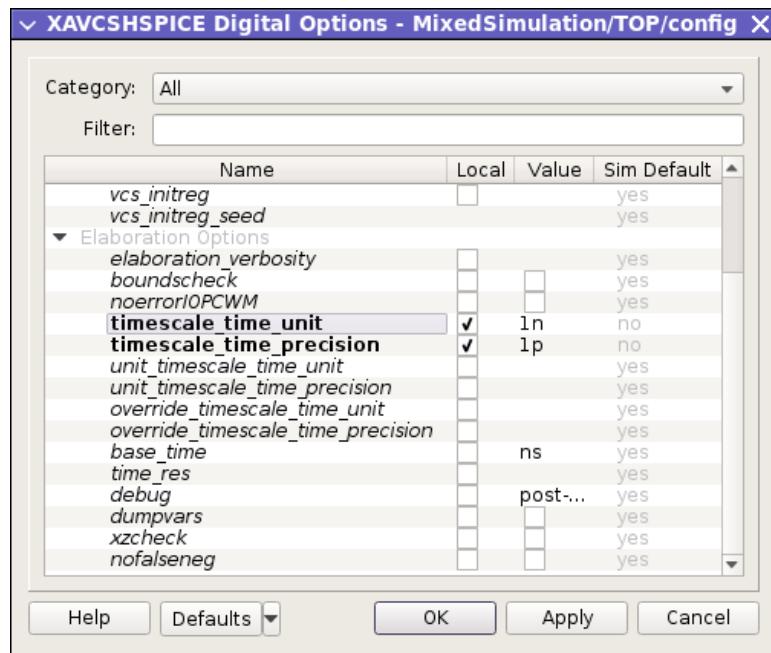
331. From SAE window set the simulation accuracy of CustomSim simulator to 3 by selecting **Simulation → Analog Block Options....** In the opened Block Options window search and select the command `set_sim_level`, specify 3 in the Level field and press Add button to add that command in Command summary field. The screenshot shows how that dialog should look like at this point:



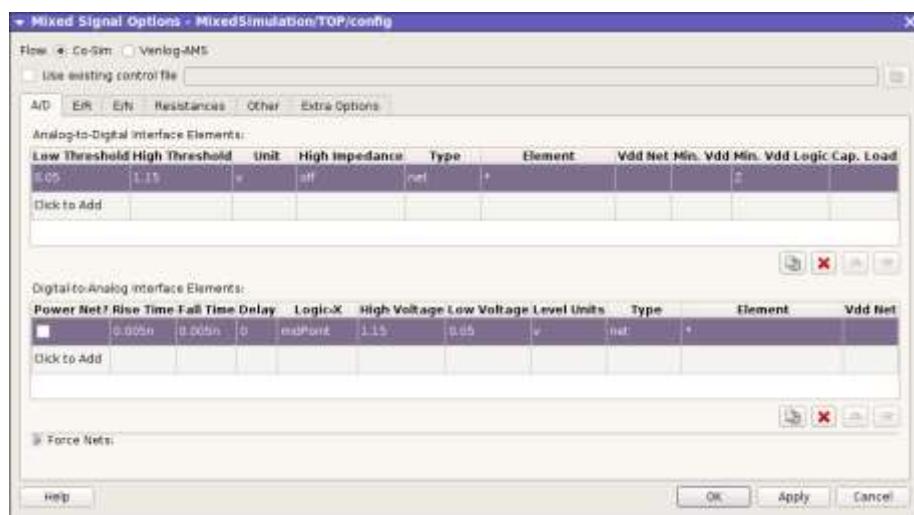
Note: SAE supports some of the CustomSim options in standalone integration in SAE. Those options can be controlled by **Simulation → Analog Global Options** dialog.

332. Click OK to save the settings and close the window.
333. In order to run accurate co-simulation, we need to setup timing options properly. To do that, set the simulation timescale unit as 1ns and precision as 1ps. Select **Simulation → Digital Options**, the **XAVCSHSPICE Digital Options** dialog will be opened. This dialog allows controlling the options that are passed on the command line to VCS and the simulation executable.

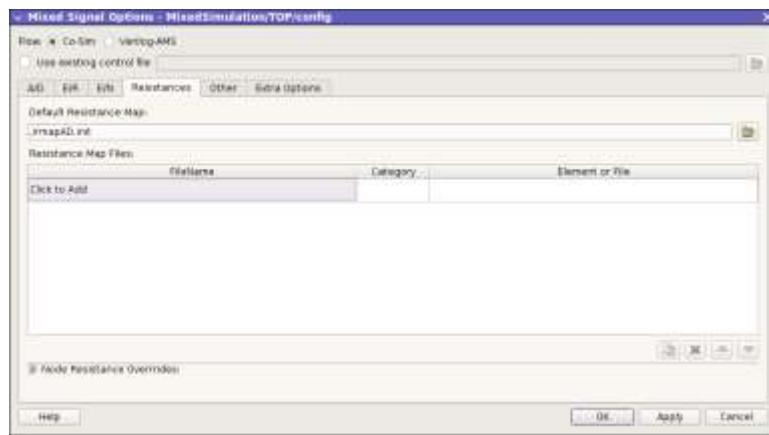
Some modules in the design may have timescale defined for them, or `resetall directive which will reset timescale directive for module after that directive. Specifying *timescale_time_unit* as 1ns and *timescale_time_precision* as 1ps in that window, will add elaboration option –timescale=1ns/1ps in elaborate.cmd, which will be used for all modules. Below screenshot shows how that dialog should look like:



334. Click OK to save the settings and close the **Digital Options** window.
335. Specify mixed-signal options, which control the mechanism of how analog and digital simulators interact. Select **Simulation → Mixed-Signal Options** to open the *Mixed-Signal Options* dialog. Select A/D tab in that dialog, which controls all aspects of the analog to digital and digital to analog interfaces of the Co-SIM simulation. Specify the values of that tab like it is shown in the screenshot



336. Specify resistance map file by choosing the *Resistances* tab of *Mixed-Signal Options* dialog. The resistance mapping information controls mapping of analog drive resistance ranges to Verilog strengths. Select browse button in *Default Resistance Map* field and choose rmapAD.init file as the default resistance map file which will be used during the co-simulation.



Note: In this dialog user can specify separate resistance map file for each element of the design.

Question 7. What does the *Force Nets* field control in the **Mixed-Signal Options** dialog?

337. Click **OK** to save the settings and close the **Mixed-Signal Options** window.

Task 84. Netlist the Design

The next step in the design cycle is to netlist the test circuit. The generated netlist file is the input for the simulation tools to verify the electrical performance and the functionality of the circuit.

338. Generate the netlist using **Simulation → Netlist → Create (N)**.

Note: It opens up the generated final verilog and hspice netlists in the Custom Compiler Text Viewer window.

339. Close the Custom Compiler Text Viewer by using **File → Close Window**.
340. Choose **Simulation → Launch Terminal**, type **ll** and in the opened terminal observe the files which were generated for running VCS-AMS mixed simulation.
341. Close the terminal window.

Question 8. What files are generated in the **netlist** directory?

Task 85. Simulate the Design

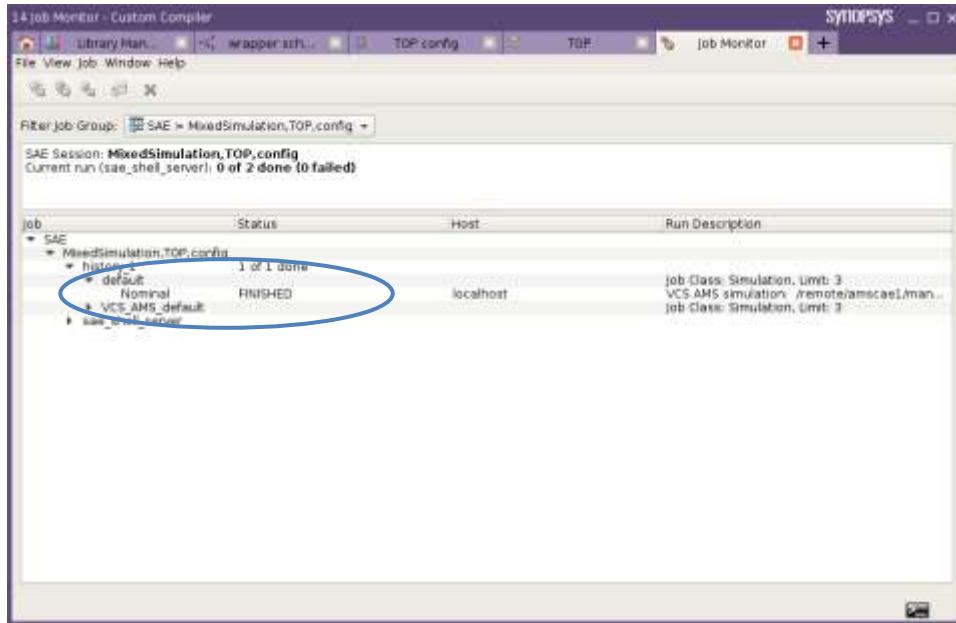
Once all the inputs are defined for the simulator, the next step is to simulate the design. In this task, you will simulate the *TOP* circuit using the XA-VCS mixed simulation.

342. From SAE window start the simulation using **Simulation → Run**

Note: The VCS-AMS mixed signal simulator will be launched in the specified run directory (in this case `./simulation`) and will simulate the design.

Note: By default, it opens up the simulation log in the Custom Compiler Text Viewer window.

343. You can observe the status of simulation on the Job Monitor window as shown in the image.



344. Close the Custom Compiler Text Viewer after finishing of the simulation.

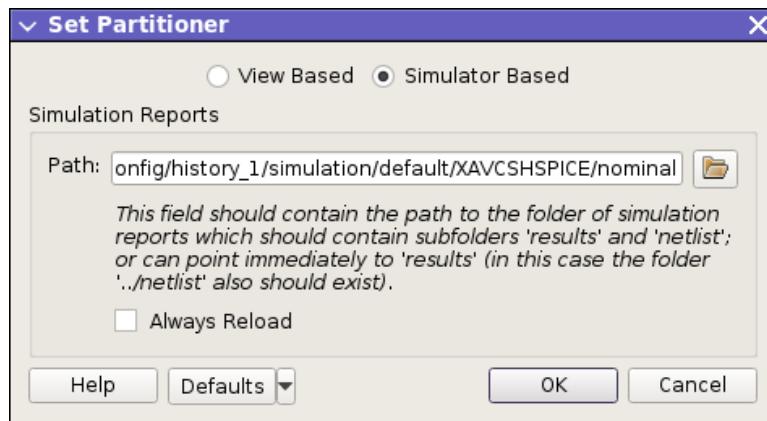
Task 86. Simulation data base partitioning visualization

345. Got to Schematic Editor window where the schematic design (MixedSimulation/wrapper/schematic) is open. In AMS Visualization assistant window Click on

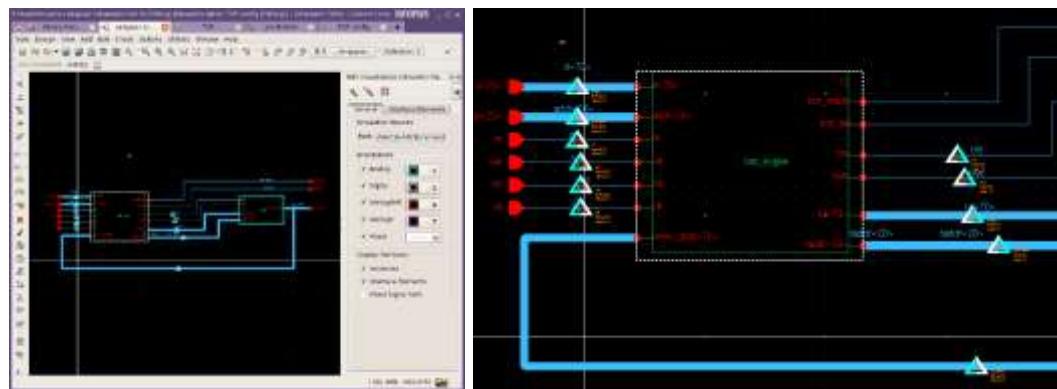


to open "Set Partitioner" dialog. Select **Simulation Based** option in the dialog.

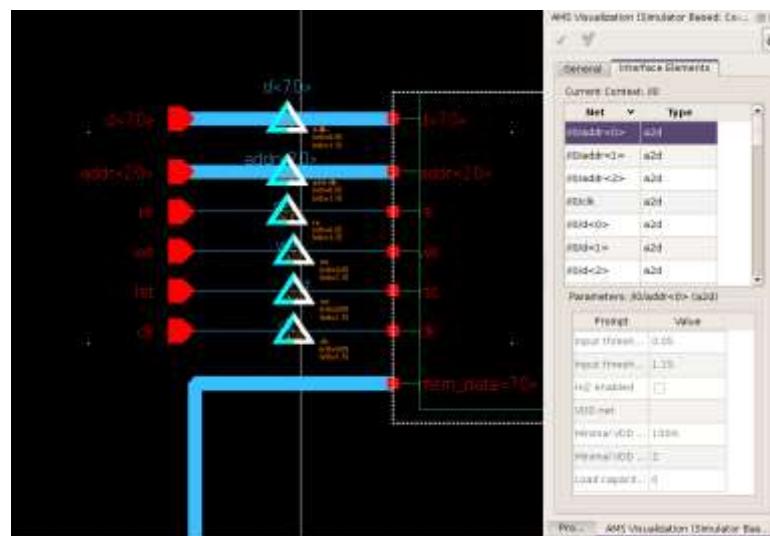
346. Fill the path to simulation results directory and click **OK** button:
`./simulation/MixedSimulation, TOP, config/history_1/simulation/default/XAVCSHS PICE/nominal`



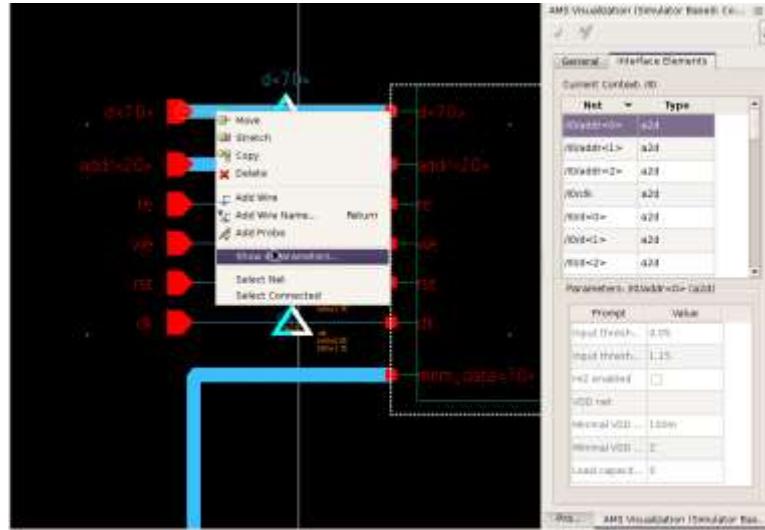
- 347.** Analyze the AMS partitioning visualization in schematic design. Now it also shows data conversion (analog to digital and digital to analog) interface elements based on simulation data.



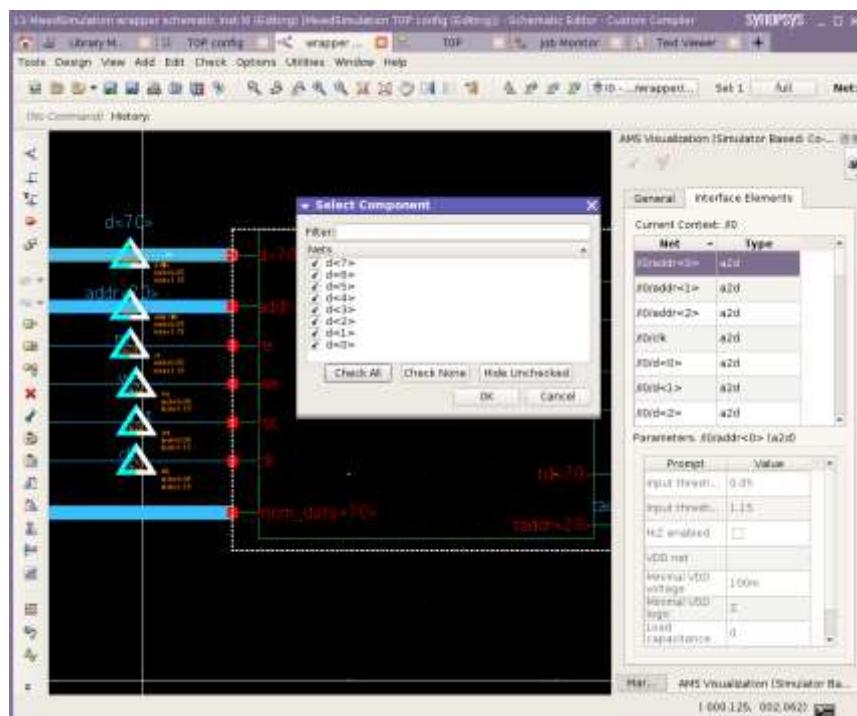
- 348.** Notice that **AMS Visualization** assistant now contains **Interface Elements** tab as shown in the picture below. Open this tab and analyze the generated interface elements in the design. As you can see they are **a2d** and **d2a** conversion elements which are used for signal type conversion between analog and digital domain.



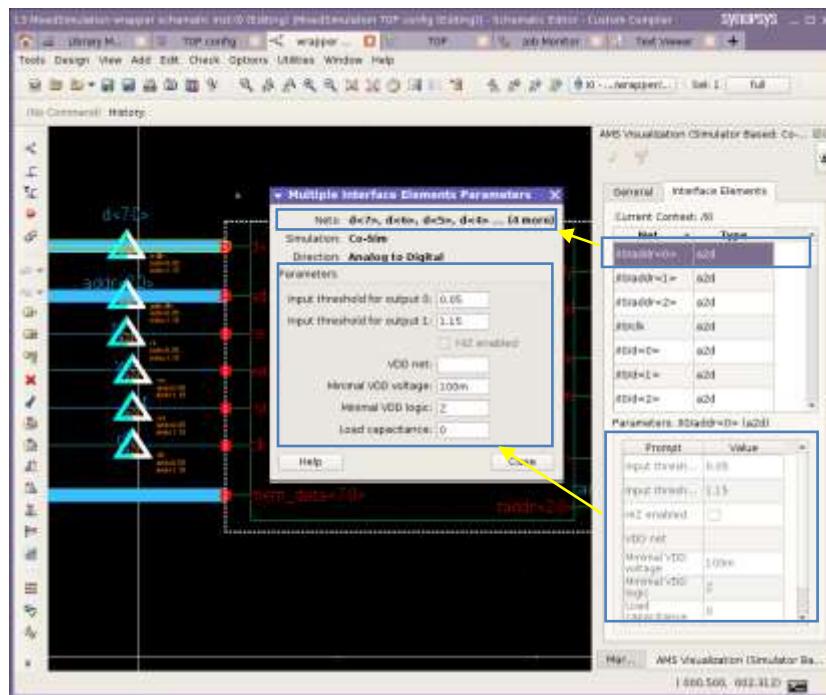
349. Notice that AMS Visualization assistant now contains **Interface Elements** tab as shown in the picture below. Open this tab and analyze the generated interface elements. They contain information which you specified in **Mixed-Signal Options** dialog on simulation setup stage.
350. In the schematic editor selec **d<7:0>** net and launch CSM with mouse right click. Notice that the CSM contains **Show IE Parameters** options. Select it to specify data interface elements on **d<7:0>** nets. This will launch **Select Component** dialog, where you need to choose the interested nets.



351. In the **Select Component** dialog select all bits of **d<7:0>** bus, as shown in the picture below and click **OK**. This will launch **Multiple Interface Elements Parameters** dialog.

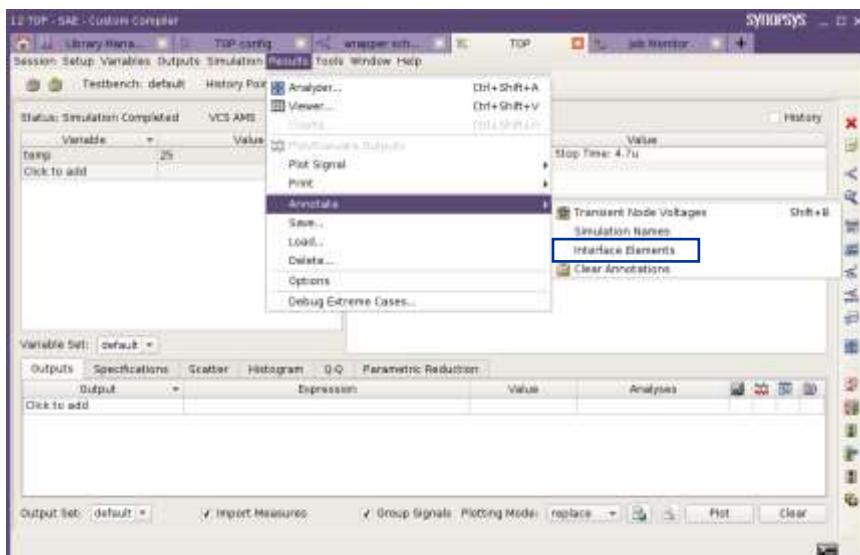


352. In the **Multiple Interface Elements Parameters** dialog you are prompted to analyze interface elements in mixed signal options which you specified during simulation setup in **Mixed Signal Options** dialog .

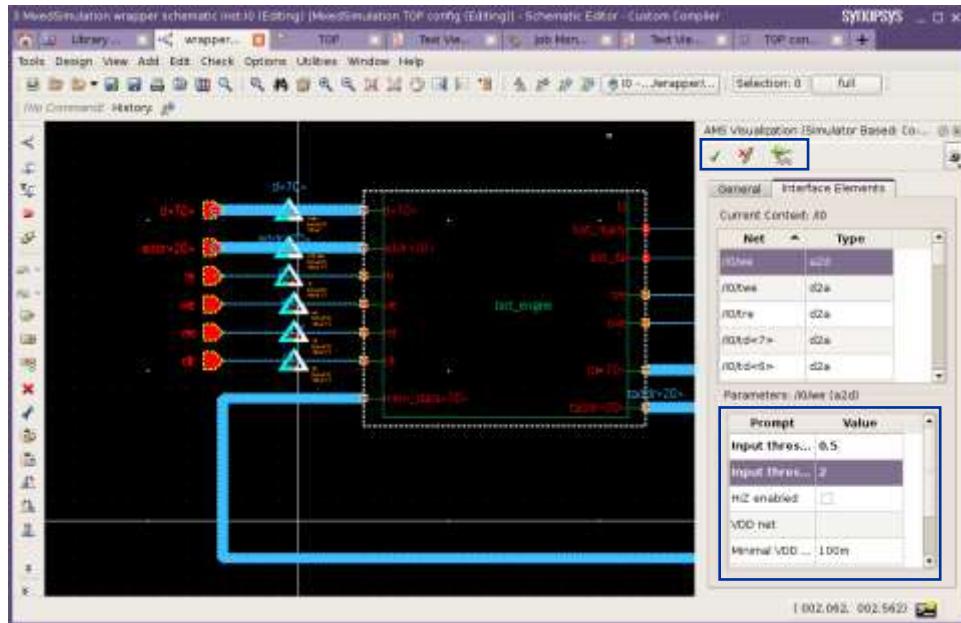


Task 87. Interface elements back annotation

353. When simulation is finished and the results are existing, you can back annotate interface elements into schematic design. This feature depicts simulator generated interface elements on the schematic design. Go to SAE window and perform **Results->Annotate->Interface Elements**



- 354.** In this case the interface elements' properties users can modify. Go to Schematic Editor Window and in AMS Visualization assistant select one of available an listed there interface elements. Notice that now it is possible to change parameters.



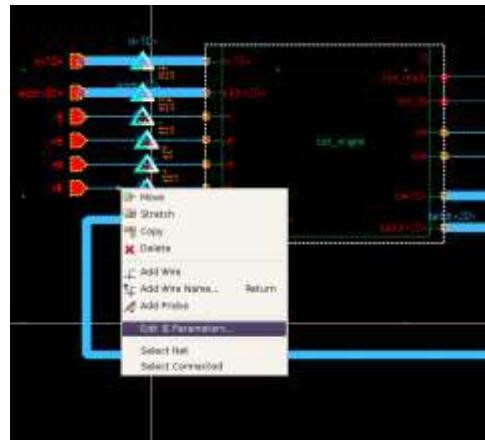
Note:

There are three buttons on the AMS Visualization assistant window which controls interface element parameter editing. When any of parameters is modified, the button submits the changes. The button launches SAE Mixed Signal Options dialog where signal type conversion interface elements are specified. In our case these are analog to digital and digital to analog interface elements.

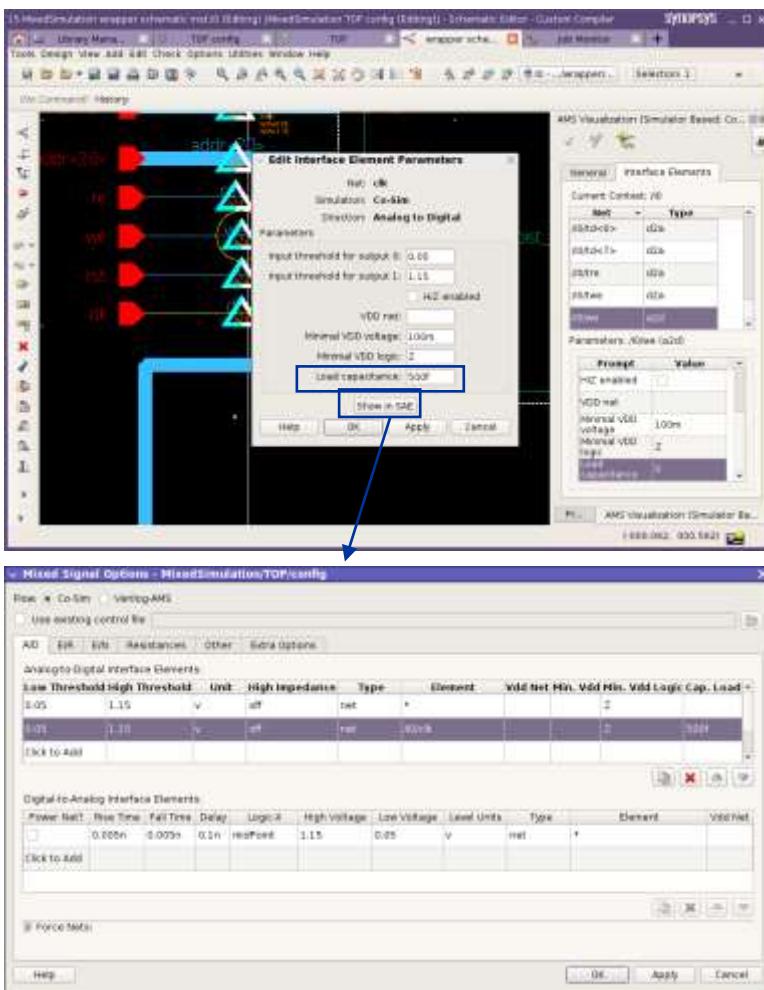
Note:

Be aware that you can launch **Edit Interface Element** dialog from selected net CSM in Schematic Editor Window and modify interface element parameter in design editor window also. On the canvas select the net which has an interface element (for example *clk*), right click on it and in CSM select **Edit IE Parameter**

- 355.** In the design editor select *clk* net and right click on it. IN the CSM select Edit IE Parameters.



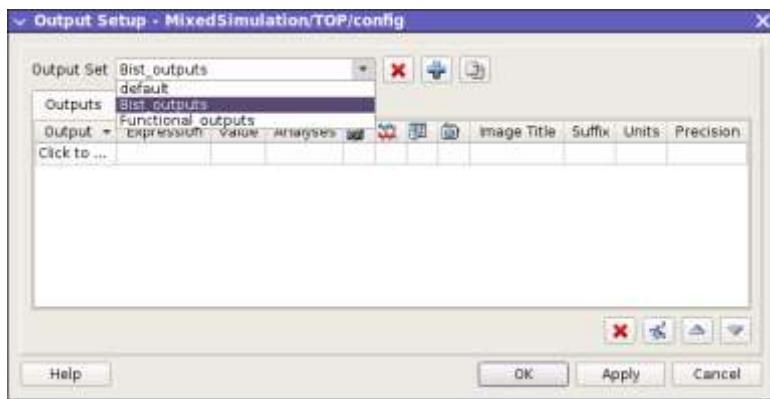
356. In the launched **Edit Interface Element Parameters** dialog, set Load capacitance to 500n. Click Apply button, then **Show in SAE** button. This will bring SAE window and launch **Mixed-Signal Options** dialog where you can see analog to digital interface element specification for /IO/clk net. Save the settings with clicking OK button.



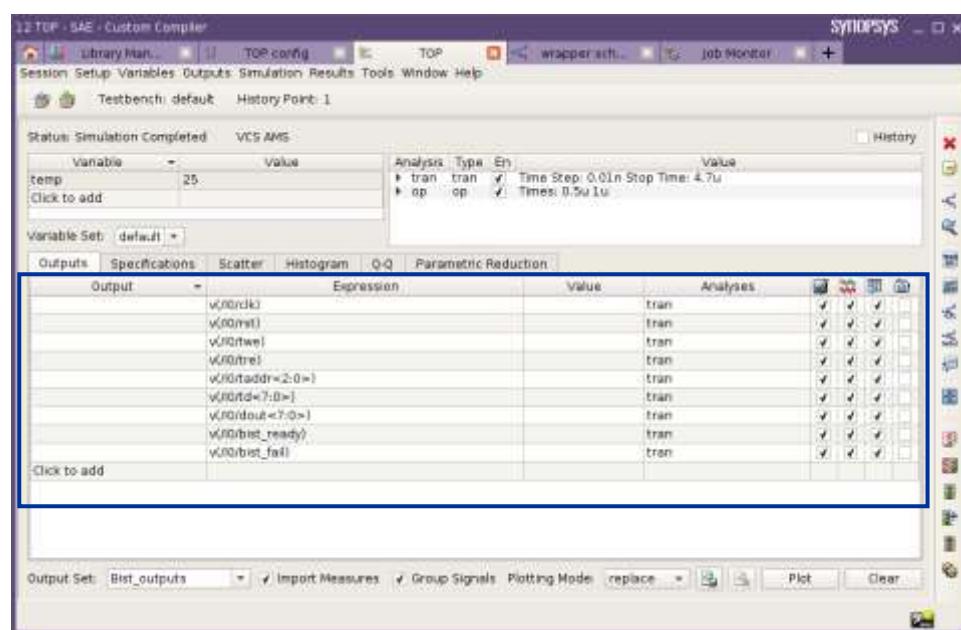
Task 88. Plotting waveforms in WaveView

Now let us analyze the simulation results in the waveform viewer.

357. In the SAE main window choose **Outputs → Edit**, and in the opened *Output Setup* window add two output sets with the names *Bist_outputs* and *Functional_outputs*. The first output set will contain the system signals needed to debug the BIST test, the second output will contain the system signals which are needed to view the memory functionality.

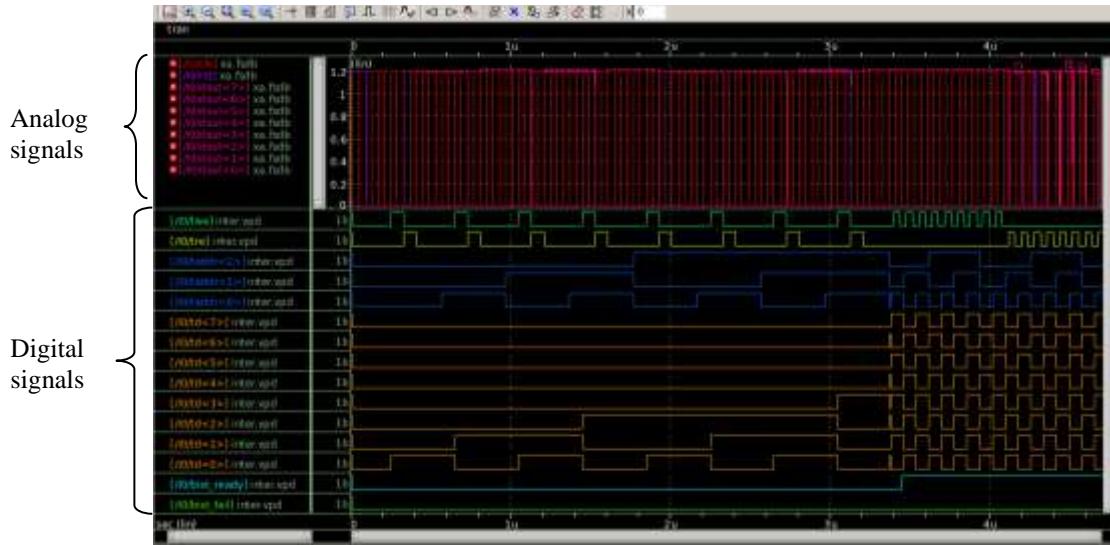


358. Press OK to close the *Output Setup* window.
359. Now in SAE main window select *Bist_outputs* as the Output Set.
360. Choose **Outputs → Add from Design (Ctrl+P)**.
361. In the TOP schematic window, descend into *wrapper* I0 instance and select the following signals with the stated order : *clk, rst, twe,tre, taddr<2:0>,td<7:0>, dout<7:0>, bist_ready, bist_fail*. Press **ESC** button to return to SAE window.

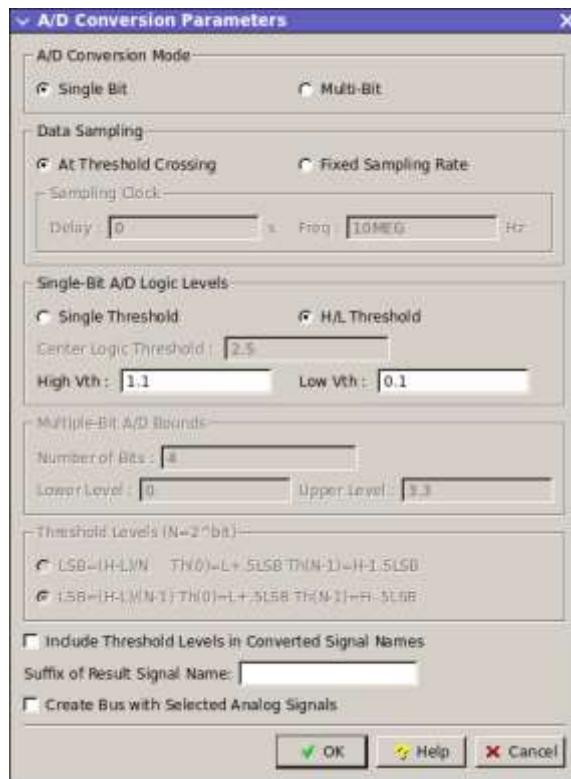


362. Press **Plot** button in SAE window to plot the signals.

At this point the WaveView should look like the below screenshot



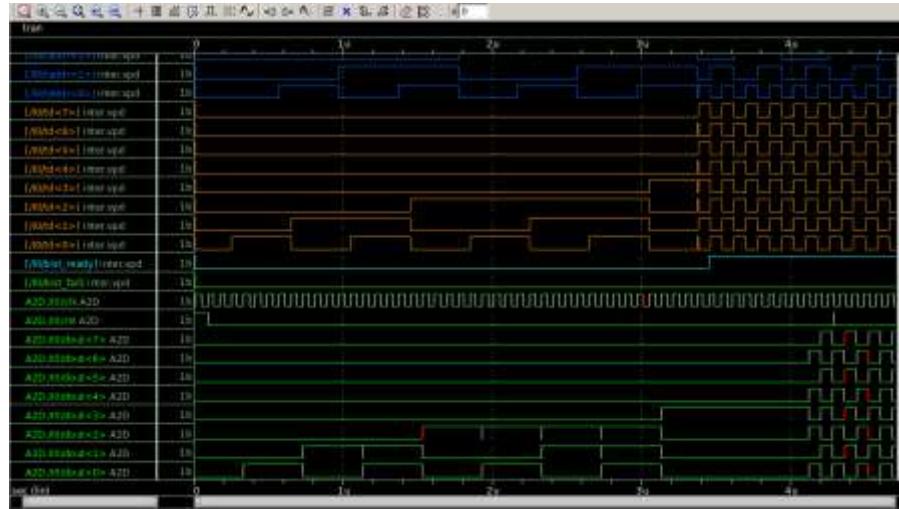
363. For easy debugging of these digital and analog signal sets, we will convert them to the same, digital, type. Select the analog signals in WaveView, choose **A to D** in *Utilities* section and in the opened “*A/D Conversion Parameters*” window, select *H/L Threshold* in “*Single-Bit A/D Logic Levels*” field, and specify the **High Vth** value as 1.1, **Low Vth** value as 0.1.



364. Press OK to perform A2D conversion.

Note: You can perform analog to digital conversation by using SAE a2d calculator function.

365. After having the converted digital signals, delete the analog signal from WV panel.
366. WaveView main window should look like as shown in the image



367. In the WaveView panel select signals $td<0>$ to $td<7>$, right-click on the signal panel of the WaveView window and selec **Group**, in the opened Bus Configuration window press “*sort signal order*” to change the grouped signals order and press Ok.
368. Perform the previous 10) point grouping action for *taddr* and *dout* bus bits.

Note: While grouping these signals don't forget to change the signals sorting order.

369. Now you can clearly see in the waves that after reset signal de-asseration BIST engine writes data, then reads that data for all addresses of the memory.



When reset, *rst*, signal goes to low value i.e. goes to its inactive state, BIST module starts to test the memory. By *td[7:0]* memory input bus it writes the data into memory, *we* signal high value enables writing data in memory. After writing the data in an address BIST module reads the data from the same address, *re* signal high value enables reading the data from memory. After reading the data, it compares the initially wrote data with the read data, if those date match then BIST module increases the address, increasing *taddr[2:0]* bus value, and continues to test the remaining bits of memory. When BIST module finish testing all memory addresses and no error is detected then *bist_ready* signal goes to high value, indicating that BIST engine has finish the test and no error is detected.

370. To see the memory input and output signals in functional mode, change the output signals set to **Functional_outputs** and perform the points 4)-12) for following signals: *clk*, *rst*, *bist_ready*, *bist_fail*, *twe*, *tre*, *taddr<2:0>*, *td<7:0>*, *dout<7:0>*.
371. Observe the waves after the time point when *bist_ready* signal goes to high value, which means BIST engine has finished testing of the memory and memory is in functional state. Below screenshot shows the system waves in functional mode.



When *bist_ready* signal goes to high value this means that BIST module finished testing the memory circuit and didn't detect any errors in the memory, after this memory is ready for correct operation. After this the test-bench writes data in memory, *we* signal activation. When it finishes writing the data in memory, test-bench starts to read that data, *re* signal activation. As it can be seen from picture the read data matches to the written data, hence the memory operates correctly in its functional mode, the same result that BIST module has identified.

Task 89. Back-annotating Results

In this task, you will learn how to back-annotate the results to the schematic.

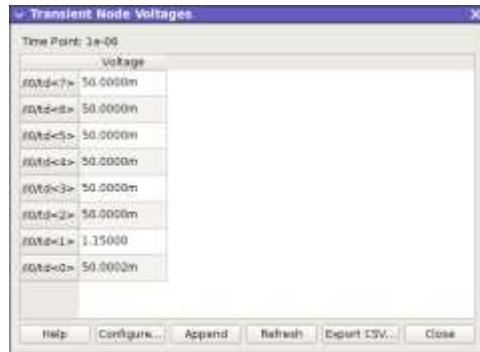
372. From the SAE window back-annotate the DC operating point using **Results → Annotate → Transient Node Voltages**
373. This will bring up the Back annotate Transient Node Voltages dialog.
374. Select *1u* as Time Point and click OK.
375. Descend one level down the hierarchy in the schematic and you will see the transient node voltages corresponding to the *1u* time point.

Task 90. Printing Results

In this task, you will print out the DC Operating points of the devices for the analysis purpose.

376. From the SAE window, print the DC Operating points using **Results → Print → Transient Node Voltages**
377. This will bring up the Transient Node Voltages dialog.

378. Write $1u$ as the time point to print and click OK.
379. You will be prompted to pick the object in the schematic.
380. As you click on different wires the node voltages will be printed corresponding to $1u$ time point.



381. Press **Configure...** button in that dialog and notice that you can set the corners there also.
382. **Close** the Transient Node Voltages.
383. Close all the windows.

Congratulations!

You have successfully simulated and verified the mixed-signal design TOP in the Simulation and Analysis Environment using VCS-AMS!

Answers / Solutions

Task 19. Setup mixed simulation

Question 6. How can users specify VCS compilation, elaboration or simulation options?

1. Users can specify VCS compilation options by using **Setup → Environment Options...** dialog, writing the options in the appropriate fields.

Task 20. Setup simulation options

Question 7. What controls *Force Nets* field in the **Mixed-Signal Options** dialog?

1. This field allows to choose the net/s which value will be forced to exact voltage during simulation.

Task 21. Netlist the design

Question 8. What files are generated in the netlist directory?

1. The following files are generated in that directory, which will be used for running mixed-signal simulation

runSimulation – this is the top file which is being sourced when we run the CustomSim-VCS mixed simulation. This file contains commands for calling VCS on the top design generate simv executable file.

vcsAD.init – this file contains all configuration data for mixed-signal simulation. By default, spice_top command is assumed to be specified in this file, resistance map file also is being specified in this file. Also VCS looks for vcsAD.init file as the mixed-signal simulation setup file if no file name is specified with the VCS switch "-ad".

compile.cmd –this file controls the VCS compiling phase, it contains all compiling options which VCS should consider while compiling the design.

elaborate.cmd - this file contains the VCS elaboration commands.

simulate.cmd –this file contains simulation options which are being specified while calling the VCS created simv executable file.

xa.cmd – contains CustomSim simulator options

xa.spi – this file is structural netlist, without analyses parameters and so on, of the analog design

netlist – this is full analog block netlist file

netlist.v – the verilog netlist of digital block,

cnl – this folder contains mapping data.