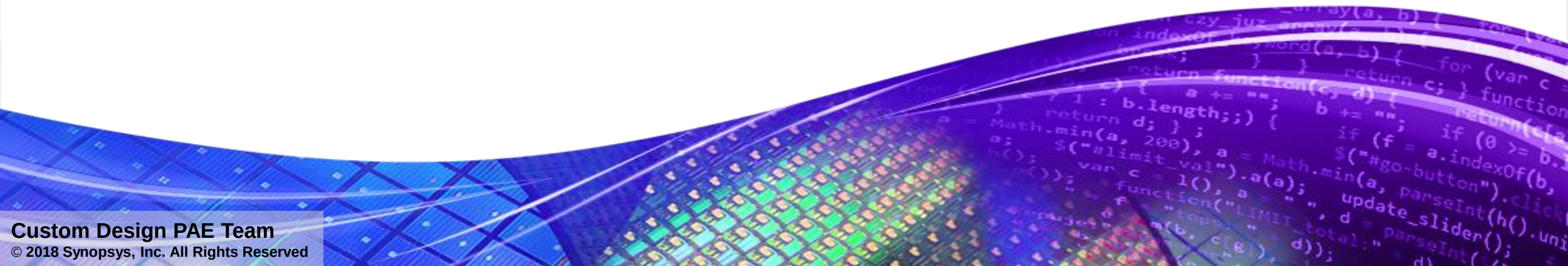
SYNOPSYS®
Silicon to Software™

Custom Compiler

Schematic Editor (SE)

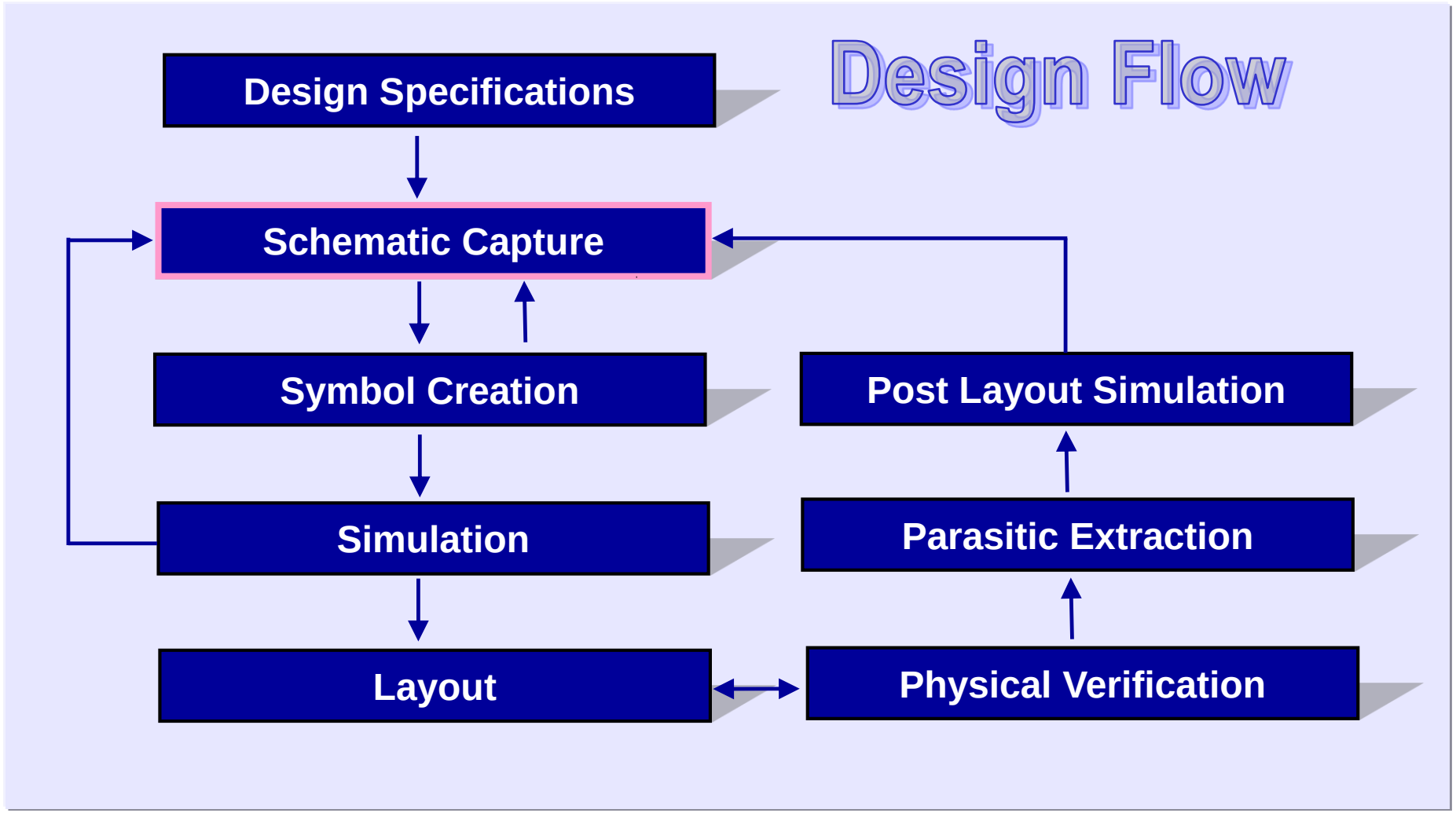
Advanced Schematic Editing

O-2018.09



Custom Design PAE Team

Full Custom Compiler Flow

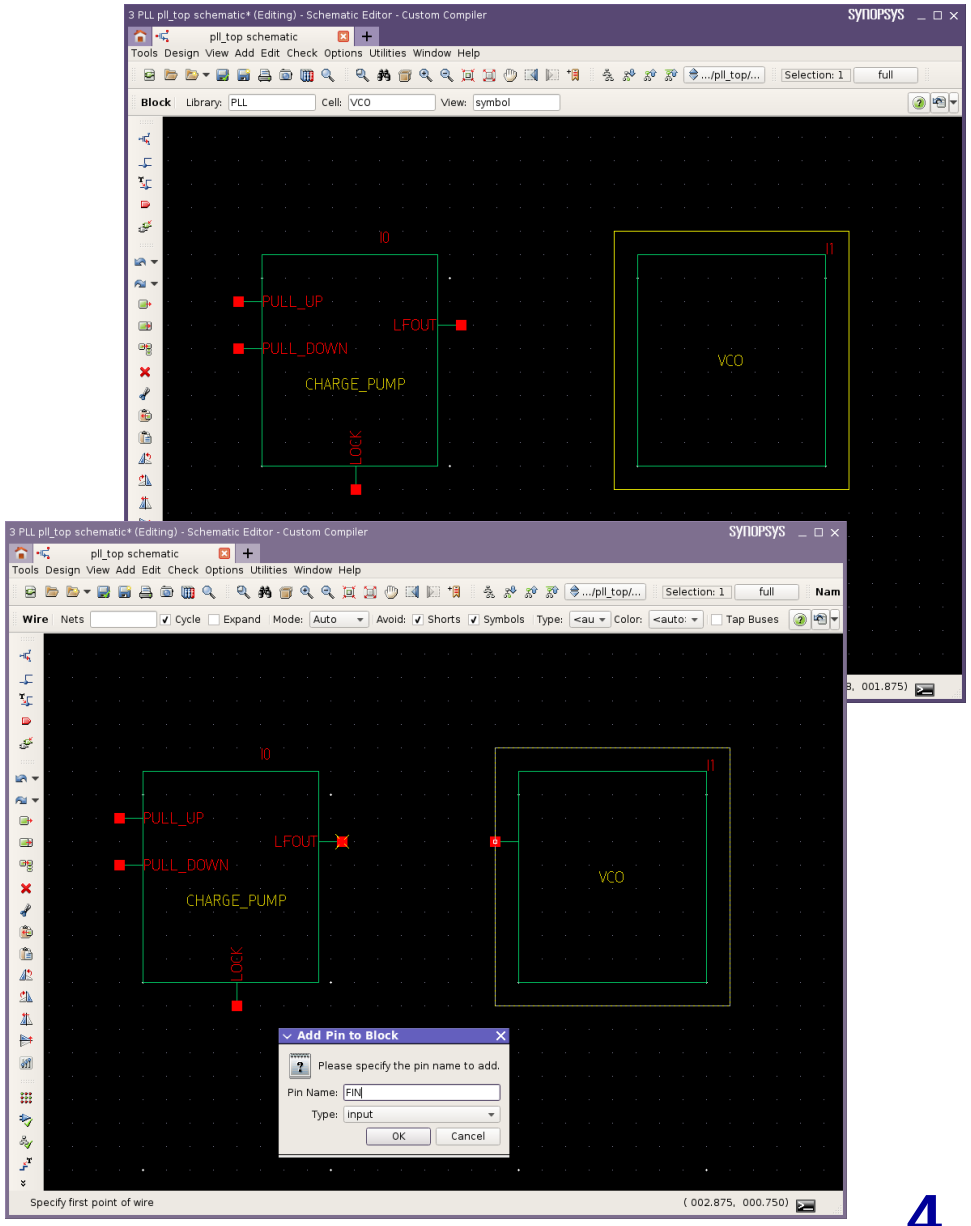


Unit Objectives

- **After completing this unit, you should be able to:**
  - Create block
  - Use bus tapping
  - Rename Instances
  - Align schematic objects
  - Route multiple pins
  - Automatically create wire stubs
  - Chop wires
  - Pick and Magnify
  - Create table
  - Insert images
  - Create Multi-Sheet design
  - Use Schematic Object Filter assistant
  - Filter Simulation Parameters

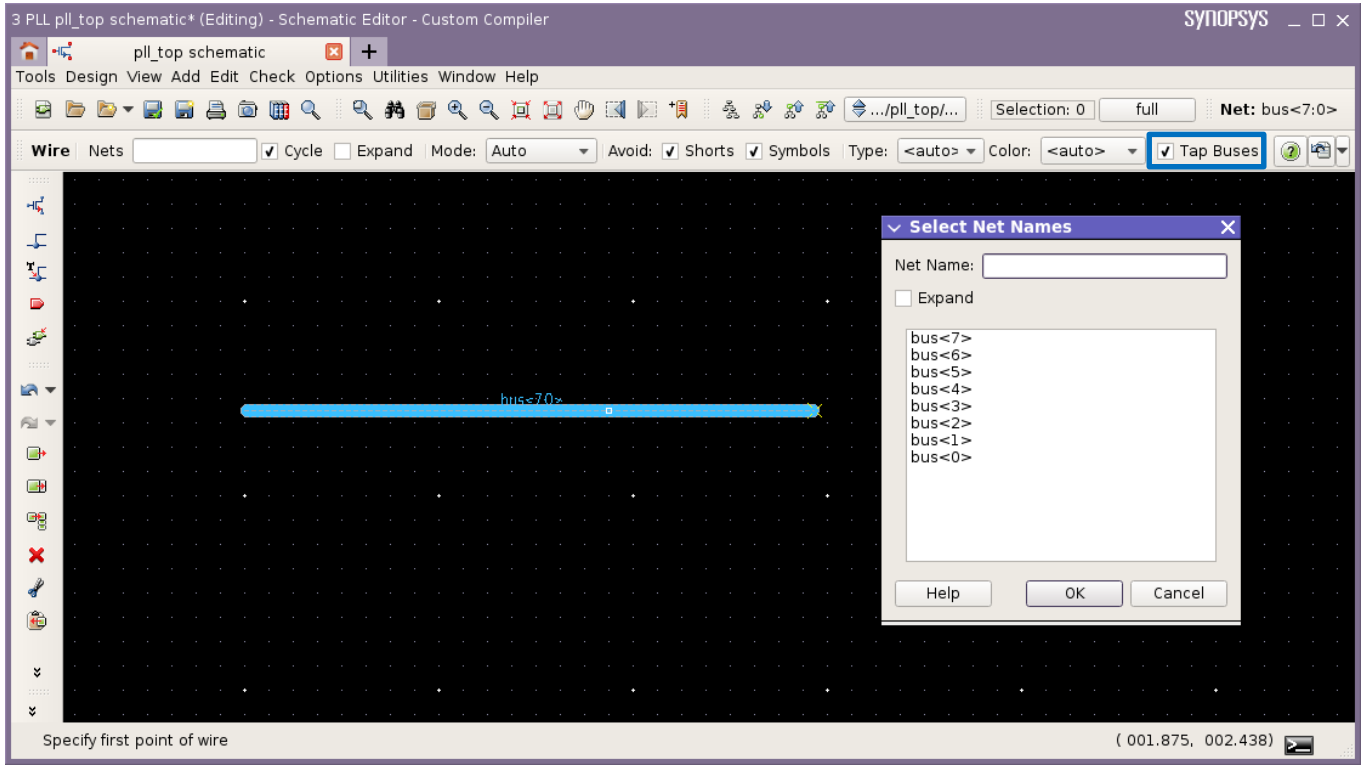
Block Creation

- **Supports top-down design methodology**
- **Allows to create symbols in place**
- **Use model**
  - Invoke the command (Add > Block)
  - Specify LCV
  - Draw the shape for the symbol
  - Add Pins
    - Invoke the Wiring command
    - Click on the boundary of the symbol shape
    - Specify the pin name and type
    - Click OK



Bus Tapping

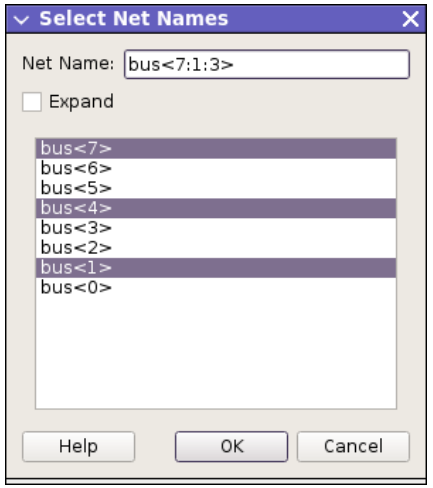
- Allows to select single and multiple bits from the bus or bundle
- Available from the wiring command



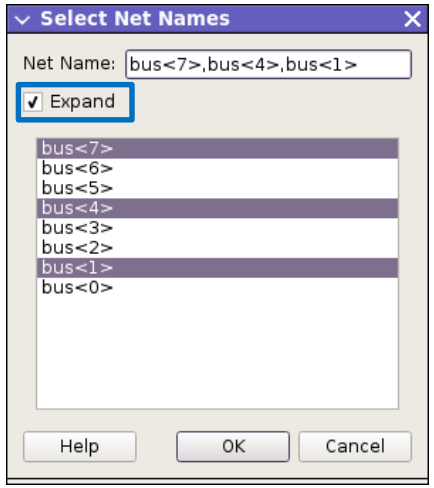
Bus Tapping

- **Tapping multiple bits from the bus results in new bus/bundle**
- **Example: Tapping bus bits: *bus<1> bus<4> bus<7>***

  - Expand Option: OFF
    - Results in bus<7:1:3>, meaning every 3 bits till 7th bit

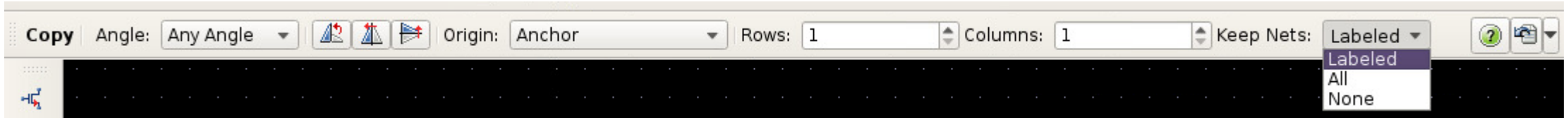


  - Expand Option: ON
    - Results in bus bus<7>,bus<4>,bus<1>



Net Name Propagation on Copy

- **Keep nets option allows to select what the final net should be assigned to copied wire segments**

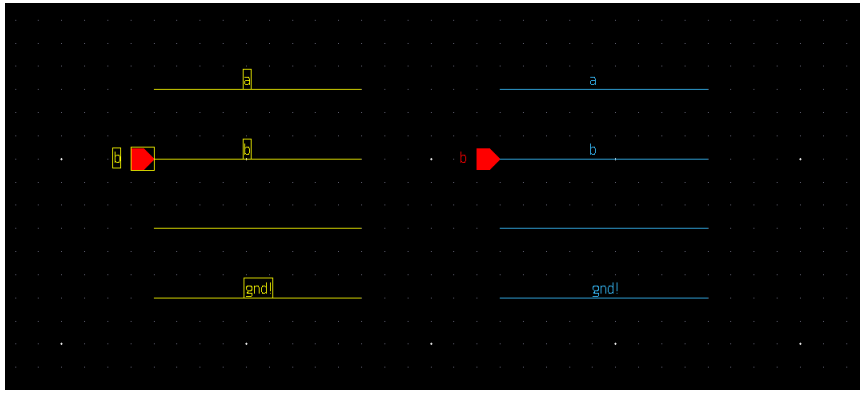


  - Labeled - copy all attached wire labels of selected wire segments
  - All - create wire labels for unlabeled nets to keep final nets of all copied segments the same as their sources
  - None - prevent copy command from creating wire label objects of copied segments. This option doesn't affect on selected segments labeled as global

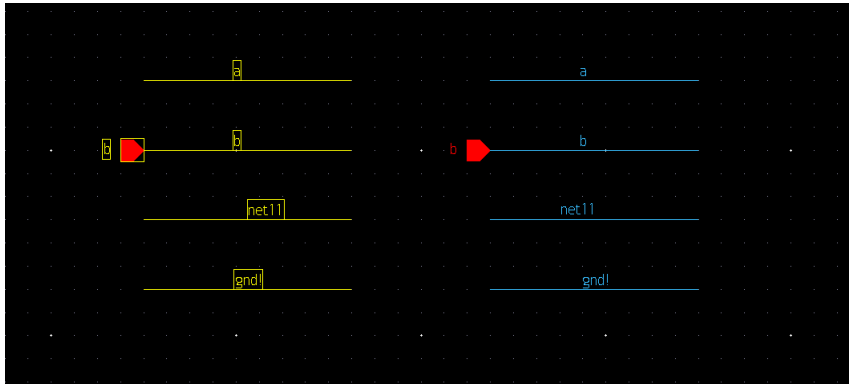
- **Logic is applied to wire labels regardless if they are selected or not**

Net Name Propagation on Copy

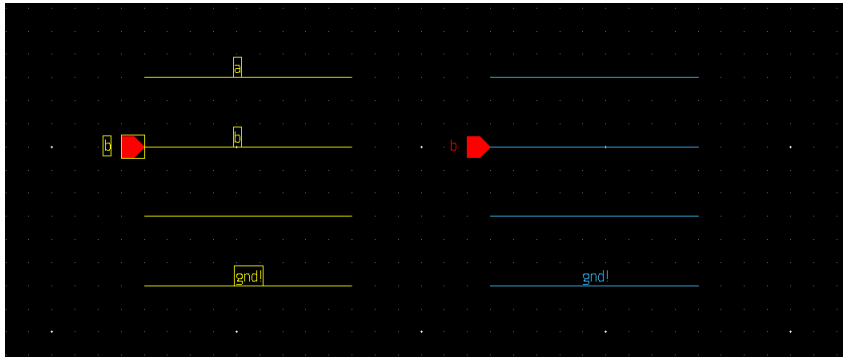
Keep nets - Labeled



Keep nets - All

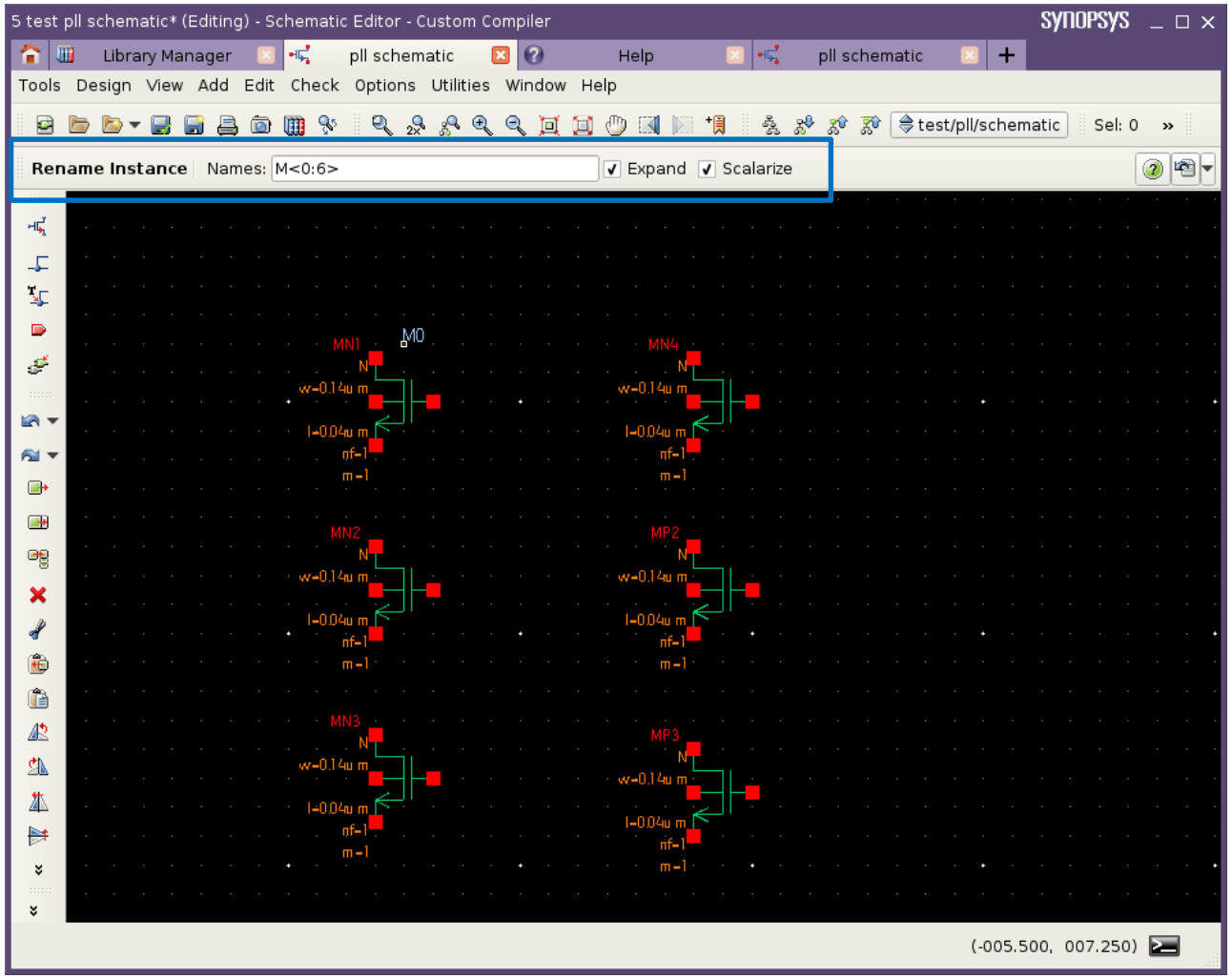


Keep nets - None



Rename Instances

- **Choose Edit > Rename Instance**
  - Specify the options
    - Expand: If the Names field contains a non-scalar name (for example, vectors like A<0:10> or bundles like "X,Y"), the names splits into bits before using.
    - Scalarize: Makes the vector bit names scalar by removing the brackets
  - Hover over the instance and click the rename
  - Press Esc to end the command

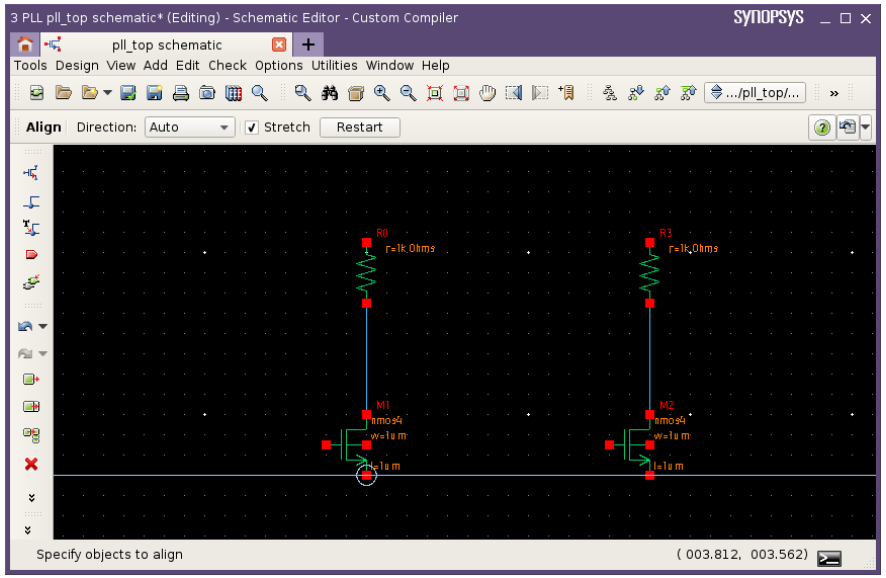


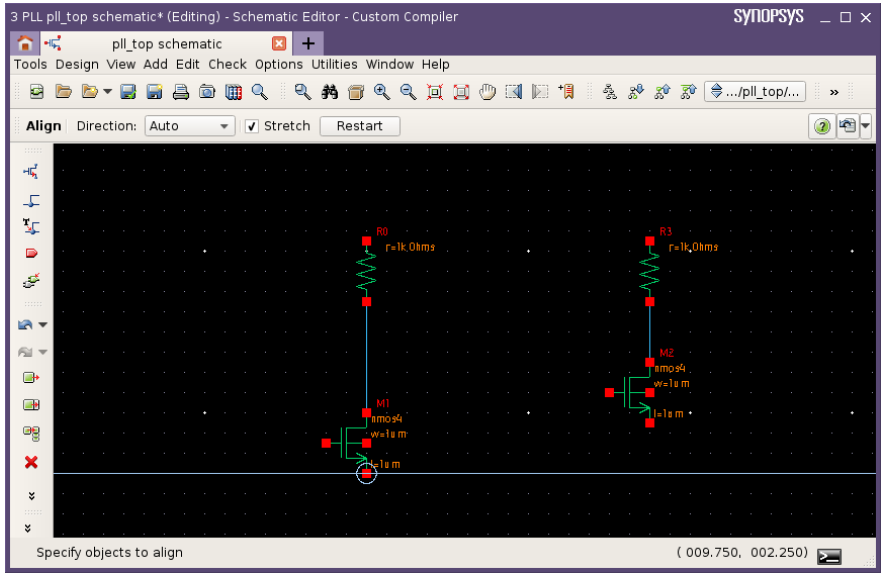
Schematic Objects Alignment

- **Improves the readability of the schematic**
- **Simplifies routing between aligned pins and instances**
- **Supports alignment direction:**
  - vertical
  - horizontal
  - auto
- **Align schematic objects by instance origins**
- **Preserve connectivity during alignment**
- **Supports "Restart" option to continue the alignment from the start**

Schematic Objects Alignment

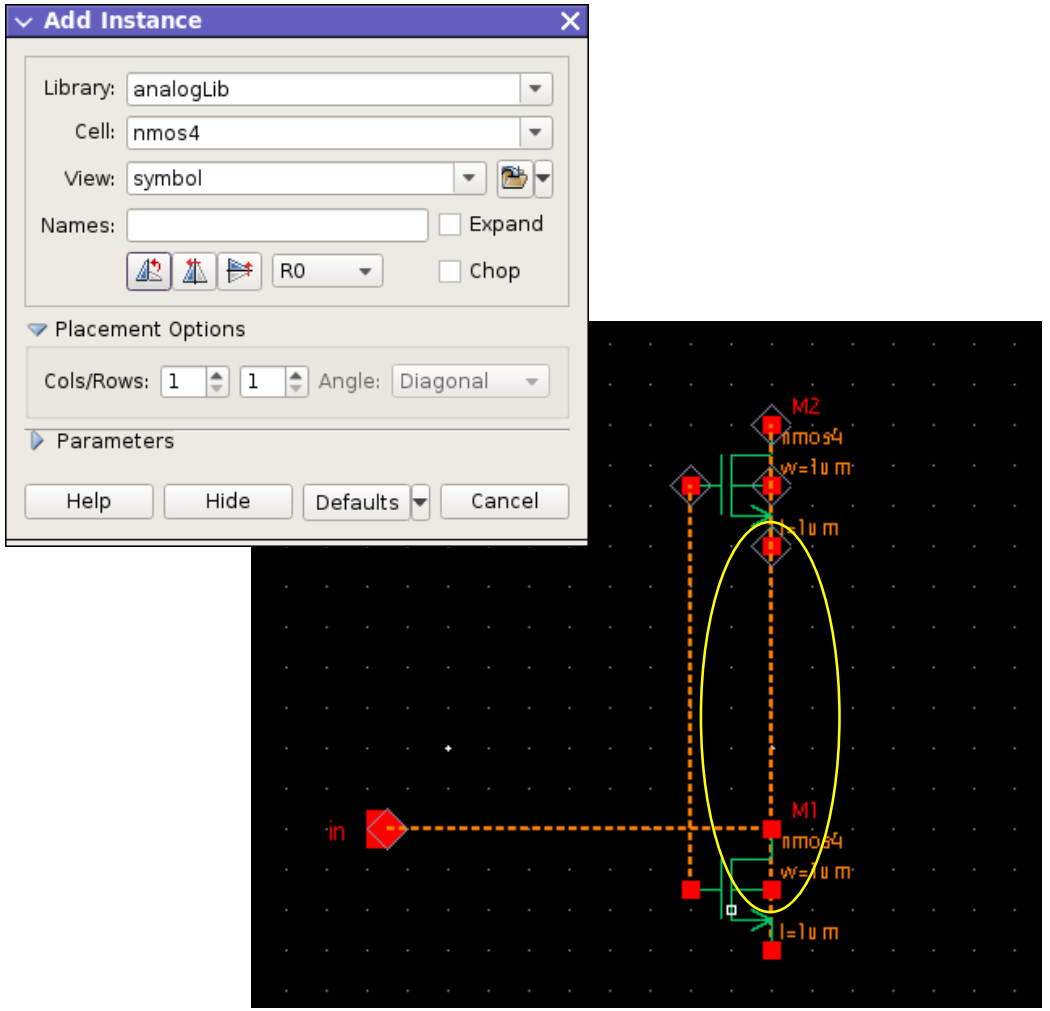
- **Use model:**
  - Invoke the command (Edit > Align)
  - Specify alignment direction
  - Click to specify source object
  - Click again to specify target object
    - Once target object is specified, it will be aligned with source object





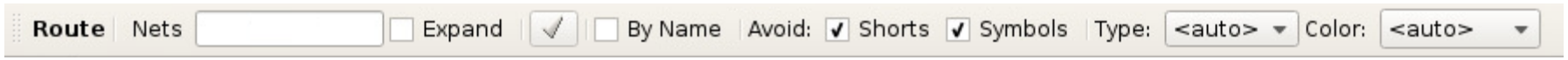
Schematic Objects Alignment Aids

- **Displays alignment lines between instance terminals and pins during instance placement**
- **Enables correct placement of new instances and pins**
  - No need to align instances and pins location later
- **Use the ALT+A bindkey to toggle this feature on or off**



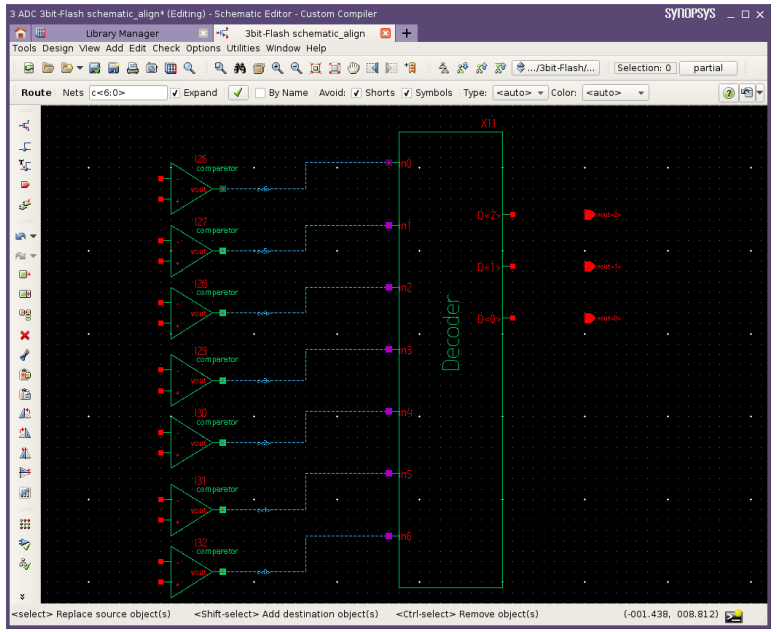
River Routing

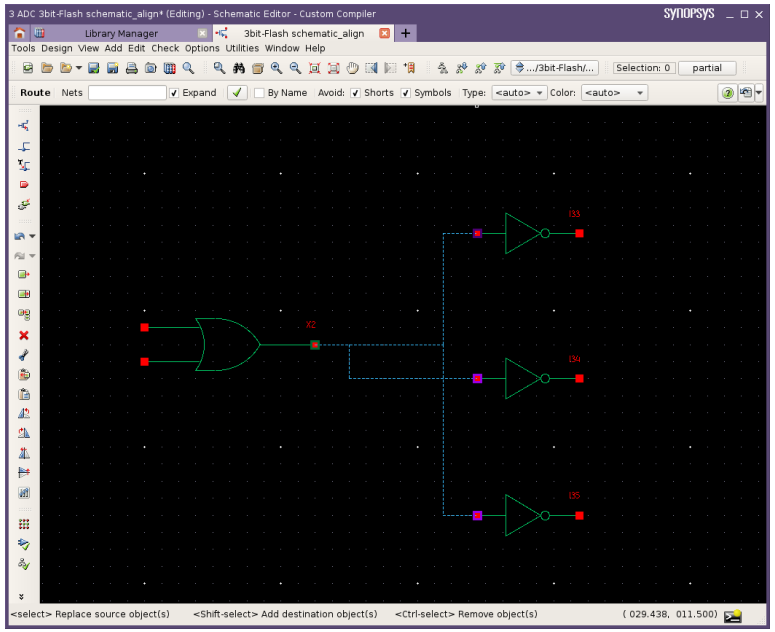
- **Creates**
  - Parallel routing
  - One to many routing
  - Many to one routing
- **Routes multiple pins at once**
- **Routing Supports:**
  - Connection by name
  - Avoid Shorts
  - Avoid Symbols



River Routing

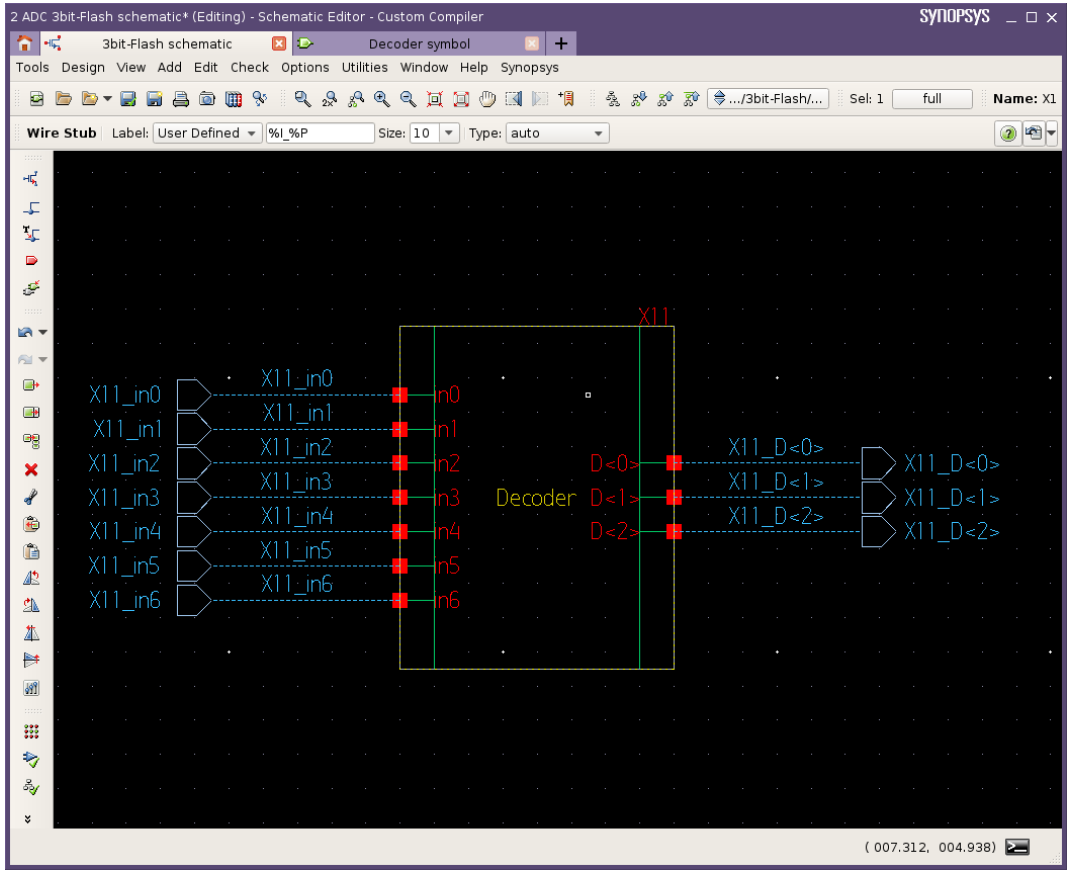
- **Use model:**
  - Invoke the command (Add > Route)
  - Select source pin/pins to route from
  - Select destination pin/pins to route to
  - Commit the routing





Automatic Stub Creation

- Speeds up the routing process
- Creates wire stubs on the instance terminals

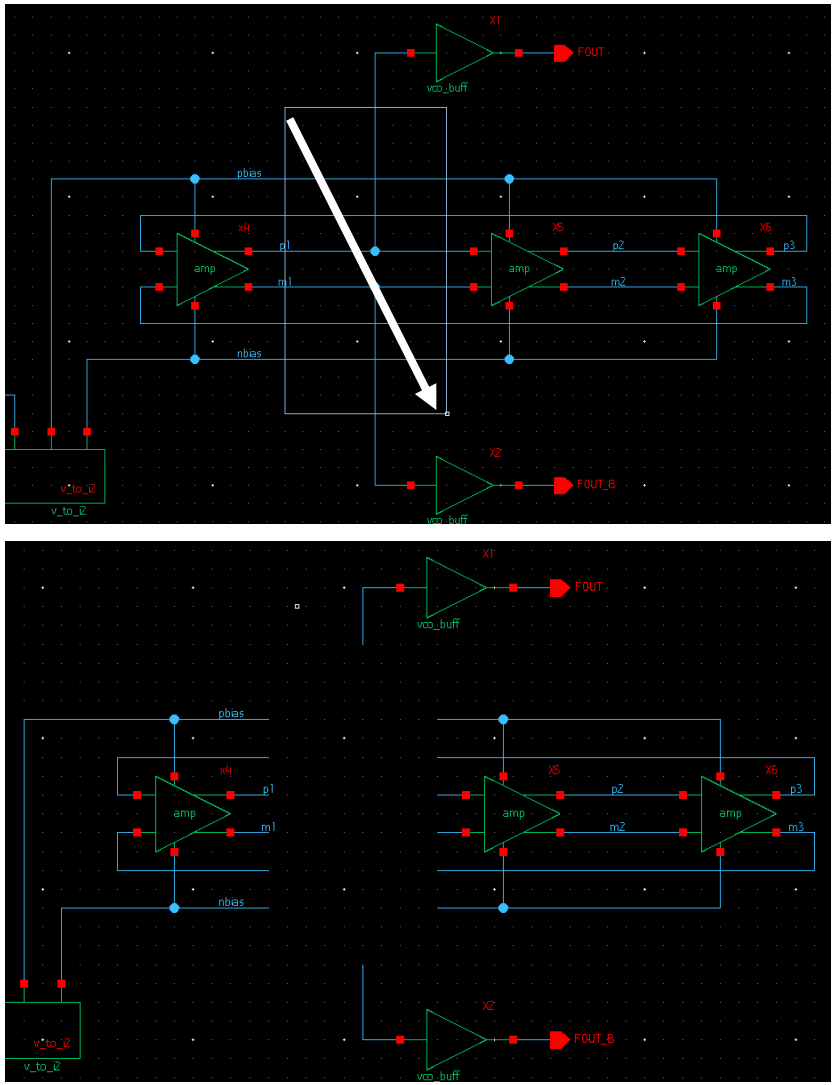


Automatic Stub Creation

- **Label Creation**
  - None – wire stubs are auto named
  - Pin Name - labels with the name of the pins are created
  - User Defined – supports parameterized names with predefined variables
    - %I – substituted by instance name
    - %P – substituted by pin name
- **Stub Size**
  - Auto - Adjust wire stub length according to the wire label length
  - Wire stub length in grids
- **Type**
  - Connect wire stub to no connection symbol
    - Prevents "Floating Instance Pins" connectivity rule violation
  - auto, input, output, inputOutput
    - Create pin and attach to wire stub
    - auto - adds pins according to pin direction defined in instance master

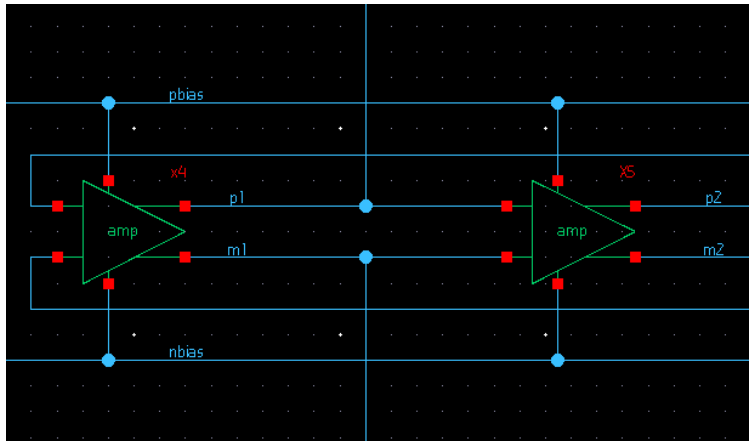
Chop Wires

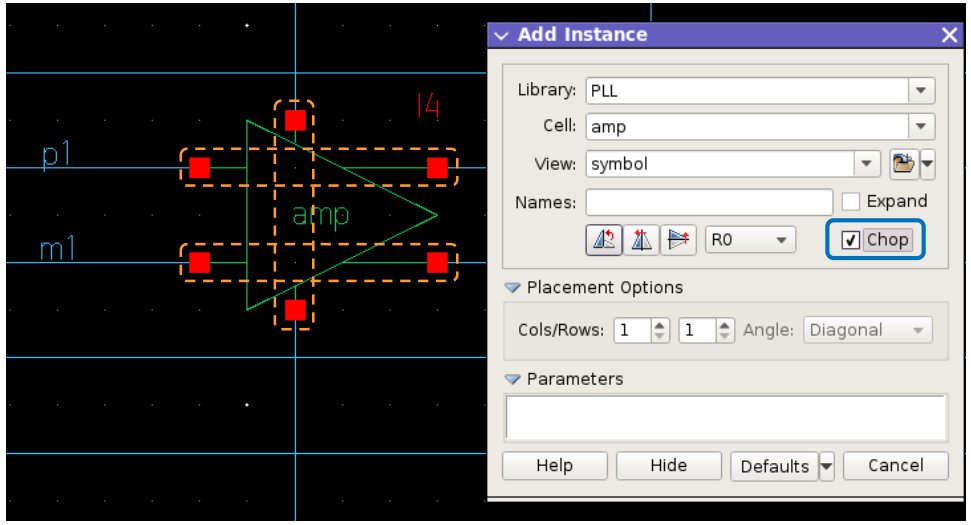
- **Ability to delete all wiring objects in the specified area from design**
- **Use Model:**
  - Choose Edit > Chop Wires
  - Click and drag to select the area
  - Second click to end the selection and chop the wiring objects
- **Wire segments/Net name labels located completely in the chopping area are deleted**
- **Wire segments located partially in the chopping area are cut at the point of intersection with area border**
- **Net name labels located partially in the chopping area are not deleted**
- **Instances, Pins, Notes, … are ignored**



Wires Auto Chopping in Instance Creation

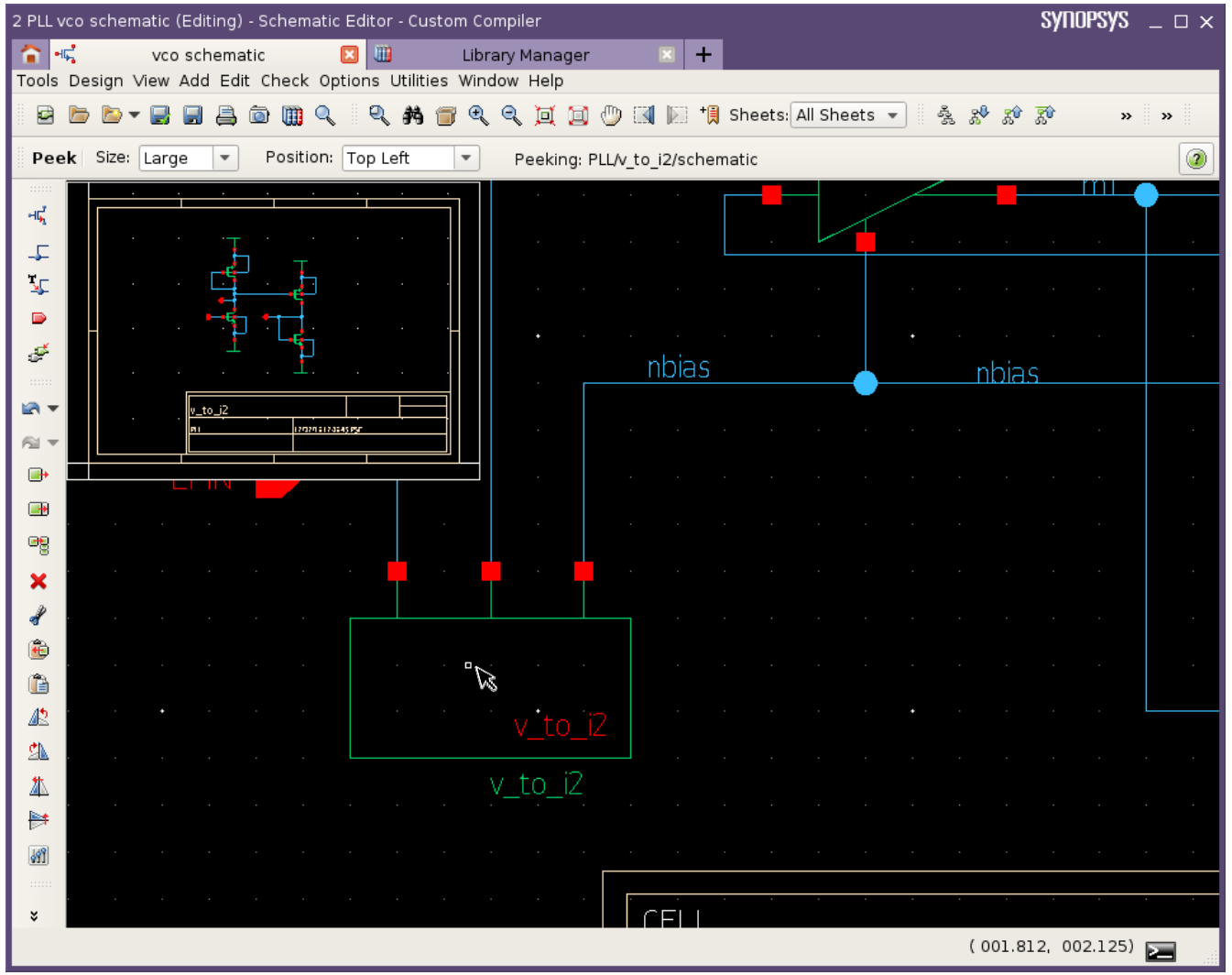
- **When “Chop” option is enabled in “Create Instance” dialog, creates a gap in the existing wire(s) and inserts the instance to this gap with one action**
- **After the instance is added (that is, after the instance pins are already connected to the wire ends), the shorting wires are chopped under the instance area**
  - Only the wire segments of nets that are connected to more than one pin of this instance are affected.





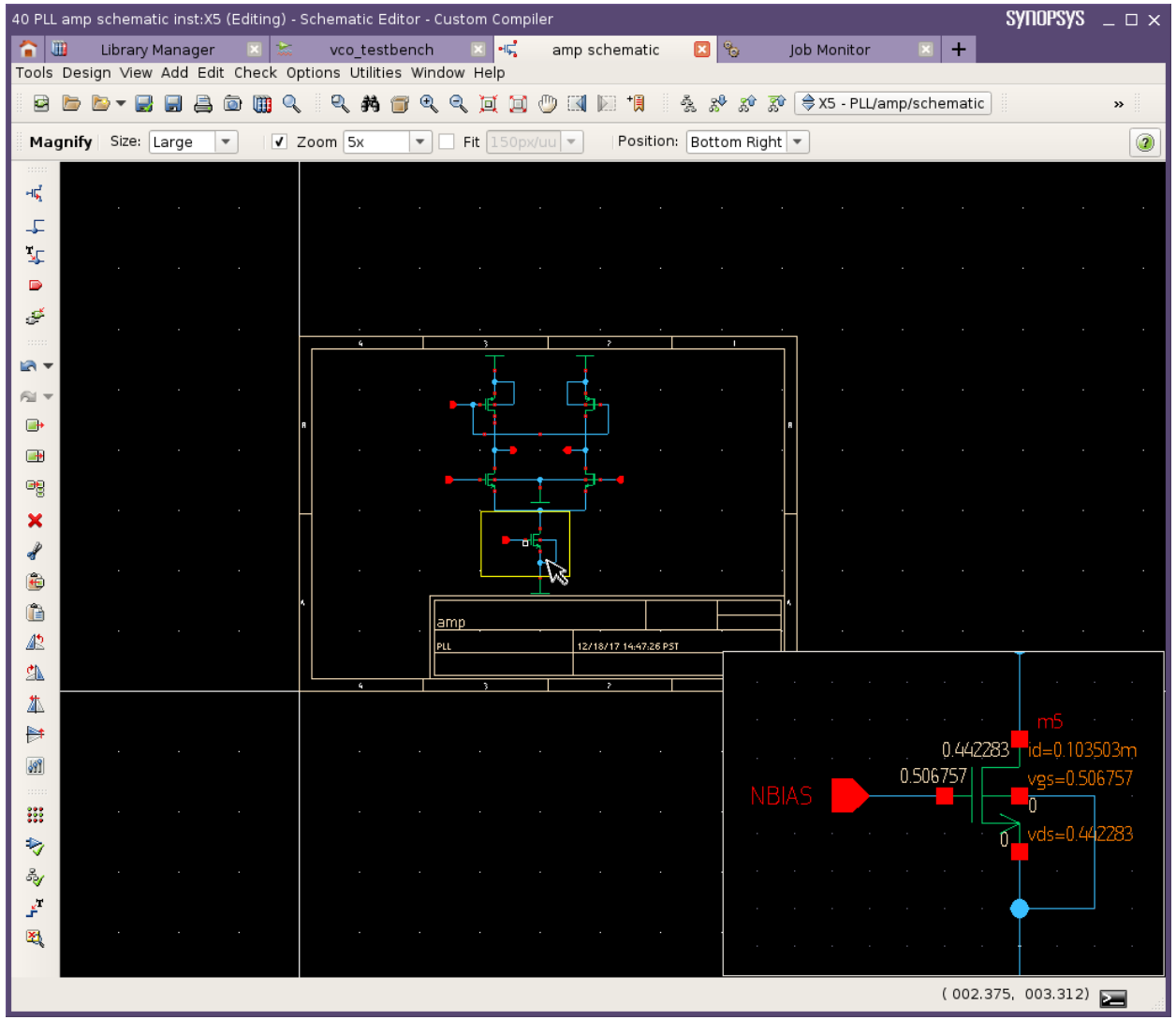
Peek Command (Visual Descend)

- **Peek enables visual “Descend” without descending**
  - When the mouse is over an instance the next level down is displayed in dynamic window
- **Invoke the command using View > Peek**
- **Eliminates unneeded navigation**
- **Specify size and position of a window used to peek hovered instance**
- **View heat map annotations inside peek window**



Magnify Command

- **Magnify specific area in the design without zoom in/out commands**
- **Prevents unneeded zoom actions**
  - Observe annotated OP Point or node voltage values
  - Checking parameter values
- **Invoke the command using View > Magnify**



Edit / Synchronize Port Order Dialog

- **Cleans up obsolete ports from portOrder property**
- **Maintains consistent port ordering across different views**
- **GUI can be invoked from Schematic Editor, using Edit > Port Order Edit/Synchronize**
- **Supports:**
  - Drag-and-drop operation
  - Add operation
  - Control ordering
  - Obsolete port highlighting

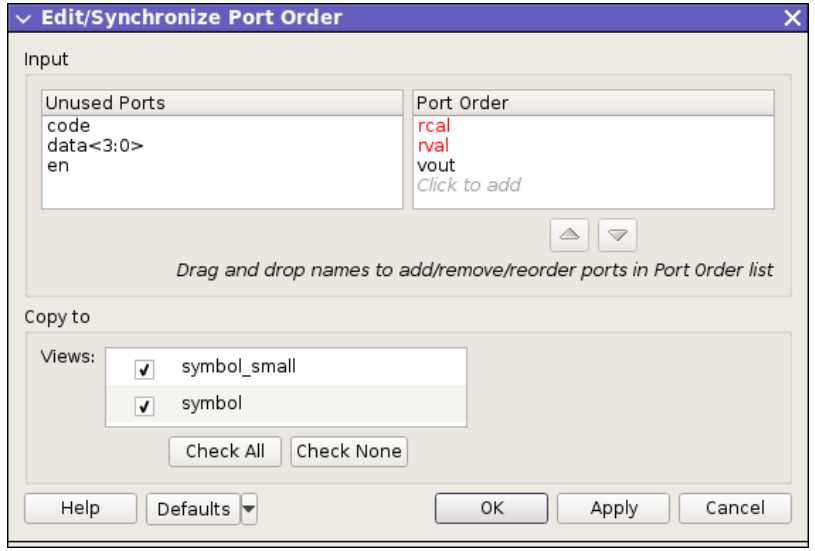


Table Creation

- **Improves the readability of the annotation data**
  - Invoke the command using Add > Table

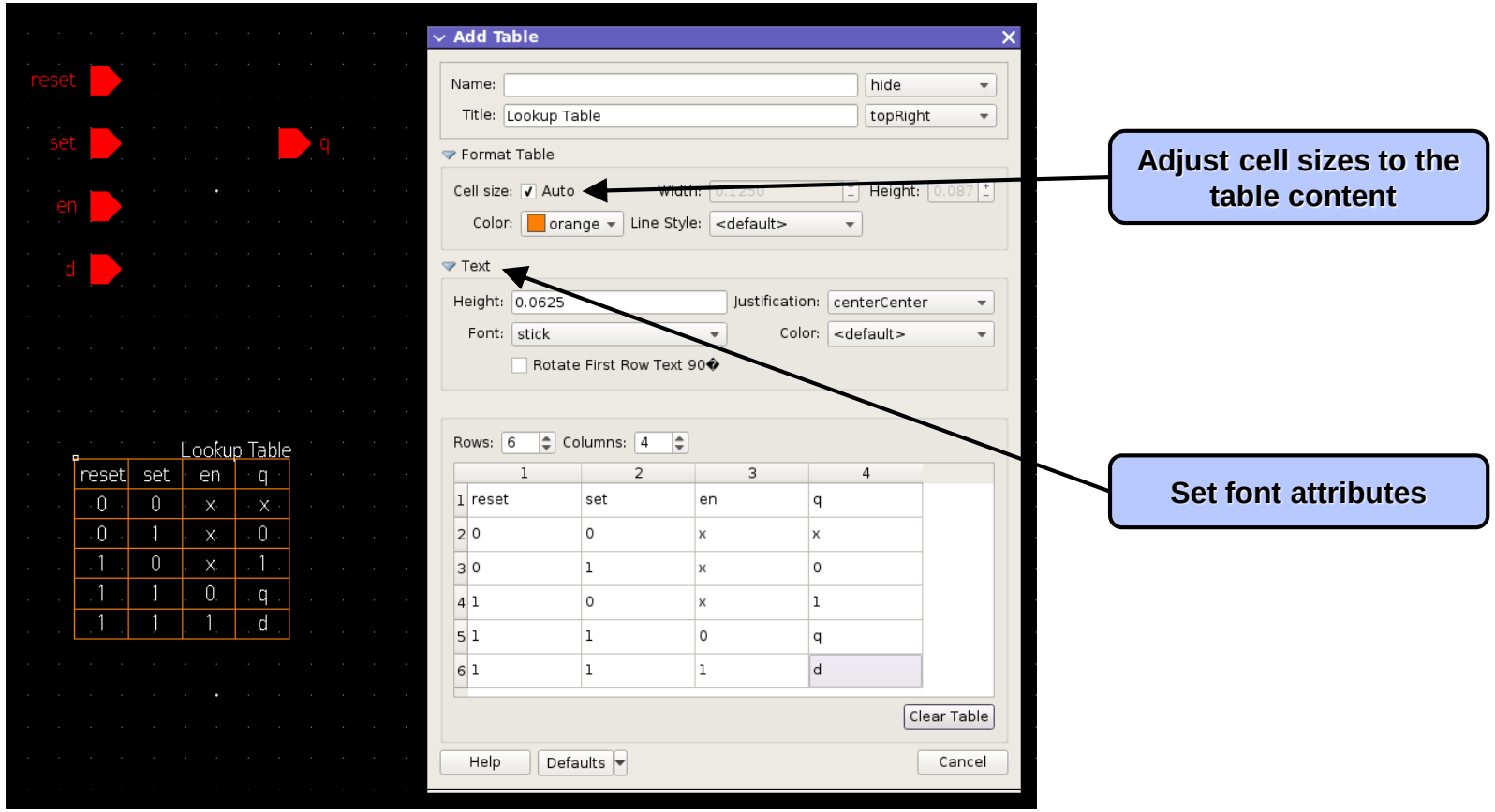
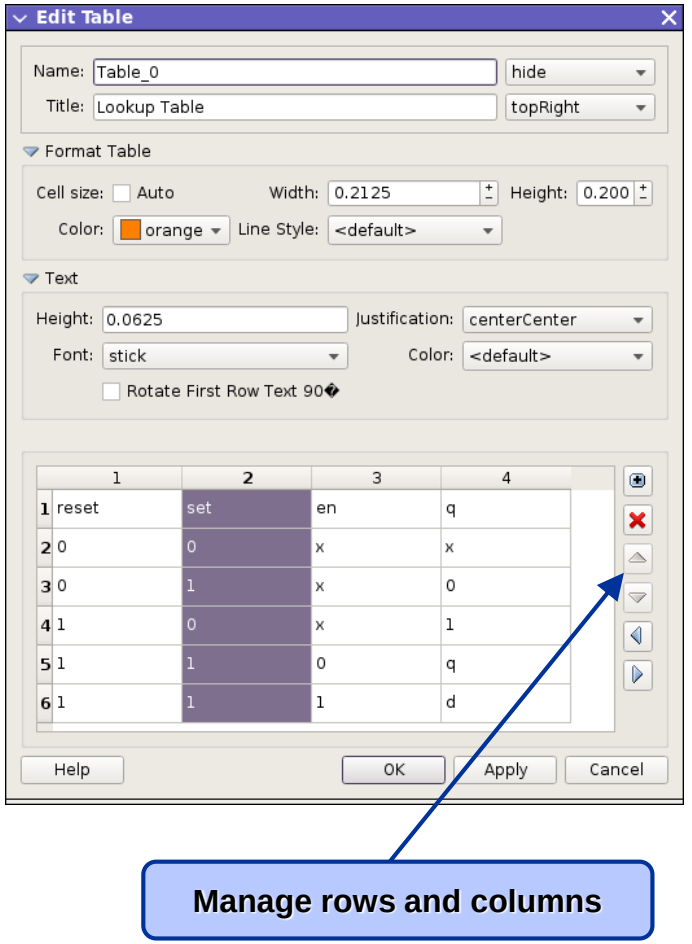


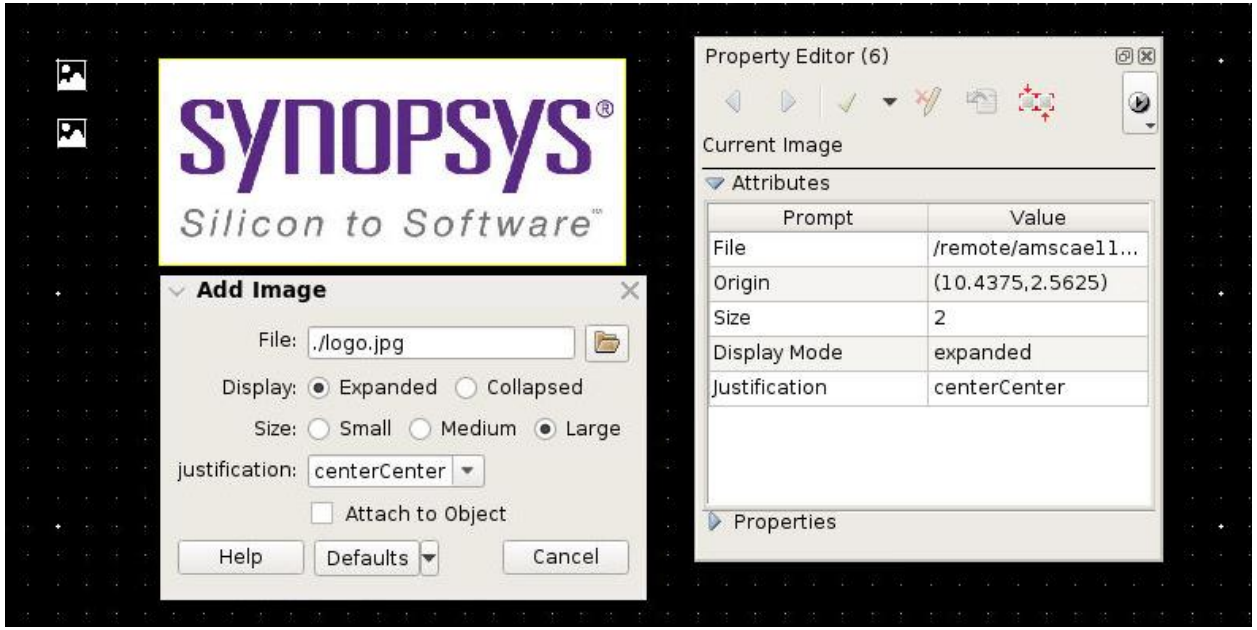
Table Editing

- **Double click on cell label to edit cell value on canvas**
- **Double click on table or use “q” bindkey to invoke editing dialog**
  - Change position of rows and columns
  - Add/delete rows and columns
  - Change table title and name
  - Update cell values
  - Change font and border attributes



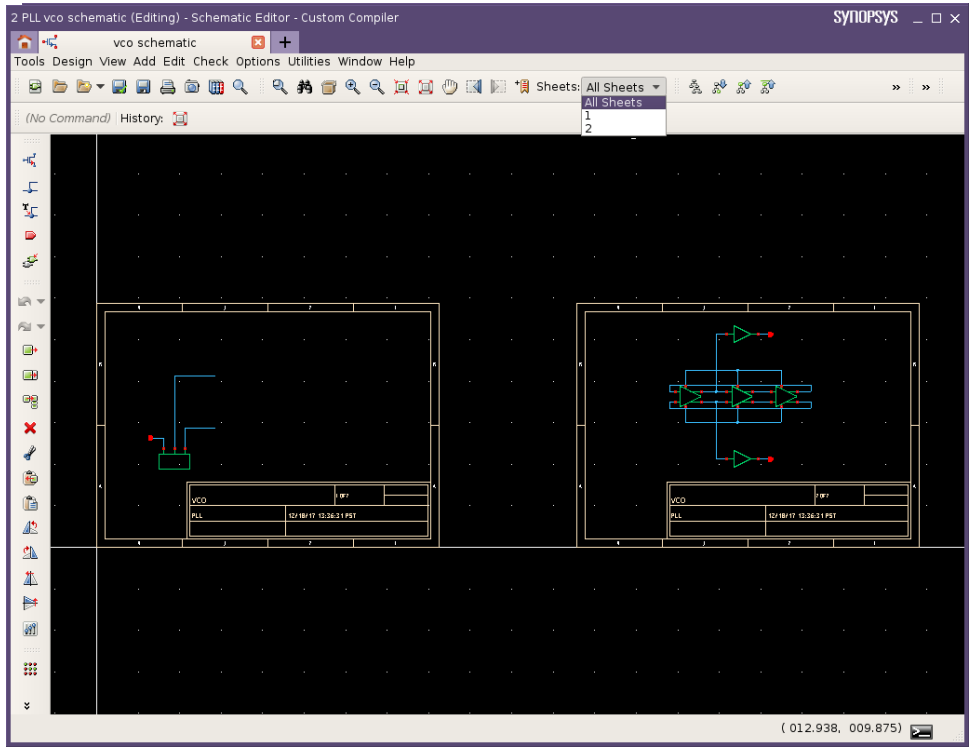
Insert Images in Schematic

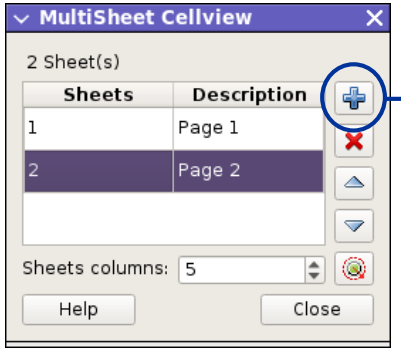
- **Invoke the command using Add > Image**
- **Supported formats: BMP, GIF, PNG, JPG, JPEG, PBM, PGM, PPM, XBM, XPM**
- **Attach image to any figure (including other images)**
- **Two modes of images:**
  - Expanded
  - Collapsed - show a small icon on canvas, which can be expanded
- **Editing of image attributes can be done on the image Tcl object and Property Editor**

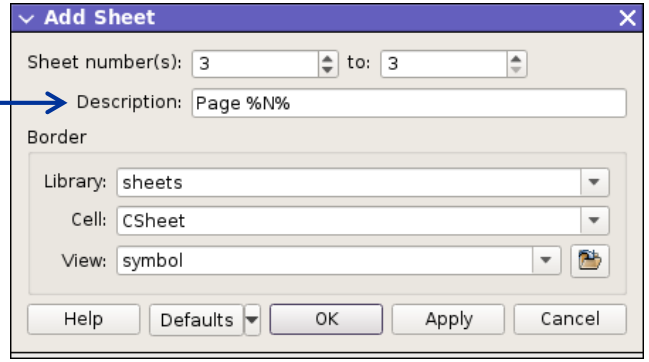


Multi-Sheet Schematic Cellview

- **Easy navigation between sheets**
- **MultiSheet Cellview dialog allows sheets to be**
  - Added
  - Removed
  - Re-arranged
  - Resized
- **Enable Mutli-Sheet**
  - Add > Sheets

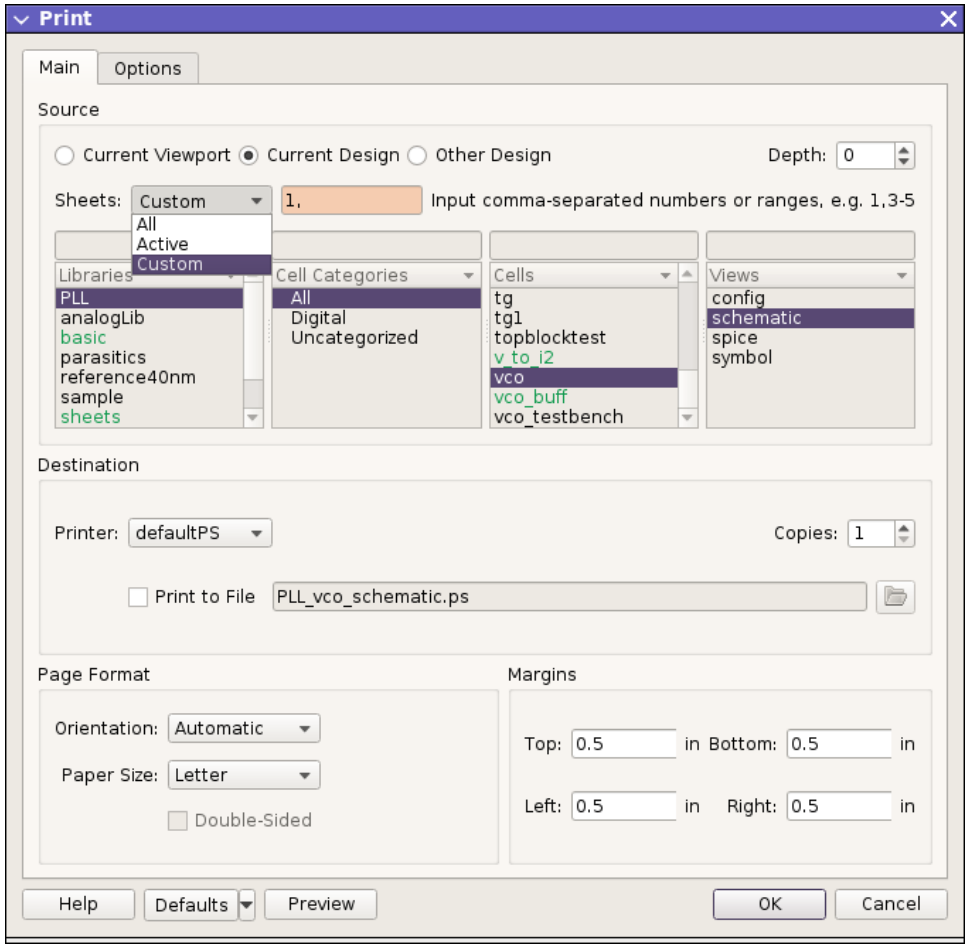






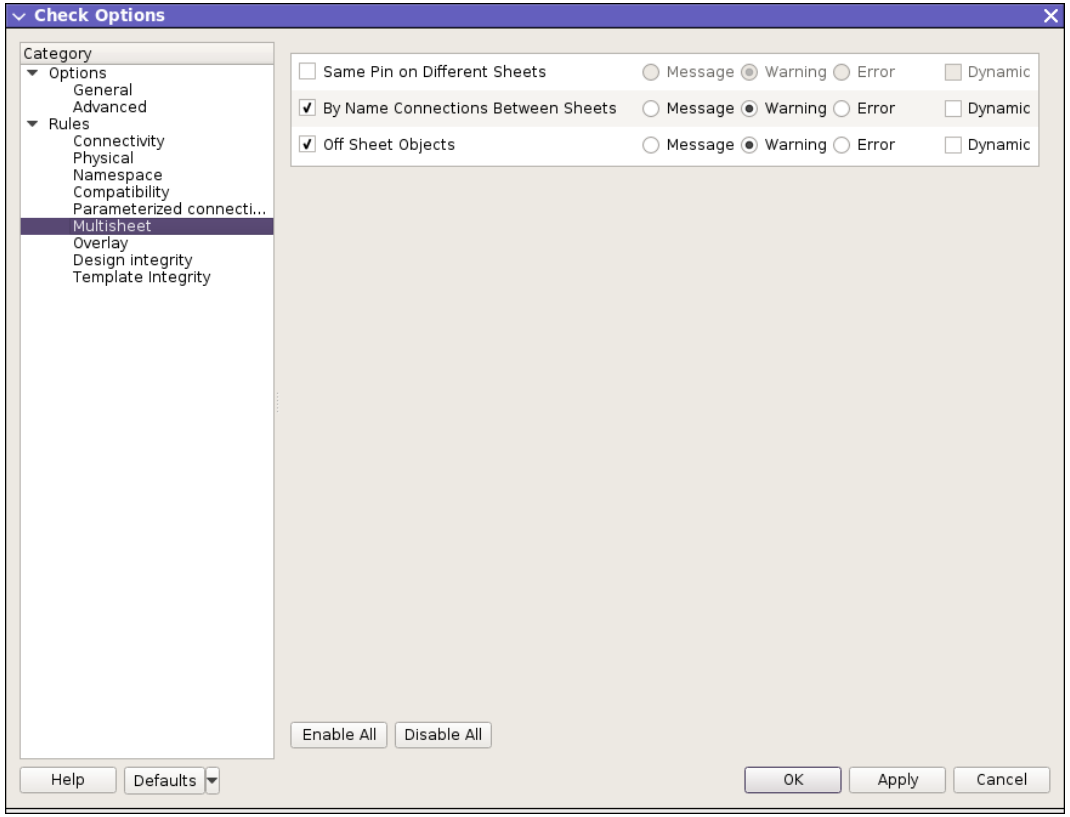
Multi-Sheet Printing

- **Specify sheets to be printed**
  - All
  - Active
  - Custom
    - Comma-separated



Multi-Sheet ERC Rules

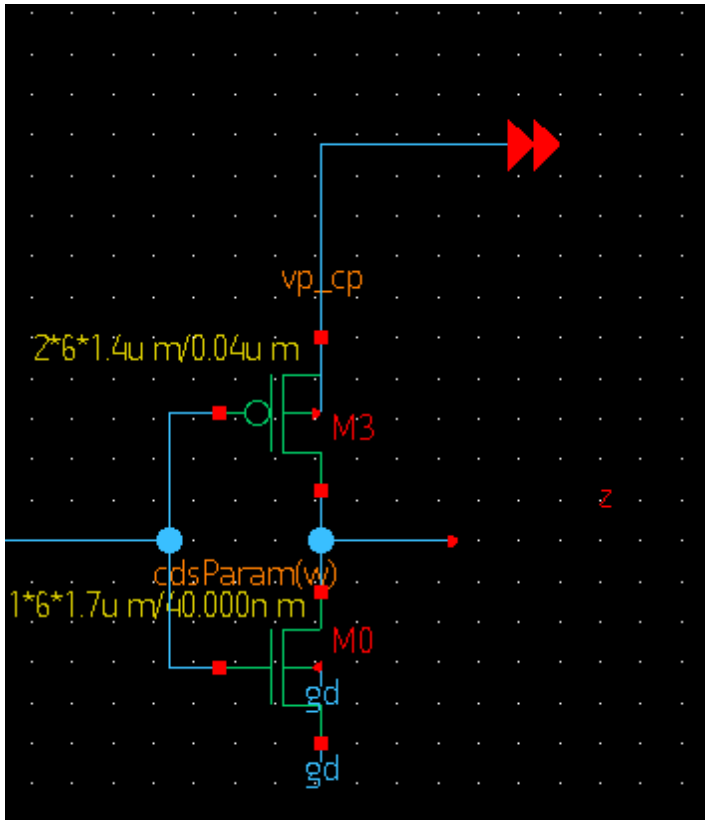
- **Same Pin on Different Sheets**
- By Name Connections Between Sheets
  - Not reported when the by name connection between sheets is created by a global net
- **Off Sheet Objects**



Multi-Sheet Off-Sheet Connector

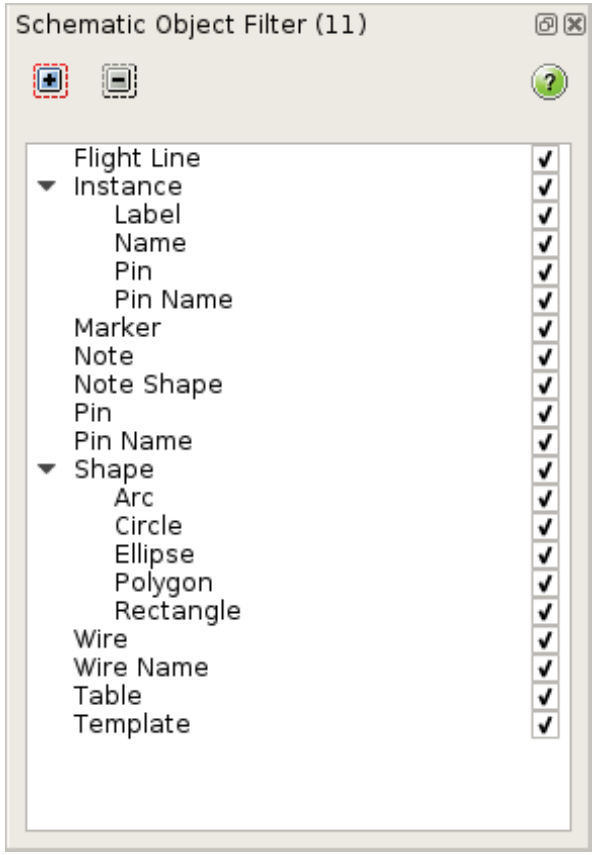
- **Used when users want to explicitly connect nets from different sheets to avoid ERC error reporting**
- **Denoted by the symbol:**

- **Invoked from:**
  - Add > Sheet Connector



Schematic Object Filter Assistant

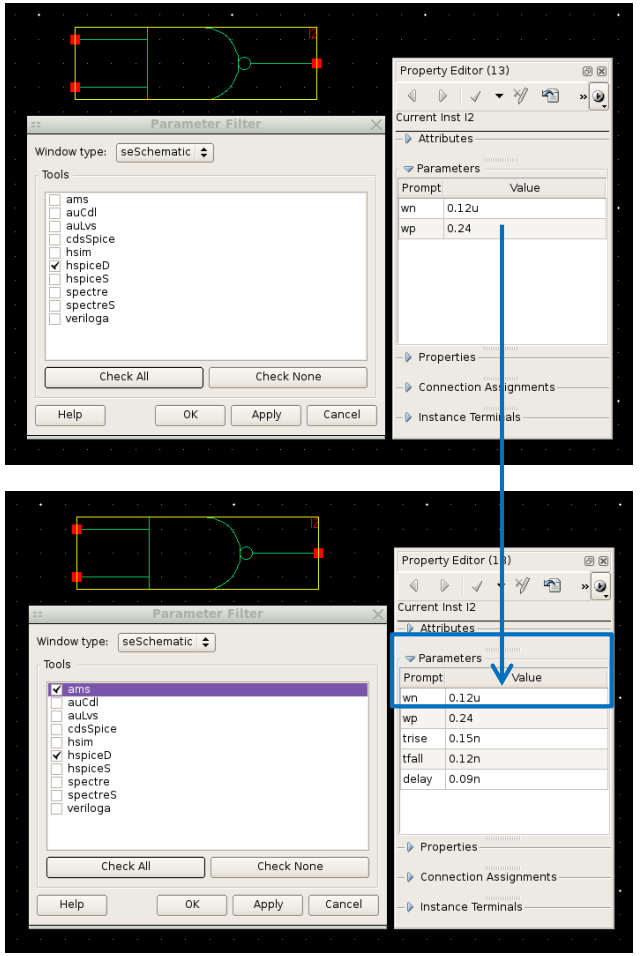
- **Controls the selection of schematic objects**
  - All objects in schematic are selectable by default
- **Useful when certain type of objects need to be modified**
  - Examples:
    - Changing font size of all the wire names
    - Deleting all the wires
- **Invoked from:**
  - Window > Assistants > Schematic Object Filter
- **Tcl command**




```
db::setAttr visible -of [de::getObjectFilters -filter {%name=="seSchPinName"}] -value 0
```

Parameter Filter

- **The Parameter Filter allows to reduce the set of displayed instance parameters using CDF information**
  - instParameters and otherParameters simInfo fields are used for determining the parameters of interest
  - It does not modify the behavior of the parameter “display” attribute
- **Invoked from:**
  - Edit > Properties > Parameter Filter
- **Tcl command**




```
db::setParamFilter {hspiceD auCdl veriloga} -windowType [gi::getWindowTypes seSchematic]
```

Test for Understanding

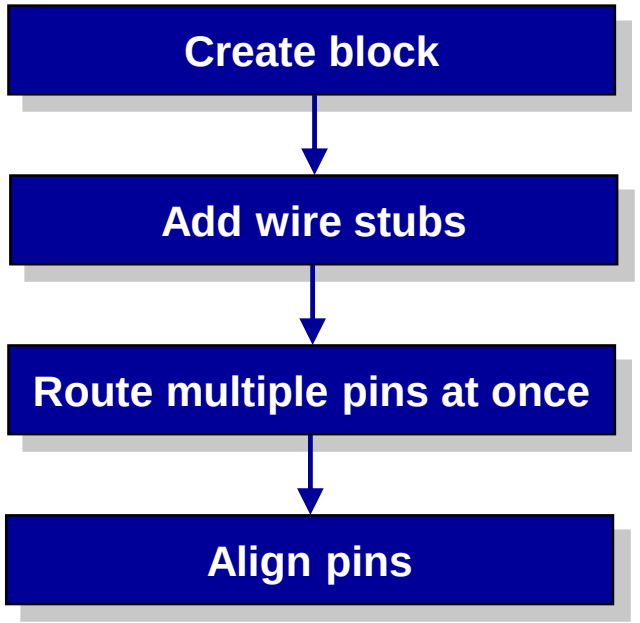
- How can I create pins on newly created block?
- Multiple Pins cannot be routed with River Route. True / False

Lab 1: Schematic Entry Using Wiring Accelerators

20 minutes

Goals:

- To understand the advanced editing functions (accelerators)



Lab 2: Controlling Port Ordering During Netlisting

20 minutes

Goals:

- To understand how to control port ordering during netlisting