

Custom Compiler

Schematic Editor (SE)

Symbol Creation

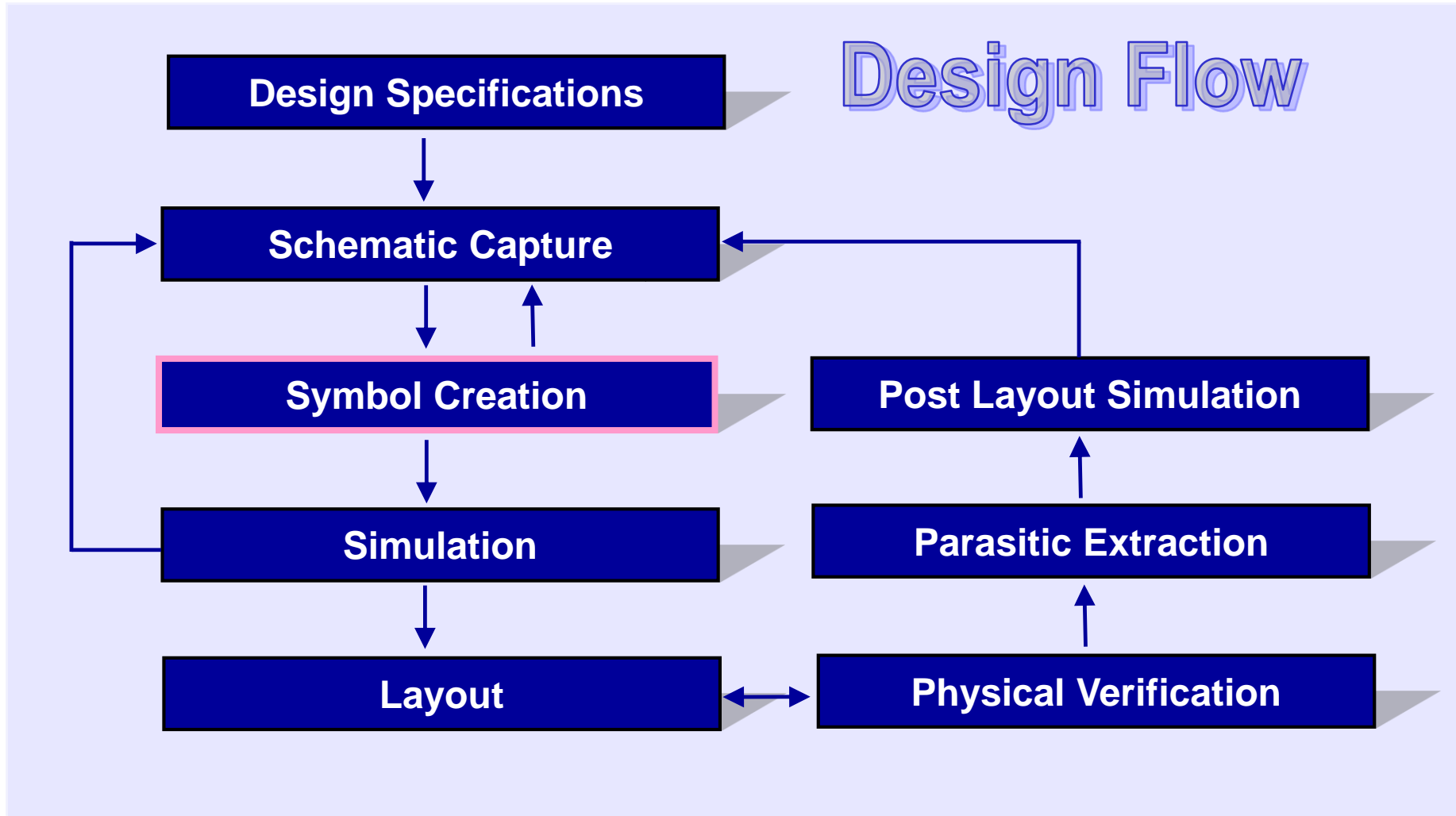
O-2018.09

Unit Objectives



- **After completing this unit, you should be able to**
 - Understand the symbol generation flow
 - Create and Edit the symbol
 - Understand labels around the symbol
 - Add selection shape
 - Check the symbol
 - Save the symbol

Full Custom Compiler Flow



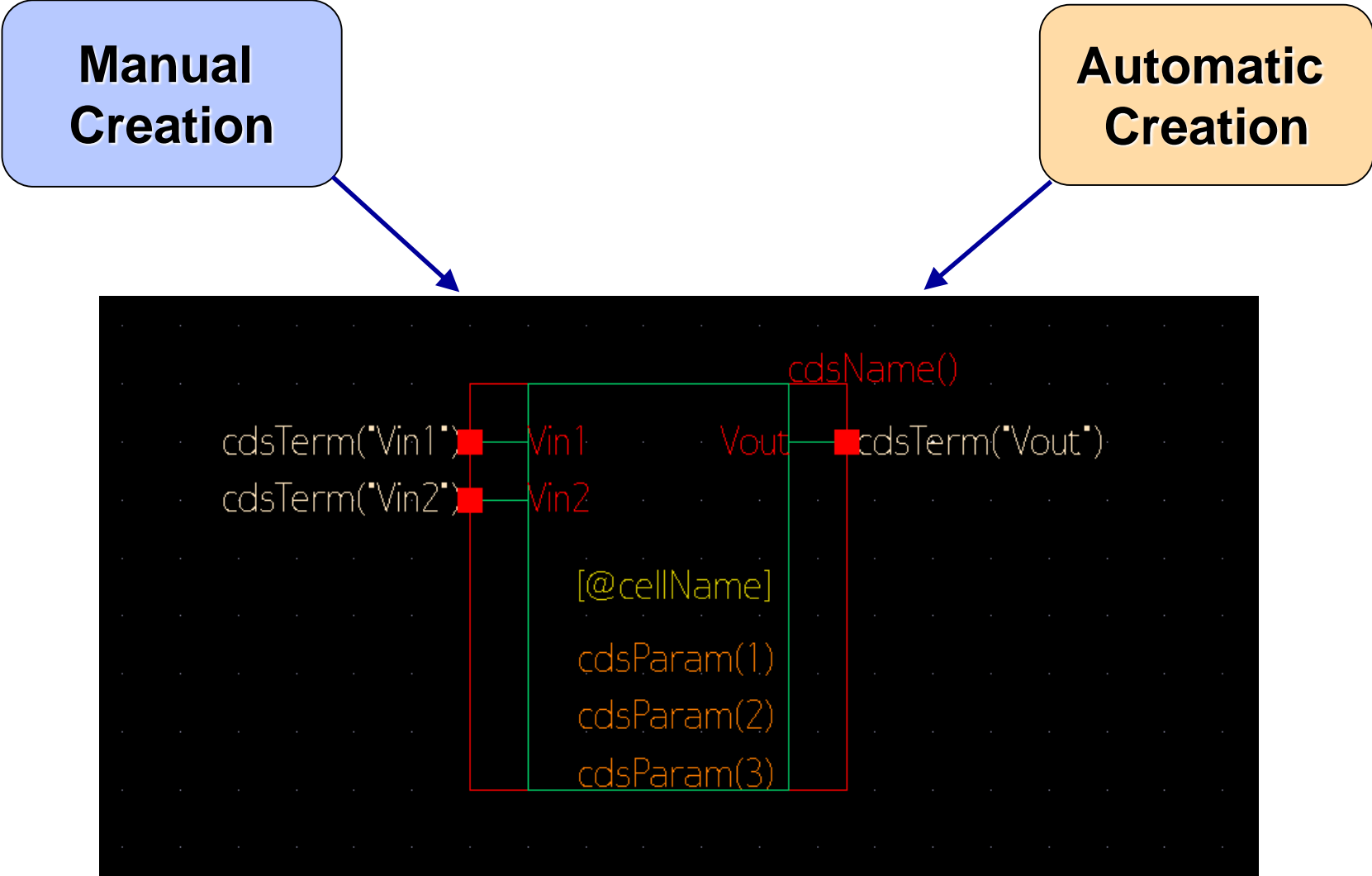
Symbol and its Importance

- A symbol is a graphical representation of a hierarchical design.
- It has properties that describe characteristics of a model or schematic it represents.
- Useful for creating designs where it is impractical to show every transistor on the top level schematic
- Useful for creating test benches

Symbol Generation

Manual
Creation

Automatic
Creation

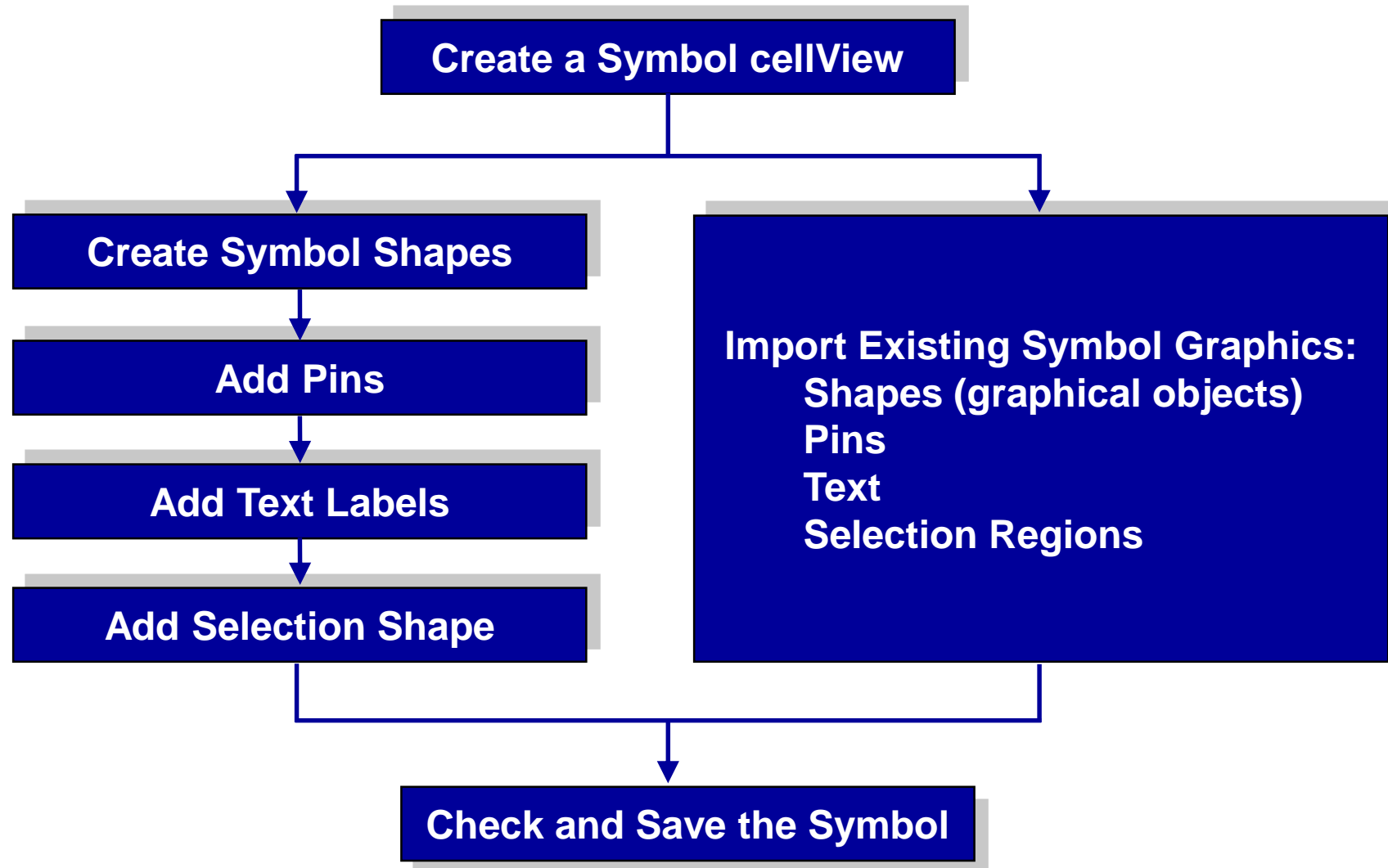


The diagram illustrates two methods of symbol generation: Manual Creation and Automatic Creation. Both methods lead to a central code block. The code block contains the following text:

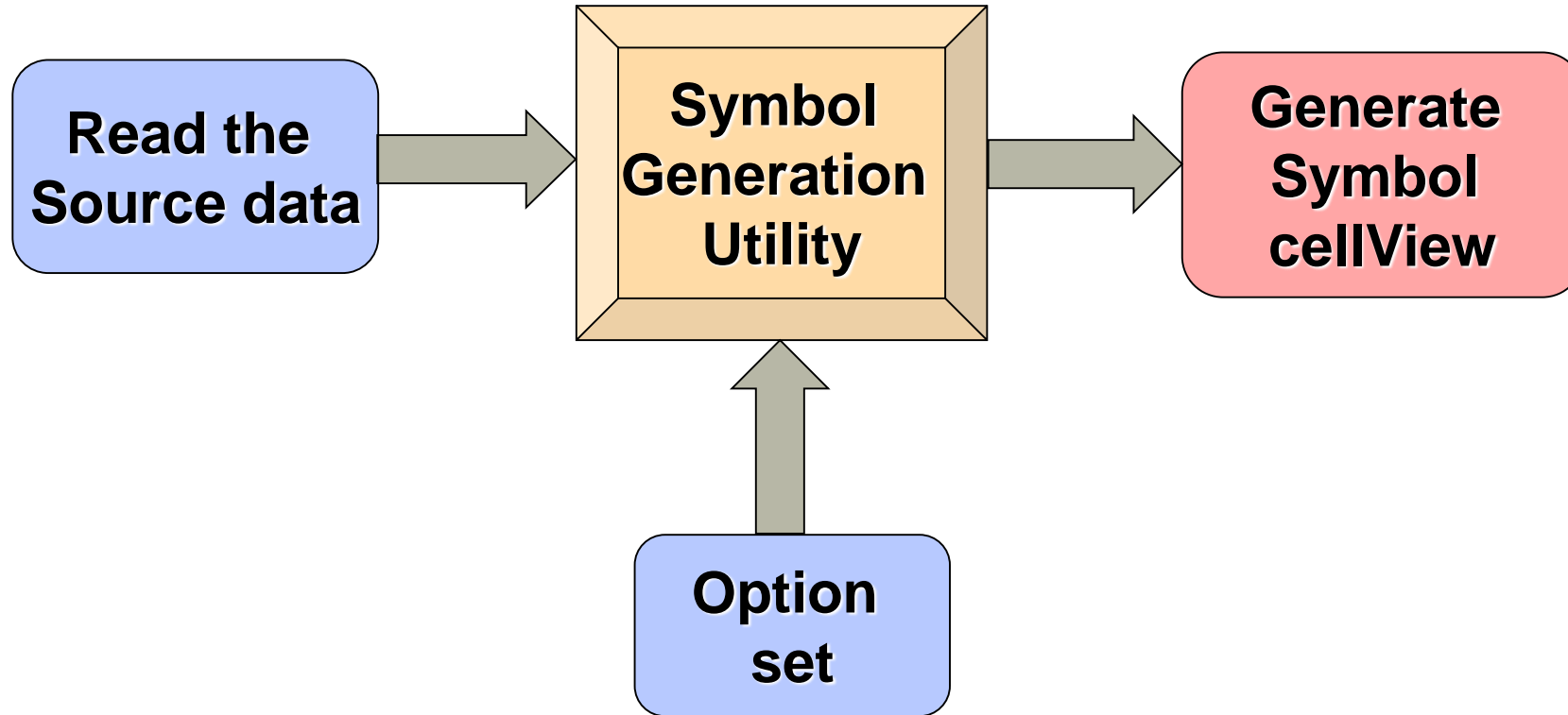
```
cdsTerm("Vin1")■ Vin1      Vout ■ cdsTerm("Vout")  
cdsTerm("Vin2")■ Vin2  
[ @cellName ]  
cdsParam(1)  
cdsParam(2)  
cdsParam(3)
```

The code is displayed on a black background with a grid of small dots. The text is color-coded: "cdsTerm" and "cdsParam" are in yellow, "Vin1", "Vin2", and "Vout" are in red, and "[@cellName]" is in green. There are red squares between "cdsTerm" and the variable names, and a green square between "cdsTerm" and "Vout". A green box highlights the parameter list section, and a red box highlights the entire code block.

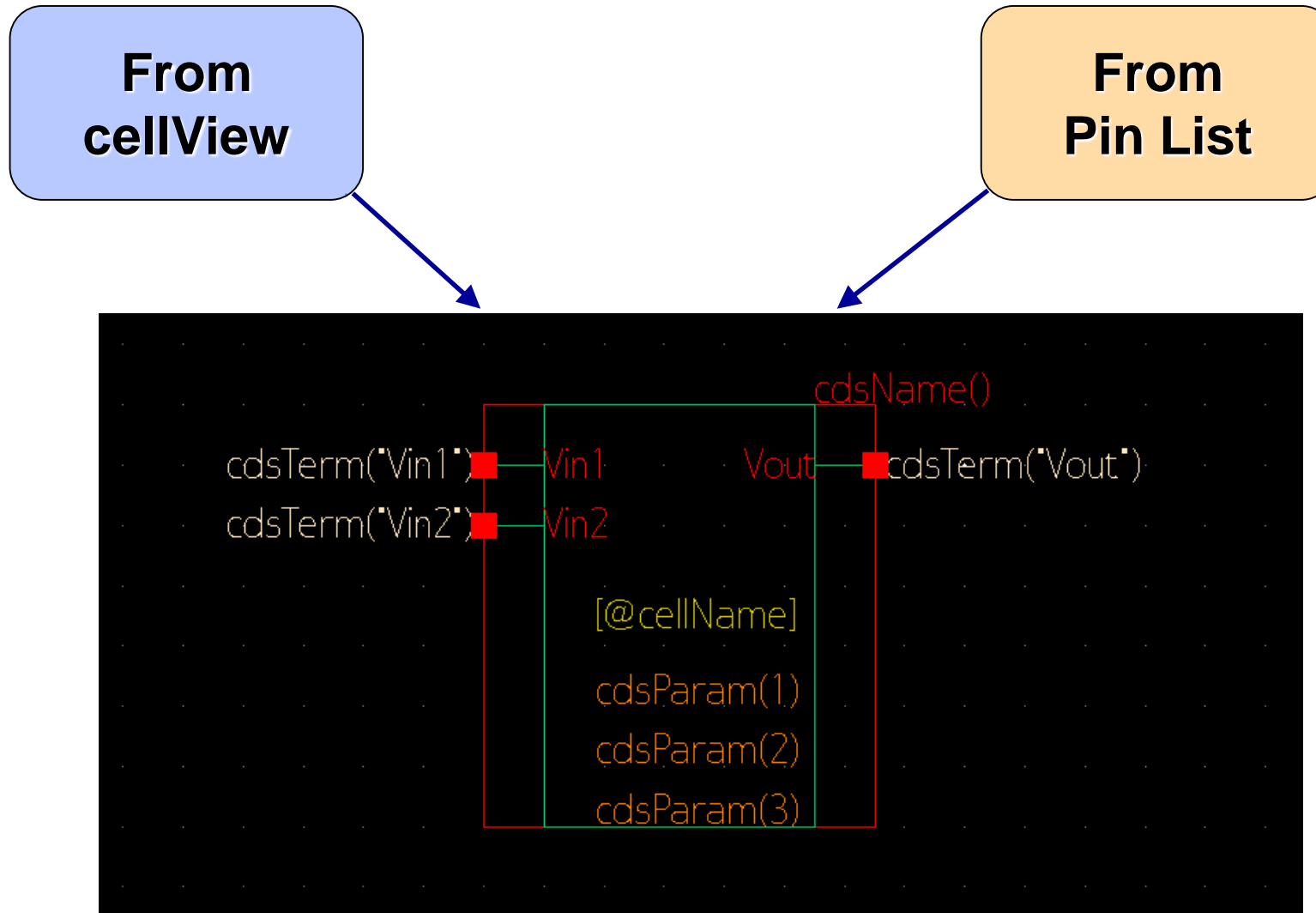
Manual Symbol Generation Flow



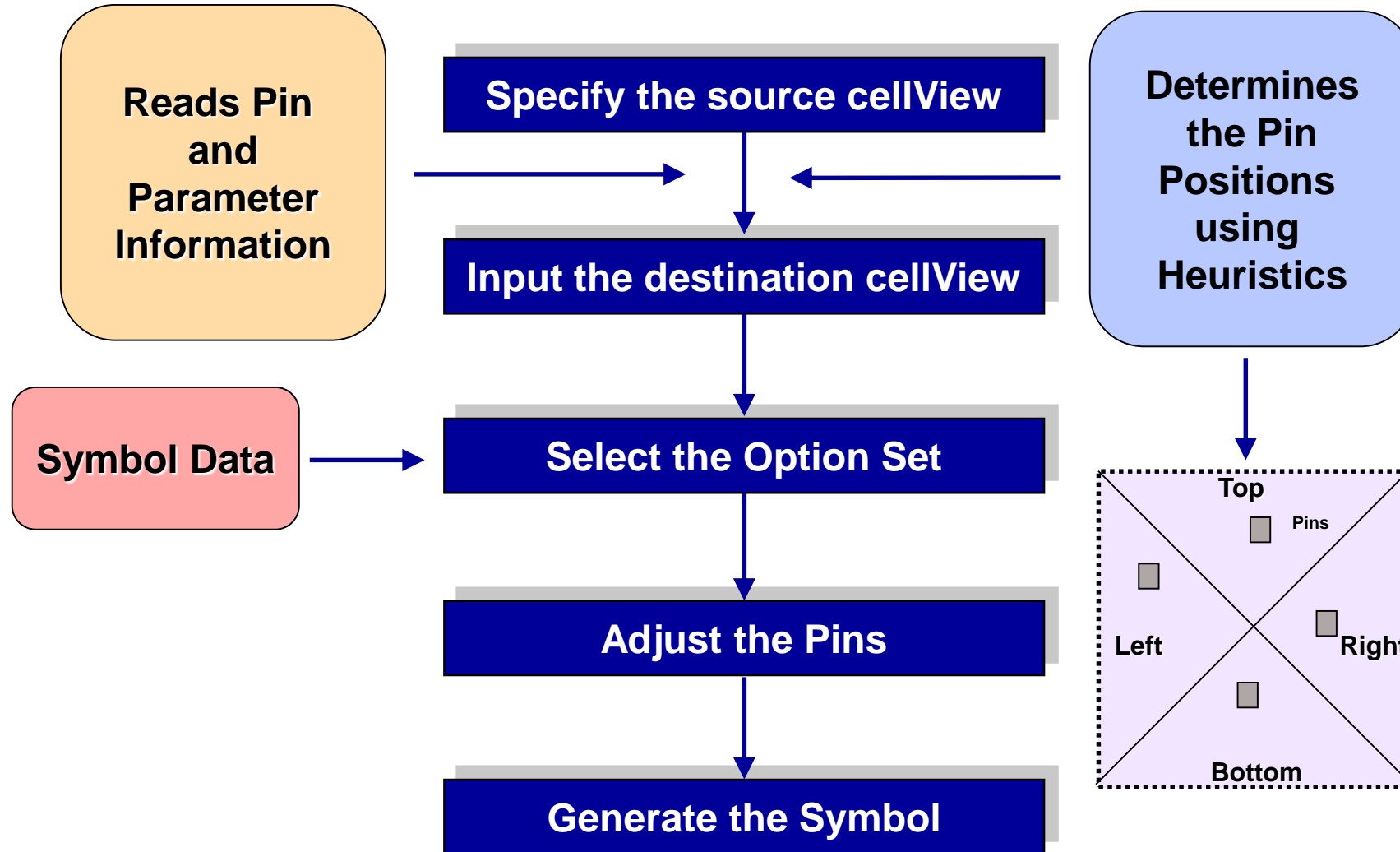
Automatic Symbol Generation Flow



Automatic Symbol Generation

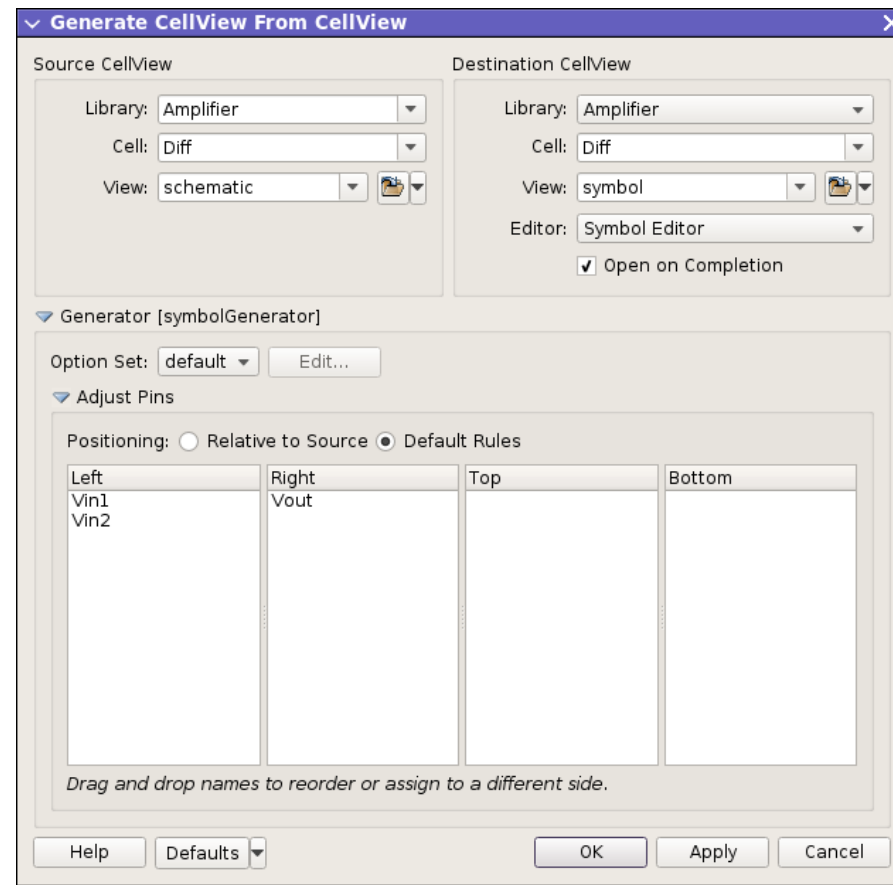


Symbol Generation from CellView

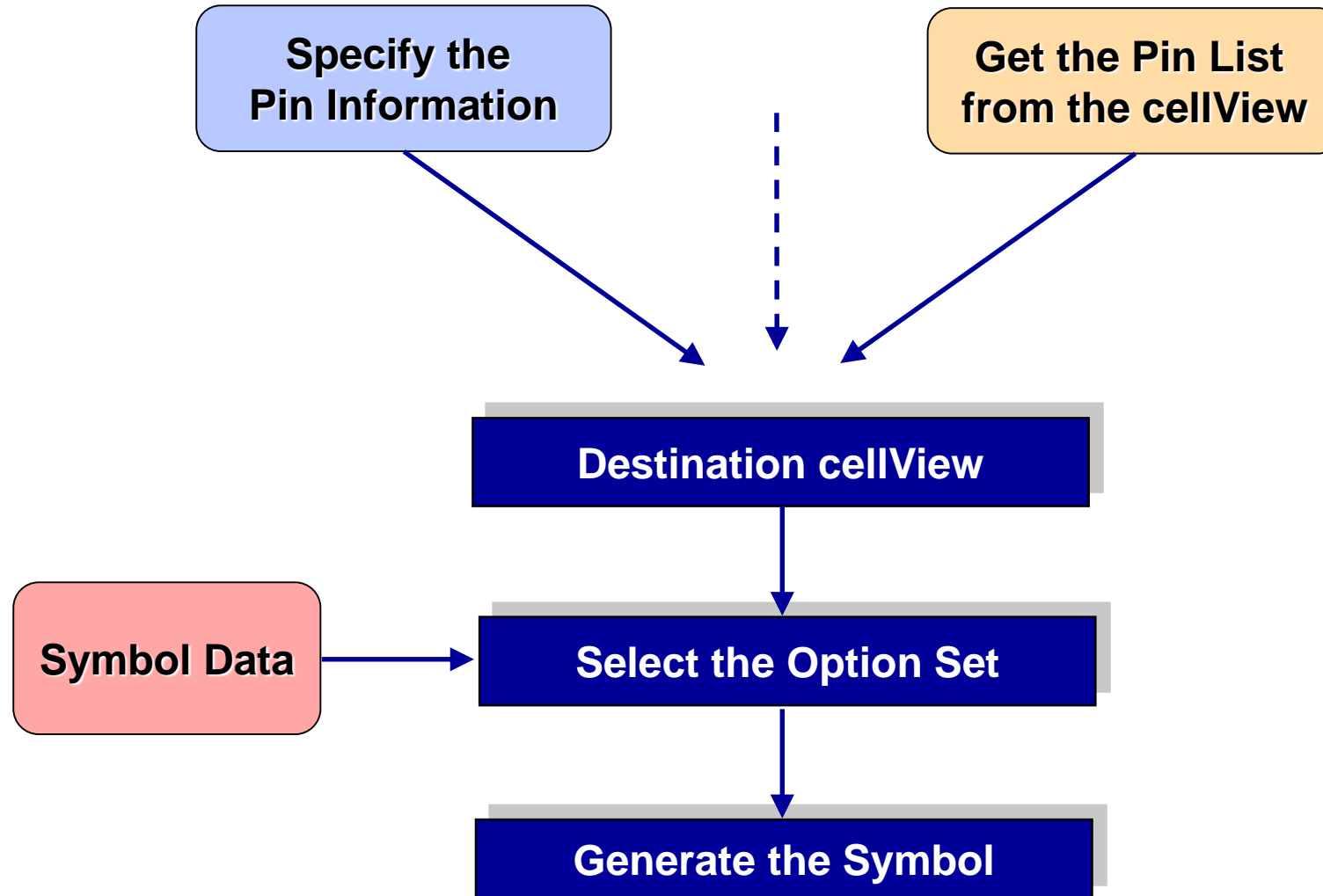


Symbol Generation from CellView User Interface

- Invoke from Design → New CellView → From CellView

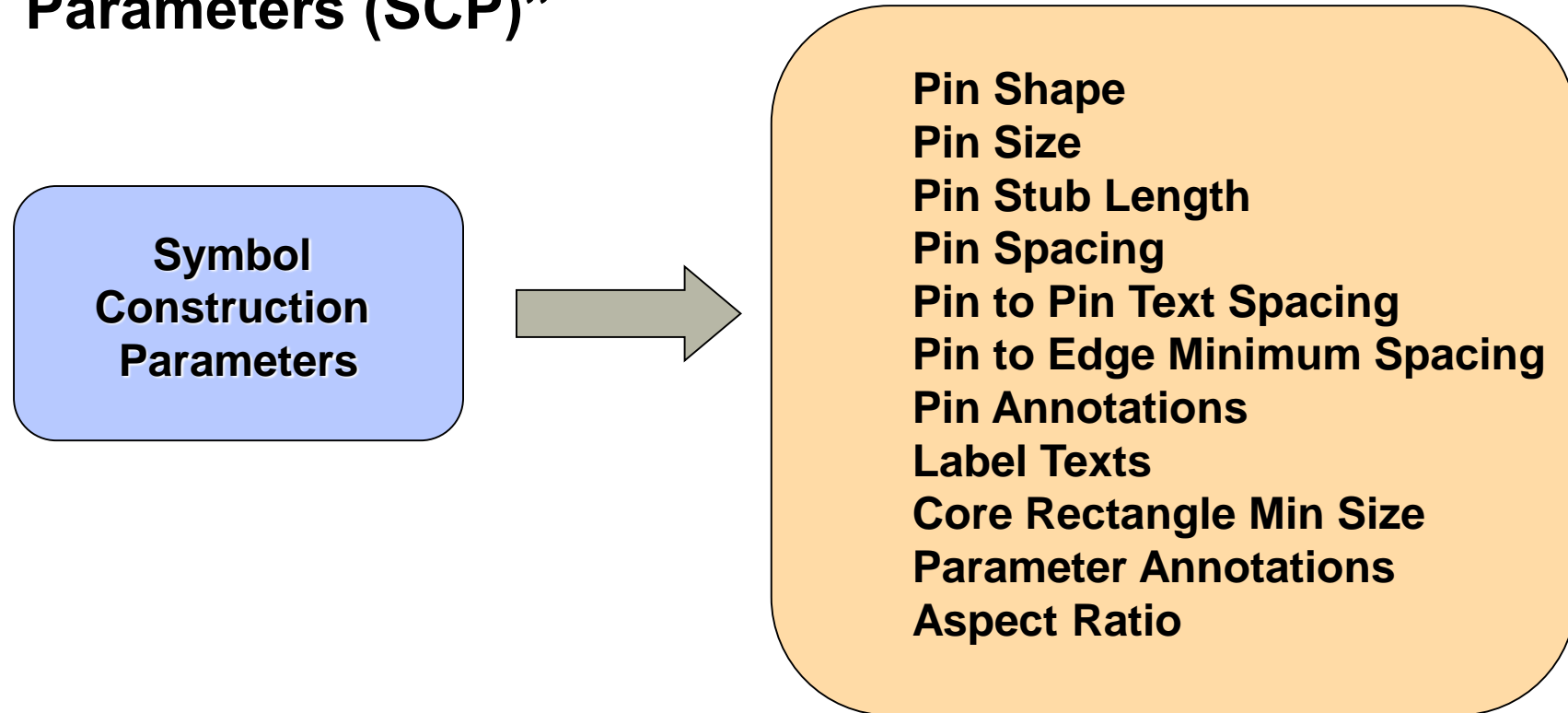


Symbol Generation from Pin List

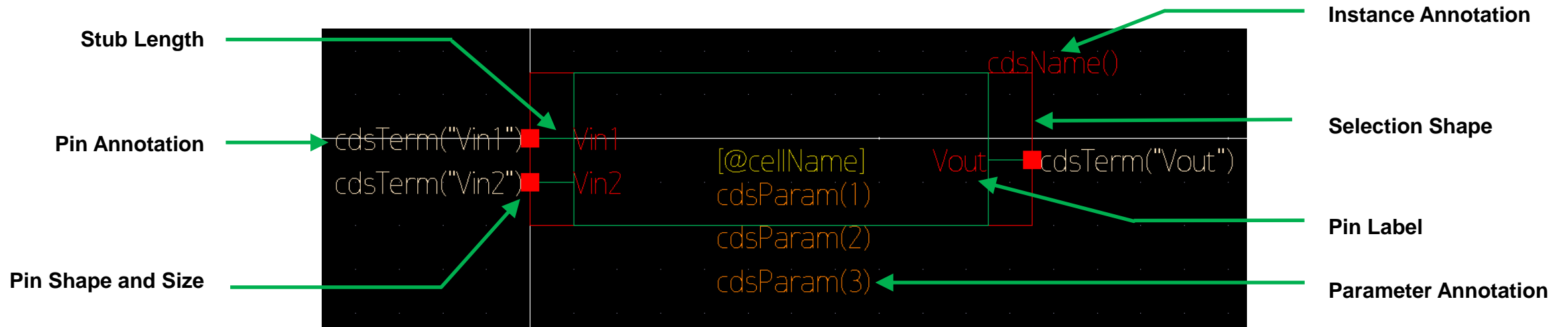


Option Set

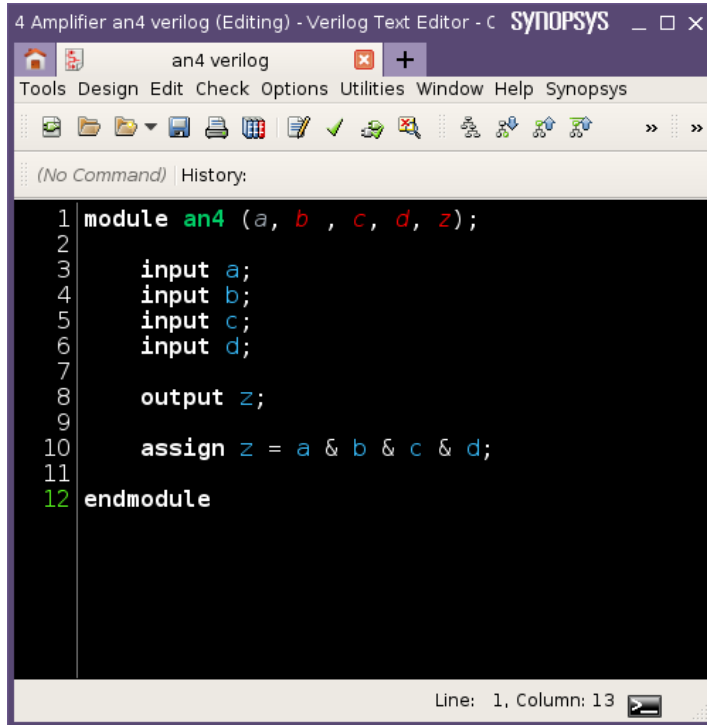
- Contains the list of symbol data available for user control.
- Construction of the symbol data is controlled by a list of settings called “Symbol Construction Parameters (SCP)”



Generated Symbol View

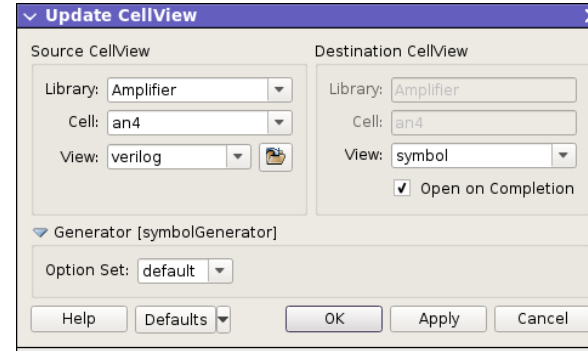


Update Symbol View



```
1 module an4 (a, b, c, d, z);  
2  
3     input a;  
4     input b;  
5     input c;  
6     input d;  
7  
8     output z;  
9  
10    assign z = a & b & c & d;  
11  
12 endmodule
```

Line: 1, Column: 13

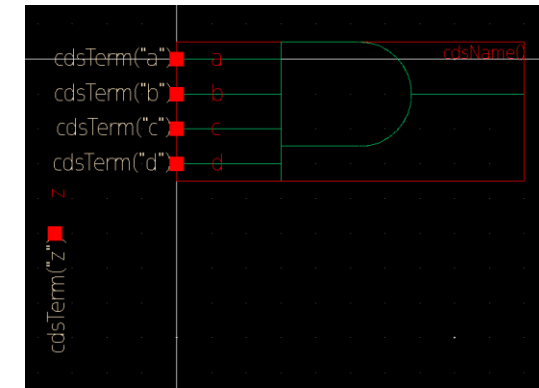
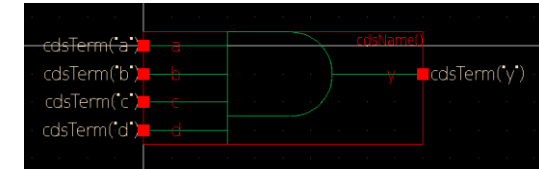


Update CellView

Source CellView	Destination CellView
Library: Amplifier	Library: Amplifier
Cell: an4	Cell: an4
View: verilog	View: symbol
<input checked="" type="checkbox"/> Open on Completion	

Generator [symbolGenerator]
Option Set: default

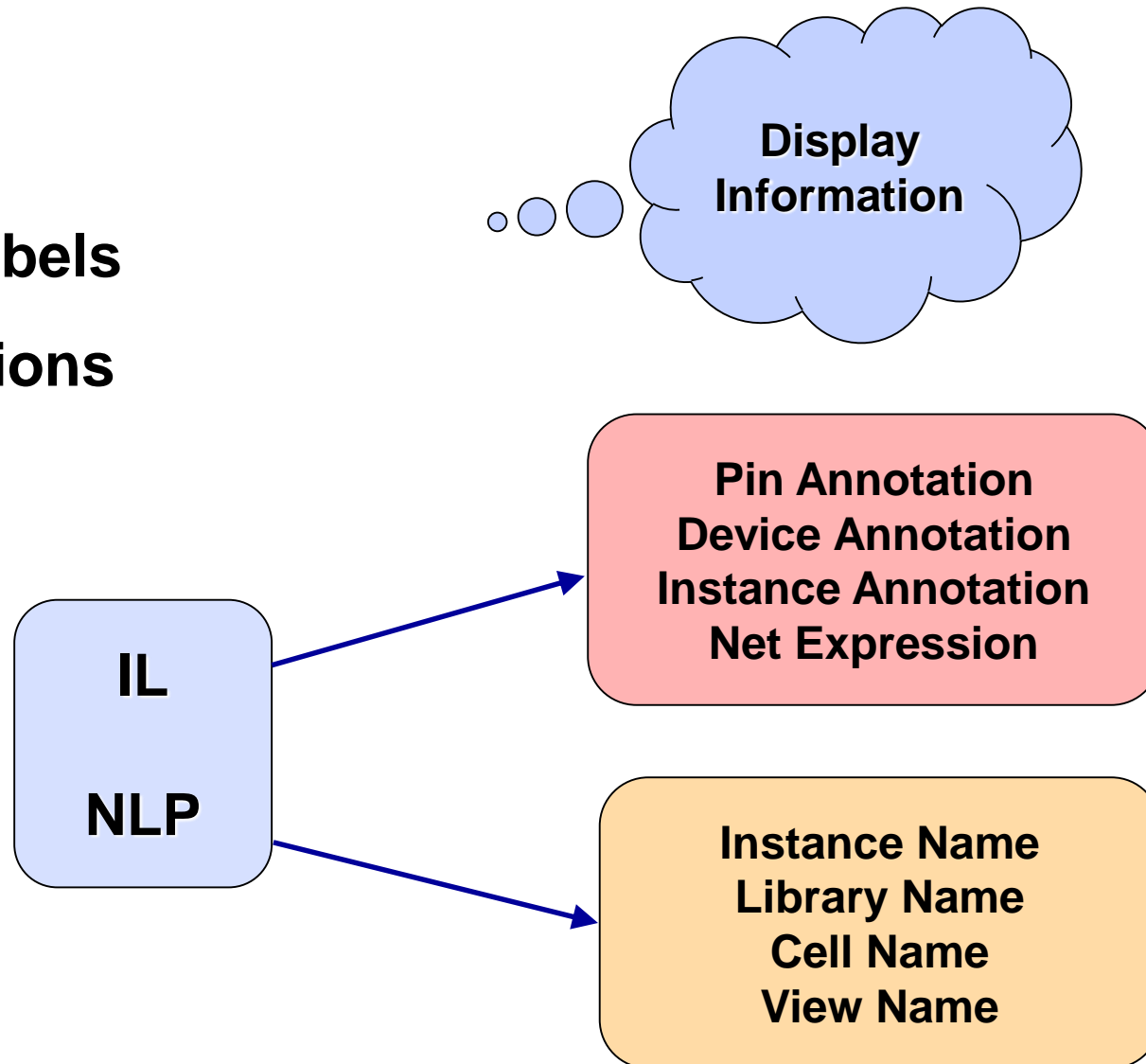
Buttons: Help, Defaults, OK, Apply, Cancel



- Deleted pins are removed
- New pins are placed at the bottom of the symbol

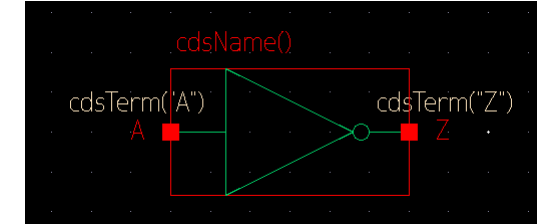
Labels

- Static labels
- Interpreted labels
- NLP Expressions



Device Label Editor Assistant

- Select interpretation of IL labels
 - Instance
 - Master
 - Library
 - Design
- Select interpretation scope
 - Instance
 - Master
 - Library
 - Design



`cdsName()` →
`cdsTerm("T")` →

Device Label Editor (10)

Current instance: I16

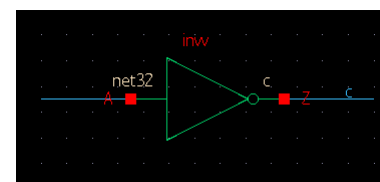
Attributes

Label	Value
Name	cell
Terminals	term

Parameters

Use Defaults: ☐ parameter

Value	Type	Visibility
	default	
	default	
	default	



Device Label Editor (10)

Current instance: I16

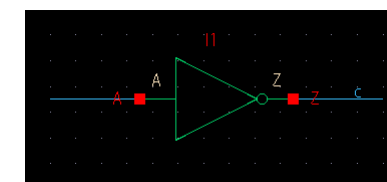
Attributes

Label	Value
Name	inst
Terminals	term

Parameters

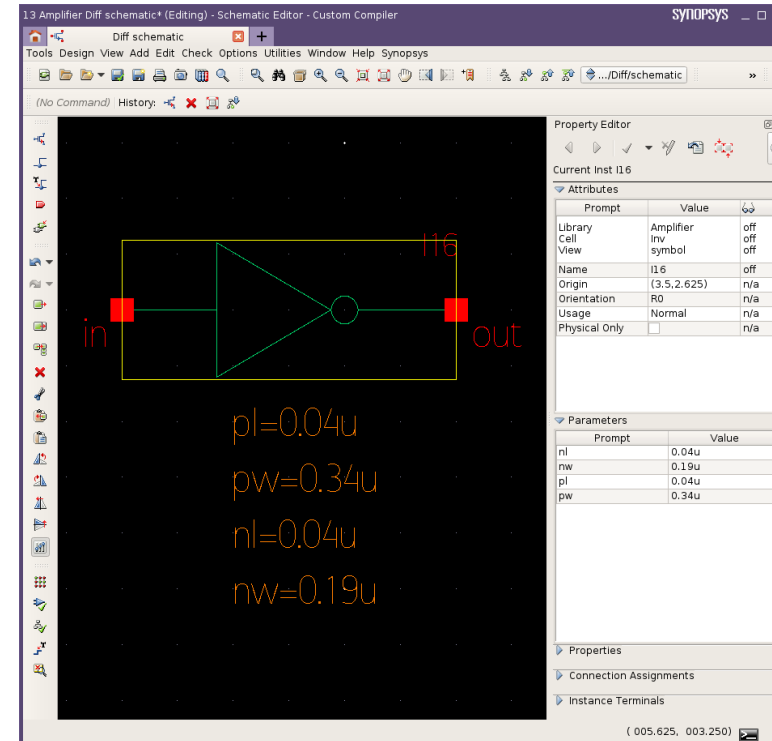
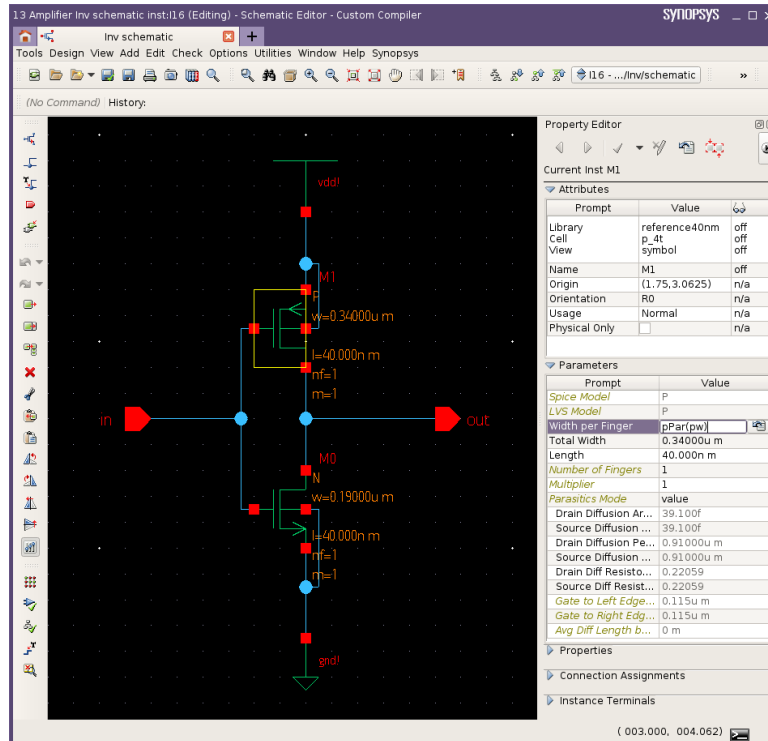
Use Defaults: ☐ parameter

Value	Type	Visibility
	default	
	default	
	default	



Passing Parameters Through Symbol

- Pass parameters to lower level circuitry
- Enables reuse of same circuit with different parameter values
- Use pPar(<parameter name>) as values of device parameters





- What is the necessary and sufficient information to create the symbol ?
- Labels are used to display _____
- Choose the correct statements:
 - Symbols are used to create hierarchical designs.
 - Heuristics are used to identify the pin size.
 - The option set contains the list of symbol data.
 - Labels are used to verify the connectivity.

Lab 1: Symbol Creation



30 minutes

Goals:

- To understand the symbol generation flow in the Custom Compiler Environment

