

Custom Compiler

Schematic Editor and Simulation Analyses Environment (SE SAE)
Utilities

O-2018.09

Unit Objectives



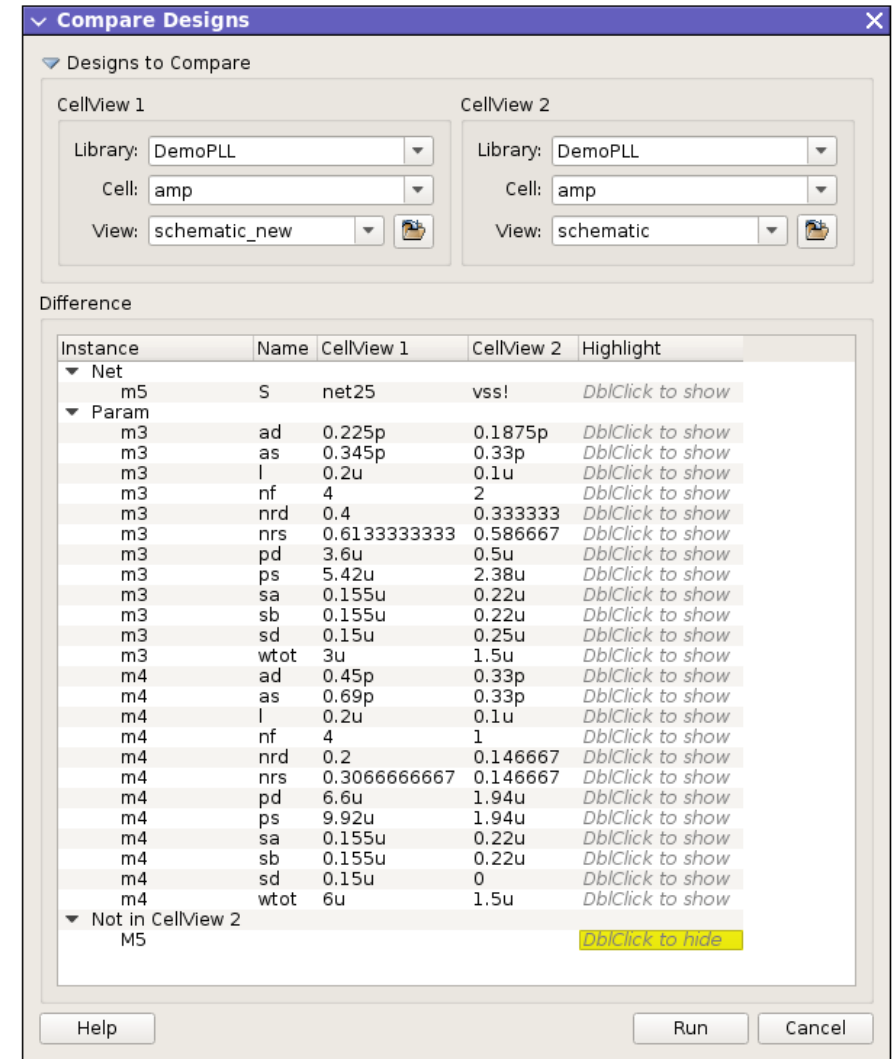
■ After completing this unit, you should be able to use:

- Compare Designs
- Power Domain Analyzer
- Net Tracer
- Constraint Editor
- Plot Signals From Simulator Output Files
- Colorize Nets
- Operating Point Report
- Timestamps Dashboard

Schematic Editor Utilities

Compare Designs

- Choose **Utilities > Compare Designs** from the **Schematic Editor** main menu bar
 - Highlight differences between any two schematic views
 - Detect mismatches for
 - ◆ instance terminal
 - ◆ Parameter
 - ◆ Instance Masters
 - Detect missing objects
 - ◆ Instance
 - ◆ Terminal
 - Display both designs in the same window



Compare Designs

■ Cross-probing with schematic

- Double-click on the row of interest to zoom to schematic view

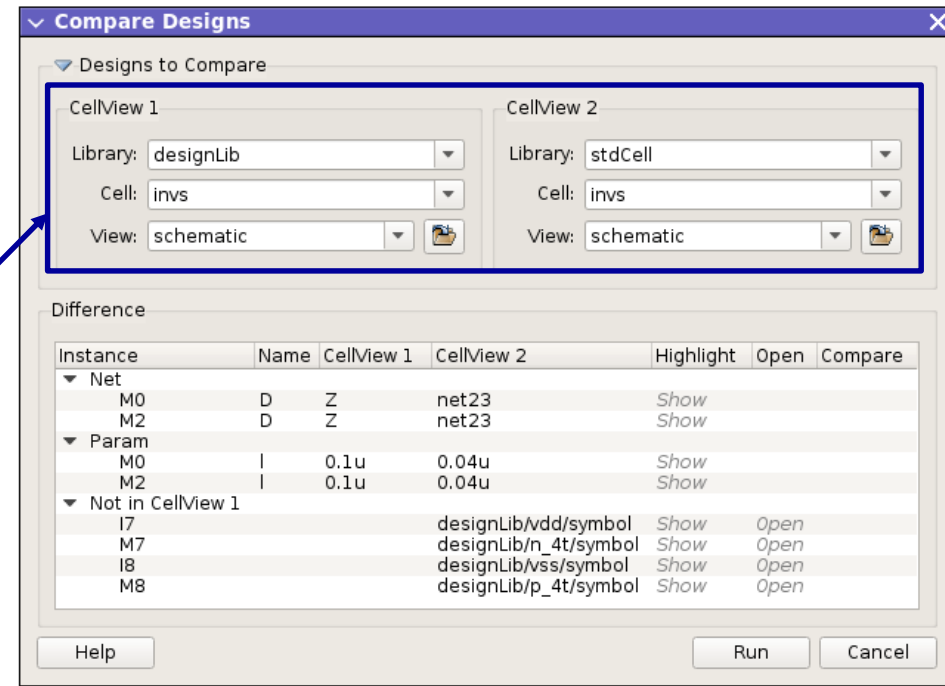
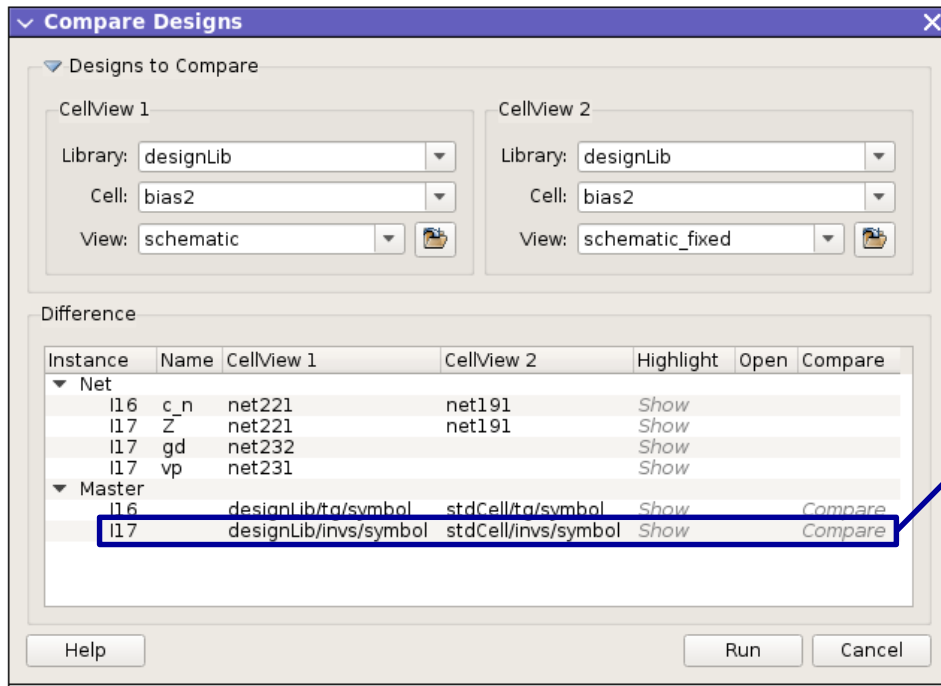
The image shows the Synopsys Compare Designs dialog box and the Schematic Editor. The dialog box is titled "Compare Designs" and has two tabs: "Designs to Compare" and "Difference". The "Designs to Compare" tab is active, showing two designs: "CellView 1" and "CellView 2". Both designs are from the "DemoPLL" library, using the "amp" cell, and are in the "schematic_new" view. The "Difference" tab shows a table of differences between the two designs.

Instance	Name	CellView 1	CellView 2	Highlight
Net				
m5	S	net25	vss!	DbClick to show
Param				
m3	ad	0.225p	0.1875p	DbClick to show
m3	as	0.345p	0.33p	DbClick to show
m3	l	0.2u	0.1u	DbClick to show
m3	nf	4	2	DbClick to show
m3	nrd	0.4	0.333333	DbClick to show
m3	nrs	0.6133333333	0.586667	DbClick to show
m3	pd	3.6u	0.5u	DbClick to show
m3	ps	5.42u	2.38u	DbClick to show
m3	sa	0.155u	0.22u	DbClick to show
m3	sb	0.155u	0.22u	DbClick to show
m3	sd	0.15u	0.25u	DbClick to show
m3	wtot	3u	1.5u	DbClick to show
m4	ad	0.45p	0.33p	DbClick to show
m4	as	0.69p	0.33p	DbClick to show
m4	l	0.2u	0.1u	DbClick to show
m4	nf	4	1	DbClick to show
m4	nrd	0.2	0.146667	DbClick to show
m4	nrs	0.3066666667	0.146667	DbClick to show
m4	pd	6.6u	1.94u	DbClick to show
m4	ps	9.92u	1.94u	DbClick to show
m4	sa	0.155u	0.22u	DbClick to show
m4	sb	0.155u	0.22u	DbClick to show
m4	sd	0.15u	0	DbClick to show
m4	wtot	6u	1.5u	DbClick to show
Not in CellView 2				
M5				DbClick to hide

The Schematic Editor shows two circuit diagrams side-by-side. The left diagram is the "amp schematic_new" and the right diagram is the "vco_tb" schematic. Both diagrams show a similar circuit structure with a differential pair of transistors. The right diagram is highlighted in yellow, indicating it is the selected design. The status bar at the bottom of the Schematic Editor shows "UPDATED 11/20/17 1" and "003.375, 001.375".

Compare Designs (O-2018.09-SP1)

- Quickly compare and see differences inside different master designs
 - Double Click on *Compare* text to compare



Power Domain Analyzer

■ Power Design Analyzer dialog

• Nets

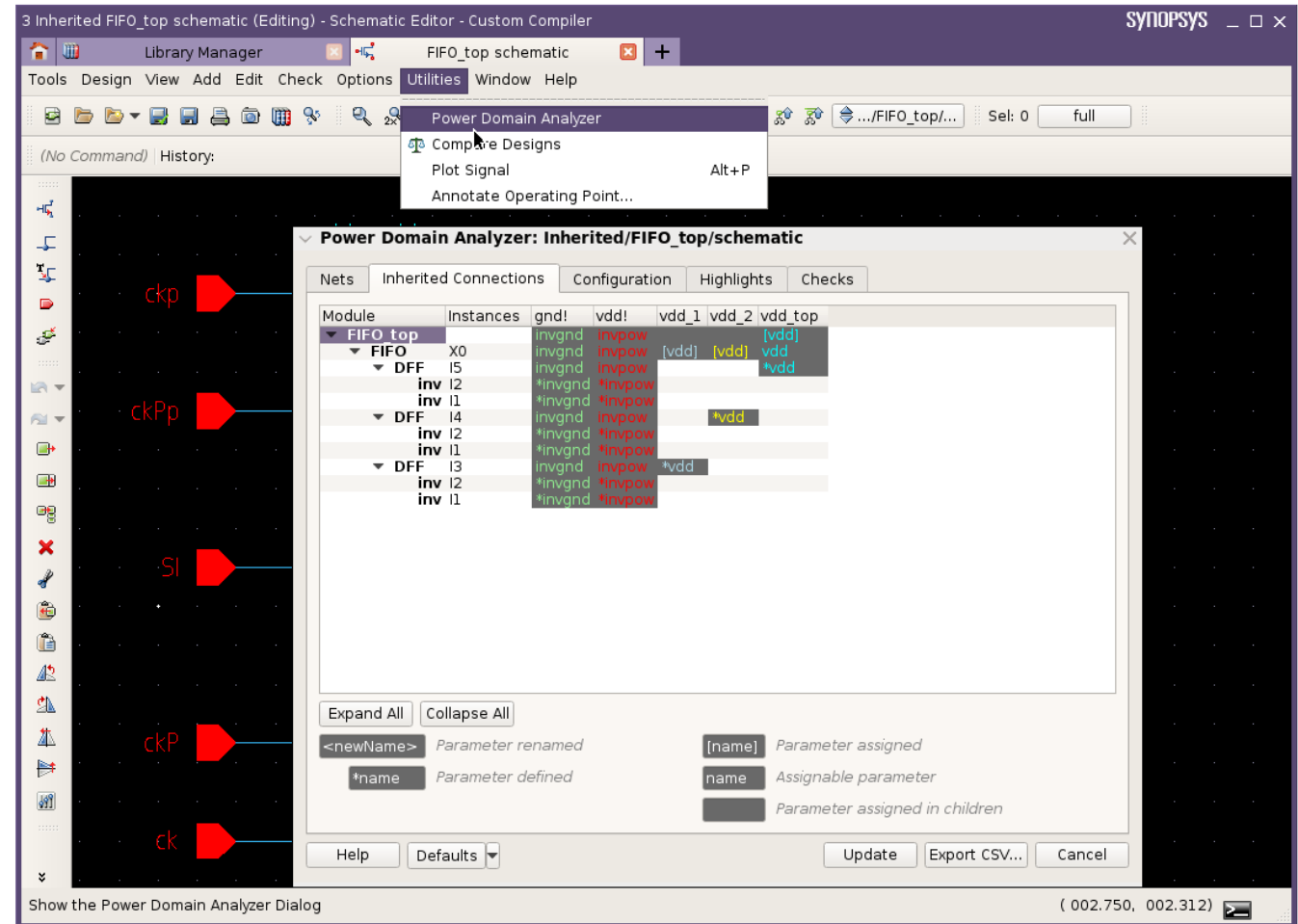
- ◆ Power domain nets through design hierarchy
- ◆ User defined nets (clock, reset, etc.)
- ◆ Modules using Power/Ground nets
- ◆ Instances using Power/Ground nets

• Inherited Connections

- ◆ NetSet assignments
- ◆ Connection Definition assignments

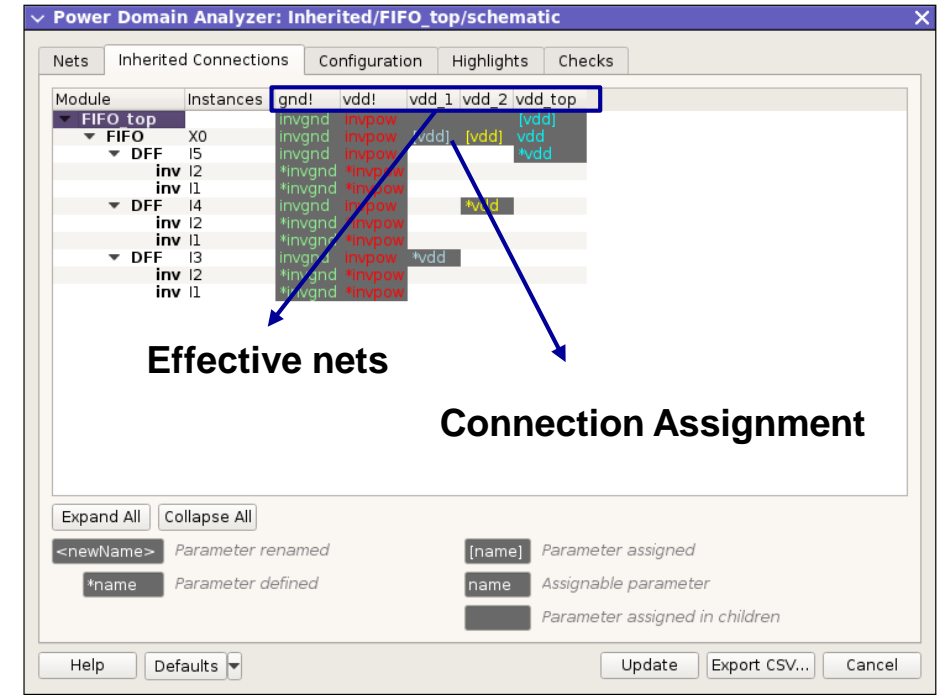
• Configuration

- ◆ Viewer related settings



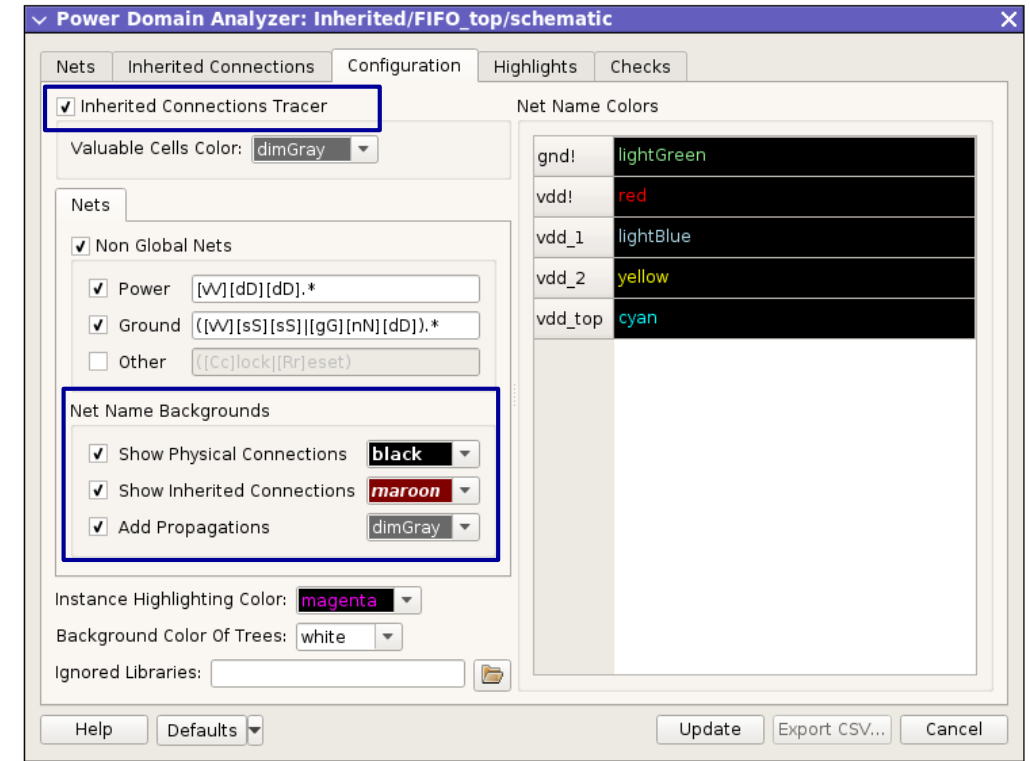
Power Domain Analyzer

- **Inherited Connections tab like Nets tab shows**
 - **Modules:** shows design folded modules
 - **Instances:** shows instances of corresponding module instantiations in the parent design
 - **Effective Nets:** shows effective nets as column headers, which is connected using connection definitions listed in that particular column
- **Is available only if Inherited Connections Tracer check box is set in Configuration tab**



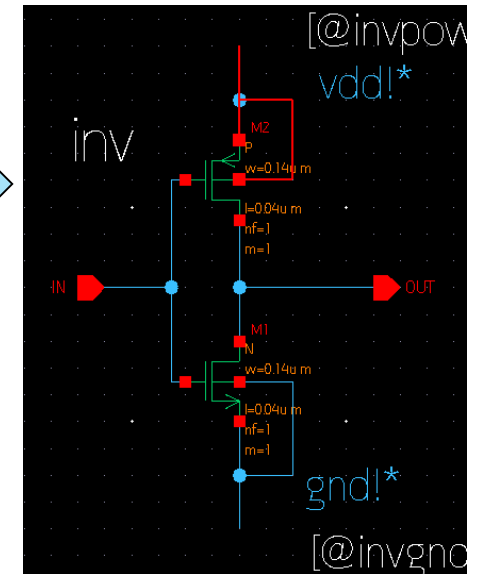
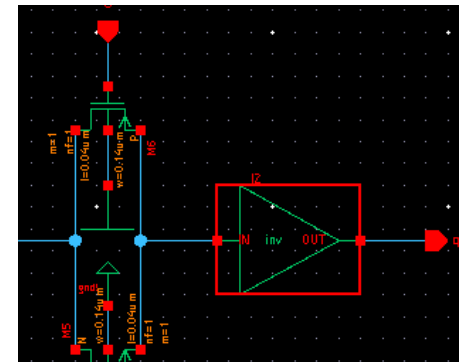
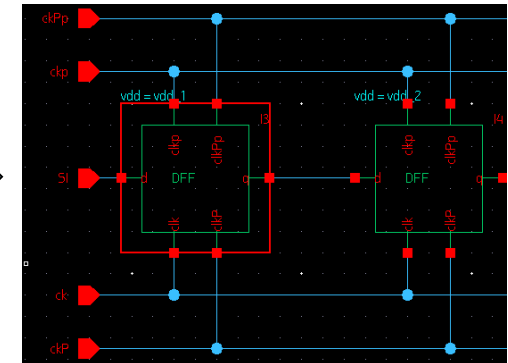
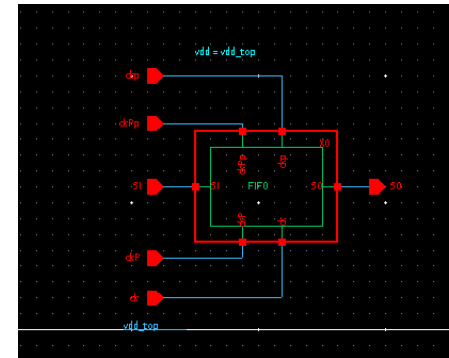
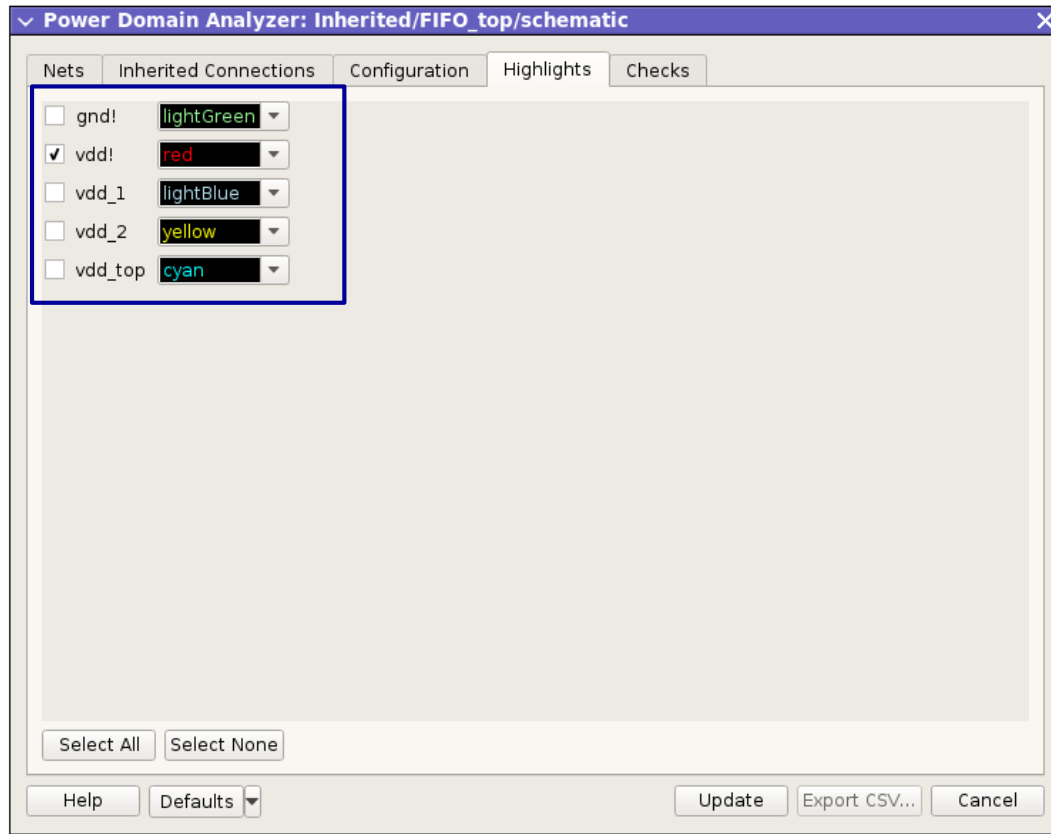
Power Domain Analyzer

- Is available only if Inherited Connections Tracer check box is set in Configuration tab
- Different Backgrounds for Nets with
 - Physical Connections
 - Inherited Connections
 - Propagations through design hierarchy
- Ignored Libraries
 - List of libraries from which the cells will not be processed, together with their entire lower hierarchy



Power Domain Analyzer

■ Highlight nets through hierarchy



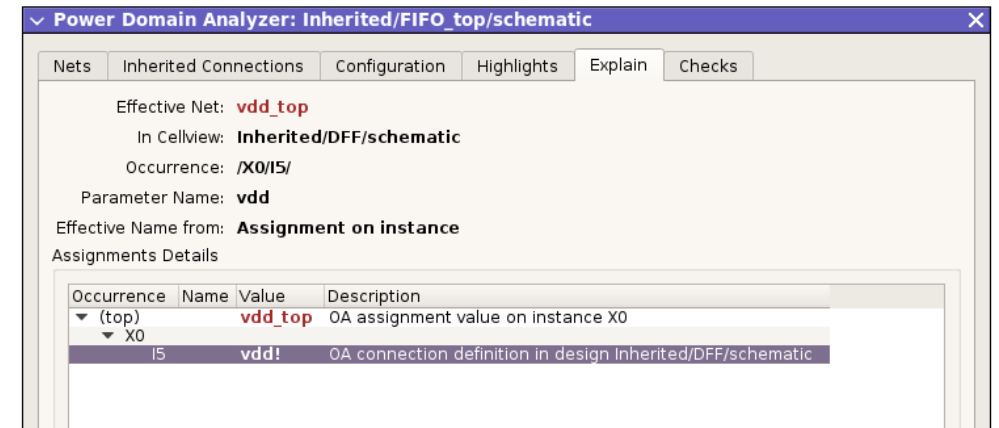
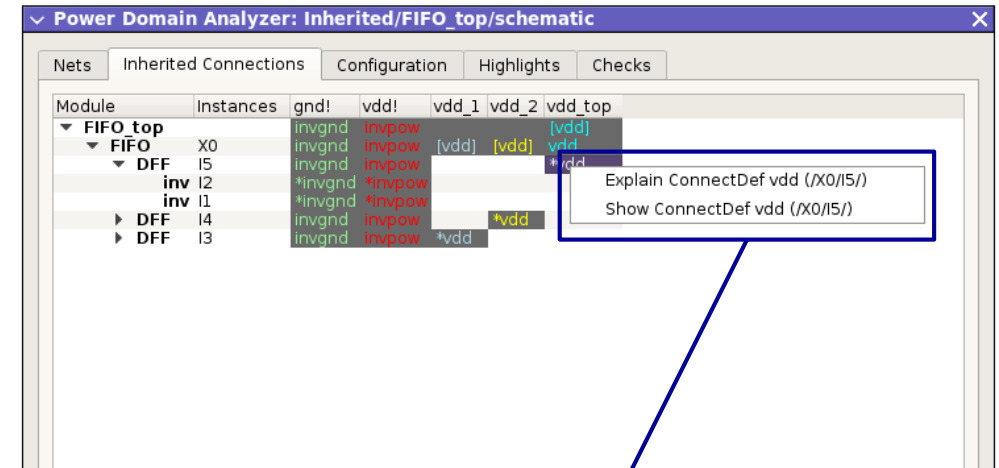
Power Domain Analyzer

■ Explain Connection

- Describes all the details of the connection (effective net name calculation) for the selected connection definition in the Inherited Connection results table

■ Assignments Details table

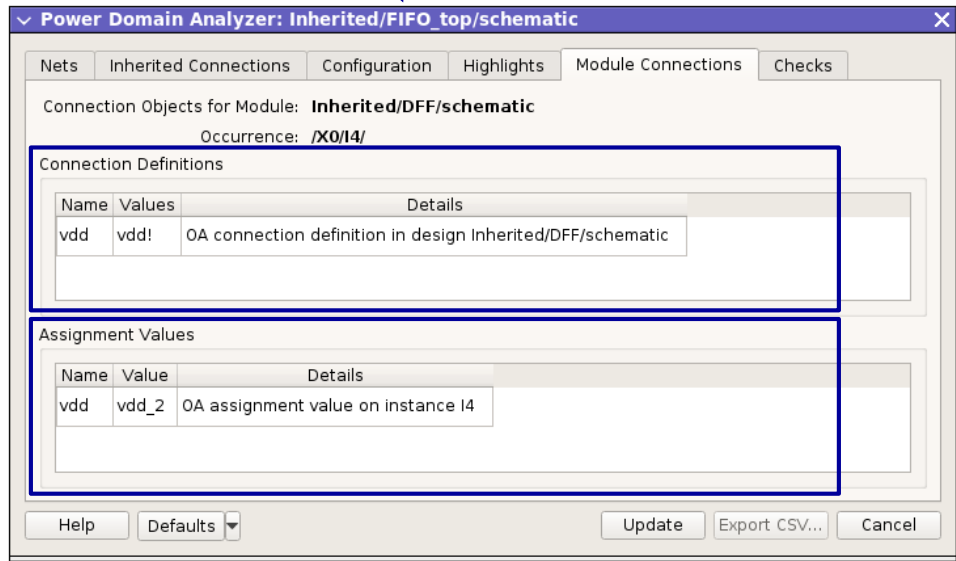
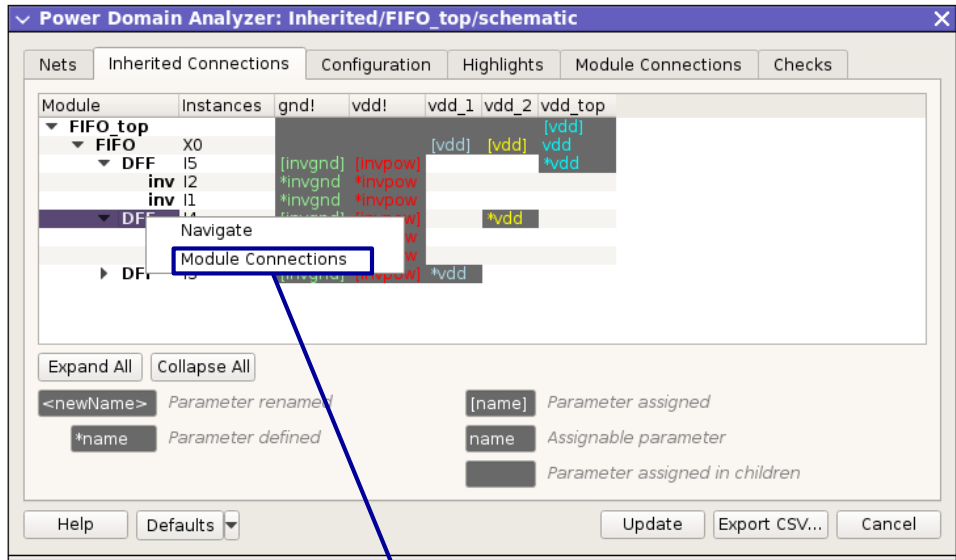
- Shows assignments and assignments throughout the hierarchy for given connection definition



Power Domain Analyzer

■ Module Connections tab

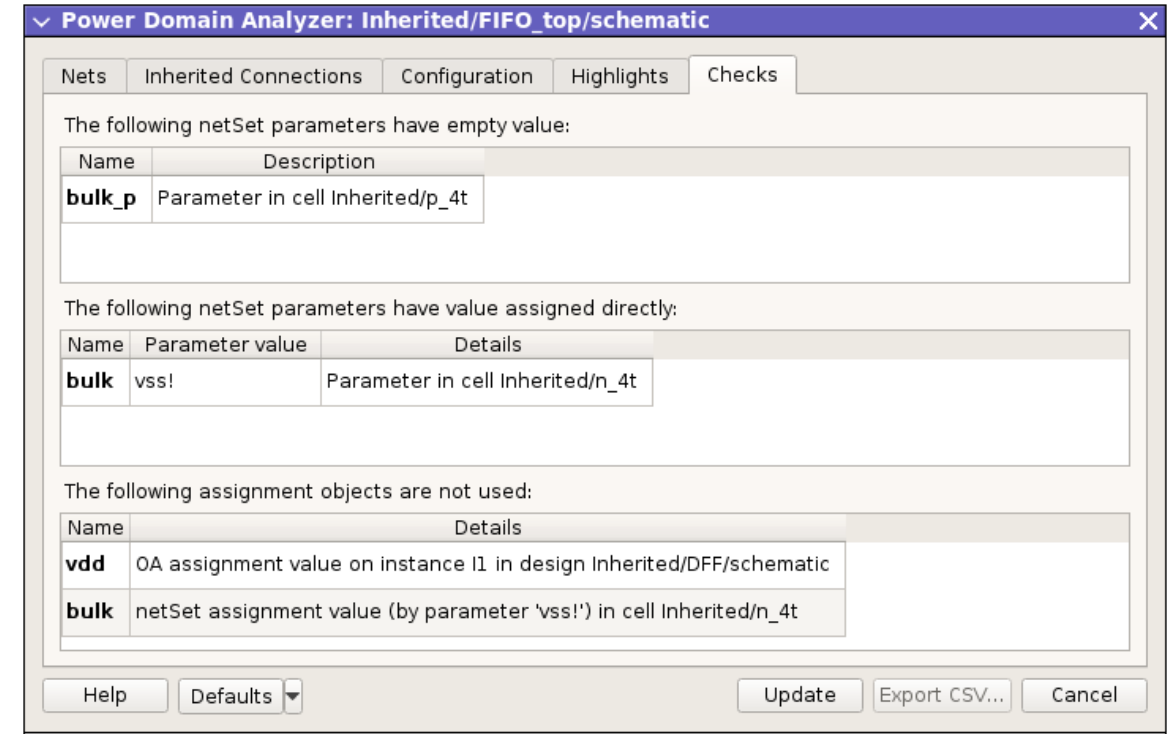
- Gets opened from appropriate module's CSM selected
- Lists the connection definitions defined in the module
- Shows assignment values related to this module through the hierarchy
 - ◆ Details highlights assignment type (assign value or assign-assignment)



Power Domain Analyzer

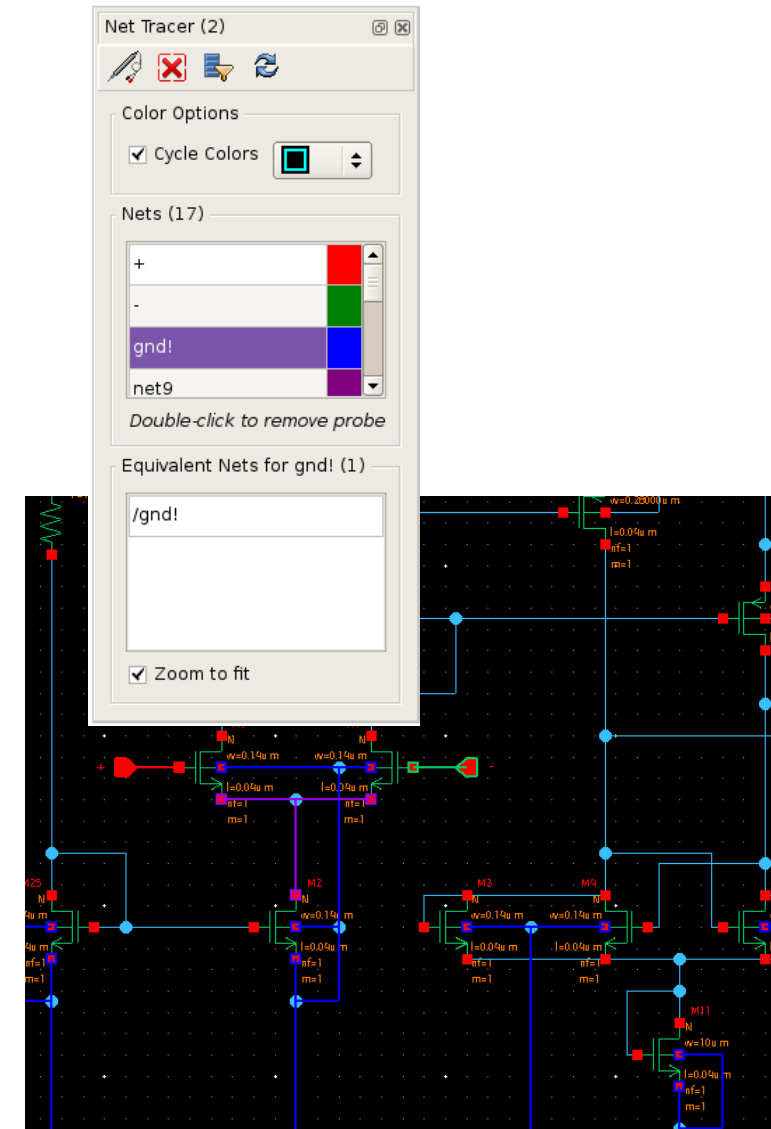
■ Checks tab

- Shows connection definition violations in the design hierarchy
- Includes violations for
 - ◆ NetSet parameters with empty value
 - ◆ NetSet parameters with direct assignments
 - ◆ Unused assignment objects



Net Tracer

- Can be used for interactive probing of nets throughout the design hierarchy
- Net is highlight with the same color across hierarchy
 - Multiple nets can be highlighted with different colors
- Nets section lists the nets found in the current edit design
- Equivalent Nets section lists the hierarchical electrically equivalent nets for currently selected net in Nets section
- Zoom to fit equivalent nets at any level in hierarchy



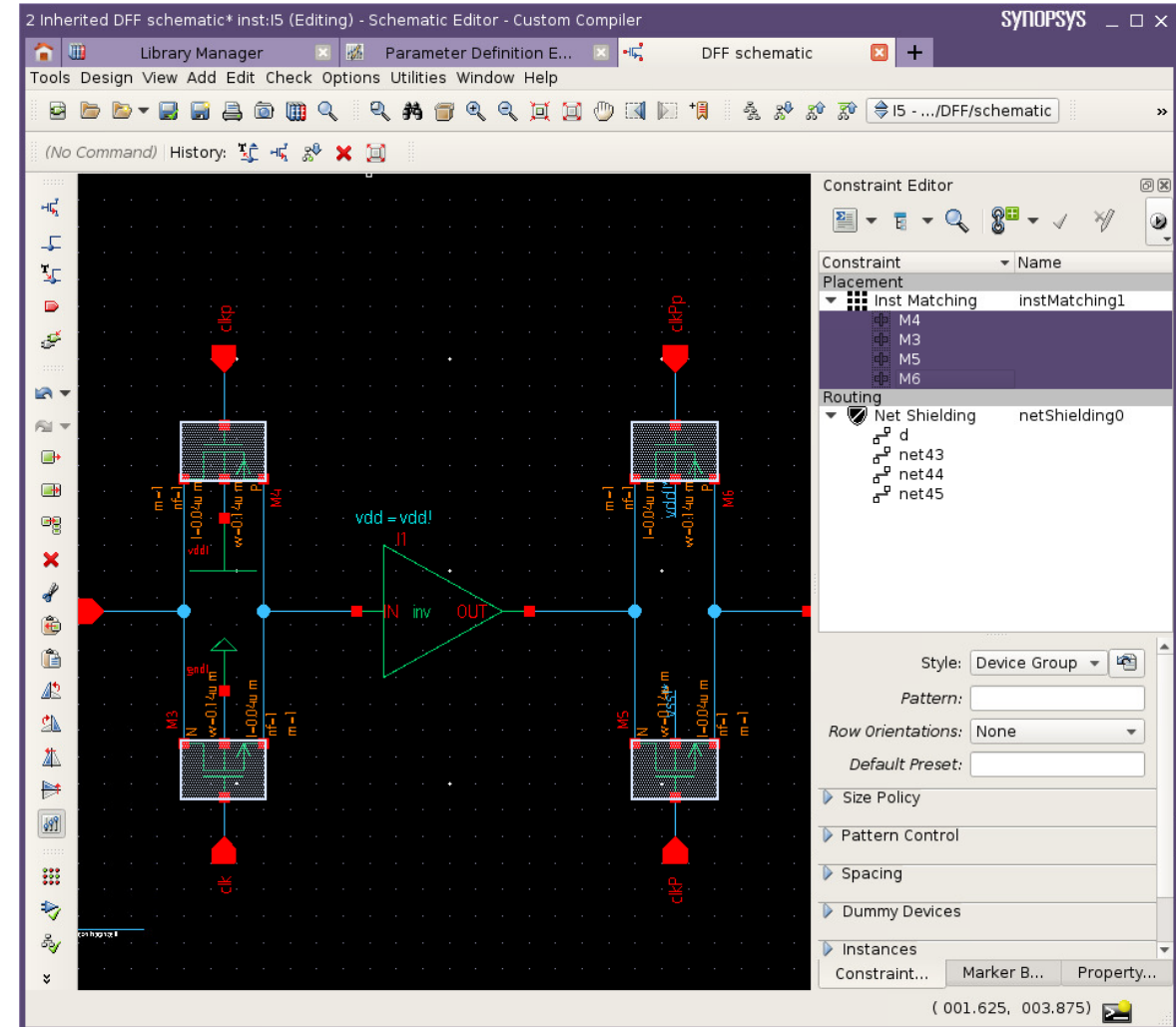
Constraint Editor

- Choose **Window > Assistants > Constraint Editor** from the Schematic Editor main menu bar

- Placement Constraints
 - ◆ CMOS
 - ◆ Inst Matching
- Routing Constraints
 - ◆ Color Matching
 - ◆ Net Shielding

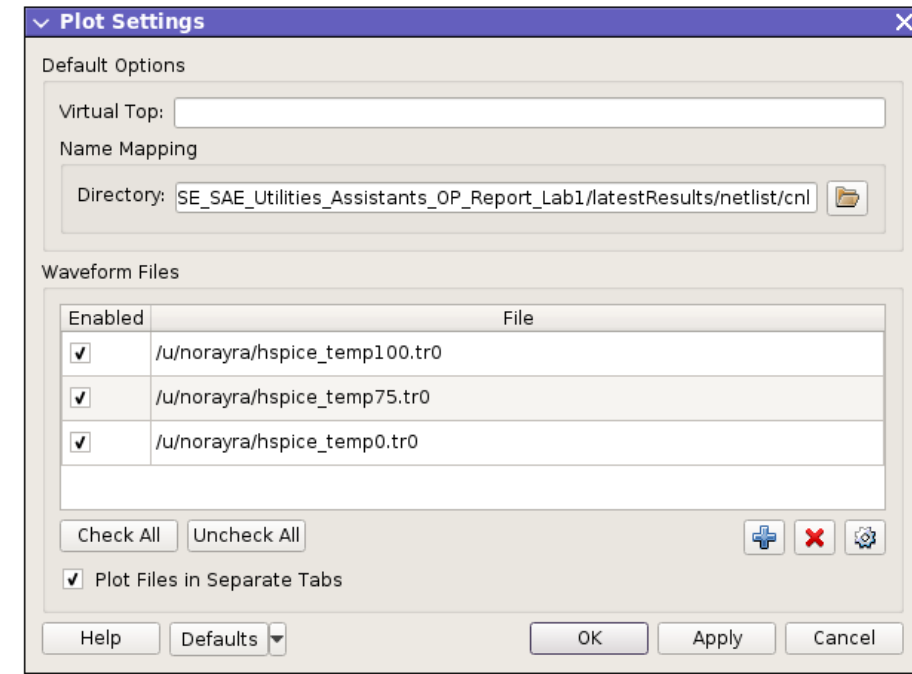
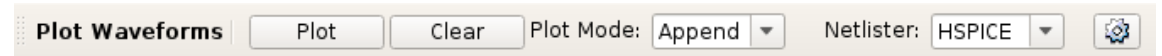
- Create, delete, modify and highlight constraints in Schematic Editor Windows

- Constrains get transferred to layout through SDL
- Layout constrains get updated automatically during SDL initialization if necessary



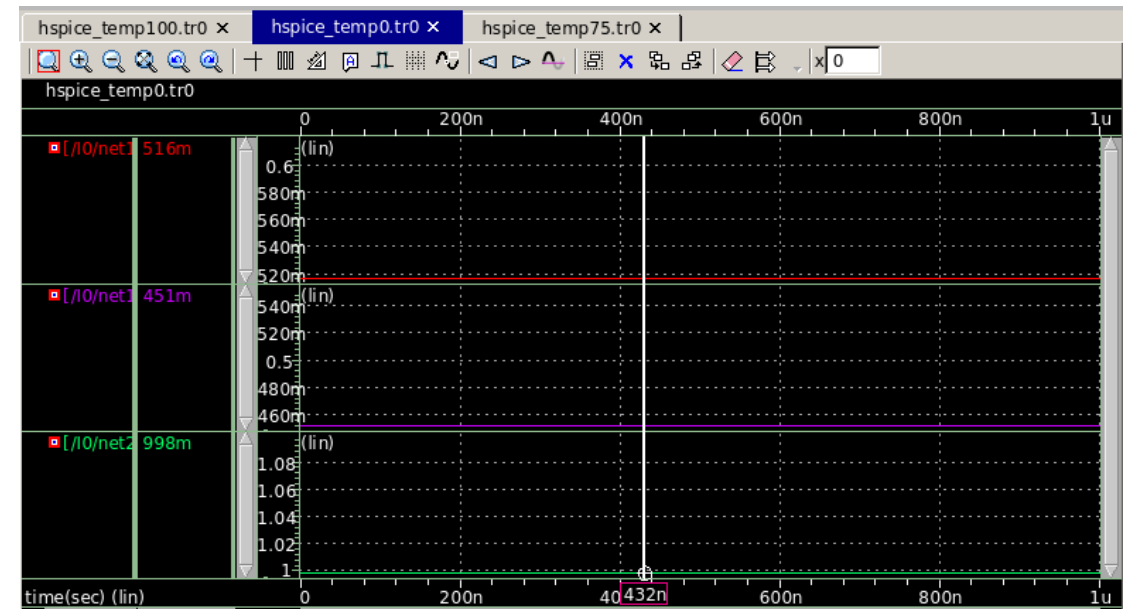
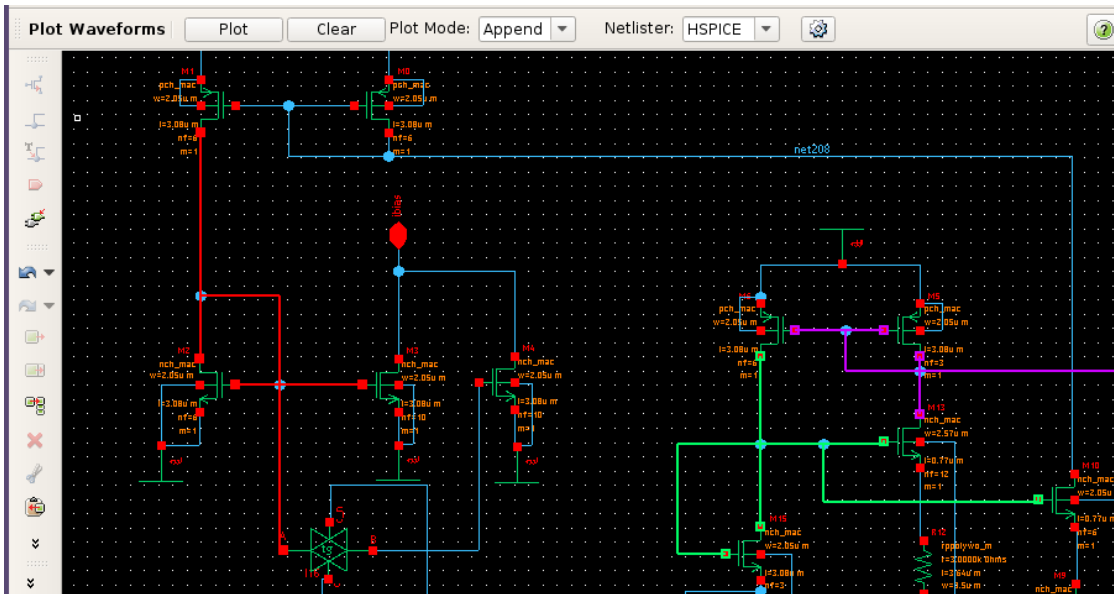
Plot Signal

- Use **Utilities > Plot Signal** command
- **Directly plot signals from simulator output files**
 - Interactively pick signals from Schematic Editor
 - Append and Replace plot mode support
- **Setup Name Mapping and add simulator files**



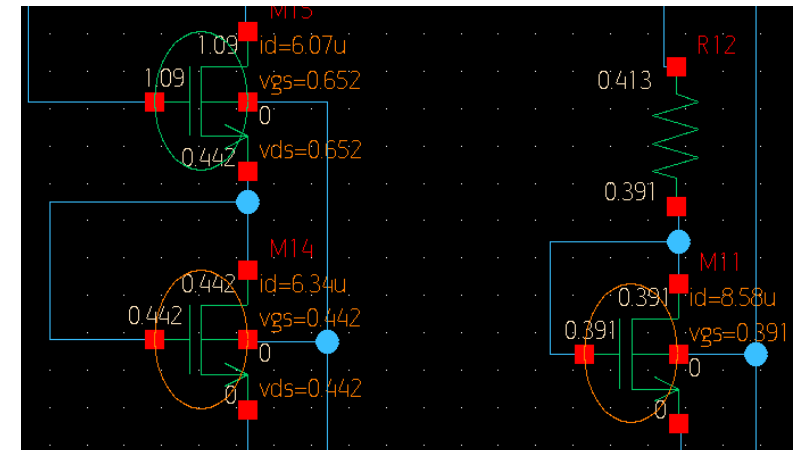
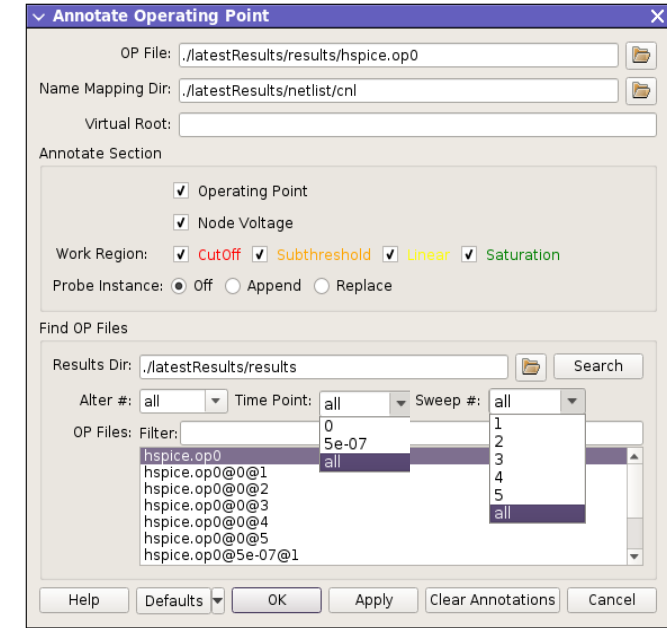
Plot Signal

- **Cross Probe signals from Schematic Editor**
 - Select net and press **Plot** button



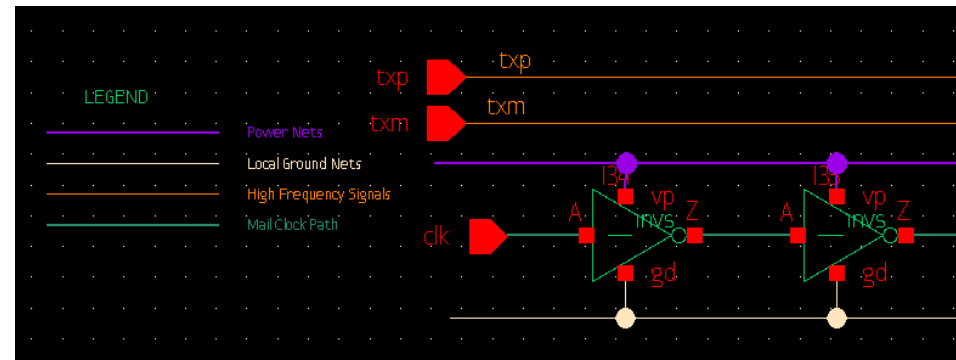
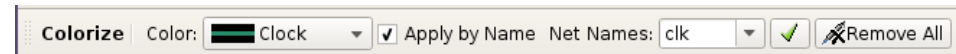
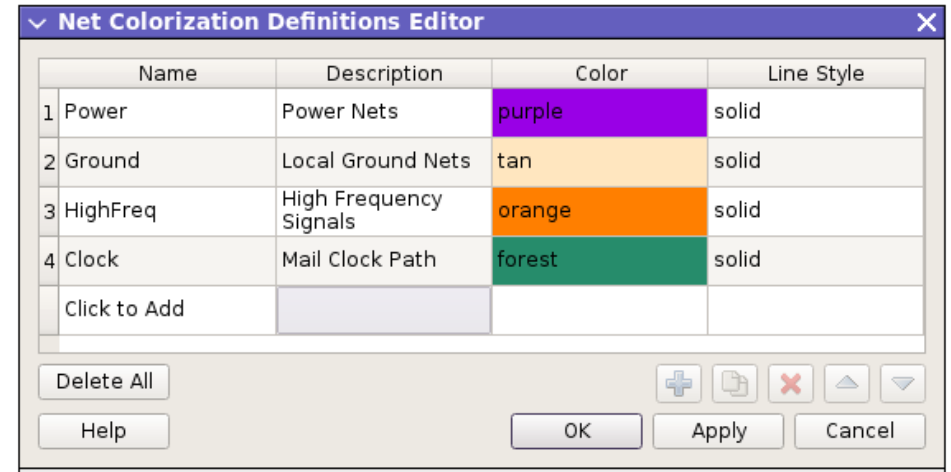
Annotate Operating Point

- Use **Utilities > Annotate Operating Point** command
- Setup OP file and Name Mapping settings
 - Search for OP files inside results directory
 - Filter by Alter #, Time Point or Sweep #
- Specify what to annotate
 - Operating Point
 - Node Voltages
 - Work Region



Colorize Nets (O-2018.09-SP1)

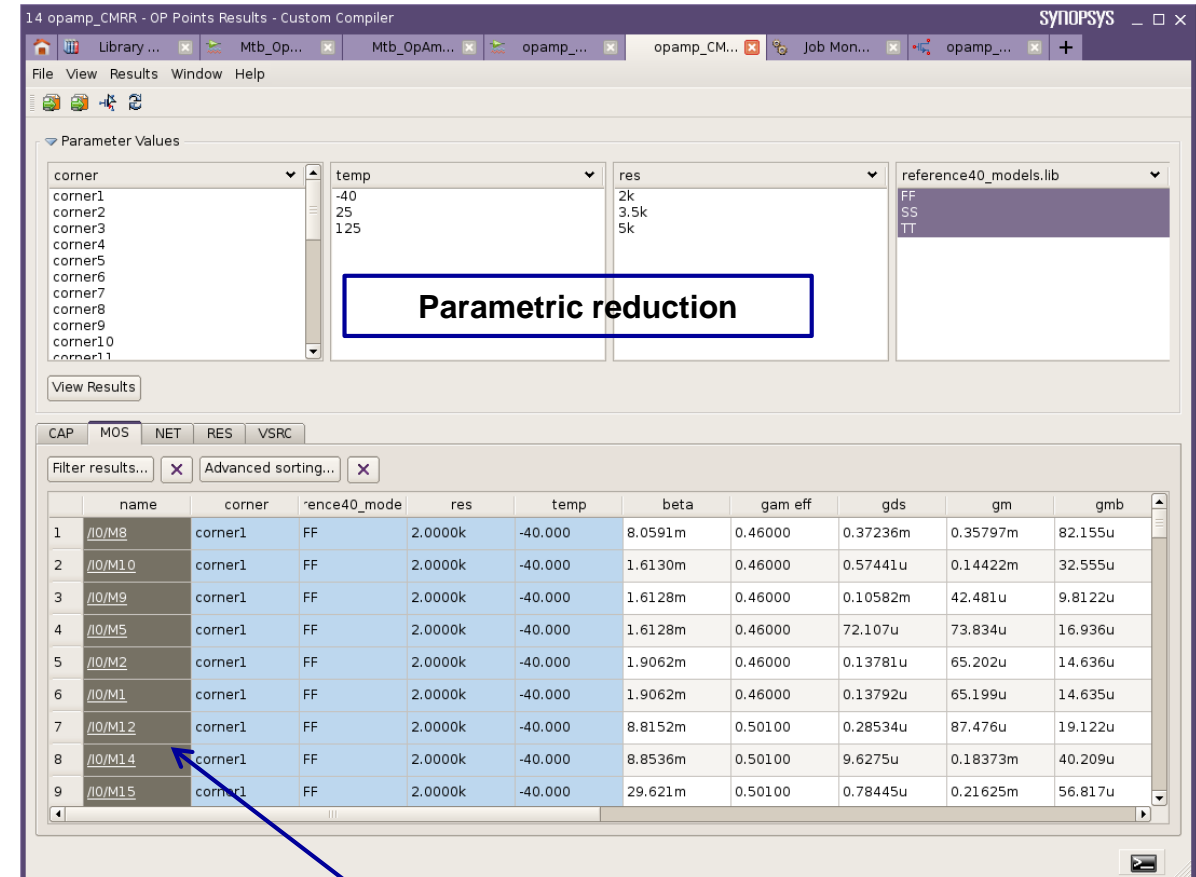
- **Colorize special nets based on designers preferences**
 - Power and ground nets
 - High frequency paths
 - Clock signals
 - Etc.
- **Setup through Utilities > Net Colorization Definitions dialog**
- **Colorize nets using Edit > Colorize Nets command**
 - Choose color and click on a net
 - Check Apply by Name, select net name and apply color
- **Add color legend instance**
 - Library: basic
 - Cell: net_legend
 - View: symbol



SAE Utilities

Operating Point Report

- DC Operating Point Viewer can be invoked using Results > Print > Operating Point Report
- Displays DC OP for all leaf cells in hierarchy
 - Separate tab is used for each type of device
- Supports
 - Parametric reduction
 - Cross probing with Schematic Editor
 - Showing/Hiding operating points of interest
 - Filtering
 - Sorting
- Export results to CSV or HTML formats



Double Click to Cross Probe with SE

Operating Point Report

- Filter DC OP results based on defined conditions

- Supported Conditions

- equal (=)
- more (>)
- less (<)
- range
- in

The screenshot displays the 'Filter By' dialog box and a table of results. The dialog box contains three conditions:

- reference40_models.lib is in SS
- beta is > 7m
- gm is > 60u

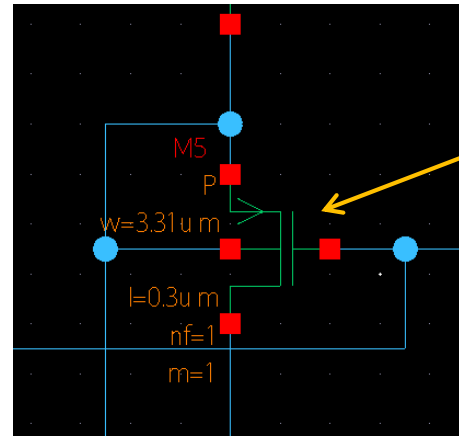
The table shows results for various corners and models. The columns are: name, corner, reference40_models.lib, res, temp, beta, gam eff, gds, gm. The results are filtered based on the conditions defined in the dialog box.

	name	corner	reference40_models.lib	res	temp	beta	gam eff	gds	gm
1	/I/O/M8	corner1	FF	2.0000k	-40.000	8.0591m	0.46000	0.37236m	0.35797m
2	/I/O/M8	corner4	FF	3.5000k	-40.000	7.9460m	0.46000	0.25337m	0.35547m
3	/I/O/M8	corner7	FF	5.0000k	-40.000	7.8625m	0.46000	0.17823m	0.34870m
4	/I/O/M8	corner10	FF	2.0000k	25.000	3.3681m	0.46000	0.24201m	0.16313m
5	/I/O/M8	corner3	TT	2.0000k	-40.000	7.0689m	0.48800	0.27311m	0.24184m
		corner13	FF	3.5000k	25.000	3.3649m	0.46000	0.19496m	0.16636m
		corner6	TT	3.5000k	-40.000	6.9925m	0.48800	0.20574m	0.24014m
		corner16	FF	5.0000k	25.000	3.3604m	0.46000	0.16093m	0.16780m
		corner9	TT	5.0000k	-40.000	6.9343m	0.48800	0.15920m	0.23695m
		corner19	FF	2.0000k	125.00	1.4161m	0.46000	0.16924m	73.049u
		corner22	FF	3.5000k	125.00	1.4276m	0.46000	0.14979m	75.725u
		corner25	FF	5.0000k	125.00	1.4361m	0.46000	0.13434m	77.695u

	name	corner	reference40_models.lib	res	temp	beta	gam eff	gds	gm	gm
1	/I/O/M14	corner8	SS	5.0000k	-40.000	9.4935m	0.55400	1.9134u	62.909u	15.032u
2	/I/O/M14	corner8	SS	5.0000k	-40.000	30.260m	0.55400	0.24681u	68.288u	19.802u
3	/I/O/M14	corner5	SS	3.5000k	-40.000	9.4923m	0.55400	2.4102u	69.615u	16.636u
4	/I/O/M15	corner5	SS	3.5000k	-40.000	30.223m	0.55400	0.27437u	75.814u	21.993u
5	/I/O/M14	corner2	SS	2.0000k	-40.000	9.4916m	0.55400	3.2198u	78.631u	18.792u
6	/I/O/M15	corner2	SS	2.0000k	-40.000	30.179m	0.55400	0.31185u	86.065u	24.982u
7	/I/O/M7	corner17	SS	5.0000k	25.000	8.9114m	0.55400	0.36289u	0.11623m	37.091u
8	/I/O/M7	corner14	SS	3.5000k	25.000	8.9083m	0.55400	0.37361u	0.11978m	38.218u
9	/I/O/M7	corner11	SS	2.0000k	25.000	8.9050m	0.55400	0.38566u	0.12377m	39.486u
10	/I/O/M7	corner8	SS	5.0000k	-40.000	37.058m	0.55400	0.67044u	0.22218m	64.241u
11	/I/O/M7	corner5	SS	3.5000k	-40.000	37.079m	0.55400	0.70533u	0.23426m	67.697u
12	/I/O/M7	corner2	SS	2.0000k	-40.000	37.104m	0.55400	0.74704u	0.24876m	71.842u

Operating Point Report

- Filter Operating Point information based on selected devices from Schematic Editor
- Click on devices to include them in OP Report
- Hold Ctrl and click to devices to remove them from selected devices
- Filter expression is created from selected devices



The screenshot shows the '14 opamp_CMRR - OP Points Results - Custom Compiler' window. The 'MOS' tab is selected. The table below shows the results for the MOSFETs.

	name	corner	reference40_models.lib	res	temp	be
1	/I/O/M8	corner1	FF	2.0000k	-40.000	8.0591

The screenshot shows the 'Parameter Values' window. The 'MOS' tab is selected. The table below shows the results for the MOSFETs. A 'Filter By' dialog box is open, showing the filter expression: 'name is in /I1/M5'. The 'Filter By' dialog box also shows the 'corner' and 'time' filters.

	name	analysis	corner	reference40_model	time	beta	gam eff	gds	
1	/I1/M5	tran	corner1	FF	20.000n	1.3359m	1.1010	1.8247m	23.3
2	/I1/M5	op						1.8247m	23.3
3	/I1/M5	tran						1.5108m	22.4
4	/I1/M5	op						1.5108m	22.4
5	/I1/M5	tran						1.6533m	22.8
6	/I1/M5	op						1.6532m	22.8
7	/I1/M5	tran						1.8260m	22.7
8	/I1/M5	op	corner4	FF	0	1.3359m	1.1010	1.8260m	22.8
9	/I1/M5	tran	corner5	SS	20.000n	1.1536m	1.1550	1.5118m	22.6

Operating Point Report

■ Sort DC OP results

- Ascending
- Descending

■ Chain multiple parameter sorting

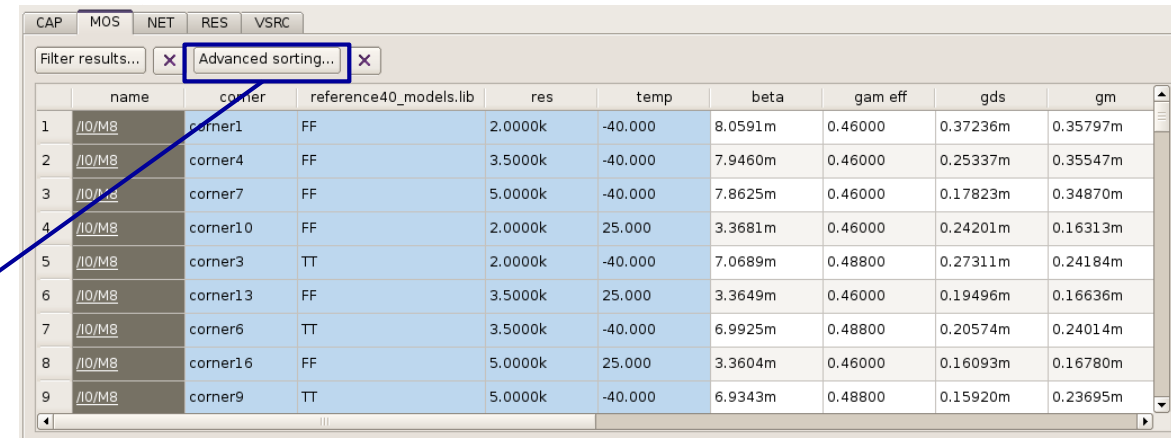
Sort By

1: beta descending

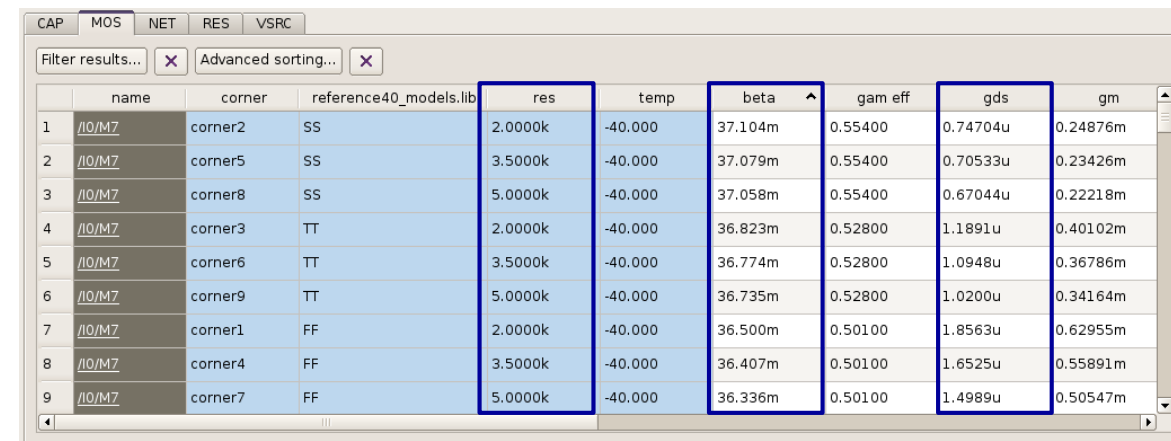
2: res ascending

3: gds descending

OK Apply Cancel



	name	corner	reference40_models.lib	res	temp	beta	gam eff	gds	gm
1	/I0/M8	corner1	FF	2.0000k	-40.000	8.0591m	0.46000	0.37236m	0.35797m
2	/I0/M8	corner4	FF	3.5000k	-40.000	7.9460m	0.46000	0.25337m	0.35547m
3	/I0/M8	corner7	FF	5.0000k	-40.000	7.8625m	0.46000	0.17823m	0.34870m
4	/I0/M8	corner10	FF	2.0000k	25.000	3.3681m	0.46000	0.24201m	0.16313m
5	/I0/M8	corner3	TT	2.0000k	-40.000	7.0689m	0.48800	0.27311m	0.24184m
6	/I0/M8	corner13	FF	3.5000k	25.000	3.3649m	0.46000	0.19496m	0.16636m
7	/I0/M8	corner6	TT	3.5000k	-40.000	6.9925m	0.48800	0.20574m	0.24014m
8	/I0/M8	corner16	FF	5.0000k	25.000	3.3604m	0.46000	0.16093m	0.16780m
9	/I0/M8	corner9	TT	5.0000k	-40.000	6.9343m	0.48800	0.15920m	0.23695m



	name	corner	reference40_models.lib	res	temp	beta	gam eff	gds	gm
1	/I0/M7	corner2	SS	2.0000k	-40.000	37.104m	0.55400	0.74704u	0.24876m
2	/I0/M7	corner5	SS	3.5000k	-40.000	37.079m	0.55400	0.70533u	0.23426m
3	/I0/M7	corner8	SS	5.0000k	-40.000	37.058m	0.55400	0.67044u	0.22218m
4	/I0/M7	corner3	TT	2.0000k	-40.000	36.823m	0.52800	1.1891u	0.40102m
5	/I0/M7	corner6	TT	3.5000k	-40.000	36.774m	0.52800	1.0948u	0.36786m
6	/I0/M7	corner9	TT	5.0000k	-40.000	36.735m	0.52800	1.0200u	0.34164m
7	/I0/M7	corner1	FF	2.0000k	-40.000	36.500m	0.50100	1.8563u	0.62955m
8	/I0/M7	corner4	FF	3.5000k	-40.000	36.407m	0.50100	1.6525u	0.55891m
9	/I0/M7	corner7	FF	5.0000k	-40.000	36.336m	0.50100	1.4989u	0.50547m

Timestamps Dashboard

■ Purpose

- Highlights if netlists or simulation results are out of date

■ Scan on demand Simulation Results, Netlist, Design timestamps and SAE setup

■ Colorize outdated data

■ Re-run netlisting and simulation from Context Sensitive Menu (CSM)

- Highlights rows as netlisting occurs

■ A preference can be set to ignore libraries

- Helps reduce the content that is tracked (PDK lib)

`saTimestampDashboardFilterList`

Simulation Results

Netlisted Design

Design Hierarchy

Status

Perform Full Scan

Data	View	Modified By	Timestamp	Status
Results		norayra	12/12/2017 15:36:53	
Final Netlist		norayra	12/12/2017 14:44:45	
Structural Netlist		norayra	12/12/2017 14:44:45	
buffer	schematic	norayra	11/27/2017 17:02:42	Has Newer Child
inverter	schematic	norayra	11/27/2017 17:02:42	
inverter_hv	schematic	norayra	12/12/2017 15:37:18	Newer
vdc	hspice	ids_cm	11/23/2017 14:48:33	
vpulse	hspice	ids_cm	11/23/2017 14:48:34	
SAE Data				
Analyses				
Design Variables				Mismatch
Simulation Options				

Session: saeSession0 | Testbench: initial

Results Dependencies

☐ Show Out-of-date Only

Filtering libraries: ""

Help Defaults

Quick Scan Full Scan

Last Full Scan: Never

Close