University of Waterloo
Electrical & Computer Engineering Department

ECE 331
ELECTRONIC DEVICES

LAB 1 READINGS

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1. Introduction

Welcome to the world of semiconductor devices! In this lab, you'll learn a little about how diodes and transistors are fabricated. You'll get a chance to probe actual devices, fabricated here at the University of Waterloo, and perform simple test measurements on them. The purpose of the lab is not only to give you an idea of how microelectronic devices and circuits are made, but also to introduce you to many of the terms and concepts important in semiconductor device engineering.

2. Before the Lab

One of your prelab assignments is to read and familiarize yourself with the lab. You'll find that many of the terms and concepts are completely new to you. Keep track of the things you find confusing, and then ask a teaching assistant or the lab instructor for clarification during the lab period. Alternatively, you might want to check the references listed at the end of the lab.

3. Background

Before doing any measurements, you need to understand the basics. We'll review how semiconductor devices are made, and then consider some of the units and dimensions commonly used in semiconductor engineering.

3.1. How are semiconductor devices made?

The Planar Fabrication Process

The most common semiconductor material used for electronic devices today is silicon. Devices are fabricated in silicon by means of a *planar process*. This process is based on the *diffusion* of *impurities* into the surface of a single-crystal silicon wafer. *(Note also that ion implantation is another method for introducing impurities).* The impurities make regions of the silicon either rich in *holes* or *electrons*, the two current-carrying particles found in semiconductors. Regions rich in holes are called *p-type*, and regions rich in electrons are called *n-type*. When a *p*-type region meets an *n*-type region, a structure called a *pn junction* is formed. This structure is the basic building block of all semiconductor devices.

A *diode* is formed using just a single *pn* junction. A simplified cross-section of a planar diode is given in figure 1. From your study of basic circuit theory, you may already be familiar with the current-voltage law for such a planar diode:

$$I_d = I_S \left(\exp\left(V_d / m V_t \right) - 1\right) \quad \text{Equation 1}$$

where I_d is the current through the diode, V_d is the voltage applied across its terminals, V_t is the *thermal voltage*, and I_S and m are parameters related to the properties of the diode. However, you probably don't know how the structure in figure 1 leads to this law, or how the constants I_S and m are related to the physical properties of that structure. These are some of the things that you'll learn in **this** course!

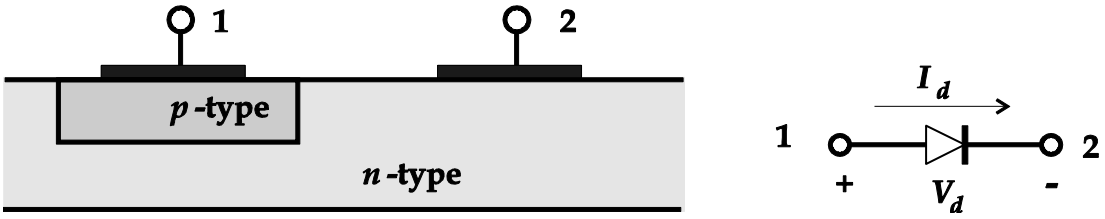

Figure 1: Sketch of a planar diode, which is actually just a single *pn* junction.

So how a planar diode is made using the diffusion process? The procedure begins with an engineer defining a set of *mask diagrams*, such as those shown in figure 2. These diagrams, which are drawn using a CAD program, define the type of fabrication to be performed on a given area of the silicon. The mask diagrams are used to create a set of *glass processing masks*. Using the processing masks, the fabrication steps, which are illustrated in figures 3 and 4, are as follows:

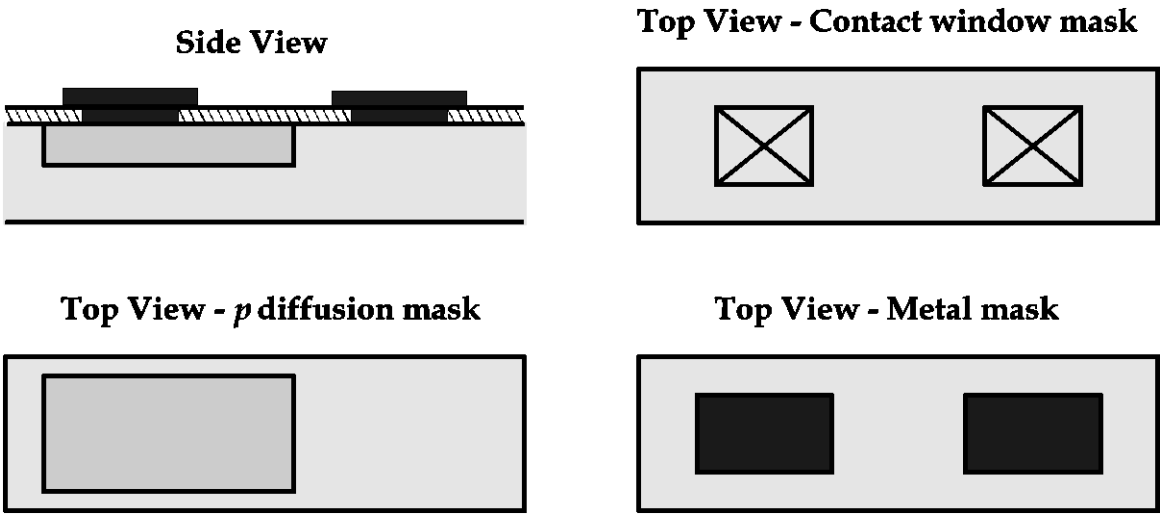

Figure 2: The masks needed to make the diode of figure 1.

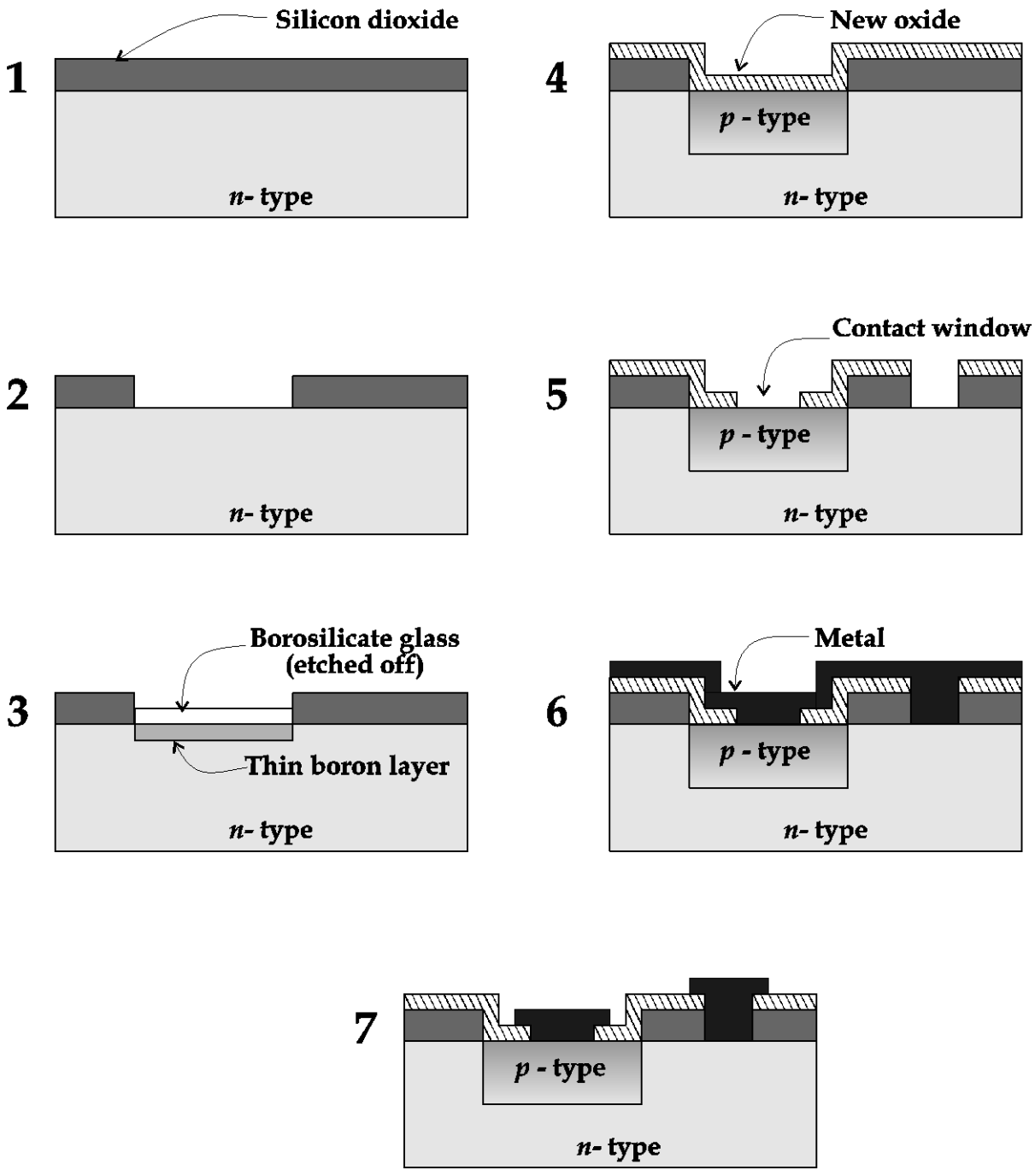

Figure 3: Pictures of the silicon wafer after **each processing step. The substeps used in step 2 are illustrated in figure 4.**

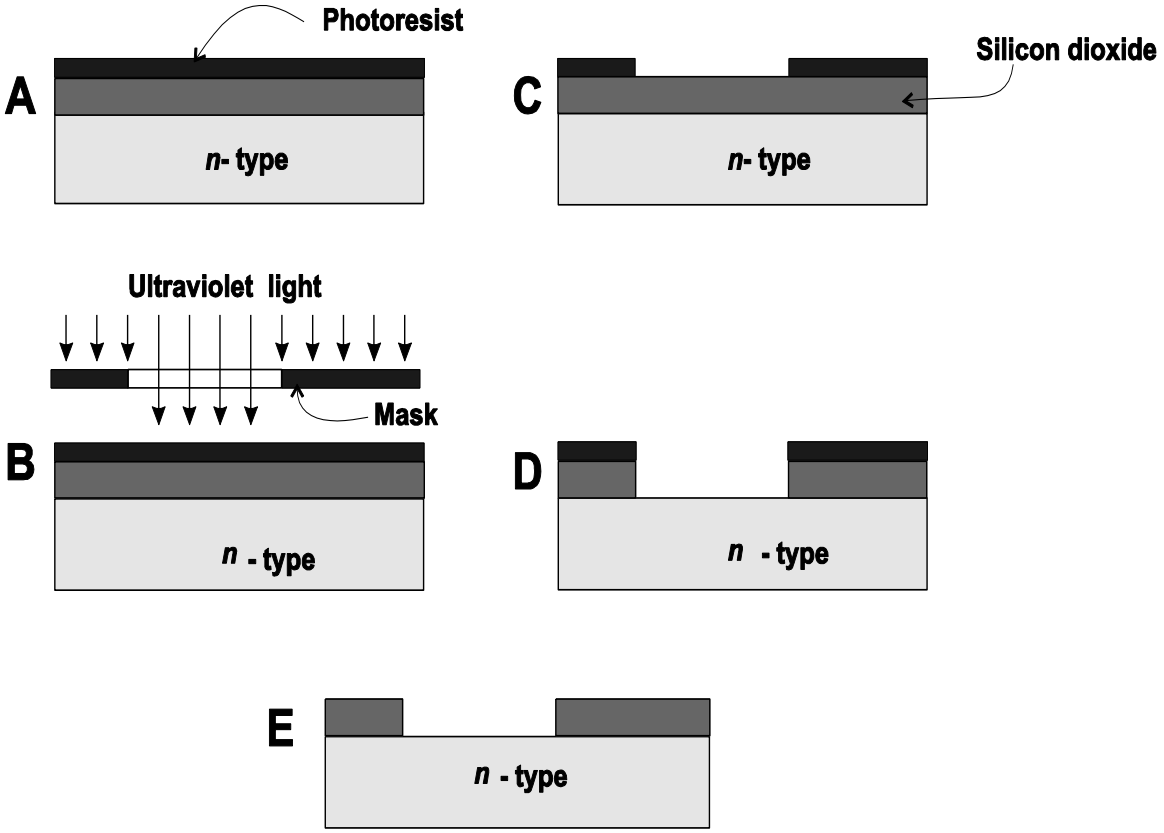

Figure 4: Pictures of the silicon wafer after each substep in step 2.

1) A layer of silicon dioxide SiO_2 is *thermally grown* all over the surface of an *n*-type silicon wafer.
2) The oxide is selectively *etched* using a process called *photolithography*. This involves the following substeps:
    a. The surface of the silicon dioxide is coated with a film of material called *photoresist*. The resist is lightly baked to drive off solvents and to dry it.
    b. The *p*-diffusion processing mask is placed near the coated wafer and exposed to ultraviolet light. The light degrades exposed photoresist.
    c. The slice is rinsed in a solvent which removes the degraded photoresist.
    d. Exposed silicon dioxide is etched in buffered hydrofluoric acid.
    e. The remaining layer of photoresist is removed.
3) The slice is cleaned and placed in a *deposition furnace*. A thin layer of boron, which is an impurity known to make silicon *p*-type, is deposited and just diffused into the surface of the silicon. Note that the boron diffuses into the silicon only where the oxide has been etched away. This is why processing steps 1 and 2 were needed! During the deposition, a thin layer of oxide rich in boron, called *borosilicate glass*, is formed on the surface of the silicon, but is etched off.
4) The slice is transferred to a *diffusion furnace*. The deposited boron surface layer is *driven* more deeply into the wafer; in other words, the boron atoms are made to *diffuse* more deeply into the silicon, converting it to *p*-type material rich in holes. Since the amount of

boron available is fixed from step 3, the concentration of boron at the wafer surface falls while that at regions below the surface increases. During the diffusion cycle, a new layer of oxide is grown at the surface. The oxide forms a seal preventing boron atoms from escaping, and it is needed to allow further selective processing of the silicon.

5) Contact windows are etched in the oxide. This step is the same as step 2 except that the contact window processing mask is used, and it is aligned with respect to the pattern already on the surface of the silicon.
6) The slice is cleaned and placed in a *vacuum deposition system*. A layer of aluminum is deposited all over the surface.
7) Aluminum is selectively removed, in a manner similar to step 2, using the metal processing mask, and the slice is baked to bond the aluminum to the silicon surface. The wafer is then ready for test measurements.
8) The *wafer*, or *slice*, actually contains several copies of the devices to be fabricated. For the fabrication of a single planar diode, this means several copies of the diode would actually be made all over the wafer. Therefore, the last step is usually to *dice* the wafer into individual *chips*, every chip having one copy of the devices to be fabricated. Each chip is then *packaged* in a hermetically sealed case. *Bonding wires* are used to connect the chip to *pins*, and the pins are brought out of the package for connection to the outside world.
9) Note: Resistors can be fabricated by making contact to special diffused layer patterns.

For this lab, step 8 is omitted, and you'll work with entire wafers that have undergone various degrees of processing between steps 1 and 7.

What about transistors? How are they made? A planar *npn bipolar transistor* may be made by performing extra processing between steps 4 and 5 listed above. The extra processing is needed to create a region extremely rich in electrons, called n^+-type material, and requires the use of an impurity known to make silicon *n*-type, such as phosphorus. The n^+ region is created within the *p* region formed after step 4. Figure 5 shows a simplified cross-section of a planar *npn* bipolar transistor. The fabrication required to make a *field-effect transistor* is more complicated, and you'll learn about these devices later. In this lab, we'll stick to resistors, diodes and *pn* junctions of bipolar transistors.

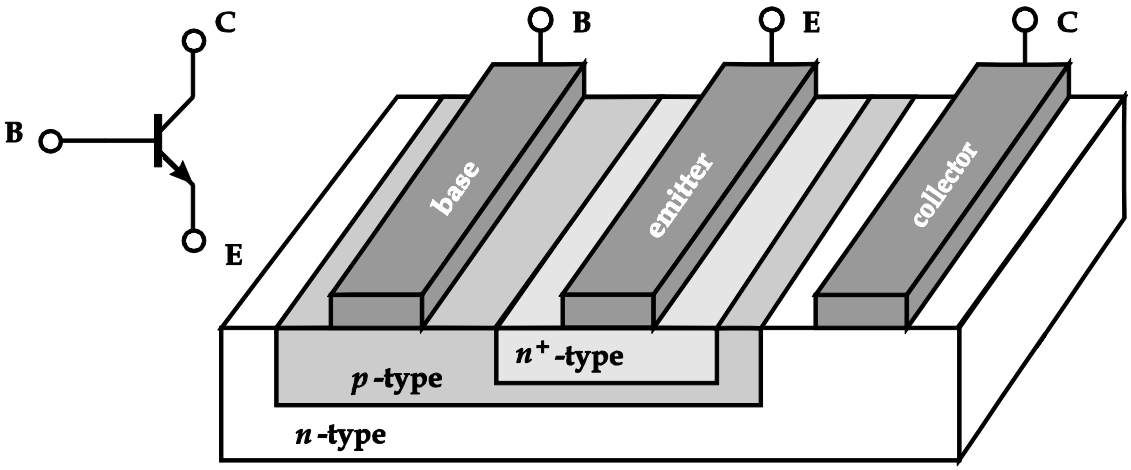

Figure 5: A simplified cross-section of a planar *npn* bipolar transistor. The *emitter* contact is E, the *base* contact is B, and the *collector* contact is C.

Real Devices

Although the above description is enough for you to get a basic idea of how resistors, diodes and transistors are made, it doesn't quite tell the whole story. To illustrate, let's have a brief look at the construction of a **real** *npn* bipolar transistor. Real transistors (and diodes) can be divided into those that are *discrete*, and those that are *integrated*.

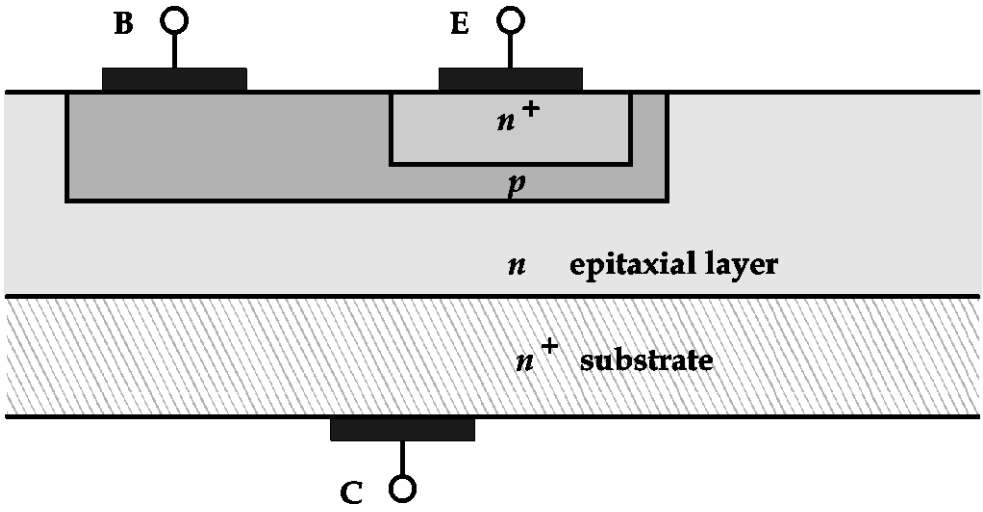

Figure 6: A cross-section of a real discrete *npn* bipolar transistor. The figure is not drawn to scale; in reality, the n^+ substrate is about 10 to 100 times the thickness of the epitaxial layer.

A device is discrete if it is the only device fabricated on a chip. Figure 6 shows a cross-section of a real discrete *npn* bipolar transistor. Compare it to the simple sketch in figure 5. Note that the *n*-type material in figure 5 actually refers to what is called an *n epitaxial layer*. This material,

moderately rich in electrons, is *grown* on top of a thick n^+ *substrate*. The substrate provides mechanical support and allows for a good electrical contact --- note the difference in location of collector contacts between figures 5 and 6.

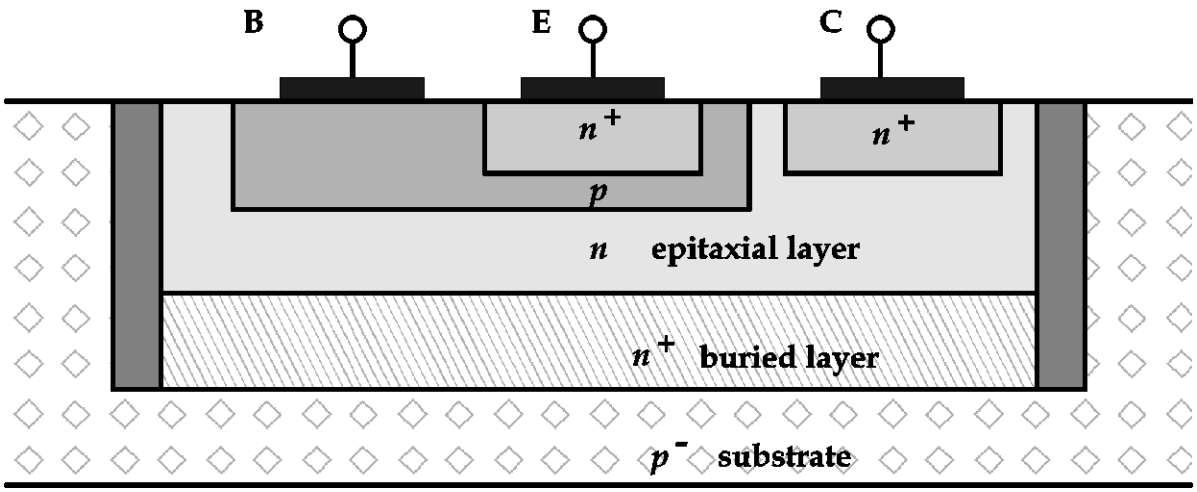

Figure 7: A cross-section of a real integrated *npn* bipolar transistor. In reality, the p^- substrate is much thicker than shown.

Integrated devices exist with several other devices on the same chip. All the devices on the chip are combined to form a circuit, called an *integrated circuit*. Figure 7 shows a cross-section of a real integrated *npn* bipolar transistor. Compare it to the simple sketch in figure 5. As in the case of the discrete device, the *n*-type material in figure 5 corresponds to an *n* epitaxial layer. However, unlike the discrete device, the epitaxial layer is grown on top of an n^+ *buried layer* that is diffused into a p^- substrate. The buried layer, it turns out, is needed to lower the *collector resistance* of the transistor. The p^- substrate, in conjunction with deep p^+ *walls* surrounding the device, provides a method to *isolate* the transistor from other devices on the chip. Isolation is achieved by ensuring that all the *pn* junctions formed between the *n* epitaxial layer, n^+ buried layer, p^+ walls, and p^- substrate are always under *reverse bias*, since a *pn* junction under reverse bias conducts virtually no current. Finally, an n^+ diffusion, usually made at the same time as the n^+ emitter diffusion, is required at the location of the collector lead. This diffusion is needed because it turns out that a good electrical contact cannot be made between metal and the epitaxial layer.

You're probably wondering how the structures in figures 6 and 7 end up working as bipolar transistors. Stay tuned. Before the end of this course, you'll find out!

3.2. A Note on Dimensions and Units

It is conventional to use a variety of mixed units to describe the various dimensions encountered in semiconductor engineering. You should be prepared to meet any of them.

The dimensions of a single semiconductor device, such as a diode or transistor, are typically quoted in **microns** (μm). One micron is equal to 10^{-6} m. For example, high-performance bipolar transistors typically have emitter diffusions that are a few microns wide. Think about this! Can you see how it is thus possible to have a huge number of these devices on a single chip of area, say, the size of your fingertip?

Oxide thickness is usually given in angstroms (Å). One angstrom is equal to 10^{-10} m. Sometimes, oxide thickness is also quoted in fractions of a micron. For example, an oxide layer with thickness 2.0×10^{-7} m may be referred to as being 2000 Å or 0.2 μm thick.

Overall chip sizes are often quoted in **mils**. One mil is 10^{-3} inches. Therefore, 25.4 μm = 1 mil. The mil, being non-metric, is an inconvenient unit. You won't encounter the mil too much in this course.

A unit you **will** have to get accustomed to using is the centimeter. At first, you may find this awkward, since when studying basic electricity and magnetism you more commonly used the meter. In semiconductor engineering, the centimeter is preferred over the meter. For example, **free carrier concentrations**, namely the number of electrons or holes available for current conduction, are quoted as a number per cubic centimeter; thus, one might give the free hole concentration as $p = 10^{17}$ cm^{-3}, meaning there are 10^{17} holes per cubic centimeter available for conduction. Even quantities that you are familiar with are quoted in terms of the centimeter rather than the meter. For example, the electric field is quoted in units of V/cm as opposed to V/m, and resistivity is quoted in units of Ω• cm instead of Ω• m. Be careful!