COMP 305 - Computer Organization, Fall 2019, Midterm-I

Number :

Name-Surname :

Date : 31st October 2019

**Q1(20p).** For an application coded by you in C, it is compiled and executed in two different computer systems; Sys1and Sys2. In both systems, there are only two types of instructions; TypeA and TypeB:

In SysA: The application consists of 100.000 machine instructions. 70% of them are in TypeA and 30% of them are in TypeB. It takes 3 cycles to execute TypeA instructions and 4 cycles to execute TypeB instructions.

In SysB: The application consists of 50.000 instructions and 40% of them are TypeA and 60% are TypeB instructions. It takes 2 cycles to execute TypeA and 5 cycles to execute TypeB.

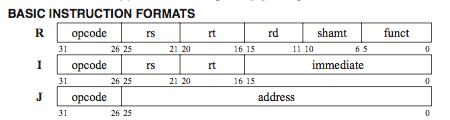
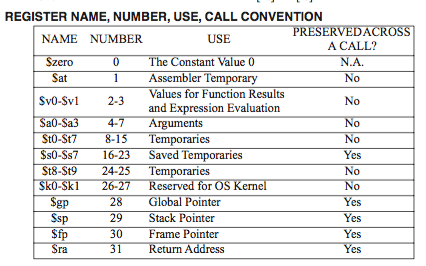
**a (15p)** Performance of a computer is calculated by the formula above;

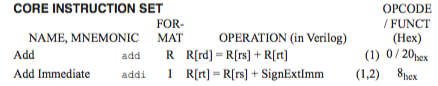
Find which system executes your application faster and show its speed up compared to the other one.

**b) (5p**) The computation stack is given below. Between SysA and SysB; which levels are 1)DIFFERENT 2)MAY BE DIFFERENT 3)SAME mark them and explain if you need.

|  |
| --- |
| Problem |
| Algorithm |
| Program/Language |
| Runtime (OS) |
| ISA |
| Microarchitecture |
| Logic (Gates) |
| Circuit |
| Transistors |

**Q2 (20p)** Convert given instructions to binary format (MIPS reference data is at the last page).

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a) nor $s0, $s1, $s2

b) lw $s1, 8($sp)

c) addi $t1, $zero, 128

d)add $s0, $s0, $s1

**Q3 (20p)** What is the compiled versions of the following code segment in MIPS? Note that i is in $s2, k is in $s3 and the base address of Array is in $s4.

while ( i != 0){

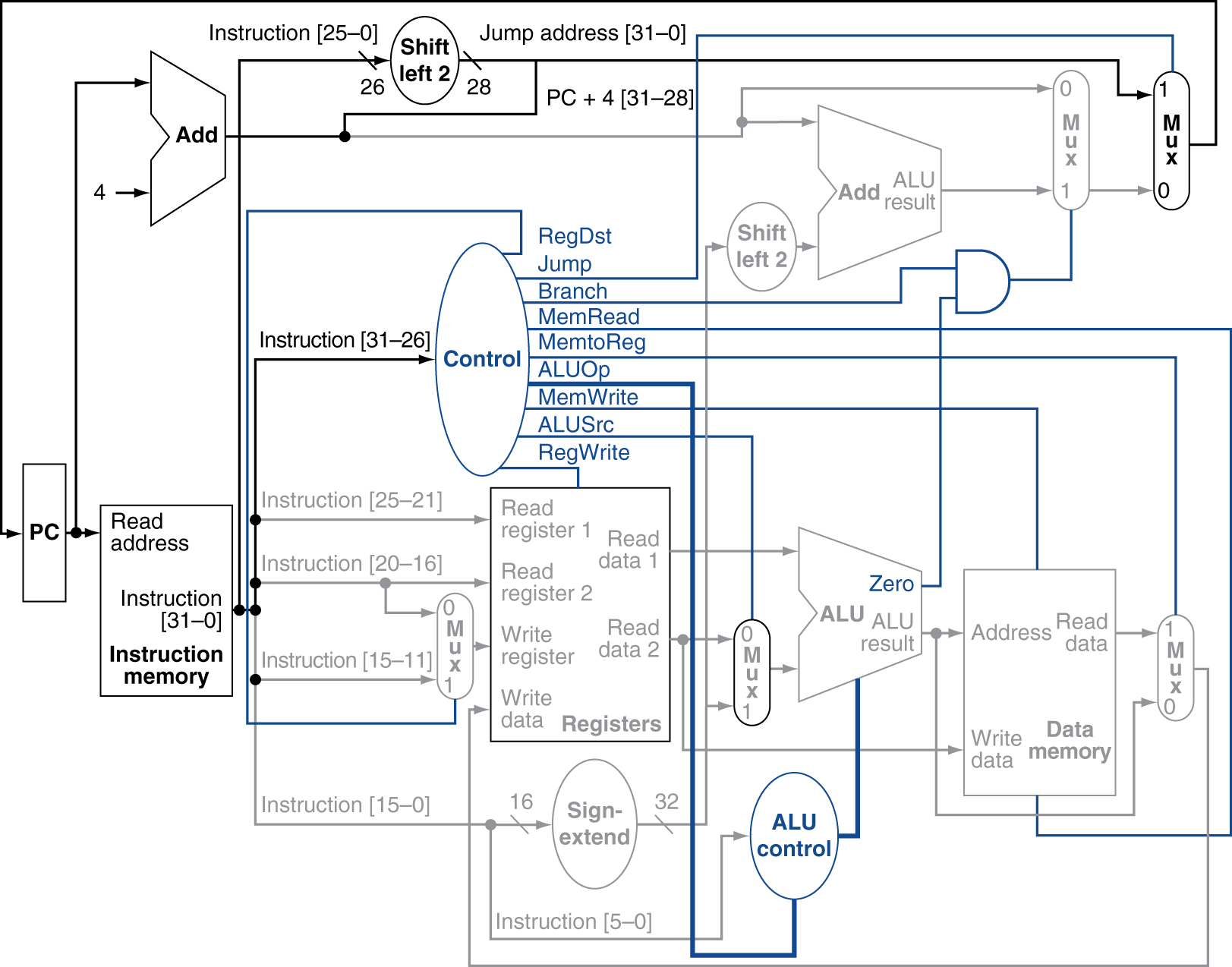
k = Array[i];

i--;

Array[i] = k+1;

i--;}

**Q4(20p).** The datapath in a MIPS architecture is given as in the figure.

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a. Write down the value of each signal for the given instructions in the table.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Instruction** | **Jump** | **Branch** | **MemRead** | **MemWrite** | **ALUSrc** | **RegWrite** |
| ADD R1, R2, R3 |  |  |  |  |  |  |
| JUMP LOOP |  |  |  |  |  |  |
| BNE R1, R2, Exit |  |  |  |  |  |  |
| LW R1, 0(R2) |  |  |  |  |  |  |
| SW R1, 4(R5) |  |  |  |  |  |  |

b. In the figure there are two “Shift Left 2” logics and one “Sign Extend” logic. Explain their usage and give one example instruction for usage of each of them.

**Q5 (20p).** By using a MIPS-like logic design, you are trying to implement the microarchitecture; 1) as a single-cycle machine (SSM) 2) as a pipelined machine (PM). In the logic design, according to gate delays, Fetch, Execute and Memory takes 300ps while Decode/RegisterRead and Write Back take 150ps.

a) What are the minimum lengths of one cycle for SSM and PM?

b) How many cycles would take to execute 4 instructions in SSM and PM?

c) How many picoseconds would take to execute 4 instructions in SSM and PM?

d) What is the speedup of PM compared to SSM for 4 instructions?

e) If we execute infinite number of instructions, what would be the maximum speedup of PM compared to SSM?

**Q6 (20)** Write down the addressing modes in MIPS and give an example instruction for each mode.