LAB #01. LOGIC GATES

Objective

To learn how to generate a design with Vivado software using simple logic gates and to execute the design with a Basys3 board.

Main-lab

1) Generate a behavioral VHDL code to design a circuit given in Figure 2. Module0 (M0) has 6 inputs and inverts all inputs. M1 is a 3-inputs AND gate, M2 is a 3-inputs AND gate. M3 is 2-inputs NOR gate. M4 as an entire circuit has a 6-bits input and a single bit output.

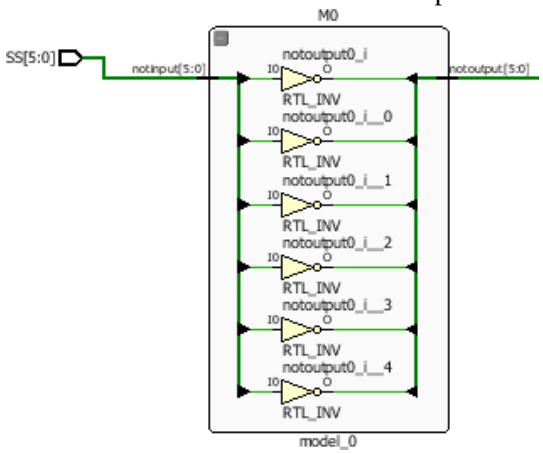

Figure 1. Schematic diagram of M0

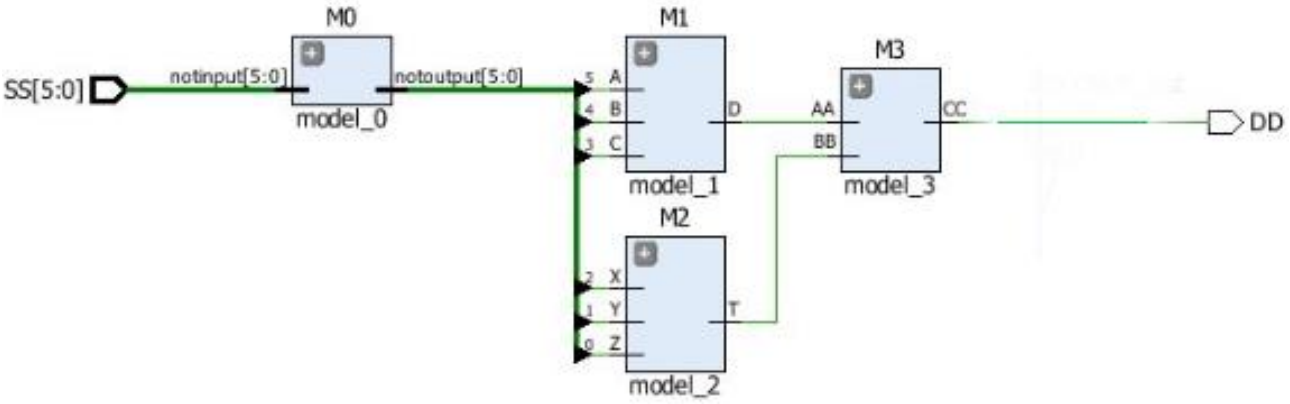

Figure 2. Schematic diagram.

2) Modify the xdc file accordingly. Synthesize your design and show the elaborated design.

3) Generate a bit stream file and program the Basys3 board. Use switches for the inputs and an LED for the output to check your design.

Tips:

- Use components to combine the modules. Define internal signals to connect M1 and M2 to M3.