

See discussions, stats, and author profiles for this publication at: <https://www.researchgate.net/publication/26488100>

Advanced readout system IC current mode semi-Gaussian shapers using CCII_s and OTAs

Article in VLSI Design · April 2007

DOI: 10.1155/2007/71684 · Source: DOAJ

CITATIONS

10

READS

256

3 authors, including:



Thomas Noulis

Intel

36 PUBLICATIONS 146 CITATIONS

[SEE PROFILE](#)



Stylianos Siskos

Aristotle University of Thessaloniki

158 PUBLICATIONS 1,200 CITATIONS

[SEE PROFILE](#)

Some of the authors of this publication are also working on these related projects:



MOSFET Radiation Dosimeters [View project](#)



NexGenMilwave: Next Generation Millimeter Wave Backhaul Radio [View project](#)

Research Article

Advanced Readout System IC Current Mode Semi-Gaussian Shapers Using CCIs and OTAs

Thomas Noulis, Constantinos Deradonis, and Stylianos Siskos

Section of Electronics and Computers, Electronics Laboratory, Physics Department, Aristotle University of Thessaloniki, Aristotle University Campus, 54124 Thessaloniki, Greece

Received 4 November 2006; Accepted 3 February 2007

Recommended by Adoracion Rueda

Novel CMOS current mode shapers for front-end electronics are proposed. In particular, six semi-Gaussian shaper implementations based on second generation current conveyors and operational transconductance amplifiers are designed using advanced filter design techniques. Although all shaper architectures are fully integrated, they satisfy a relatively large peaking time. The topologies are analytically compared in terms of noise performance, power consumption, total harmonic distortion (THD), and dynamic range (DR) in order to examine which is the most preferable in readout applications. Design technique selection criteria are proposed in relation to the shaper structures performance. Analysis is supported by simulations results using SPICE in a $0.6\ \mu\text{m}$ process by Austria Mikro Systeme (AMS).

Copyright © 2007 Thomas Noulis et al. This is an open access article distributed under the Creative Commons Attribution License, which permits unrestricted use, distribution, and reproduction in any medium, provided the original work is properly cited.

1. INTRODUCTION

Recent developments in semiconductors detectors, VLSI electronics, and information technology enabled the adaptation of radiation detecting systems used in high energy physics experiments in various imaging applications. These radiation detecting systems require compact, low-cost, and low-noise electronics with a high number of channels. Several motivations suggest that most of these applications can benefit from the use of ASIC (application specific integrated circuit) readouts instead of discrete solutions. The most crucial motivation is that the implementation of readout electronics and semiconductor detectors onto the same chip offers enhanced detection sensitivity thanks to improved noise performances [1–5]. Placing the very first stage of the front-end circuit close to the detector electrode, without using external wires, may reduce the amount of material and complexity in the active detection area and minimize connection-related stray capacitances. This method allows the noise optimization theory predictions [6, 7] to be satisfied more effectively, especially in the case of silicon sensors with very low-anode capacitance (silicon drift detectors, CCDs, pixels). On the other hand, the use of discrete transistors, with their relatively high (a few picofarads) gate capacitances, as front-end elements of hybrid

circuits cannot comply with the stringent low noise requirements. As a result, continuous efforts were performed in order to implement readout systems in monolithic form, and CMOS technologies have been chosen due to the high integration density, relatively low-power consumption and capability to combine analog and digital circuits on the same chip.

The preamplifier-shaper structure is commonly adopted in the design of the above systems. A block diagram of such a detection system is shown in Figure 1. An inverse biased diode (Si or Ge) detects radiation events by generating electron-hole pairs proportional to the absorbed energies. A low-noise charge sensitive preamplifier (CSA) is widely used at the front end due to its low-noise configuration and insensitivity of the gain to the detector capacitance variations. The generated charge Q is integrated onto a small feedback capacitance C_f , which gives rise to a step voltage signal at the output of the CSA with an amplitude equal to Q/C_f . This is fed to a main amplifier, called pulse shaper, where pulse shaping is performed to optimize the S/N system ratio. The resulting output signal is a narrow pulse suitable for further processing.

Although the above typical voltage mode architecture was sufficiently studied mainly in terms of the charge sensitive preamplifier (CSA) input transistor for noise reduction

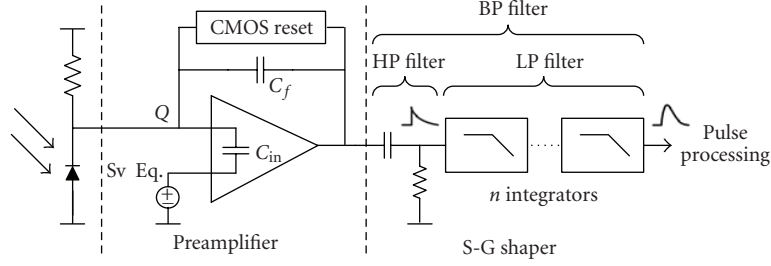


FIGURE 1: Block diagram of a detector readout system.

[6–8], few studies have been performed on pulse shapers and especially on current mode designs.

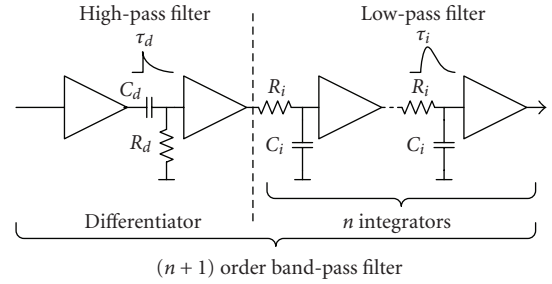
After all, many current mode preamplifiers were so far suggested [9–13]. This is due to the fact that a current mode structure could be an attractive alternative to the more typical voltage mode one, since the signal is processed in the current domain, avoiding charging and discharging of the parasitic capacitance to high-voltage levels and keeping the internal nodes of the circuit at low-impedance values [14–18].

In this work, current mode S-G shaper designs based on second generation current conveyors (CCII) and operational transconductance amplifiers (OTAs) are proposed. Advanced filter design techniques [19, 20], which provide full integration, are used and novel CR-RC² implementations are suggested. All the implementations are compared in terms of noise performance, power consumption, total harmonic distortion (THD), and dynamic range (DR) in order to conclude which the optimum one is.

2. SEMI-GAUSSIAN SHAPER ANALYSIS

Pulse shaping filters are used in electronics spectrometer instruments to measure the energy of charge particles [21]. The purpose of such filters is to provide a voltage pulse whose height is proportional to the energy of the detected particle.

The theory behind pulse shaping systems, as well as different realization schemes, can be found in the literature [21–23]. It has been proved that a Gaussian shaped step response provides optimum signal-to-noise characteristics. However, the ideal S-G shaper is noncasual and cannot be implemented in a physical system. A well-known technique to approximate a delayed Gaussian waveform is to use CR-RCⁿ filter [21]. Such shaper principal schema is shown in Figure 2. A high-pass filter (HPF) sets the duration of the pulse by introducing a decay time constant. The low-pass filter (LPF), which follows, increases the rise time to limit the noise bandwidth. Although pulse shapers are often more sophisticated and complicated, the CR-RCⁿ shaper contains the essential features of all pulse shapers, a lower frequency bound, and an upper frequency bound and it is basically a $(n + 1)$ order band pass filter (BPF), where n is the lossy integrators number. The transfer function of an S-G pulse shaper consisting of one CR differentiator and n lossy integrators (Figure 2) is

FIGURE 2: Principal diagram of n order semi-Gaussian shaper using a CR HP filter.

given by [6]

$$H(s) = \left(\frac{s\tau_d}{1 + s\tau_d} \right) \left(\frac{A}{1 + s\tau_i} \right)^n = H(s)_{BPF}, \quad (1)$$

where τ_d is the time constant of the differentiator, τ_i of the integrators, and A is the integrators dc gain. The number n of the integrators is called shaper order. Peaking time is the time that shaper output signal reaches the peak amplitude and is defined by $\tau_s = n\tau_i$. The order n or the peaking time τ_s , depending on the application, can be predefined by the design specifications or not.

The operating bandwidth of an S-G shaper is given by

$$BW = f_i - f_d = \frac{1}{2\pi\tau_i} - \frac{1}{2\pi\tau_d}. \quad (2)$$

Most of the work done on pulse shaping filters is addressed on discrete systems using operational amplifiers as the basic active building block and not in integrated structures [24]. This is due to the fact that the main problem in the design of VLSI shaping amplifiers for nuclear spectroscopy is the implementation of long shaping times of the order of μs for which high value resistors (in the M Ω range) and/or capacitors (in the 100 pF range) are demanded. In fact, the practical values in terms of occupied area that can be integrated are in the tens of k Ω range for the resistors and in the pF range for the capacitors. However, considering the above shaper models, and using specific advanced filter design techniques, and transconductance circuits and current conveyors as the basic building cells, fully integrated SG shapers with long shaping times can be provided.

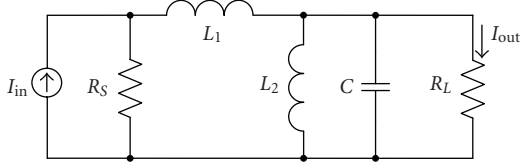


FIGURE 3: third-order band pass RLC minimum capacitance two port filter representing a second-order S-G shaper.

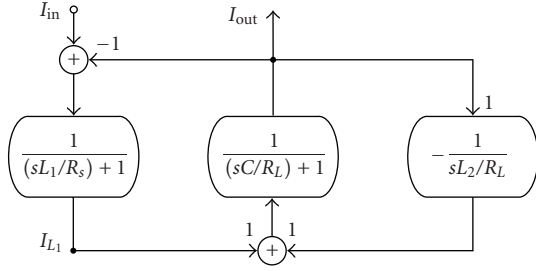


FIGURE 4: Signal flow graph of a current mode third-order BP RLC filter.

In order to design fully integrated shaper structures, advanced filter design methods were used [19, 20]. The respective passive minimum capacitance third-order band pass filter RLC equivalent two port circuit and the signal flow graph (SFG) of a second-order current mode SG shaper are shown in Figures 3 and 4, respectively.

The output current of the RLC BPF describing the SFG is given below providing basically the respective transfer function of the RLC equivalent circuit of Figure 3,

$$\frac{1}{sL_1/R_S + 1} (I_{in} - I_{out}) = I_{out} \frac{1}{sL_2/R_L} + I_{out} sCR_L + I_{out}. \quad (3)$$

From the above SFG and using three advanced filter design methods the Leapfrog (LF) technique, the Ladder simulation method by element replacement, and the typical cascade filter technique with element replacement [25], three fully integrated current mode S-G shapers are designed using CCII and three respective structures using OTAs.

In order to calculate the values of the RLC two port equivalent passive elements and consequently the shaper passive elements, the total system transfer function should be studied in the time domain.

The total CSA second-order S-G Shaper system transfer function is given by

$$H(s)_{total} = \underbrace{\left(\frac{A_{pr}}{1 + s\tau_{pr}} \right)}_{H(s)_{preamp}} \underbrace{\left(\frac{s\tau_d}{1 + s\tau_d} \right) \left(\frac{A_{sh}}{1 + s\tau_i} \right)}_{H(s)_{shaper}}, \quad (4)$$

where A_{pr} is the preamplifier gain and τ_{pr} is its rise time constant.

If the system input signal is a dirac pulse $\delta(t)$, by taking the inverse Laplace transform of the product, the output signal in the time domain is given by

$$h_{total}(t) = \int_{\sigma-j\omega}^{\sigma+j\omega} H_{total}(s) \cdot e^{st} ds. \quad (5)$$

By solving the above integral, the output signal of the readout system is found,

$$h_{total}(t) = A_{pr} \cdot A_{sh} \cdot (k_1 e^{-t/\tau_{pr}} + k_2 e^{-t/\tau_d} + k_3 e^{-t/\tau_i} + k_4 t e^{-t/\tau_i}), \quad (6)$$

where k_1, k_2, k_3 , and k_4 are constants. Their values are given below:

$$\begin{aligned} k_1 &= \frac{1}{\tau_{pr}} \left/ \left[\left(\frac{1}{\tau_{pr}} \right)^3 - \left(\frac{1}{\tau_{pr}} \right)^2 \left(\frac{1}{\tau_d} + 2 \frac{1}{\tau_i} \right) + \frac{1}{\tau_{pr}} \cdot \frac{1}{\tau_i} \left(\frac{1}{\tau_i} + 2 \frac{1}{\tau_d} \right) - \frac{1}{\tau_d} \left(\frac{1}{\tau_i} \right)^2 \right] \right., \\ k_2 &= \frac{1/\tau_d}{(1/\tau_d - 1/\tau_{pr}) \cdot (1/\tau_i - 1/\tau_d)^2}, \\ k_3 &= \frac{1/\tau_{pr} \cdot 1/\tau_d - (1/\tau_i)^2}{(1/\tau_i - 1/\tau_{pr})^2 \cdot (1/\tau_i - 1/\tau_d)^2}, \\ k_4 &= \frac{(1/\tau_{pr} + 1/\tau_d - 1/\tau_i) \cdot (1/\tau_i)^2 - 1/\tau_{pr} \cdot 1/\tau_d \cdot 1/\tau_i}{(1/\tau_i - 1/\tau_{pr})^2 \cdot (1/\tau_i - 1/\tau_d)^2}. \end{aligned} \quad (7)$$

Using the above equations, the values of all shaper model passive elements (R, L, C) and consequently the final integrated shaper structure elements are selected in order to design shaper structures which would satisfy the respective peaking time specification.

3. CURRENT MODE S-G SHAPERS USING ADVANCED DESIGN TECHNIQUES

Six current mode second-order S-G shaper topologies were designed. The first three topologies were based on a second generation current conveyor (CCII) and the other three on an operational transconductance amplifier (OTA). All the configurations were designed for a specific low-energy X-rays strip detector (for a specified preamplifier rise time constant equal to $1.83 \mu\text{sec}$, differentiator time constant equal to $1.5 \mu\text{sec}$ and integrators time constant of $0.5 \mu\text{sec}$) [26] and provide an operating bandwidth (BW) of 230 kHz which respects to a peaking time equal to $1.7 \mu\text{s}$. The passive element values of the RLC band pass filter of Figure 3 where the Leapfrog and the LC Ladder configurations are based, and provide the ideal ac response, are $R_S = 100 \text{ k}\Omega$, $R_L = 100 \text{ k}\Omega$, $L_1 = 103.3 \text{ mH}$, $L_2 = 74.4 \text{ H}$, and $C = 11.71 \text{ pF}$.

3.1. CCII-based current mode shapers

Three second-order shapers are designed using the Leapfrog (LF), the Ladder simulation method by element replacement,

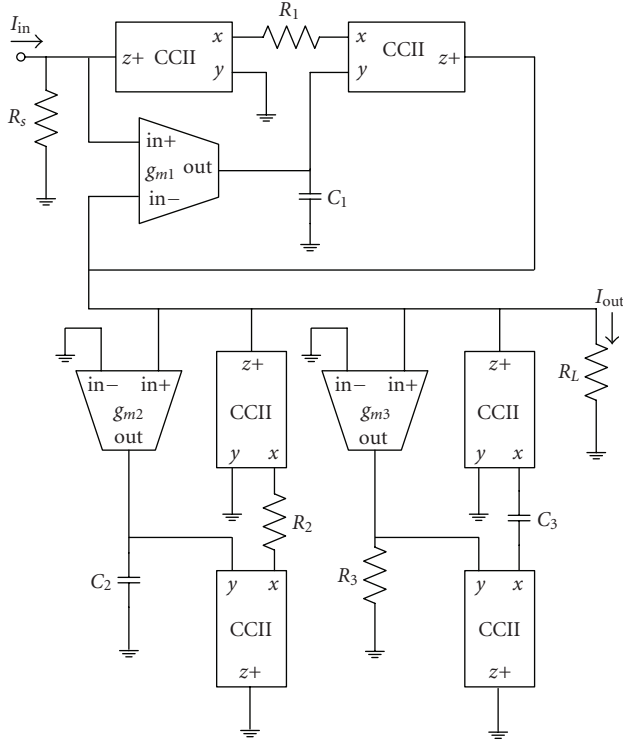


FIGURE 5: CCII-based LC ladder second-order S-G shaper using simulation by element replacement.

TABLE 1: Shapers passive elements and transconductances.

LC ladder	Leapfrog	Cascade
R_S, R_L 1 k Ω	R_1 100 k Ω	R_1 100 Ω
R_1 10 k Ω	R_2 100 k Ω	R_2 100 k Ω
R_2 65 k Ω	R_3 5 k Ω	R_3 50 k Ω
R_3 100 k Ω	R_4 100 k Ω	C_1 5 pF
C_1 9.2 pF	C_1 9.1 pF	C_2 5 pF
C_2, C_3 15 pF	C_2 11.7 pF	C_3 5 pF
g_{m1} 91 μ A/V	C_3 12.1 pF	g_m 1.6 μ A/V
g_{m2} 1.3 μ A/V	g_{m1} 91 μ A/V	—
g_{m3} 780 μ A/V	—	—

and the typical cascade filter technique. The basic circuit block of all three shapers is a second-generation current conveyor (CCII). Figures 5, 6, and 7 show the LC ladder shaper with simulation by element replacement, the leapfrog shaper, and the CCII cascade method shaper, respectively. In all the above CCII shaper systems, the same passive element simulator based on two CCII and one operational transconductance amplifier (OTA) is applied [25].

The passive elements and the OTA transconductances of all the above configurations are given in Table 1. The passive elements simulated value and the specific simulation topologies are shown in Table 2.

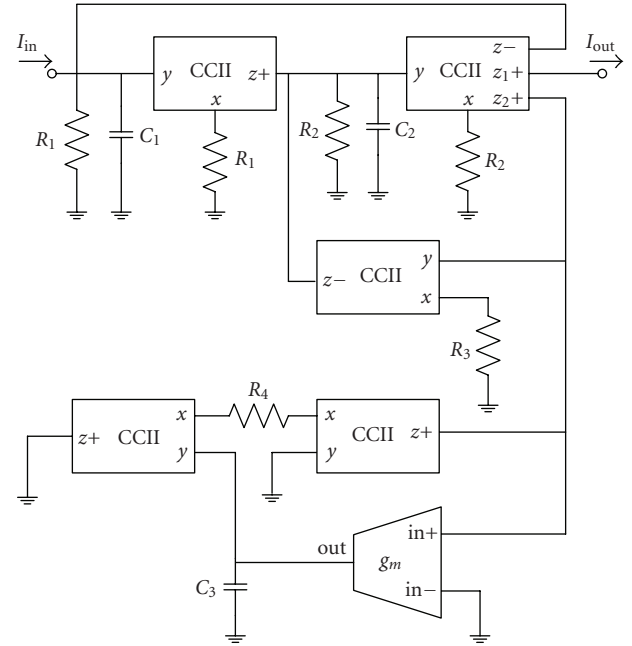


FIGURE 6: CCII-based leapfrog second-order S-G shaper.

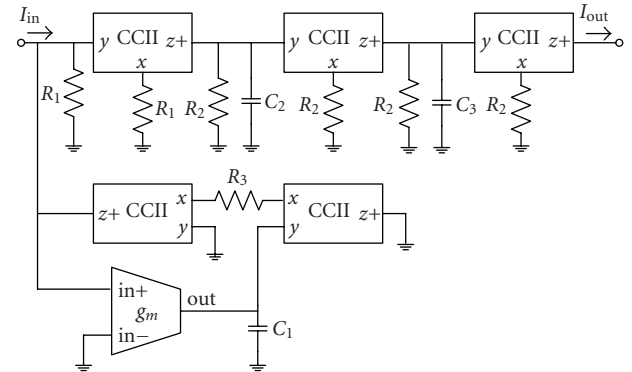


FIGURE 7: CCII-cascade method second-order S-G shaper with inductor simulator.

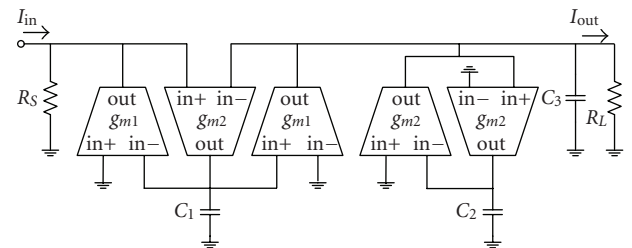

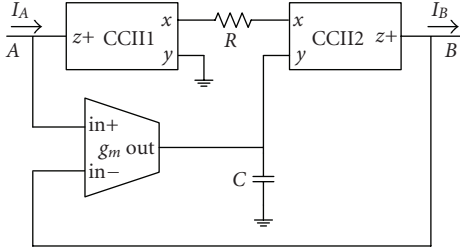

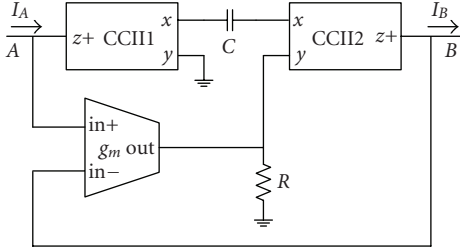


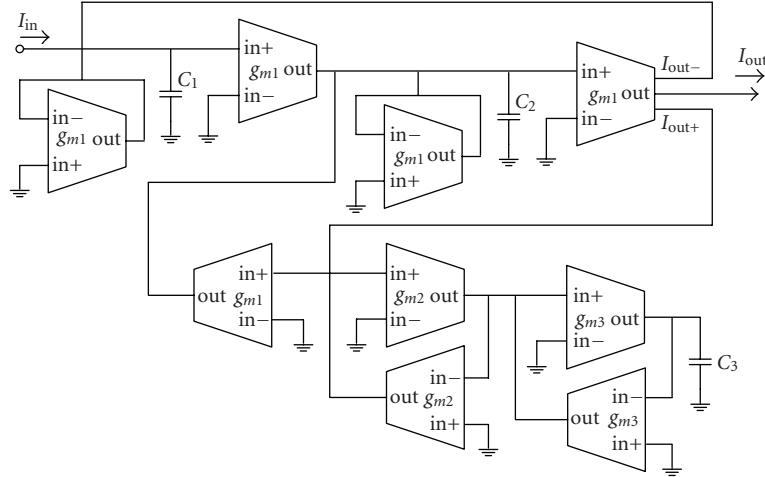
FIGURE 8: OTA-based LC ladder second-order S-G shaper using simulation by element replacement.

3.2. OTA-based current mode shapers

Three respective current mode shaper structures were also designed using operational transconductance amplifiers (OTAs). Figures 8, 9, and 10 show the LC ladder shaper with

TABLE 2: Passive element simulators.

	Passive element	Simulator	Simulated value
Inductor			$L_{eq} = \frac{R}{g_m} C$
Capacitor			$C_{eq} = R g_m C$

FIGURE 9: OTA-based leapfrog second-order S-G shaper with capacitance simulator (considering $R_s = R_L$).

simulation by element replacement, the leapfrog shaper, and the OTA-based cascade method shaper (cascading of a differentiator and two lossy integrators), respectively, using only OTAs as the shaper building blocks. OTA-based inductance and capacitor boosting topologies are used in the cascade OTA shaper and the LF shaper, respectively [19].

The passive elements and the OTA transconductances of all the above configurations are given in Table 3. The respective OTA-based passive elements simulators [27, 28] are given in Table 4.

4. SIMULATION RESULTS

All the above shaper implementations were designed in a $0.6\mu\text{m}$ process by Austria Mikro Systeme (AMS). The power

supplies are $V_{dd} = -V_{ss} = 2.5\text{V}$. Simulations were performed using SPICE (BSIM3V3.2 MOSFET model, Level 49).

4.1. CCII-based current mode S-G shapers

A typical CMOS second generation current conveyor was designed in order to implement the above CCII based shaper structures. The respective CCII schematic is shown in Figure 11. This CCII structure can provide one or multiple outputs (inverting Z- and noninverting Z+) and consequently ensures a more flexible system design. The design concept of the second generation current conveyors that were used in the shaper implementations is clearly demonstrated

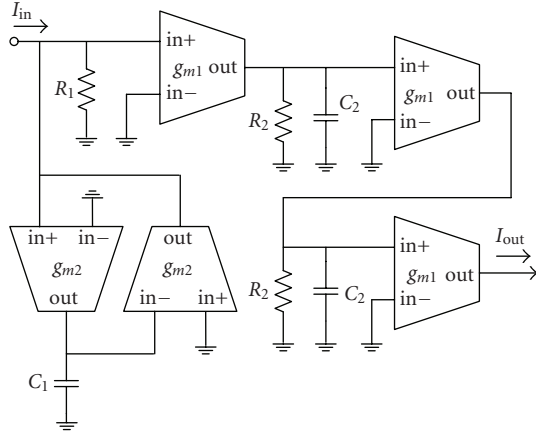


FIGURE 10: OTA-cascade method second-order S-G shaper with inductor simulator.

TABLE 3: Shapers passive elements and transconductances.

LC ladder	Leapfrog	Cascade
R_S, R_L 100 k Ω	C_1 11.7 pF	R_1 11 k Ω
C_1, C_2, C_3 11.7 pF	C_2 13.3 pF	R_2 100 k Ω
g_{m1} 24 μ A/V	C_3 3.7 pF	C_1 4.2 pF
g_{m2} 500 nA/V	g_{m1} 11.4 μ A/V	C_2 5 pF
—	g_{m2} 24 μ A/V	g_{m1} 38 μ A/V
—	g_{m3} 500 nA/V	g_{m2} 500 nA/V

in Figures 11(a) and 11(b), where the transistor level synthesis is given with the respective circuit symbol.

The operational transconductance amplifier (OTA) is implemented using a CMOS configuration with a cascade structure (Figure 12) [26].

The MOS dimensions of the OTAs and the CCII circuit which were used in the implementation of the CCII-based shaper structures are given in Table 5. The bias current I_0 in the CCII circuit was 50 μ A and the bias voltages were $V_{bias1} = 0.7$ V and $V_{bias2} = 0.3$ V. The bias voltage of each OTA circuit was -1.5 V.

The CCII-based shapers have the same operating bandwidth (BW) at 230 kHz. Their frequency response is given in Figure 13.

The difference of the output current amplitude signal and in particular the lower gain of the LC Ladder and the Leapfrog structures is caused by the fact that the specific filter design methods reduce the output signal amplitude by half.

The total performance characteristics of each shaper are listed in Table 6.

The higher maximum bias current is observed in the CCII cascade shaper and the lower minimum in the CCII-based LC ladder shaper and the CCII leapfrog shaper. The first two configurations appear to be low power in comparison to the cascade band pass filter. The third implementation, as the first one, provides a dynamic range equal to 35 dB.

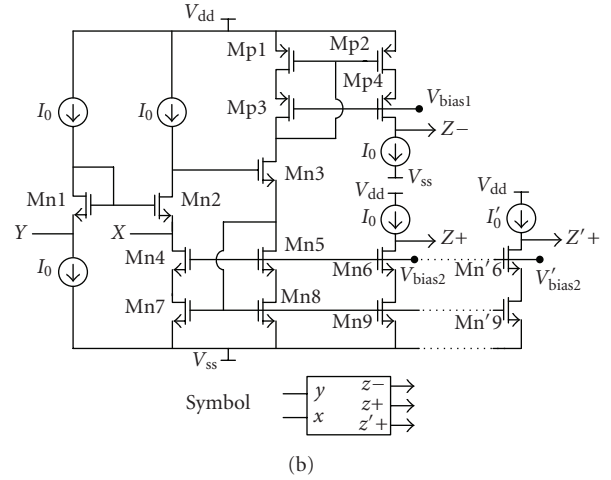
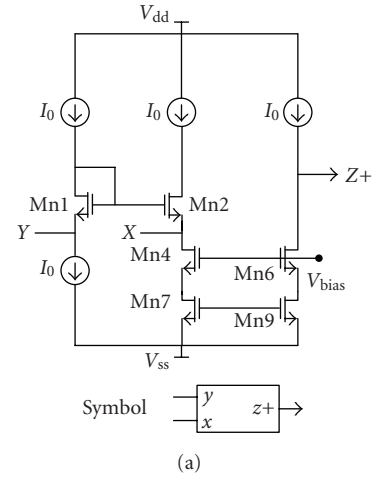


FIGURE 11: CMOS second-generation current conveyor (a) positive and (b) with positive and negative multiple outputs.

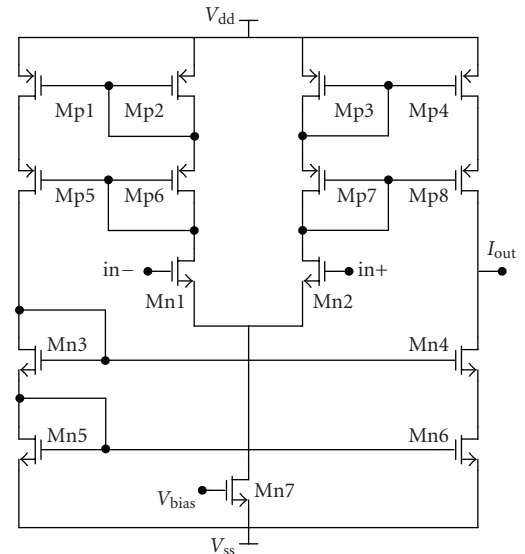


FIGURE 12: CMOS operational transconductance amplifier.

TABLE 4: OTA-based passive elements simulators [27].


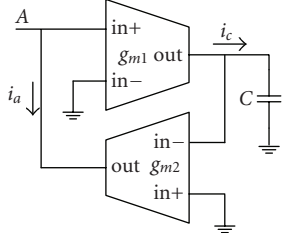

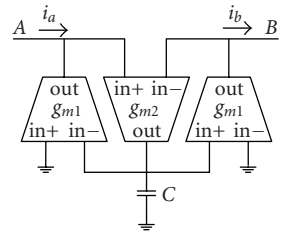

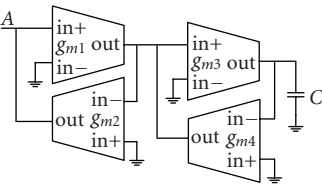
	Passive elements	OTA simulator	Simulated value
Grounded inductor			$L_{eq} = \frac{C}{g_{m1}g_{m2}}$
Floating inductor			$L_{eq} = \frac{C}{g_{m1}g_{m2}}$
Grounded capacitor			$C_{eq} = C \frac{g_{m1}g_{m2}}{g_{m3}g_{m4}}$

TABLE 5: MOS dimensions of the OTAs and the CCII circuit.

CCII	OTA (g_m)	OTA (g_{m1})	OTA (g_{m2})	OTA (g_{m3})
MOSFETs $W(\mu m)/L(\mu m)$	MOSFETs $W(\mu m)/L(\mu m)$	MOSFETs $W(\mu m)/L(\mu m)$	MOSFETs $W(\mu m)/L(\mu m)$	MOSFETs $W(\mu m)/L(\mu m)$
Mn1, Mn2, Mn3 150/4	Mn1, Mn2, Mn3, Mn4 1.5/40	Mn1, Mn2, Mn3, Mn4 1.5/50	Mn1, Mn2, Mn3, Mn4 1.5/1	Mn1, Mn2, Mn3, Mn4 3/0.8
Mn4, Mn5, Mn6 28/4	Mn5, Mn6, Mn7 26/20	Mn5, Mn6, Mn7 26/25	Mn5, Mn6, Mn7 52/1	Mn5, Mn6, Mn7 104/0.8
Mn7, Mn8, Mn9 13/4	Mp5, Mp6, Mp7, Mp8 2/20	Mp5, Mp6, Mp7, Mp8 4.5/50	Mp5, Mp6, Mp7, Mp8 4.5/1	Mp5, Mp6, Mp7, Mp8 9/0.8
Mp1, Mp2 26/4	Mp1, Mp2, Mp3, Mp4 25/20	Mp1, Mp2, Mp3, Mp4 25/25	Mp1, Mp2, Mp3, Mp4 50/1	Mp1, Mp2, Mp3, Mp4 100/0.8
Mp3, Mp4 132/4	— —	— —	— —	— —

Concerning the noise performance, the CCII leapfrog structure is the optimum since the output rms noise current is much lower in relation to the ladder shaper and the cascade one. The above characteristics, despite the fact that the same implementation is the worst in terms of the total harmonic distortion, render it suitable for applications where the DR

is not required to be very high but the noise and power consumption limits are the main factors that determine the application as in the readout front ends.

Figure 14 shows the signal-to-noise ratio of the three CCII-based shapers. As it can be seen, the Leapfrog configuration has the better SNR.

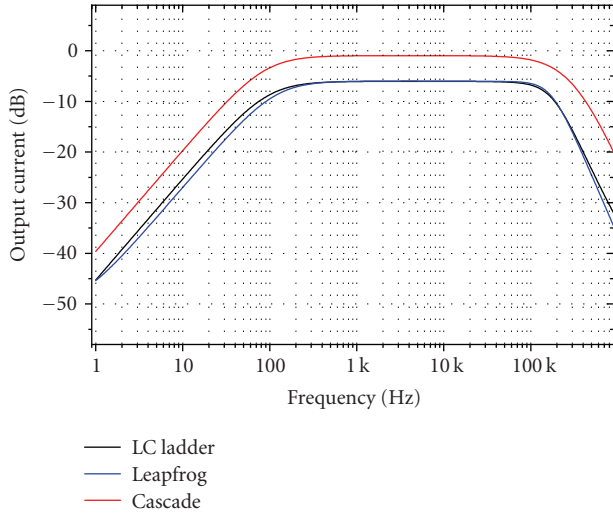


FIGURE 13: CCII-based shapers frequency response.

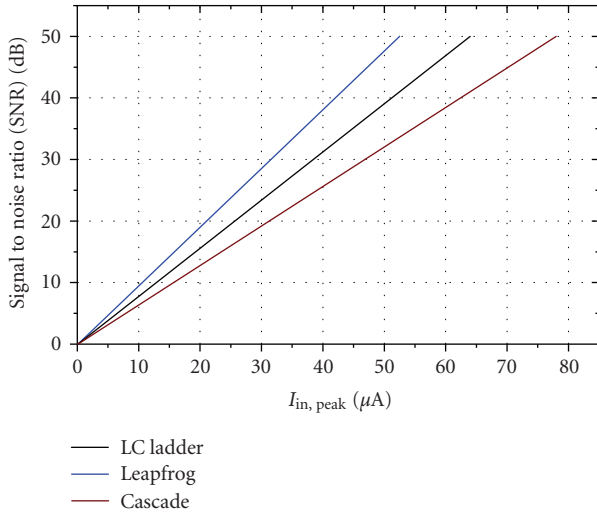


FIGURE 14: Signal-to-noise ratio of the CCII-based shapers.

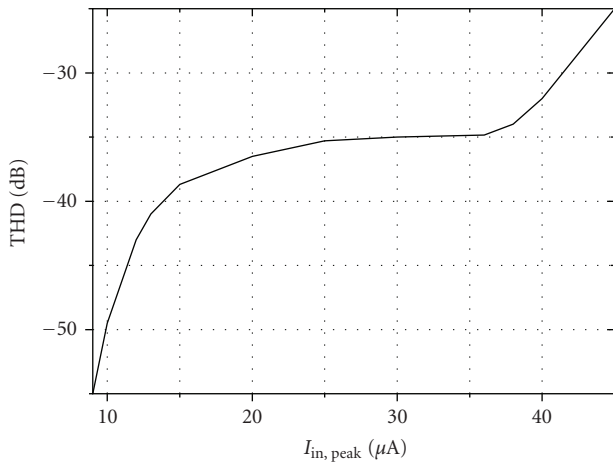


FIGURE 15: THD of the CCII-based LC ladder S-G shaper.

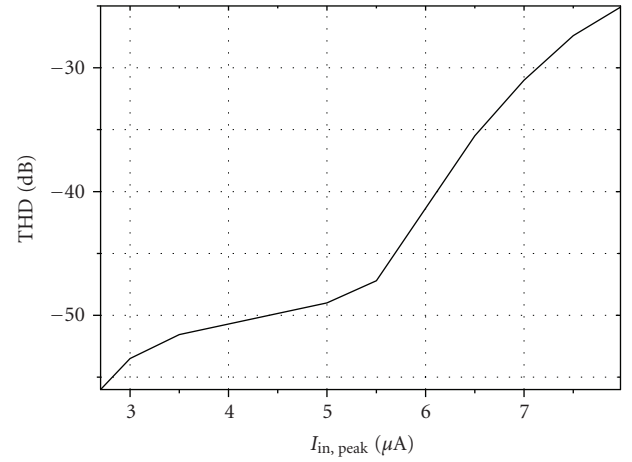


FIGURE 16: THD of the CCII-based leapfrog S-G shaper.

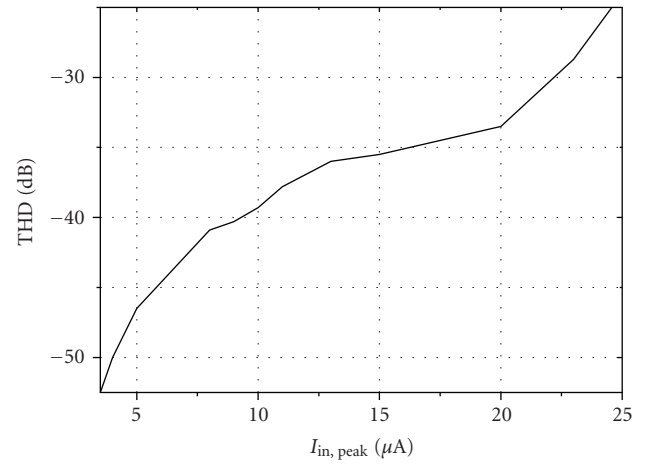


FIGURE 17: THD of the CCII-based cascade S-G shaper.

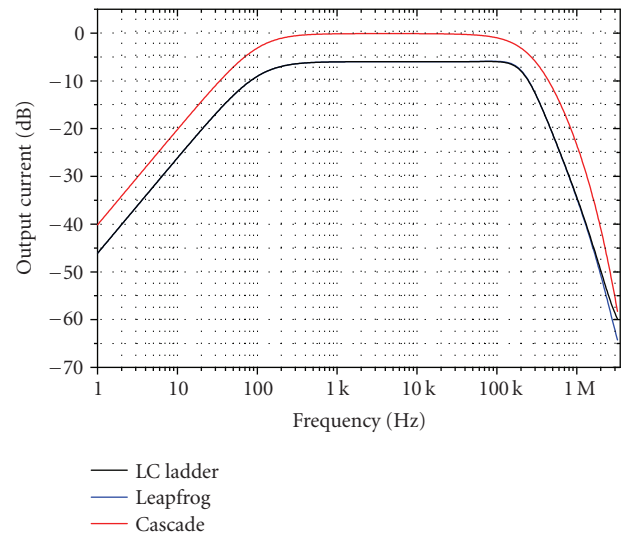


FIGURE 18: OTA-based shapers frequency response.

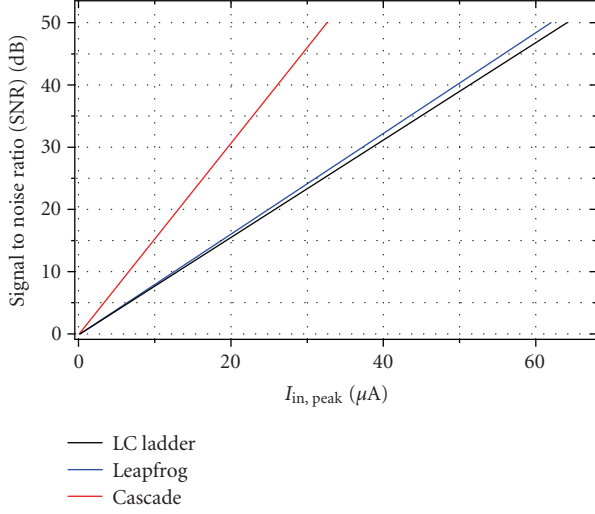


FIGURE 19: Signal-to-noise ratio of the OTA-based shapers.

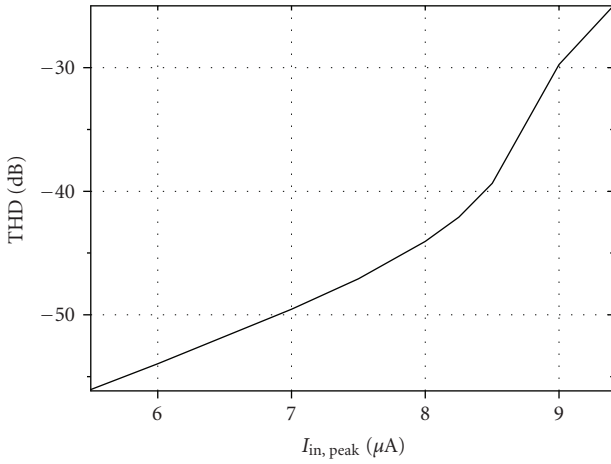


FIGURE 20: THD of the OTA-based LC ladder S-G shaper.

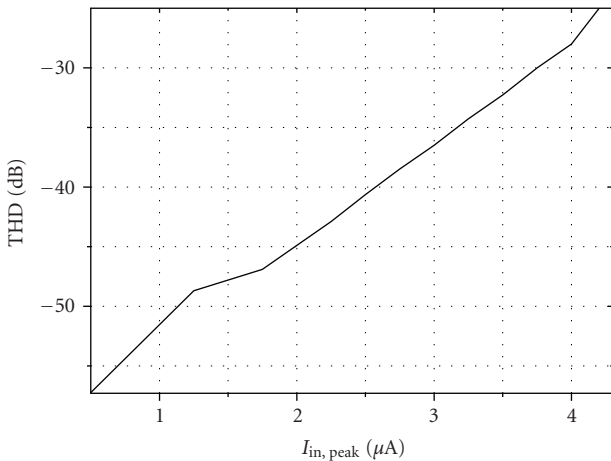


FIGURE 21: THD of the OTA-based leapfrog S-G shaper.

TABLE 6: CCII shapers performance characteristics.

	LC ladder	Leapfrog	Cascade
Maximum bias current	41 μ A	100 μ A	115 μ A
Minimum bias current	243 nA	244 nA	304 nA
Power consumption	5.5 mW	5.5 mW	9.0 mW
$I_{in,peak} - 40$ dB (THD = 1%)	14 μ A	6.1 μ A	9.2 μ A
Output noise (rms)	87 nA	72 nA	116 nA
Dynamic range (DR)	35 dB	30 dB	35 dB

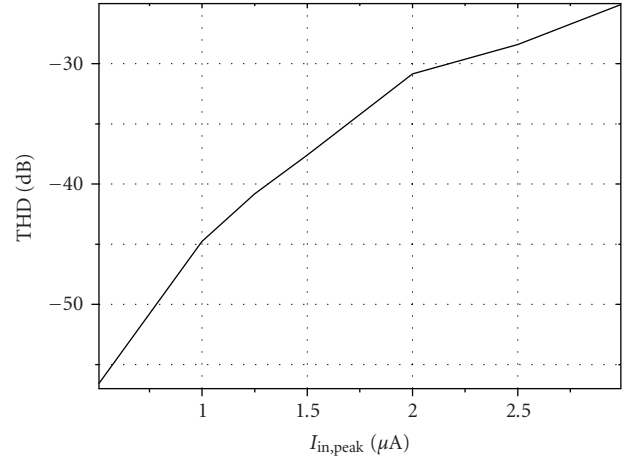


FIGURE 22: THD of the OTA-based cascade S-G shaper.

The total harmonic distortion (THD) of each CMOS CCII-based shaper topology is shown in (Figures 15–17).

4.2. OTA-based current mode S-G shapers

The same CMOS operational transconductance amplifier (Figure 12) was also used in order to implement the OTA-based shaper structures. The bias voltage of each OTA circuit was also -1.5 V.

The MOS dimensions of the transconductance circuits that were used in the implementation of the OTA-based shaper structures are given in Table 7.

Their frequency response ($BW = 230$ kHz) is given in Figure 18.

The total performance characteristics of each shaper system are listed in Table 8.

The higher maximum bias current is observed in the OTA cascade shaper and the lower minimum in almost the same in all three configurations. All the shapers appear to be low power, but the LC ladder shaper provides the optimum power consumption performance. Additionally, the cascade and the LF structure provide a dynamic range equal to 22 dB, far lower than the 32 dB value of the LC ladder topology. Concerning the noise performance, all the structures appear to have low rms output noise, with the cascade shaper being slightly worse in comparison to the other two.

TABLE 7: MOS dimensions of the OTAs.

	LC ladder		Leapfrog			Cascade	
	g_{m1}	g_{m2}	g_{m1}	g_{m2}	g_{m3}	g_{m1}	g_{m2}
MOSFETs	$W(\mu m)/L(\mu m)$						
Mn1, Mn2, Mn3, Mn4	1.4/3	1.4/6	1.4/6	1.2/100	1.4/3	1.4/7.6	1.2/100
Mn5, Mn6, Mn7	52/3	52/6	52/6	2.2/10	52/3	52/7.6	2.2/10
Mp1, Mp2, Mp3, Mp4	50/3	50/6	50/6	4.3/10	50/3	50/7.6	4.3/10
Mp5, Mp6, Mp7, Mp8	4.5/3	4.5/6	4.5/6	3.9/100	4.5/3	4.5/7.6	3.9/100

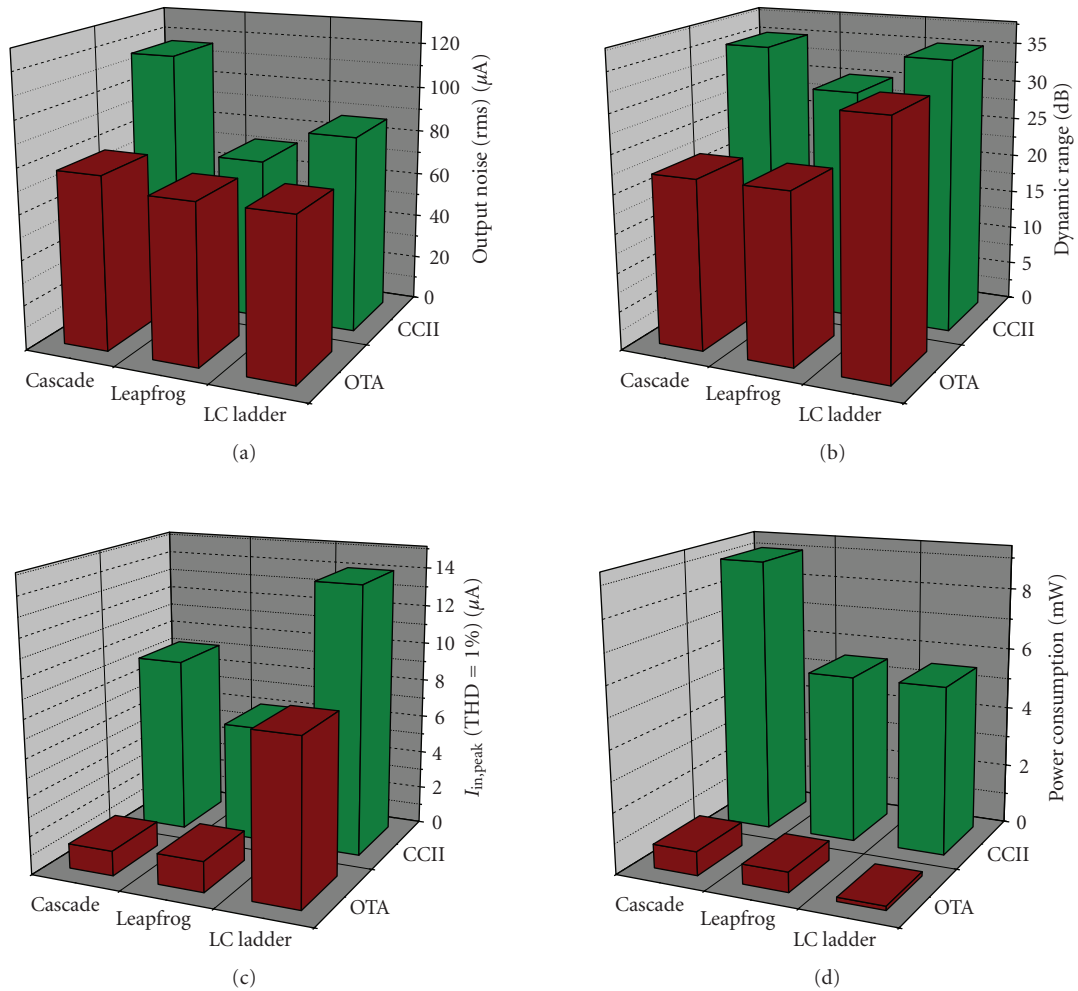


FIGURE 23: Performance comparison of the OTA- and CCII-based S-G shapers.

The above characteristics, and in relation to the fact that the LC Ladder architecture is the optimum in terms of the total harmonic distortion and the DR, render it as the most optimum among the other topologies.

Figure 19 shows the signal-to-noise ratio of the three OTA-based shapers.

The total harmonic distortion (THD) of each CMOS OTA-based shaper topology, is shown in (Figures 20–22).

TABLE 8: OTA-based shapers performance characteristics.

	LC ladder	Leapfrog	Cascade
Maximum bias current	2.2 μ A	4.7 μ A	35.8 μ A
Minimum bias current	83.5 nA	83.1 nA	83.6 nA
Power consumption	133 μ Watt	648 μ Watt	787 μ Watt
$I_{in,peak-40\text{ dB}}$ (THD = 1%)	8.43 μ A	2.6 μ A	1.3 μ A
Output noise (rms)	71 nA	71 nA	77 nA
Dynamic range (DR)	32 dB	22 dB	22 dB

4.3. Comparison of CCII- and OTA-based S-G shapers

In Figure 23, a comparison between the OTA-based shapers and the CCII shaper topologies is clearly shown. As it is obvious, the OTA-based shaper structures appear to be more advantageous in comparison to the CCII ones. The main differentiation is shown in the total harmonic distortion and in the power consumption performance. In particular, the OTA shaping structures provide much lower power consumption and distortion levels in comparison to the CCII topologies. Considering the above advantages and in relation to the fact that in the OTA shaper topologies no resistors are used, the OTA structures seem to be the optimum selection.

5. CONCLUSIONS

In this paper, a detailed examination of current conveyor and operational transconductance amplifiers-based semi-Gaussian shapers suitable for readout applications is performed. Specifically, respective current mode shaper structures of each kind are proposed to be used in front-end applications. All shaper implementations are designed using advanced filter design methods such as the Leapfrog and the Ladder LC technique by element replacement. The shapers used in this work provide large peaking time, however they are fully integrated configurations and not discrete systems. A CMOS CCII and an OTA circuit were designed in order to be used in the implementation of the above shapers. The filter configurations are analytically compared in terms of power consumption, total harmonic distortion, dynamic range, and noise performance. The CCII Leapfrog architecture is proved to be the optimum among the CCII-based shapers according to the output noise, SNR, and consumption and on the other hand, the OTA LC Ladder architecture seem to be the more suitable in the OTA topologies, considering the output noise, SNR, power consumption, and total harmonic distortion. Although both categories of topologies, and the CCII and the OTA structures provide satisfactory performance, the OTA based shapers seem to be the more optimum selection considering the power consumption performance and the total harmonic distortion.

ACKNOWLEDGMENTS

The authors wish to thank the reviewers for their constructive comments. Their contribution is greatly acknowledged.

REFERENCES

- [1] V. Radeka, P. Rehak, S. Rescia, et al., "Design of a charge sensitive preamplifier on high resistivity silicon," *IEEE Transactions on Nuclear Science*, vol. 35, no. 1, part 1-2, pp. 155–159, 1988.
- [2] V. Radeka, P. Rahek, S. Rescia, et al., "Implanted silicon JFET on completely depleted high-resistivity devices," *IEEE Electron Device Letters*, vol. 10, no. 2, pp. 91–94, 1989.
- [3] J. C. Lund, F. Olschner, P. Bennett, and L. Rehn, "Epitaxial n-channel JFETs integrated on high resistivity silicon for X-ray detectors," *IEEE Transactions on Nuclear Science*, vol. 42, no. 4, part 1-2, pp. 820–823, 1995.
- [4] P. Lechner, S. Eckbauer, R. Hartmann, et al., "Silicon drift detectors for high resolution room temperature X-ray spectroscopy," *Nuclear Instruments and Methods in Physics Research, Section A*, vol. 377, no. 2-3, pp. 346–351, 1996.
- [5] L. Ratti, M. Manghisoni, V. Re, and V. Speziali, "Integrated front-end electronics in a detector compatible process: source-follower and charge-sensitive preamplifier configurations," in *Hard X-Ray and Gamma-Ray Detector Physics III*, R. B. James, Ed., vol. 4507 of *Proceedings of SPIE*, pp. 141–151, San Diego, Calif, USA, July-August 2001.
- [6] W. M. C. Sansen and Z. Y. Chang, "Limits of low noise performance of detector readout front ends in CMOS technology," *IEEE Transactions on Circuits and Systems*, vol. 37, no. 11, pp. 1375–1382, 1990.
- [7] Z. Y. Chang and W. Sansen, "Effect of $1/f$ noise on the resolution of CMOS analog readout systems for microstrip and pixel detectors," *Nuclear Instruments and Methods in Physics Research Section A*, vol. 305, no. 3, pp. 553–560, 1991.
- [8] T. Noulis, S. Siskos, and G. Sarraayrouse, "Analysis of input and feedback capacitances effect on low noise preamplifier performance for X-rays silicon strip detectors," in *Proceedings of Design of Circuits and Integrated Systems Conference (DCIS '04)*, pp. 473–478, Bordeaux, France, November 2004.
- [9] J. Wulleman, "Current mode charge pulse amplifier in CMOS technology for use with particle detectors," *Electronics Letters*, vol. 32, no. 6, pp. 515–516, 1996.
- [10] F. Yuan, "Low-voltage CMOS current-mode preamplifier: analysis and design," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 53, no. 1, pp. 26–39, 2006.
- [11] F. Anghinolfi, P. Aspell, M. Campbell, et al., "ICON, a current mode preamplifier in CMOS technology for use with high rate particle detectors," *IEEE Transactions on Nuclear Science*, vol. 40, no. 3, pp. 271–274, 1993.
- [12] T. Vanisri and C. Toumazou, "Low-noise optimisation of current-mode transimpedance optical preamplifiers," in *Proceedings of IEEE International Symposium on Circuits and Systems (ISCAS '93)*, vol. 2, pp. 966–969, Chicago, Ill, USA, May 1993.
- [13] A. Arbel, "Innovative current sensitive differential low noise preamplifier in CMOS," in *Proceedings of the 3rd IEEE International Conference on Electronics, Circuits, and Systems (ICECS '96)*, vol. 1, pp. 69–72, Rodos, Greece, October 1996.
- [14] C. Toumazou, F. J. Lidgley, and D. G. Haigh, *Analogue IC Design: The Current-Mode Approach*, Peter Peregrinus, London, UK, 1990.
- [15] A. S. Sedra, G. W. Roberts, and F. Gohh, "Current conveyor. History, progress and new results," *IEEE Proceedings—Part G. Electronic Circuits and Systems*, vol. 137, no. 2, pp. 78–87, 1990.
- [16] S. I. Long and J. Q. Zhang, "Low power GaAs current-mode 1.2 Gb/s interchip interconnections," *IEEE Journal of Solid-State Circuits*, vol. 32, no. 6, pp. 890–897, 1997.

- [17] D. R. Frey, "Log-domain filtering: an approach to current-mode filtering," *IEEE Proceedings—Part G: Circuits, Devices and Systems*, vol. 140, no. 6, pp. 406–416, 1993.
- [18] J. B. Hughes, N. C. Bird, and I. C. Macbeth, "Switched currents—a new technique for analog sampled-data signal processing," in *Proceedings of IEEE International Symposium on Circuits and Systems (ISCAS '89)*, vol. 3, pp. 1584–1587, Portland, Ore, USA, May 1989.
- [19] T. L. Deliyannis, Y. Sun, and K. Fidler, *Continuous-Time Active Filter Design*, CRC Press, Boca Raton, Fla, USA, 1999.
- [20] R. Schaumann and M. E. Valkenburg, *Design of Analog Filters*, Oxford University Press, New York, NY, USA, 2001.
- [21] M. Konrad, "Detector pulse-shaping for high resolution spectroscopy," *IEEE Transactions on Nuclear Science*, vol. 15, no. 1, pp. 268–282, 1968.
- [22] Z. Y. Chang and W. M. Sansen, *Low Noise Wide Band Amplifiers in Bipolar and CMOS Technologies*, chapter 5, Kluwer Academic, Norwell, Mass, USA, 1991.
- [23] S. Ohkawa, M. Yoshizawa, and K. Husimi, "Direct synthesis of the Gaussian filter for nuclear pulse amplifiers," *Nuclear Instruments and Methods*, vol. 138, no. 1, pp. 85–92, 1976.
- [24] G. Shani, *Electronics for Radiation Measurements*, vol. 1, CRC Press, Boca Raton, Fla, USA, 1996.
- [25] R. Senani, "Novel lossless synthetic floating inductor employing a grounded capacitor," *Electronics Letters*, vol. 18, no. 10, pp. 413–414, 1982.
- [26] T. Noulis, C. Deradonis, S. Siskos, and G. Sarraayrouse, "Novel fully integrated OTA based front-end analog processor for X-rays silicon strip detectors," in *Proceedings of the 13th IEEE Mediterranean Electrotechnical Conference (MELECON '06)*, pp. 47–50, Malaga, Spain, May 2006.
- [27] M. Bialko and R. W. Newcomb, "Generation of all finite linear circuits using the integrated DVCCS," *IEEE Transactions on Circuits and Systems*, vol. 18, no. 6, pp. 733–736, 1971.
- [28] R. Schaumann, "Simulating lossless ladders with transconductance-C circuits," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 45, no. 3, pp. 407–410, 1998.