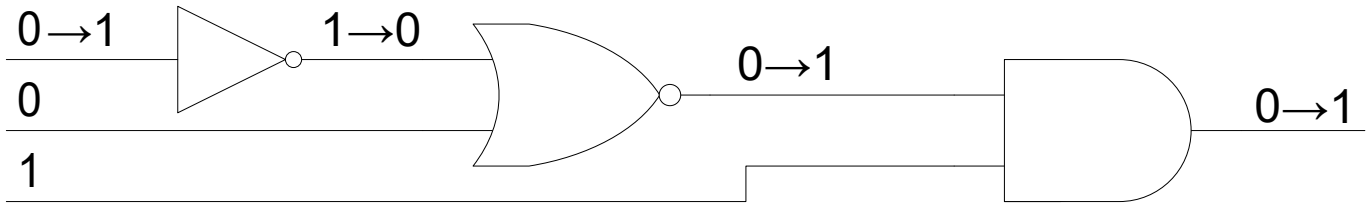
UM EECS 270 F21
Introduction to Logic Design

3. Timing and Delay

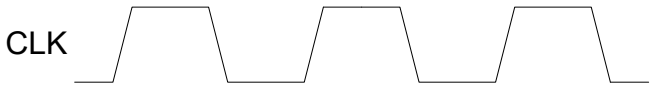
Circuit Timing

- Logic circuits are physical structures built from electronic transistors and wires
- The digital abstraction *ignores physics* and assumes that circuits respond instantaneously
- In real implementations of logic circuits, we must account for *propagation delays*
  - Change at input of gate requires time to propagate through to output
  - Change at output of one gate requires time to reach input of next gate

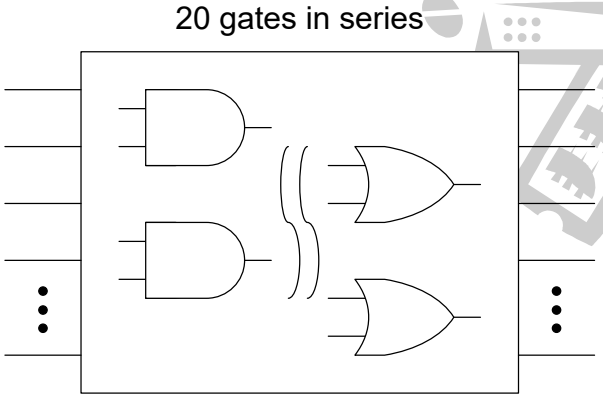


- Digital circuits operate in distinctive steps**:**
  1) Apply inputs to circuit
  2) Wait for outputs to react
  3) Sample outputs at circuit

- The speed of this process is determined by a **clock pulse** signal (often simply called a **clock**)



- Circuits require a fixed time to respond to their inputs – it's important that circuits generate correct outputs *in the alloted time*
  - Being late is as bad as being wrong!



How fast can this circuit be "clocked" if each gate has a delay of 5ns?

20 * 5ns = 100ns

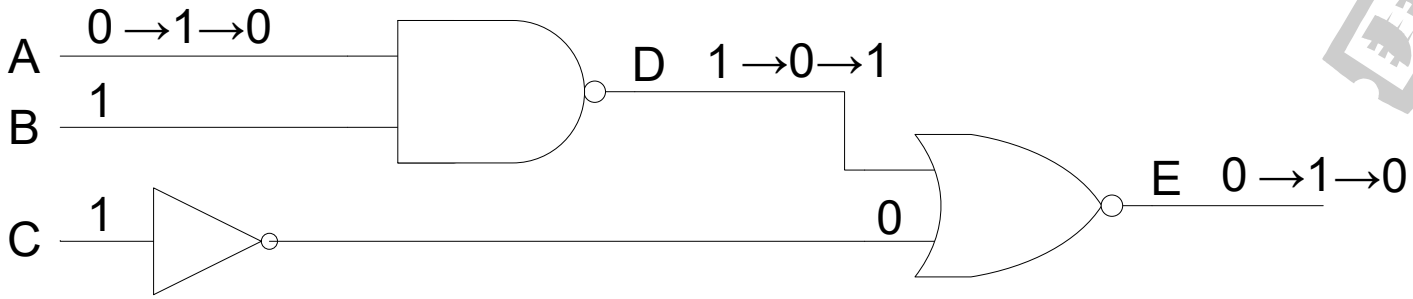
1 / 100ns = **10MHz**

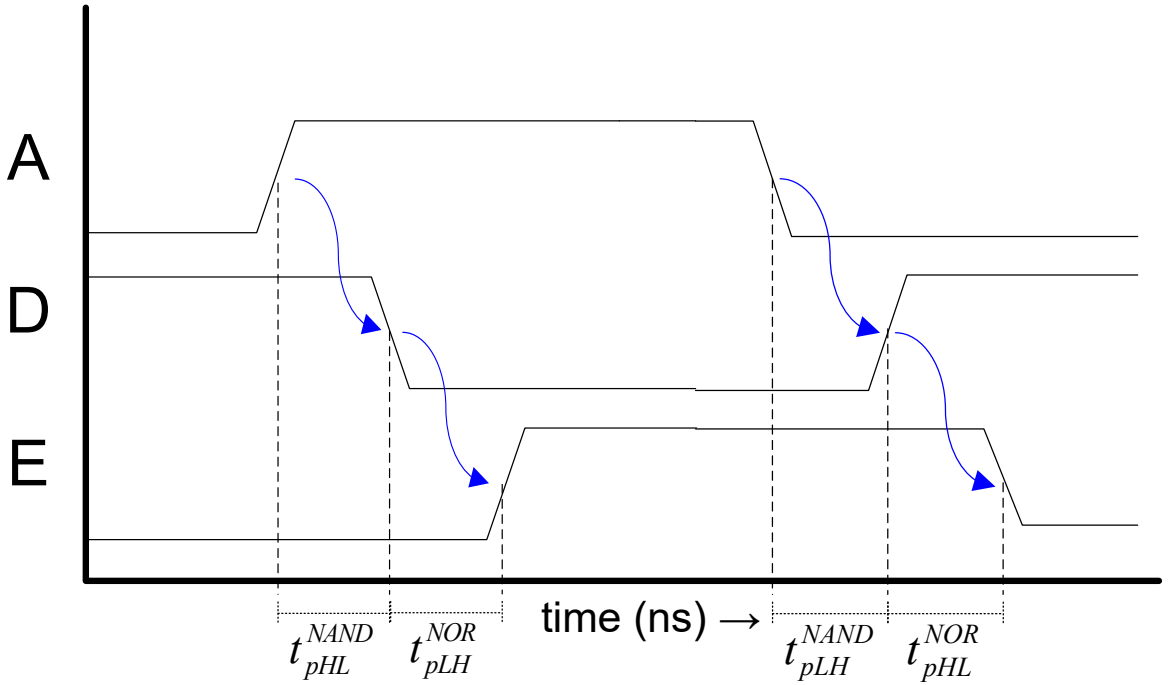
What if each gate has a delay of 50ps?

20 * 50ps = 1ns

1 / 1ns = **1GHz**

Timing Diagrams





Causality Arrow

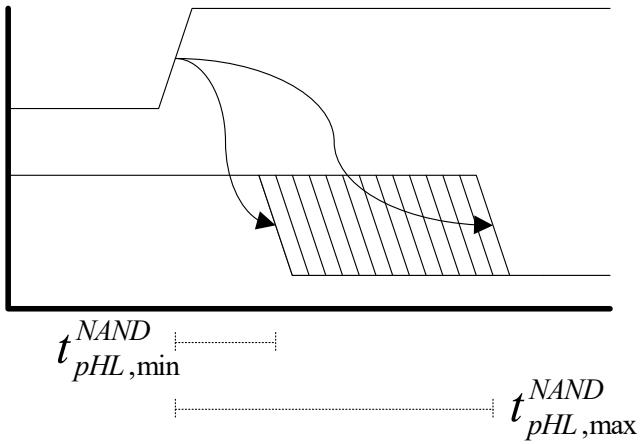
Gate Propagation Delay

t_{pHL}^{NAND}

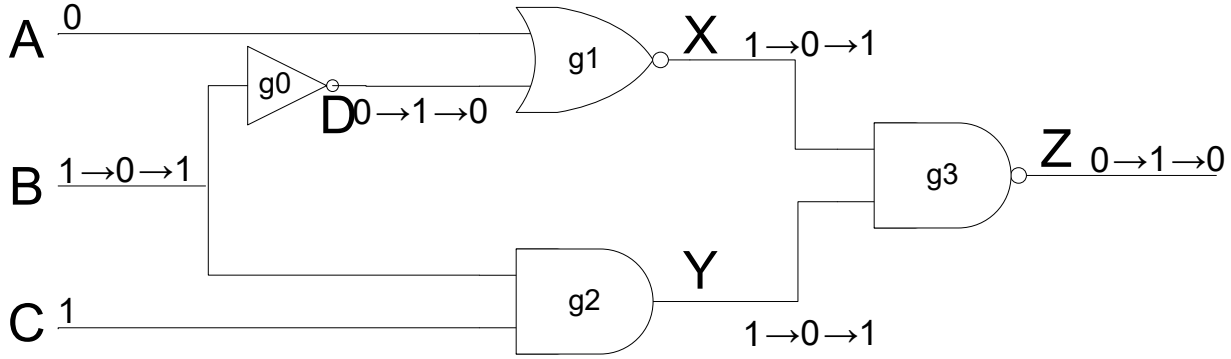
gives NAND gate propagation delay from input to output when output is changing from H to L

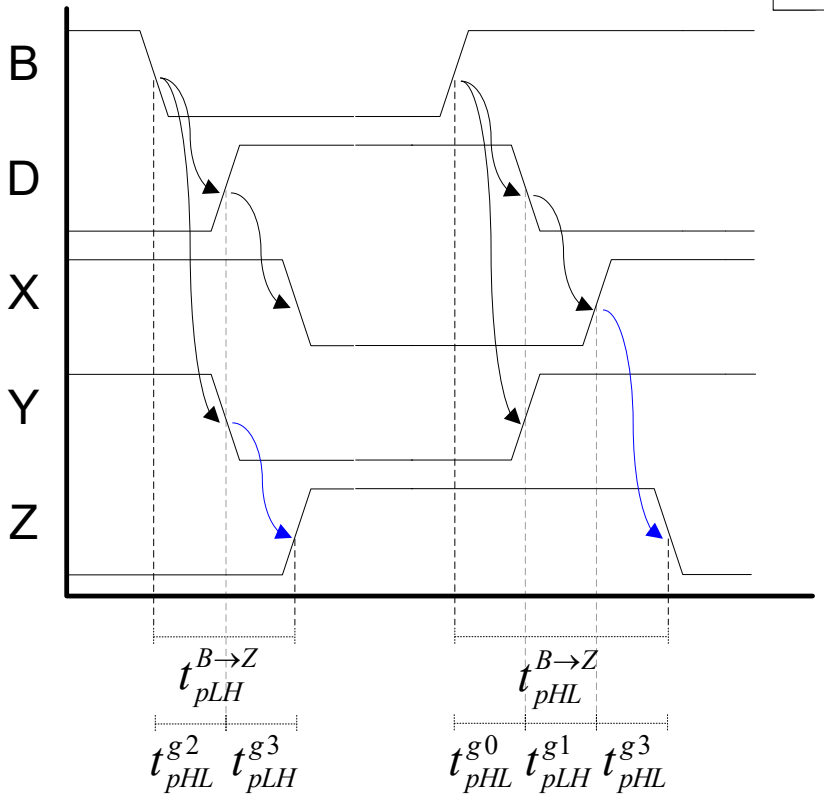
- In general, for a particular gate, $t_{pHL} \neq t_{pLH}$
- Gate delays vary with operating conditions:
  - Operating voltage
  - Temperature
  - Output capacitance
- Therefore, IC designers typically specify:
  - Minimum delay: best case (not very useful!)
  - Maximum delay: worst case
  - Typical delay: "normal" operating conditions
- Often, we'll use $t_p = \max(t_{pHL}, t_{pLH})$ for simplicity

Propagation delay in nanoseconds of 74LS family				
	Typical		**Maximum**	
Part Number	t_{pLH}	t_{pHL}	t_{pLH}	t_{pHL}
00, 01	9	10	15	15
02	10	10	15	15
04	9	10	15	15
08, 11	8	10	15	20
14	15	15	22	22
20	9	10	15	15
21	8	10	15	20
27	10	10	15	15
30	8	13	15	20
32	14	14	22	22
86	12	10	23	17



Multiple paths from input to output





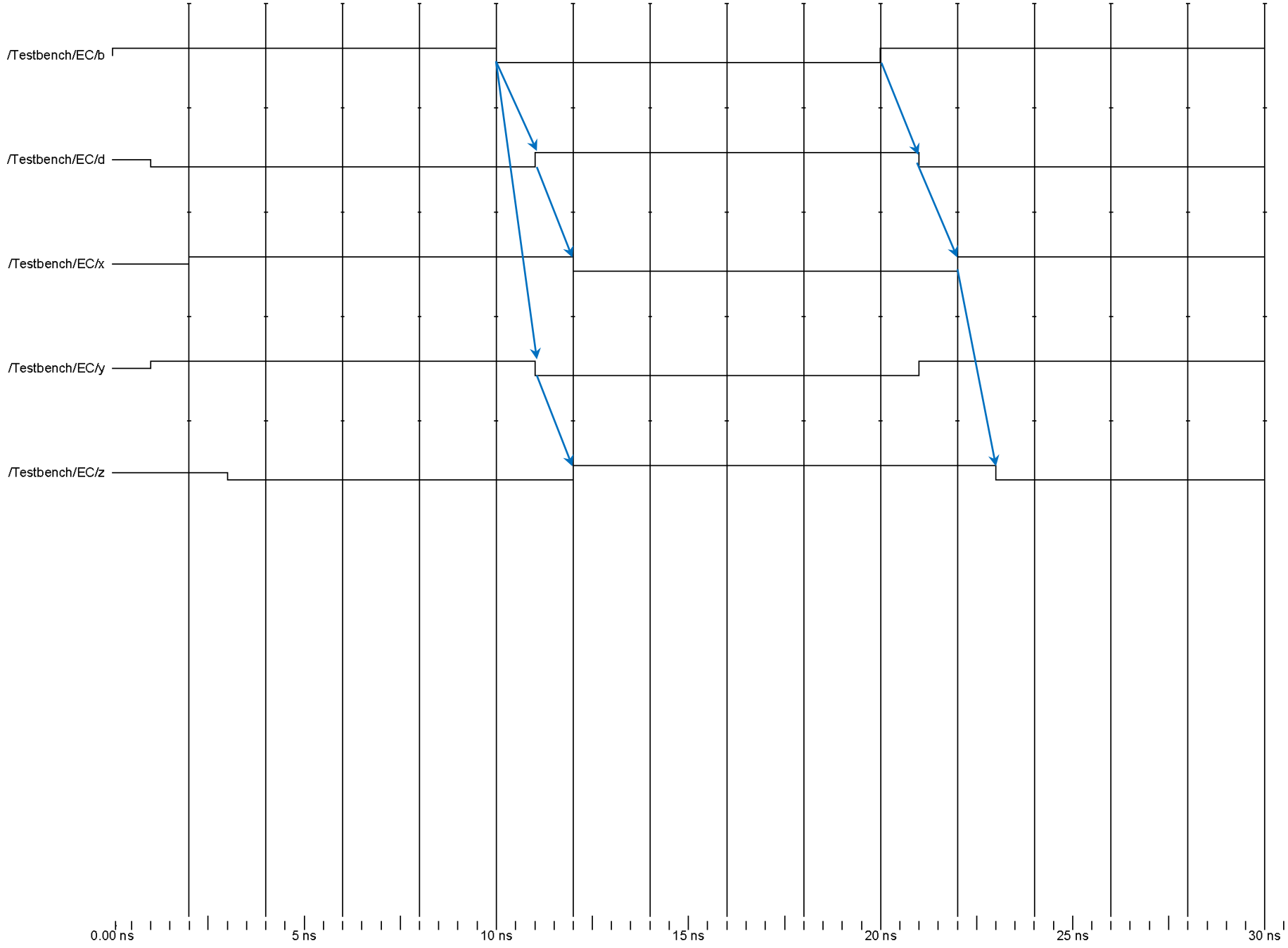
Assume all rising and falling gate delays are 1ns:

$$t_{pLH}^{B\to Z} = t_{pHL}^{g2} + t_{pLH}^{g3} = 2ns$$

$$t_{pHL}^{B\to Z} = t_{pHL}^{g0} + t_{pLH}^{g1} + t_{pHL}^{g3} = 3ns$$

The overall circuit delay depends on the transition path taken from the inputs to the output

Unit-Delay Timing Simulation



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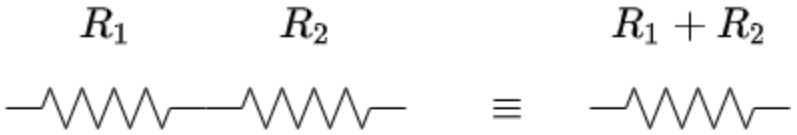
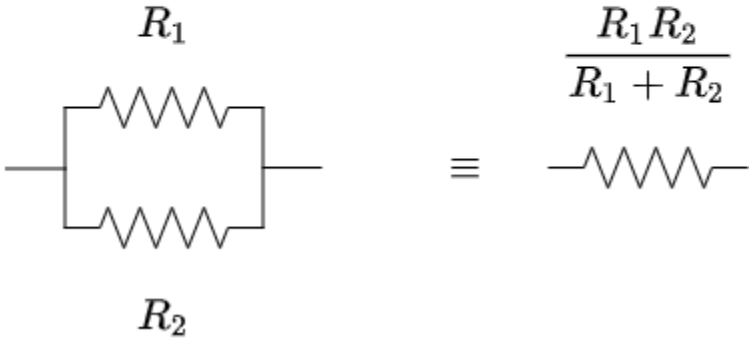
A “Slightly” More Realisitic Delay Model

Delay $\propto$ Transistor Resistance

Resistors in series



Resistors in parallel



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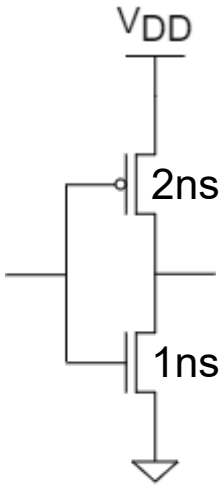
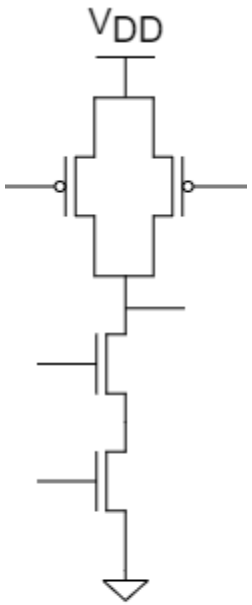
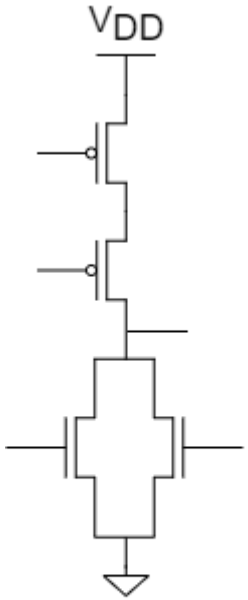
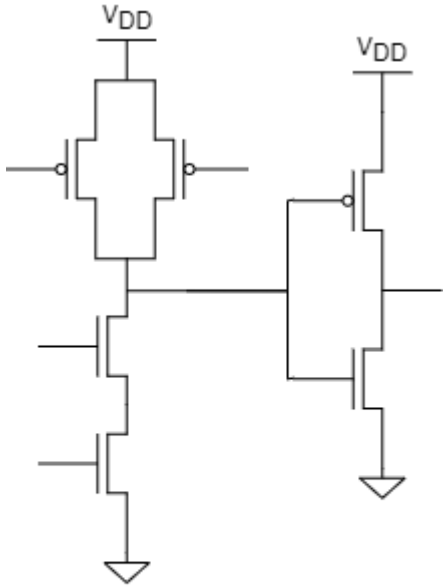








$\#(2,1)$

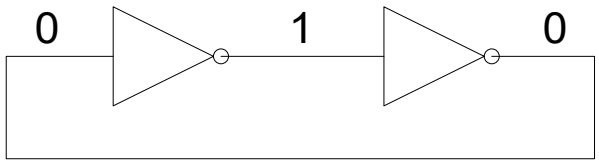
$\#(\frac{2\times 2}{2+2},1+1)$
$= \#(1,2)$

$\#(2+2,\frac{1\times 1}{1+1})$
$= \#(4,0.5)$

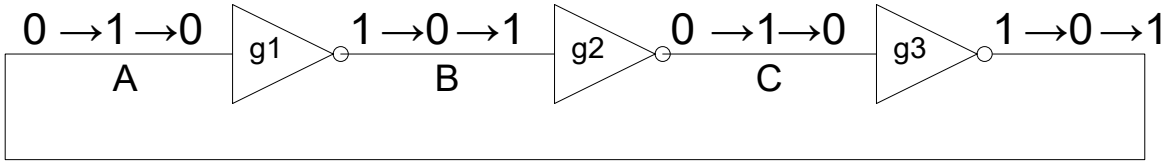
$\#(2+2,1+1)$
$= \#(4,2)$

Rise/Fall-Delay Timing Simulation

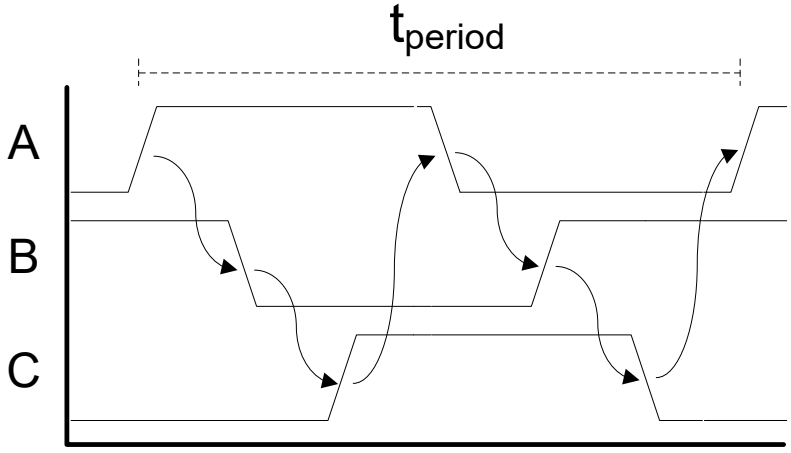
Bi-Stable Circuit & Ring Oscillator



This circuit is **bi-stable**



This circuit is known as a **ring-oscillator**



$$t_{period} = t_{pHL}^{g1} + t_{pLH}^{g2} + t_{pHL}^{g3} + t_{pLH}^{g1} + t_{pHL}^{g2} + t_{pLH}^{g3}$$

Assume all gate delays are 1ns:

$$t_{period} = 6ns \qquad f_{osc} = \frac{1}{6ns} = 166MHz$$