AND8210/D

Current Sensing Power MOSFET Use in DC-DC Converters

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APPLICATION NOTE

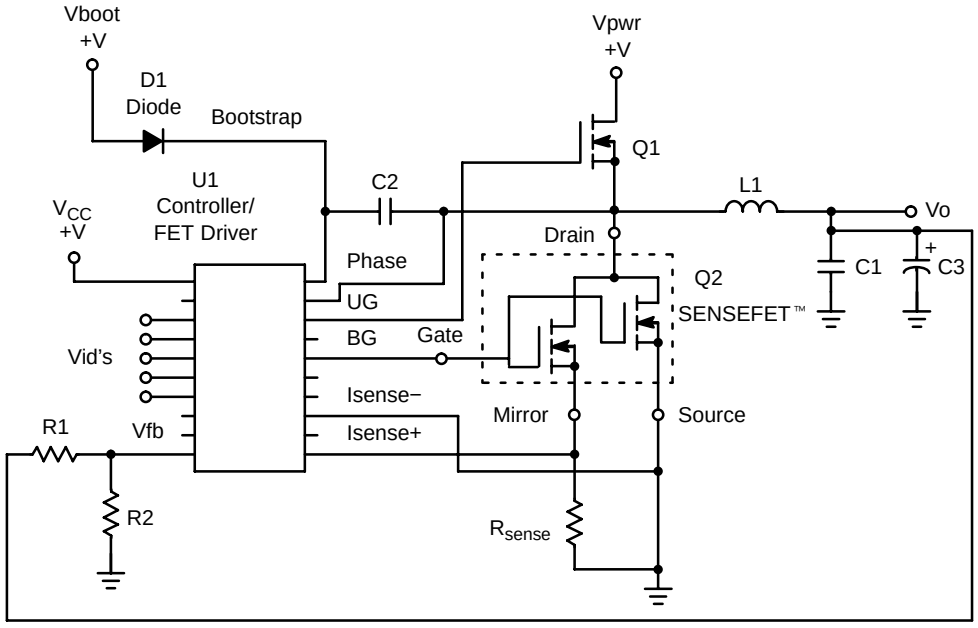

Figure 1. General Buck Converter Schematic Using SENSEFET™ (Q2) Current Sensing

General Description

Current sensing power MOSFETs (SENSEFET™) provide a highly effective way of measuring load current in power conditioning circuits. These devices split load current into power and sense components, and thereby allow signal level resistors to be used for current sampling. Since this technique results in higher efficiency, faster load current transient response, and lower system cost than competing alternatives, understanding how to use current sensing FET products is an important design issue.

There are two ways of using the current mirror signal of the SENSEFET. One utilizes the virtual ground input of a current amplifier. The other uses a resistor (R_{sense}) to develop a voltage from the current mirror signal. The following discussion examines both, and starts with a description of how SENSEFET devices work.

Principle of Operation

Current Mirror Ratio

Current sensing FET operation is based on the matched devices principle that is so commonly used in integrated circuits. Like integrated circuit transistors, the on–resistance of individual source cells in a power MOSFET tends to be well matched. Therefore, if several out of several thousand cells are connected to a separate sense pin, a ratio between sense section on–resistance and power section on–resistance is developed. Then, when the SENSEFET device is turned on, current flow splits inversely with respect to the two resistances, and a ratio between sense current and source current is established.

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The separate source connection is called a mirror. This product is designed such that the ratio between mirror cells and source cells is on the order of 1:250. Schematically, this looks like two parallel FET's with common gate and drain connections, but separate source leads. An illustration of this configuration appears in Figure 2. The relative size of the two devices determines how current is split between source and mirror terminals. The ratio of source current to mirror current is specified by Iratio, the "Current Mirror Ratio." This ratio is defined for conditions where both source and mirror terminals are held at the same potential. Since Iratio is on the order of 250:1, load current is approximately equal to the source current, and the current mirror ratio also describes the ratio of load current to sense current.

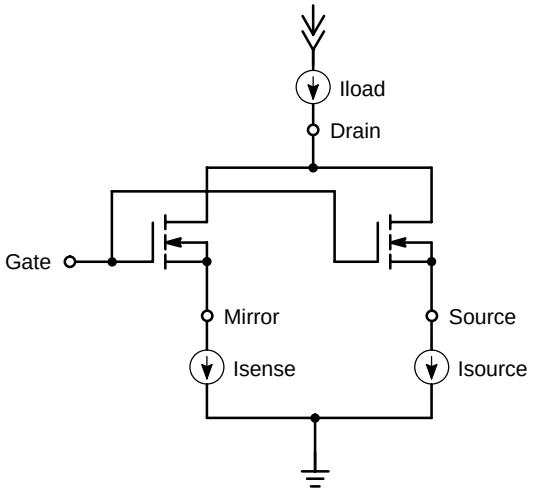

Figure 2. SENSEFET Equivalent Circuit

Using a Resistor in Mirror Terminal

When a signal level resistor is connected between mirror and source terminals, a known fraction of load current is sampled without the insertion loss that is associated with power sense resistors. For this reason, the technique of measuring load current with SENSEFET devices is called "lossless current sensing", and is shown in Figure 2. As long as the sense resistor (R_{sense}) is less than 10% of the mirror section's "on" resistance (Rdm), the current that is sampled is approximately load current divided by the current mirror ratio or Iload/n. In practice, the amount of sense voltage that is developed with such low values of sense resistance is usually not sufficient to drive current limiting circuits, nor allow sufficient output voltage droop control needed by microprocessors. Therefore, larger values of R_{sense} are normally used. These larger values appreciably affect the total resistance in the mirror leg, and therefore, alter the current mirror ratio. How to model this behavior and calculate sensing parameters is discussed as follows:

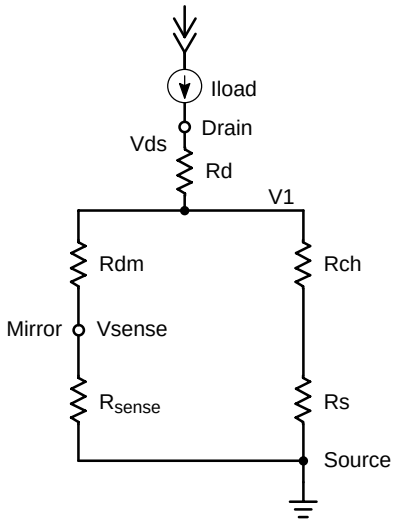

Figure 3. SENSEFET Model with R_{sense}

Vds Voltage Divider

With the aid of the model that is shown in Figure 3, calculating sense voltage and sense resistance may be done. In this model, FET on−resistance ($R_{DS(on)}$) is separated into bulk drain resistance (Rd), source wire resistance (Rs), and active components (Rch). Bulk drain resistance (Rd) is common to the entire device. A fixed internal source resistance is Rs. The active component of FET on−resistance ($R_{DS(on)}$) is modeled by Rch for the power section and Rdm for the mirror. R_{sense} is the external sense resistor that develops the voltage from the mirror sense current. Vds is the voltage developed across $R_{DS(on)}$. If R_{sense} is an open circuit, the maximum voltage that can appear at the mirror terminal is V1. V_{sense} is equal to V1 since R_{sense} is an open circuit, and is termed Vsense_open:

$$V1 := Vds \cdot \frac{Rch + Rs}{Rch + Rs + Rd} \qquad \text{(eq. 1)}$$

Let:

$$Vsense\_open := V1 \qquad \text{(eq. 2)}$$

Therefore, the mirror terminal does not sample the full $R_{DS(on)}$ voltage, but rather sees only that part that is represented by the above resistive divider. Values for (Rch + Rs) and Rd are determined by passing a fixed current (Iload) through the FET with the V_{sense} terminal in an open circuit. The sum of channel resistance and source wire resistance (Rch + Rs) is determined by the voltage (V_{sense}) at the Mirror terminal. Bulk resistance in the drain (Rd) is then determined by subtracting (Rch + Rs) from $R_{DS(on)}$.

Rdm is determined by selecting an R_{sense} approximately equal to Rdm, and then measuring V_{sense} with the same load current as was done with R_{sense} in an open circuit. Rdm for the NILMS4501N SENSEFET is 2.91 Ω. These analysis equations are summarized as follows:

Calculating $R_{DS(on)}$, Rd, and (Rch + Rs) Model Resistances

With R_{sense} in an open circuit in Figure 3, Vds and V_{sense} are measured at a selected current (Iload).

$$Vds\_open := Vds \quad \text{(eq. 3)}$$

Let:

$$Vsense\_open := Vsense \quad \text{(eq. 4)}$$

Which are the Vds and V_{sense} with R_{sense} as an open circuit.

Then:

$$R_{DS(on)} := \frac{Vds\_open}{Iload} \quad \text{(eq. 5)}$$

$$Rmain := \frac{Vsense\_open}{Iload} \quad \text{(eq. 6)}$$

$$Where: \ Rmain = Rch + Rs \quad \text{(eq. 7)}$$

$$Rd := R_{DS(on)} - Rmain \quad \text{(eq. 8)}$$

Determining Rdm Model Resistance

Selecting R_{sense} to be approximately the value of Rdm, Rdm is then calculated from the measured value of V_{sense} using the same Iload and Vsense_open as found above. This V_{sense} is called Vsense_meas.

$$Vsense\_meas := Vsense\_open \cdot \frac{R_{sense}}{R_{sense} + Rdm} \quad \text{(eq. 9)}$$

Solving for Rdm:

$$Rdm := R_{sense} \cdot \left[\left(\frac{Vsense\_open}{Vsense\_meas} \right) - 1 \right] \quad \text{(eq. 10)}$$

Calculating Iratio

$$Isense\_meas := \frac{Vsense\_meas}{R_{sense}} \quad \text{(eq. 11)}$$

$$Iratio := \frac{Iload}{Isense\_meas} \quad \text{(eq. 12)}$$

Determining V_{sense} and Iload from R_{sense}, V_{sense}, and Iratio

Using the measured and calculated values for the model resistances, V_{sense} may be calculated for any value of R_{sense} at any Iload. Also, the main FET current (Iload) may be calculated using Iratio for the value of R_{sense} in use. V1 is the internal voltage from the voltage divider of Rd and Rmain as illustrated in Figure 3.

$$Vds := Iload \cdot R_{DS(on)} \quad \text{(eq. 13)}$$

$$V1 := Vds \cdot \frac{Rmain}{Rmain + Rd} \quad \text{(eq. 14)}$$

$$Where \ Rmain = Rch + Rs \quad \text{(eq. 15)}$$

$$Iload := \left(\frac{Vsense}{R_{sense}} \right) \cdot Iratio \quad \text{(eq. 16)}$$

$$Vsense := V1 \cdot \frac{R_{sense}}{R_{sense} + Rdm} \quad \text{(eq. 17)}$$

Calculated vs. Measured Results

The results obtained from using the above equations agree well with the measured values. Using the NILMS4501N SENSEFET as an example, the calculated and measured values of V_{sense} are compared in Table 1. They are based upon 6.0 A of drain current, $R_{DS(on)}$ = 12.43 mΩ, Rmain = 11.27 mΩ, Rd = 1.17 mΩ, and Rdm = 2.91 Ω.

Table 1. Calculated vs. Measured Sense Voltage

R_{sense} (Ω)	Calculated V_{sense} (mV)	Measured V_{sense} (mV)	% Difference
0.1	2.25	2.27	0.9
1.0	17.29	17.12	1.0
2.0	27.53	27.60	0.3
4.0	39.11	39.16	0.1
8.0	49.53	49.52	0.1

The model in Figure 3 does a good job of determining V_{sense} over a wide range of R_{sense} values.

Example:

With the V_{sense} pin open, calculate Rd and Rch + Rs = Rmain

Measure Vds and V_{sense}: Vds = 0.0746 V, V_{sense} = 0.0676 V for Iload = 6.0 A

$R_{DS(on)}$ = 12.43 mΩ

Using equations (5), (6), (7), and (8), calculate:

Rmain = 11.27 mΩ

Rd = 1.17 mΩ

With R_{sense} = 4.0 Ω, calculate Rdm and Iratio

Measure V_{sense} = 0.0391 V, Vds = 0.0746 V

Using Equations (9), (10), (11), and (12), calculate:

Rdm = 2.905 Ω

Iratio = 609.6

Calculating ILoad from FET Resistances and Iratio

Let R_{sense} = 4.0 Ω

Using:

Iratio = 610

$R_{DS(on)}$ = 12.43 mΩ

Rmain = 11.27 mΩ

Rd = 1.17 mΩ

Calculate Iload from equations (13), (14), 15), (16), and (17).

Vds = 0.0745 V

V1 = 0.0675 V

V_{sense} = 0.03911 V

Then: Iload= 5.968 A

Using a Virtual Ground

In a typical current limit application, the comparator reference voltage, Vref is set to V_{sense} at the desired current limit. Therefore, substituting Vref for V_{sense} in these equations yields combinations of Id and R_{sense} for which a current limit signal is produced. For the best tolerance accuracy, it is advisable to choose a value of R_{sense} that is small as possible in comparison to Rdm, with R_{sense} = 1.4*Rdm as an upper limit. Where higher values of sense voltage are required, the technique shown in Figure 4 can be used. In this circuit, the SENSEFET mirror is held at the same potential as its source, and op amp A1 generates a positive output voltage that equals sense current times the feedback resistor Rf. This assumes that the FET is running in the synchronous mode. The sensing equations for this type of virtual ground circuit are listed as follows:

Virtual Ground Sensing Equation

$$Iload : = (-1) \cdot Isense \cdot Rf \cdot Iratio \quad \text{(eq. 18)}$$

These equations assume that both the op amp's input bias current and input offset voltage are both zero. Using a better op amp, this assumption is a good one.

$$Vsense = (-)\, Isense * Rf \quad \text{(eq. 19)}$$

V_{sense} is positive voltage for Synchronous FET use.

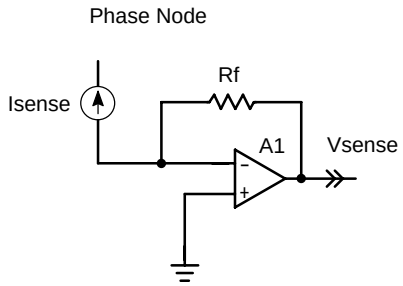

Figure 4. Using Virtual Ground Sensing Amplification

Current Mirror Ratio n as a Function of R_{sense}

Table 2 shows the current mirror ratio n as a function of R_{sense} for the NILMS4501N SENSEFET. Its specification shows the current mirror ratio (Iratio) to be x250 at 25°C with an R_{sense} resistance < 0.1 Ω. The ratio increases with increasing R_{sense} because less current passes through the Rdm path from a fixed Vds voltage.

Table 2. Current Mirror Ratio (Iratio) as Function of R_{sense}

R_{sense} (Ω)	Current Mirror Ratio (Iratio)
0.1	250
1.0	327
2.0	414
4.0	586
8.0	933

Kelvin Connection Accuracy

The inherent accuracy that is associated with splitting current between matched cells in a power MOSFET is relatively good. Assuming that both source and mirror terminals are held at the same potential, accuracy is solely dependent upon the current mirror ratio (Iratio). This parameter typically runs within ±2% of nominal at 25°C. The ratio remains within a ±4% window overtemperature. Current mirror tolerance adds with sense resistor tolerance and op amp offsets to produce a sense voltage that can be maintained within ±6% overtemperature.

Accuracy Using R_{sense}

Alternatively, if an external R_{sense} resistor is used, tolerance depends both on internal resistance ratios and the ratio of internal on–resistance to an external R_{sense}. Therefore, in this configuration, unit–to–unit variations and temperature effects are first order design considerations.

Referring again to Figure 3, the sensing model provides a schematic illustration of the issues involved. To start, let's assume that R_{sense} is equal to zero. In this condition, whatever variation that occurs in Rch are very nearly matched on a percentage basis by variations in Rdm. Therefore, even for very large changes in Rch, the ratio between Rch and Rdm remains nearly constant, assuming Rs is much smaller than Rch. Since this ratio is undisturbed, the ratio of sense current to drain current is also undisturbed, and measurement accuracy is relatively good. At the other end of the spectrum, let's assume that R_{sense} is an open circuit. In this case mirror voltage is not dependent upon ratios. The mirror terminal samples the voltage drop across (Rch + Rs), with V_{sense} = Iload • (Rch + Rs). Measurement accuracy is, therefore, directly dependent upon the value of Rch. Since Rch can vary 30% from unit to unit and 40% over derated operating temperature, an accurate measurement is not obtained in this configuration.

In between these two extremes, choosing R_{sense} becomes a tradeoff between signal level and accuracy. Useful performance is obtained with values of R_{sense} up to X1.4 of Rdm. As R_{sense} increases as a percentage of Rdm, the measurement accuracy becomes more dependent upon the absolute value of Rch than it is on the ratio. An illustration is provided in Table 3 for the NILMS4501N SENSEFET, where current mirror ratio stability is shown as a function of R_{sense} over a temperature change from 25°C to 125°C. The drain current is set to 6.0 A, and the measured Rdm is 2.9 Ω. Note that temperature stability degrades rapidly as R_{sense} is increased in value. The ratio decreases as the temperature increases, which means that more current is flowing in the mirror branch at higher temperatures.

Table 3. Current Mirror Ratio n Stability Overtemperature as a Function of R_{sense}

R_{sense}	% Change Over 25°C to 125°C	Ratio at 25°C	Ratio at 125°C
0.1 Ω	−2%	264	269
1.0 Ω	−5%	345	327
2.0 Ω	−11%	433	389
4.0 Ω	−17%	607	519
8.0 Ω	−25%	961	766

Inductor Sensing Temperature Stability

For comparative purposes, an inductor made of copper changes +38.5% (3750 ppm/°C) over the 25°C to 125°C range. Therefore, the SENSEFET temperature stability is twice as good as that of an inductor with Rsense = 4.0 Ω.

SENSEFET Temperature Compensation

Controllers are now coming into the marketplace with temperature compensation for the current sense signal. One unit compensates by −14.7%. This is not enough compensation for the inductor, but there is enough for use with the SENSEFET when used with an R_{sense} equal to approximately 3.6 Ω. This means that the temperature drift of Iratio can be almost completely cancelled. If the controller temperature change does not match the SENSEFET temperature change, then the value of R_{sense} can be adjusted to obtain a near zero temperature coefficient.

Kelvin Source Connection

In order to get the full accuracy that SENSEFET devices are capable of, a Kelvin connection to the source is required. Otherwise voltage drops that are caused by load current flowing in the ground connection will add to the sense voltage and change the Iratio. The effect of ground impedance is illustrated in Figure 5, where Rgnd has been added to the model in Figure 3. Load current flowing through Rgnd produces a voltage drop that appears in series with Rch + Rs and increases the voltage V1, which changes the Iratio.

The $R_{DS(on)}$ resistance now contains Rd, Rch, Rs, and Rgnd, and the open circuit V_{sense} voltage becomes:

Calculating V_{sense} with Rgnd

$$Vds := Iload \cdot (Rd + Rch + Rs + Rgnd) \quad \text{(eq. 20)}$$

$$V1 := Vds \cdot \frac{(Rch + Rs + Rgnd)}{(Rd + Rch + Rs + Rgnd)} \quad \text{(eq. 21)}$$

$$Vsense := V1 \cdot \frac{(R_{sense})}{(R_{sense} + Rdm)} \quad \text{(eq. 22)}$$

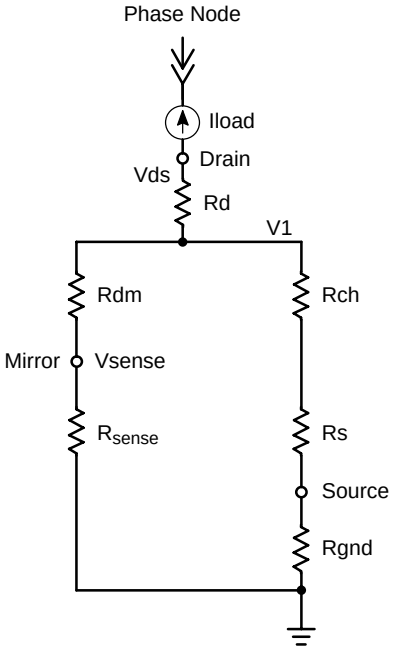

Figure 5. SENSEFET Model with Ground Resistance in the Source (Non−Kelvin Connection)

As can be seen from the above equations, Rgnd increases the $R_{DS(on)}$ and Vds, as well as changes the Iratio because the voltage divider voltage for Rdm changes. Rgnd will also change the temperature coefficient of V_{sense}.

Conclusion

SENSEFET products are conceptually simple devices that provide an alternative to power sense resistors, output inductor resistance, and current sense transformers for sensing load current. They offer lower power loss than power sense resistors and better temperature stability than inductor sensing. The sense voltage is scalable with an external resistor. With their lower temperature drift, current sensing temperature compensation is readily obtainable.

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