POWER

# DESIGN FAQs

*Frequently Asked Questions:*

# HIGH-VOLTAGE, TWO-PHASE GATE DRIVER ICs

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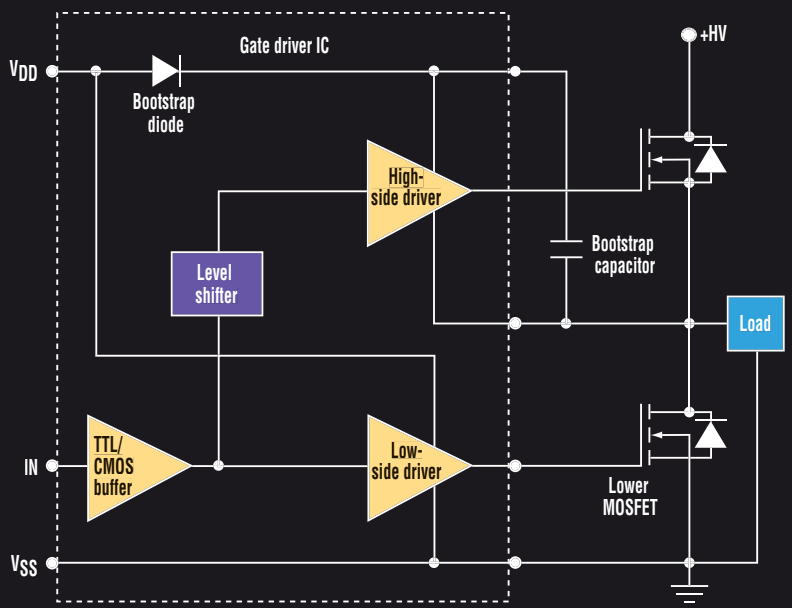
## What is a two-phase gate driver IC?

A two-phase gate driver IC is a power amplifier that produces two high-current gate drives for either a synchronous buck or half-bridge totem-pole MOSFET configuration *(see the figure)*. The two-phase driver provides the gate drive for both a low-side and high-side n-channel MOSFET. In contrast, the single-phase gate driver services only a single low-side MOSFET.




**A two-phase gate driver has a "floating" high-side driver that provides the appropriate gate voltage and current while operating reliably with the voltage applied to the drain of the upper MOSFET.**

## What is the function of the level shifter?

The level shifter must elevate the input voltage level to the appropriate range for the high-side driver *(see the figure, again)*. For best results, the level shifter must operate at high speeds while consuming low power and providing clean level translations.

## How does the high-side driver support a high-voltage MOSFET?

Gate voltage for the high-side driver employs a bootstrap supply circuit comprising a bootstrap diode and bootstrap capacitor *(see the figure, again)*. The bootstrap diode may be either integrated within the gate driver IC or external to it. Because the bootstrap capacitor value must be much higher than the MOSFET gate capacitance, it is always external to the IC. When the lower MOSFET is enabled, the bootstrap capacitor charges up to $V_{DD}$ via the bootstrap diode. Thus, the high-side gate driver "floats" at the gate voltage of the high-side MOSFET. For reliable operation, the high-side driver must be able to withstand the operating voltage of the high-side MOSFET. Typical maximum voltage ratings for high-voltage gate drivers can range from 80 to 100 V.

## What input voltage thresholds are available with high-voltage, two-phase gate driver ICs?

These gate driver ICs may accommodate CMOS or TTL input voltage thresholds.

## What are the power dissipation considerations for the gate driver?

The total IC power dissipation includes the gate driver losses and the bootstrap diode losses. Gate driver losses depend on the switching frequency, output load capacitance, and $V_{DD}$ supply voltage. The power losses associated with driving the output loads dominate the power dissipation at high frequencies and high load capacitance values. Bootstrap diode power loss consists of the forward diode loss while charging the bootstrap capacitor and reverse bias power loss during reverse recovery. These events occur once per cycle, so this diode loss is also proportional to the switching frequency.

## What are the design considerations for the capacitors employed with gate driver?

A low equivalent series resistance/equivalent series inductance (ESR/ESL) bypass capacitor must be located near the IC between $V_{DD}$ and $V_{SS}$. In addition, the bootstrap capacitor requires a low ESR/ESL type placed close to its connections to the IC. These capacitors must support high peak currents drawn from $V_{DD}$ during turn-on of the

external MOSFET. To prevent voltage transients at the drain of the upper MOSFET, connect a low ESR capacitor from its drain to $V_{SS}$ (ground).

### What are the grounding considerations for the gate driver?

Grounding connections must confine the high peak currents from charging and discharging the MOSFET gates in as small an area as possible. This will decrease the loop inductance and minimize noise on the MOSFET gates. Plus, the MOSFETs must be located as close as possible to the gate driver.

### Can you keep both the high-side and low-side MOSFETs from conducting simultaneously?

If both MOSFETs conduct at the same time, you get shoot-through current that causes electromagnetic interference (EMI), lowers efficiency, and reduces reliability. One approach to protecting against shoot-through is to control the dead time between the conduction intervals of the two MOSFETs. Insert a delay between the time that one driver turns off its associated MOSFET and the time the other driver turns on its associated MOSFET. By controlling the dead time, you optimize performance while getting the required dead time protection. Another approach to this potential problem is to include a non-overlap circuit that prevents the gate drivers from causing shoot-through of the two MOSFETs.

### What causes gate circuit transients, and how can they be controlled?

The lower MOSFET's body diode clamps the node between the source of the upper MOSFET and the drain of the lower MOSFET. Board resistances and inductances sometimes cause this MOSFET drain-source node to generate undesirable transients. You can prevent these transients by inserting an external Schottky diode from low-side driver output to ground and/or from the high-side driver output and the drain-source node.

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