Design and Simulation of Phase-Shifted Full Bridge Converter for Hybrid Energy Systems

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***Abstract*—This paper presents design and Simulink implementation of zero voltage switching (ZVS) phase-shifted full bridge dc-dc converter. The phase-shifted full bridge PWM dc-dc converter is widely used in high power, high voltage applications due to the advantages of high power handling capability with low switching and conduction losses. The phase shift feature of the control signal allows ZVS thereby eliminating the switching losses during FET device transition. It also minimize the parasitic effect and conduction losses at high frequency operation thereby increase system efficiency. A 3kW, 100 kHz high frequency phase-shifted full bridge converter was design and simulated in Matlab/Simulink to analyze the system performance prior to experimental implantation. The converter is intended for hybrid energy systems (HES) application in which a state space controller will be developed with wider dynamics to accommodate variable input sources mostly from renewable energy resources like solar and wind power. The converter simulation results shows that the system achieved greater than 90% efficiency at full load current.**

Keywords—dc-dc converter; phase-shift PWM; full bridge converter; zero voltage switching

I. INTRODUCTION

The quest for high power density called for high frequency operation of power converters [1]. Generally the FET devices which are like the backbone of power converter has non-linear characteristics with their parasitic parameters effect more pronounce at high frequency thereby deteriorating the system smooth operation for high efficiency delivery . In high power application, the full bridge converter topology is most widely used owning to its high power handling capacity because of the number of field effect transistor (FET) switch in the topology [2]. The switching mode of the FET device in full bridge converter have direct impact on the system performance in terms of smooth operation and system efficiency. The pulse width modulation (PWM) control signal to the gate of the four switches in conventional full bridge converter operation turns the diagonal pair switches at a time with or without dead time. This approach is referred to as hard switching resulting in high switching losses within the circuit module reducing system efficiency. In situation where there is dead time, all four switches will be in off state for short period and the load current freewheels through the rectifier diodes making the energy stored in leakage inductance to cause severe ringing with power FET junction capacitance [3, 4] .

The deficiency with parasitic ringing effect, conduction losses and high power switching losses are elimination by employing phase-shifted PWM control signal which allows ZVS transition of FET devices during the turn on. The ZVS soft switching is achieve during the turn on transition via resonance between the FET device output capacitance and the leakage inductance of the isolated transformer. In phase-shift full bridge dc-dc converter, the switching operation allows the transformer primary to be connected to source voltage or shorted ensuring continuous current flow thereby eliminating the ringing effect that could result from transformer leakage inductance. The energy stored in leakage inductance of the transformer is used to discharge the energy stored on the FET device (MOSFETs) junction capacitance to achieve zero voltage switching (ZVS) at turn on [3, 5].

The ZVS phase-shift full bridge converter Allows operation of switching devices at reduced switching losses and stress thereby improving energy conversion efficiency. It also allows operation of converts at high frequency resulting in high power density [6, 7]. This paper presents analysis on modes of operations of phase-shifted full bridge converter and steady state design of 3kW converter. The full bridge converter is intended for hybrid energy system (HES) as shown in Fig.1 with five input sources in which a state space controller will be developed with wider dynamics to accommodate variable input sources most especially from renewable energy sources. The designed converter is implemented in Simulink for examining the open loop performance of the system in terms of operation and efficiency delivery. The simulation results shows that the system achieved over 90% efficiency at full load capacity.

II. OPERATION AND STEADY STATE ANALYSIS

The phase-shifted PWM full bridge converter is an isolated dc-dc converter haven two stages, the dc-ac H bridge converter with high frequency transformer and the ac-dc part. The topology of the ZVS phase-shift full bridge PWM converter has four switching element like conventional full bridge converter as shown in Fig.1 with switching control signal been the major difference. The leg with pair switches S1, S2 are turned on complimentarily with 50% duty cycle minus short dead time

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and same for the second leg with pair switches S3, S4. The gating signal is shown in Fig. 2, where the control signal to switch S3 and S4 is phase-shifted with respect to gating signal to switch S1 and S2 to allow ZVS transition and also ensuring that the transformer primary is either connected to the input or shorted.

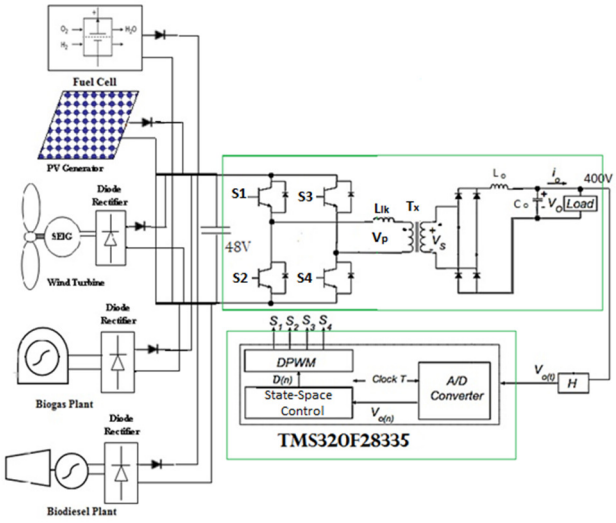

Fig. 1. HES with phase-shifted full bridge converter

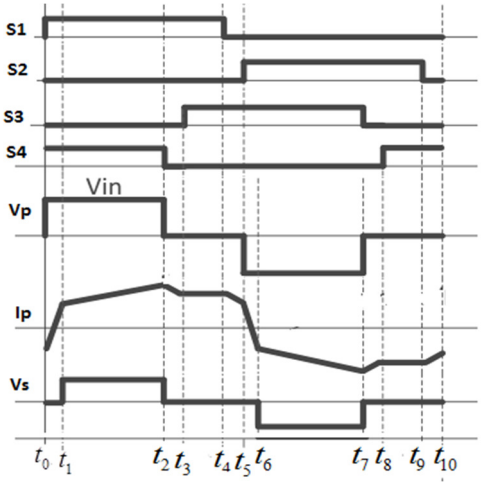

Fig. 2. PWM Phase-shift full bridge converter waveform

The operating waveform of the gating control signal and steady state transformer primary and secondary waveform of ZVS Phase-shifted full bridge converter is presented in Fig. 2. The wave form shows the different transition mode within the power circuit for a complete switching period ($t_0 \sim t_{10}$) and each of this mode are briefly explained as follows [8].

Mode 1 ($t_0 \sim t_1$), duty cycle loss

At the time, $t = t_0$ the switch S1 and S4 are in on state, the switch S1 turned on with ZVS following end of mode t_{10}. The transformer secondary voltage V_s remains zero until the primary current I_p reverse to positive direction and rise to reach reflected output inductor current (nI_{Lo}) at mode $t = t_1$.

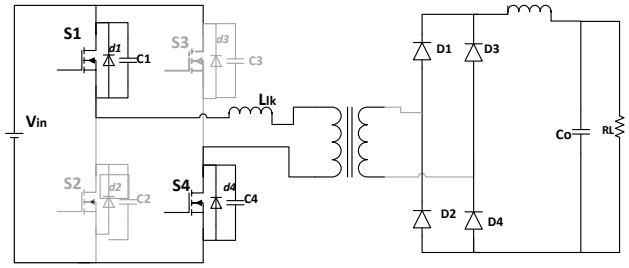

Fig. 3. Mode 1 ($t_0 \sim t_1$)

Mode 2 ($t_1 \sim t_2$), power delivery mode

At time $t = t_1$, the transformer secondary voltage is equal to nV_{in} and rectifier diode D_1 and D_4 are forward biased and conduct to transfer power from source to the load. The effective phase shift duty cycle starts with mode $t_1 \sim t_2$, the current across output filter start to rise and the primary winding current I_p then equal to reflected output inductor current (nI_{Lo}).

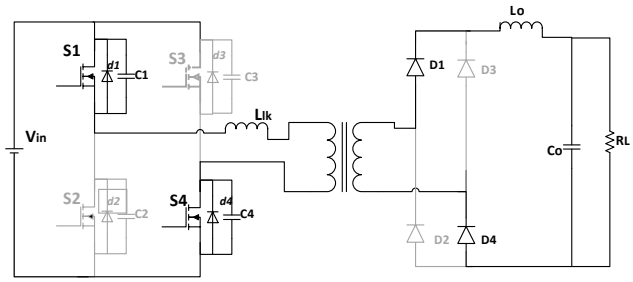

Fig. 4. Mode 2 ($t_1 \sim t_2$)

Mode 3 ($t_2 \sim t_3$), Switch S3 ZVS

At mode $t = t_2$, switch S4 is turned off and the primary current charges the snubber capacitance $C4$ of switch S4 and discharges capacitance of switch S3. When the snubber capacitance $C3$ is completely discharge from V_{in} to 0, the body diode d_3 start to conduct to achieve zero voltage switching condition for switch S3 thereby eliminating FET device switching losses. At this mode the transformer secondary voltage become zero and the rectifier diodes D_1, D_4 carrying current.

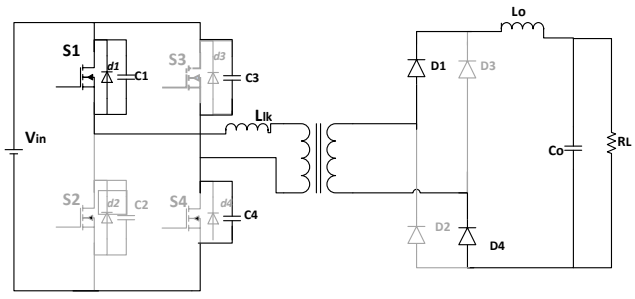

Fig. 5. Mode 3 ($t_2 \sim t_3$)

Mode 4 ($t_3 \sim t_4$), freewheeling mode

At mode $t = t_3$, switch S3 is turned on with ZVS and the primary current I_p freewheel though switch S1 and S3. The transformer secondary voltage V_s is zero and the output inductor voltage is discharged by the load.

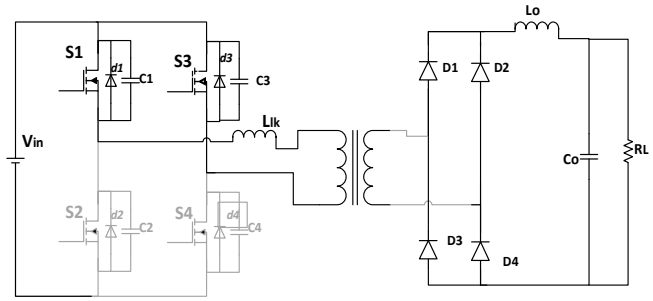

Fig. 6. Mode 4 ($t_3 \sim t_4$)

Mode 5 ($t_4 \sim t_5$), switch S2 ZVS

At time $t = t_4$, switch S1 is turned off and the transformer primary current charges the snubber capacitance $C1$ of switch S1 and discharge capacitance $C2$ of switch S2. When the snubber capacitance $C2$ is completely discharge from V_{in} to 0, the body diode d_2 start to conduct to achieve zero voltage switching condition for switch S2. The transformer secondary voltage remain zero at mode $t_4 \sim t_5$.

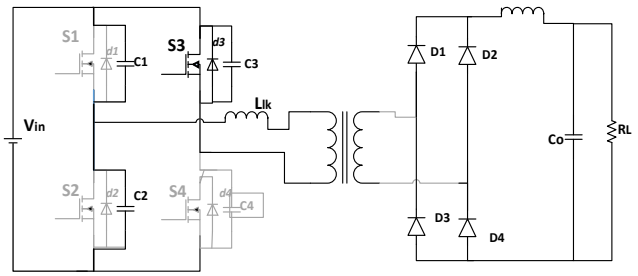

Fig. 7. Mode 5 ($t_4 \sim t_5$)

Mode 6 ($t_5 \sim t_6$), duty cycle loss

At the mode $t = t_5$, the switch S2 is turned on with ZVS following end of mode t_4. The transformer secondary voltage V_s still remain zero until the primary current I_p reverse it direction (in negative direction) and start to rise to reach reflected output inductor current nI_{Lo} at period $t = t_6$. The primary current will rise with a slop of V_{in} / L_{lk} as the V_{in} discharges the leakage inductor L_{lk} and no power is delivered to the output.

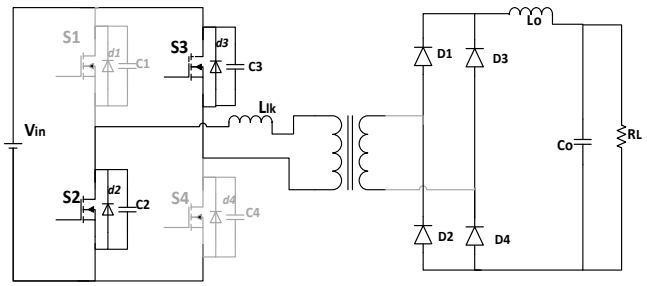

Fig. 8. Mode 6 ($t_5 \sim t_6$)

Mode 7 ($t_6 \sim t_7$), power delivery mode

At time $t = t_6$, the transformer secondary voltage V_s equals nV_{in}. The rectifier diode D_2 and D_3 are forward biased and conduct to transfer power to charge the output inductor. The effective phase shift duty cycle starts again with the mode t_6. The current across output inductor start to rise and the primary winding current I_p in negative direction equal to reflected output inductor current nI_{Lo}.

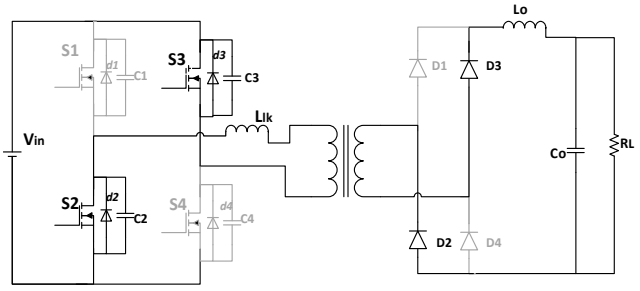

Fig. 9. Mode 7 ($t_6 \sim t_7$)

Mode 8 ($t_7 \sim t_8$), switch S4 ZVS

At mode $t = t_7$ switch S3 is turned off and the primary current charges the snubber capacitance $C3$ of switch S3 and discharges capacitance $C4$ of switch S4. When the snubber capacitance $C4$ is completely discharged from V_{in} to 0, its body diode d_4 start to conduct to achieve zero voltage switching condition for switch S4. At this mode the transformer secondary voltage become zero and the rectifier diodes carrying current.

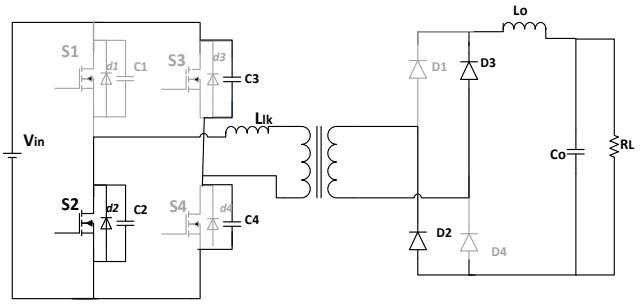

Fig. 10. Mode 8 ($t_7 \sim t_8$)

Mode 9 ($t_8 \sim t_9$), freewheeling mode

At mode $t = t_8$, switch S4 is turned on with ZVS and the primary current I_p freewheel though switch S2 and S4. The transformer secondary voltage V_s is zero and the output inductor voltage is discharged by the load.

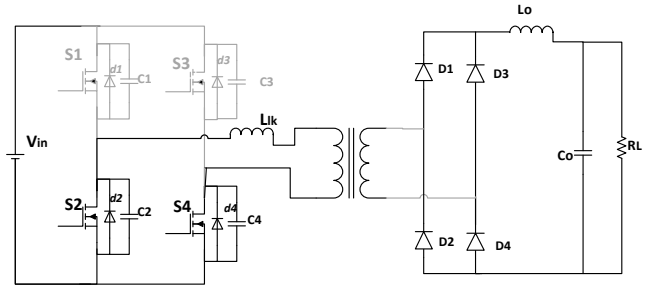

Fig. 11. Mode 9 ($t_8 \sim t_9$)

Mode 10 ($t_9 \sim t_{10}$), switch S1 ZVS

At mode $t = t_9$, switch S2 is turned off and the primary current charges the snubber capacitance $C2$ of switch S2 and discharge capacitance $C1$ of switch S1. When the snubber capacitance $C1$ is completely discharge from V_{in} to 0, the body diode $d1$ start to conduct to achieve zero voltage switching condition for S1 eliminating FET device switching losses. At this mode the transformer secondary voltage become zero and the rectifier diodes D_2, D_3 carrying current.

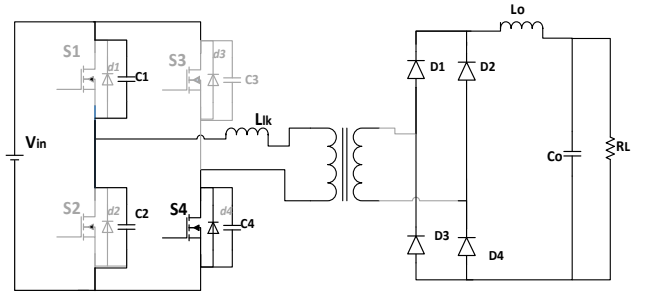

Fig. 12. Mode 10 ($t_9 \sim t_{10}$)

III. PHASE-SHIFT FULL BRIDGE CONVERTER DESIGN

A 3kW high frequency phase-shift full bridge converter with the following specification is designed and simulated in Matlab/Simulink.

- Nominal input voltage, $V_{in(nom)}$ = 48V
- Input voltage range, $V_{in(range)}$ = 36V-60V
- Output voltage, V_o = 400V
- Efficiency $n \geq 90\%$
- Output current $I_{o(\max)}$ = 7.5 A
- Output voltage ripple ΔV_o = 1V
- Output inductor current ripple ΔI_L = 1.5A
- Switching frequency f_s = 100kHz
- Maximum duty cycle $D_{\max}$ of 0.4

To reduce the losses incur by the isolation transformer, a ferrite material with low saturation flux density is considered for magnetic core with maximum magnetic flux $B_{\max}$ of 0.2T (2000G). For a core with cross area A_c of 1.5cm^2, the number of turns for primary side N_p of the high frequency transformer is determined from [9]:

$$N_p = \frac{V_{in(\min)} D}{2B_{\max}(G) A_c(cm^2) f_s(\text{Hz})} X10^8 \quad (1)$$

The transformer primary turn N_p is chosen as 3 turns

To meet the output voltage requirement and cater for voltage drop across circuit elements, the transformer secondary voltage $V_{\sec}$ should satisfy (2) [10].

$$V_{\sec} \geq \frac{V_o}{D_{\max}}, \quad (2)$$

With the duty cycle of 0.4, the output secondary voltage $V_o = D_{eff} * V_{\sec}$. The number of turns for transformer secondary N_s is calculated from:

$$N_s = N_p \frac{V_{\sec}}{V_{in(\min)}} = 42 \text{ turns} \quad (3)$$

The voltage across the output filter inductor L_o is $(nV_{in} - V_0)$ for the period $D_{eff} T_s$ is given by [11]:

$$L_o = \frac{(nV_{in} - V_o) D_{eff}}{\Delta I_L f_s} \quad (4)$$

For 20% output inductor current ripple ΔI_L, output filter inductor is 1.605 mH

The selection of output filter capacitor is specified by the output voltage ripple ΔV_o chosen as 0.25% (1V) of V_o [11].

$$\Delta V_c = \frac{V_o(1 - D_{eff})}{16 f_s^2 C L_o f_s} = 0.95\mu\text{F} \quad (5)$$

The frequency for achieving ZVS switching resonance between the stored energy in leakage inductance of the transformer and the FET device (MOSFETs) junction capacitance for all the four switches is similar and given by:

$$f_r = \frac{1}{2\pi\sqrt{L_{lk} C_r}} \quad (6)$$

Where $C_r = 2C_{oss(tr)} + C_{Tx}$, C_{Tx} is the transformer capacitance and $C_{oss(er)}$ is the FET energy stored in the nonlinear drain to source output capacitance. The transition of the voltage across the drain-source (V_{ds}) requires minimum frequency of at least 1/4th of the resonant period ($T_r/4$) i.e. $t_d \geq T_r/4$. In this project, the superFET FCH043N60 was chosen haven satisfy the required switching characteristic for experimental implantation of the phase-shift full bridge converter. The switch effective output capacitance is 730 pF

and transformer capacitance is taken as 500 pF. The total turn on delay time t_d is 200 ns, the leakage inductance is calculated from:

$$L_{lk} = 4t_d{}^2 / \pi^2 C_r = 8.3\mu H \quad (7)$$

IV. Simulation Results

The steady state designed parameters of the phase-shift full bridge dc-dc converter was used for open loop simulation in Matlab/Simulink environment. The generated control gate signal to the four switches (S1~S4) of the full bridge converter is presented in Fig. 13 showing the phase shift features that allows zero voltage switching, eliminating switching losses for high efficiency delivery.

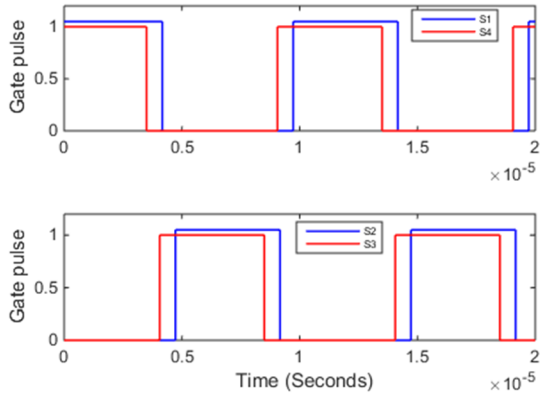

Fig. 13. Gating signal

The designed phase-shift converter performance was analysed under different loading conditions. Presented in Fig. 14 is the converter transformer primary voltage and current at full load [7.5A load current]. Also in Fig. 15 shows the transformer secondary voltage and current at full load. The transformer primary voltage takes two values of V_{in} during the effective phase-shift duty cycle twice, one along the positive plane $+V_{in}$ and the other along the negative plane $-V_{in}$ in one complete cycle. During the effective phase-shift duty cycle the transformer secondary voltage takes a values of $+nV_{in}$ on the positive plane and $-nV_{in}$ on along the negative

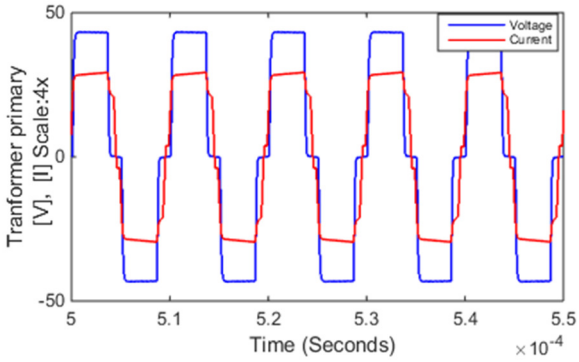

Fig. 14. Transformer primary voltage and current

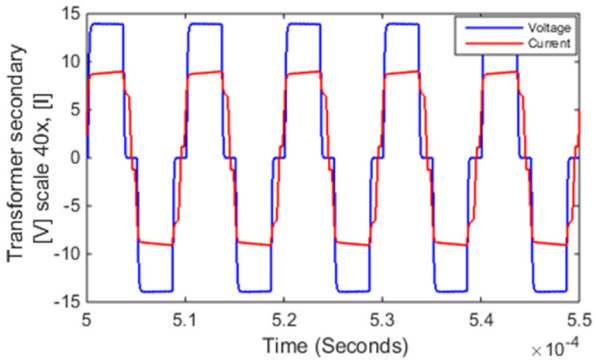

Fig. 15. Transformer secondary voltage and current

The phase-shift full bridge dc-dc converter output voltage and current under full load operation is presented in Fig.16. The open loop response shows that the system has transient voltage overshoot at start up till about 0.2ms before it finally settled to 400V. The converter efficiency with different load condition was measure and presented in Fig. 17. At rated load current, the system attained 93% efficiency.

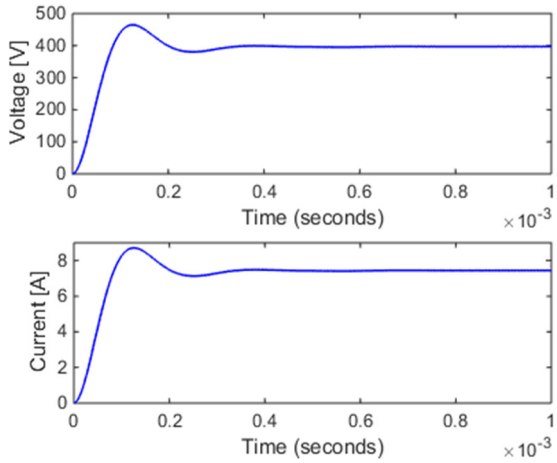

Fig. 16. Full load output voltage and current

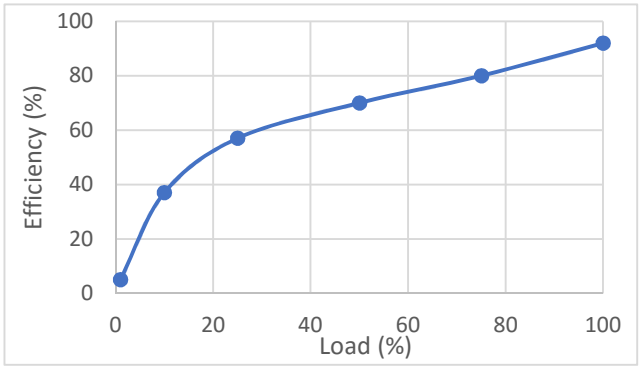

Fig. 17. % Load current Vs Efficiency

V. CONCLUSION

A ZVS phase-shifted full bridge dc-dc converter of 100 kHz switching frequency has been designed and model in Simulink environment. The switching stages of the phase-shift full bridge dc-dc converter during power transfer in a complete switching cycle was analyzed with circuit illustration. The steady state circuit parameter for a 3kW converter was designed with the circuit elements including the isolated transformer and the performance of the system was verified in Matlab/Simulink environment. The converter voltage, current waveforms and the output power is satisfactory for the designed power rating. The system performance was further analyzed under different loading conditions and was able to deliver 93% efficiency at rated load current of 7.5A.

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