Introdução à Arquitetura de Computadores

Aula24

µArquitetura Single-Cycle: Exercícios

Instruções Adicionais

- sll - Shift Left Logical
- lui - Load Upper Immediate
- slti - Set on Less Than Immediate
- jal - Jump And Link
- jr - Jump Register
- jal e jr

Exercícios SC (1) - Enunciado

Consulte o Apêndice B para a definição das instruções.
Faça uma cópia da Figura 7.11 (*Datapath*) para desenhar as modificações necessárias.
Assinale os novos sinais de controlo.
Faça uma cópia da Tabela 7.3 (*Main Decoder*) e Tabela 7.2 (ALU Decoder) para anotar as modificações necessárias. Descreva quaisquer outras alterações relevantes.

Exercício 7.3

Modifique o CPU Single-cycle para adicionar suporte para uma das seguintes instruções:

(a) sll
(b) lui
(c) slti
(d) blez

Exercício 7.4

Repita o Exercício 7.3 para as seguintes instruções:

(a) jal
(b) lh
(c) jr
(d) srl

Exercícios SC (2) - ApdxB - OpCodes - Type-I

Opcode	Name	Description
000000 (0)	R-type	all R-type instructions
000001 (1) (rt = 0/1)	bltz rs, label / bgez rs, label	branch less than zero/branch greater than or equal to zero
000010 (2)	j label	jump
000011 (3)	jal label	jump and link
000100 (4)	beq rs, rt, label	branch if equal
000101 (5)	bne rs, rt, label	branch if not equal
000110 (6)	blez rs, label	branch if less than or equal to zero
000111 (7)	bgtz rs, label	branch if greater than zero
001000 (8)	addi rt, rs, imm	add immediate
001001 (9)	addiu rt, rs, imm	add immediate unsigned
001010 (10)	slti rt, rs, imm	set less than immediate
001011 (11)	sltiu rt, rs, imm	set less than immediate unsigned
001100 (12)	andi rt, rs, imm	and immediate
001101 (13)	ori rt, rs, imm	or immediate
001110 (14)	xori rt, rs, imm	xor immediate
001111 (15)	lui rt, imm	load upper immediate
010000 (16) (rs = 0/4)	mfc0 rt, rd / mtc0 rt, rd	move from/to coprocessor 0
010001 (17)	F-type	fop = 16/17: F-type instructions
010001 (17) (rt = 0/1)	bc1f label / bc1t label	fop = 8: branch if fpcond is FALSE/TRUE

Opcode	Name	Description
011100 (28) (func = 2)	mul rd, rs, rt	multiply (32-bit result)
100000 (32)	lb rt, imm(rs)	load byte
100001 (33)	lh rt, imm(rs)	load halfword
100011 (35)	lw rt, imm(rs)	load word
100100 (36)	lbu rt, imm(rs)	load byte unsigned
100101 (37)	lhu rt, imm(rs)	load halfword unsigned
101000 (40)	sb rt, imm(rs)	store byte
101001 (41)	sh rt, imm(rs)	store halfword
101011 (43)	sw rt, imm(rs)	store word
110001 (49)	lwc1 ft, imm(rs)	load word to FP coprocessor 1
111001 (56)	swc1 ft, imm(rs)	store word to FP coprocessor 1

Single-cycle: LUI, SLTI, JAL

Multicycle: BNE, ORI, LBU

Exercícios SC (3) - ApdxB - FunctField - Type-R

Table B.2 R-type instructions, sorted by funct f

Funct	Name	Description
000000 (0)	sll rd, rt, shamt	shift left logical
000010 (2)	srl rd, rt, shamt	shift right logical
000011 (3)	sra rd, rt, shamt	shift right arithmetic
000100 (4)	sllv rd, rt, rs	shift left logical variable
000110 (6)	srlv rd, rt, rs	shift right logical variable
000111 (7)	srav rd, rt, rs	shift right arithmetic variable
001000 (8)	jr rs	jump register
001001 (9)	jalr rs	jump and link register
001100 (12)	syscall	system call
001101 (13)	break	break
010000 (16)	mfhi rd	move from hi
010001 (17)	mthi rs	move to hi
010010 (18)	mflo rd	move from lo
010011 (19)	mtlo rs	move to lo
011000 (24)	mult rs, rt	multiply
011001 (25)	multu rs, rt	multiply unsigned
011010 (26)	div rs, rt	divide
011011 (27)	divu rs, rt	divide unsigned

Table B.2 R-type instructions, sorted by funct field-

Funct	Name	Description
100000 (32)	add rd, rs, rt	add
100001 (33)	addu rd, rs, rt	add unsigned
100010 (34)	sub rd, rs, rt	subtract
100011 (35)	subu rd, rs, rt	subtract unsigned
100100 (36)	and rd, rs, rt	and
100101 (37)	or rd, rs, rt	or
100110 (38)	xor rd, rs, rt	xor
100111 (39)	nor rd, rs, rt	nor
101010 (42)	slt rd, rs, rt	set less than
101011 (43)	sltu rd, rs, rt	set less than unsigned

Single-cycle: SLL, JR

Multicycle: SRLV

Exercícios SC (4) - Figura 7.11 - Datapath

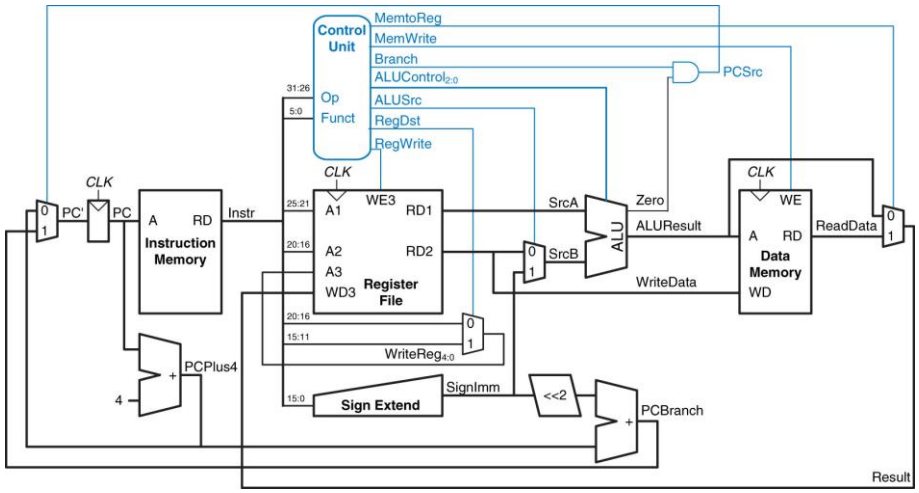
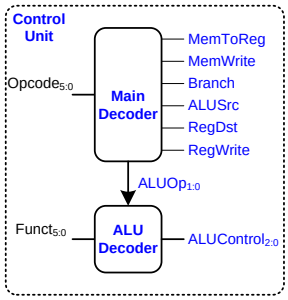


Figura 7.11 Processador MIPS *single-cycle* completo

Exercícios SC (5) - TabelasV - ALU + Main Decoders



$ALUOp_{1:0}$	$Funct_{5:0}$	$ALUControl_{2:0}$
00	X	010 (Add)
X1	X	110 (Subtract)
1X	100000 (add)	010 (Add)
1X	100010 (sub)	110 (Subtract)
1X	100100 (and)	000 (And)
1X	100101 (or)	001 (Or)
1X	101010 (slt)	111 (SLT)

Tabela 7.2 Tabela de verdade do *ALU decoder*

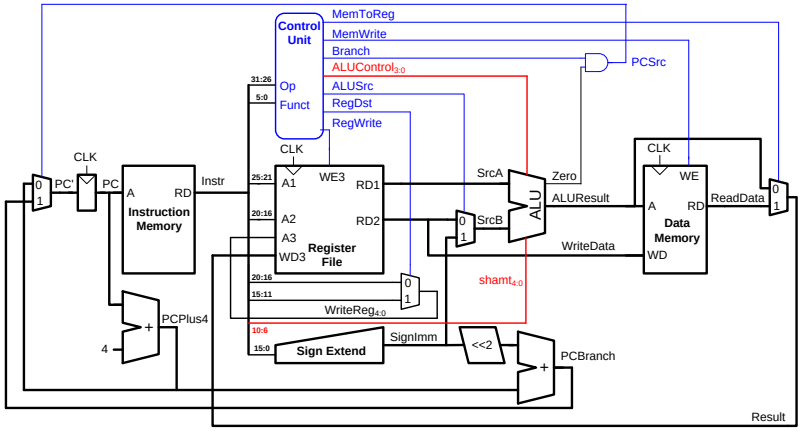
Instruction	$Op_{5:0}$	RegWrite	RegDst	AluSrc	Branch	MemWrite	MemToReg	$ALUOp_{1:0}$
R-type	000000	1	1	0	0	0	0	10
lw	100011	1	0	1	0	0	1	00
sw	101011	0	X	1	0	1	X	00
beq	000100	0	X	0	1	0	X	01

Tabela 7.3 Tabela de verdade *do Main decoder*

ProbSC (1), P7.3a (1) - SLL: Datapath

31:26	25:21	20:16	15:11	10:6	5:0
0	rs	rt	rd	shamt	0

`sll rd, rt, shamt` — tipo-R



Datapath single-cycle modificado para sll

1. $ALUControl_{3:0}$ passa de 3 para 4 bits
2. ALU precisa duma entrada extra: $shamt_{4:0}$

shamt = shift amount

ProbSC (2), P7.3a (2) - SLL: ALU Decoder + ALU

31:26	25:21	20:16	15:11	10:6	5:0
0	rs	rt	rd	shamt	0

`sll rd, rt, shamt` — tipo-R

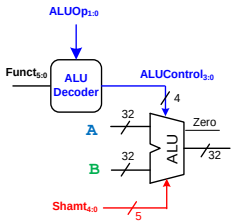
(`rs` ignorado)

$ALUOp_{1:0}$	$Funct_{5:0}$	$ALUControl_{3:0}$
00	X	0010 (Add)
X1	X	0110 (Subtract)
1X	100000 (add)	0010 (Add)
1X	100010 (sub)	0110 (Subtract)
1X	100100 (and)	0000 (And)
1X	100101 (or)	0001 (Or)
1X	101010 (slt)	0111 (SLT)
1X	000000 (sll)	1000 (Shift Left Logical)

Tabela de verdade do *ALU decoder* para sll

$F_{3:0}$	Função
0000	A & B
0001	A | B
0010	A + B
0011	not used
0100	A & ~B
0101	A | ~B
0110	A - B
0111	SLT
1000	SLL

ALU para sll



SLL:
`Result = B << shamt`
(`A` ignorado)

`rd:= rt << shamt`
(`rs` ignorado)

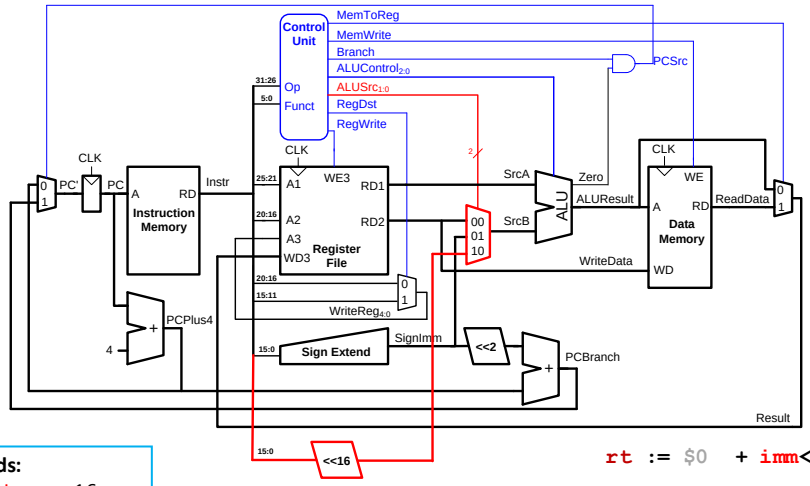
1. $ALUControl_{3:0}$ tem agora 4 bits (+1bit para tb suportar outros *shifts*)
2. ALU tem uma entrada extra: $shamt_{4:0}$

ProbSC (3), P7.3b (1) - LUI: Datapath

(rs = 0)

31:26	25:21	20:16	15:0
15	0	rt	imm

lui rt,imm($0) tipo-I



Mods:
1. Imm << 16
2. AluSrc: 3 inputs

Datapath single-cycle modificado para lui

rt := $0 + imm<<16

Result = $0 + imm<<16

ProbSC (4), P7.3b (2) - LUI: Main Decoder

Instruction	$Op_{5:0}$	RegWrite	RegDst	$AluSrc_{1:0}$	Branch	MemWrite	MemToReg	$ALUOp_{1:0}$
R-type	000000	1	1	00	0	0	0	10
lw	100011	1	0	01	0	0	1	00
sw	101011	0	X	01	0	1	X	00
beq	000100	0	X	00	1	0	X	01
lui	001111	1	0	10	0	0	0	00

$AluSrc_{1:0}$ = 10 e $ALUOp_{1:0}$ = 00

Tabela de verdade do *ALU decoder* para lui

ProbSC (5), P7.3c (1) - STLI: ALU + Main Decoders

10	rs	rt	imm

`slti rt,rs,imm` — `tipo-I`

slti é uma instrução do **tipo-I**, por isso precisamos de criar um novo código ALUOp.

No caso de addi (visto na aula anterior) não era necessário porque o código ALUOp=00 já existia.

$ALUOp_{1:0}$	$Funct_{5:0}$	$ALUControl_{2:0}$
00	X	010 (Add)
01	X	110 (Subtract)
10	100000 (add)	010 (Add)
10	100010 (sub)	110 (Subtract)
10	100100 (and)	000 (And)
10	100101 (or)	001 (Or)
10	101010 (slt)	111 (SLT)
11	X	111 (SLT)

O *datapath* não precisa de ser modificado. Só a Unidade de Controlo tem de ser adaptada.

Tabela de verdade do ALU decoder para slti

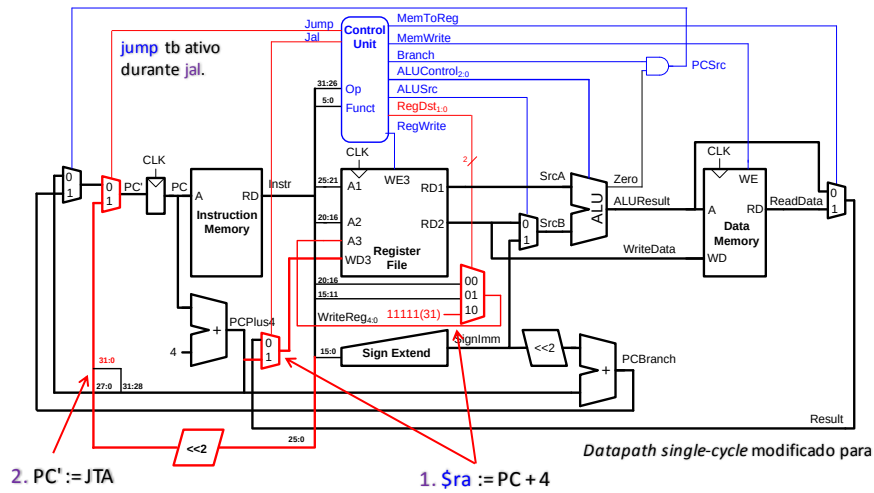
Instruction	$Op_{5:0}$	RegWrite	RegDst	AluSrc	Branch	MemWrite	MemToReg	$ALUOp_{1:0}$
R-type	000000	1	1	0	0	0	0	10
lw	100011	1	0	1	0	0	1	00
sw	101011	0	X	1	0	1	X	00
beq	000100	0	X	0	1	0	X	01
slti	001010	1	0	1	0	0	0	11

Tabela de verdade do *Main decoder* para slti

ProbSC (6), P7.4a (1) - JAL: Datapath

31:26	25:0
3	imm26

`jal imm26` — `tipo-J`



Datapath single-cycle modificado para jal

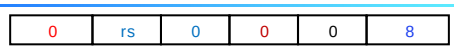
jal label: 1. $ra (31) := PC + 4 ; 2. PC' := JTA com JTA = $(PC + 4)_{31:28}$: ($Imm_{25:0}$ <<2)

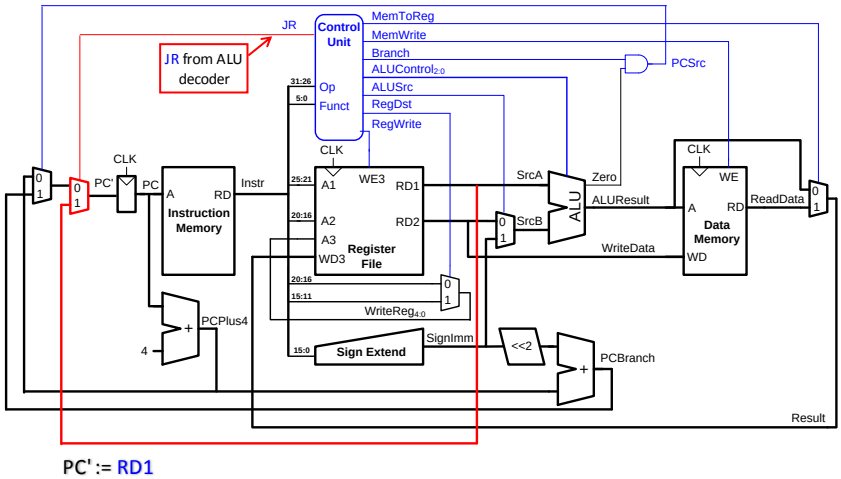
ProbSC (7), P7.4a (2) - JAL: Main Decoder

Instruction	$Op_{5:0}$	RegWrite	$RegDst_{1:0}$	AluSrc	Branch	MemWrite	MemToReg	$ALUOp_{1:0}$	Jump	Jal
R-type	000000	1	01	0	0	0	0	10	0	0
lw	100011	1	00	1	0	0	1	00	0	0
sw	101011	0	XX	1	0	1	X	00	0	0
beq	000100	0	XX	0	1	0	X	01	0	0
addi	001000	1	00	1	0	0	0	00	0	0
j	000010	0	XX	X	X	0	X	XX	1	0
jal	000011	1	10	X	X	0	X	XX	1	1

Tabela de verdade do *Main decoder* para jal

ProbSC (8), P7.4c (1) - JR: Datapath





PC' := RD1

Datapath single-cycle modificado para jr

ProbSC (9), P7.4c (2) - JR: ALU Decoder

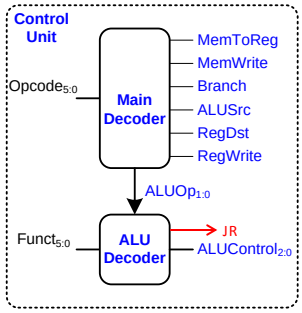
(rd=rt=0)

0	rs	0	0	0	8	jr rs

Tipo-R

$ALUOp_{1:0}$	$Funct_{5:0}$	$ALUControl_{2:0}$	JR
00	X	010 (Add)	0
X1	X	110 (Subtract)	0
1X	100000 (add)	010 (Add)	0
1X	100010 (sub)	110 (Subtract)	0
1X	100100 (and)	000 (And)	0
1X	100101 (or)	001 (Or)	0
1X	101010 (slt)	111 (SLT)	0
1X	001000 (jr)	XXX	1

Tabela de verdade do *ALU decoder* para jr

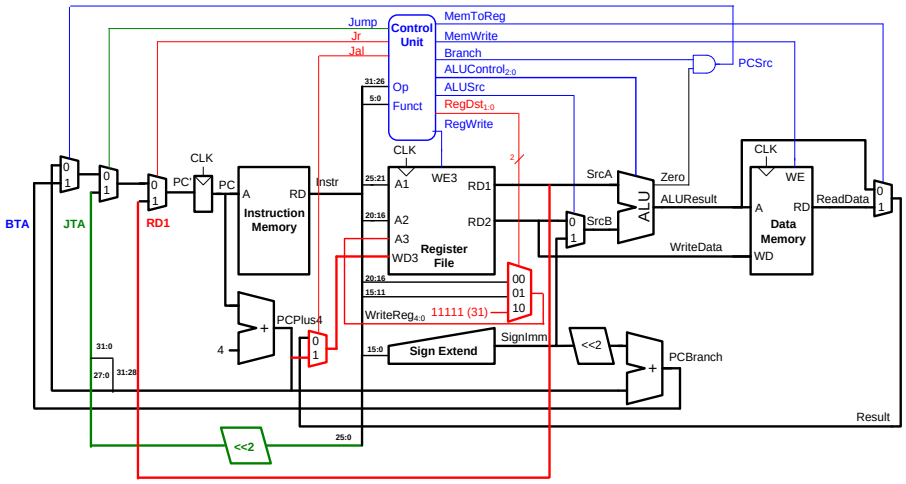


O sinal JR é gerado no *ALU decoder*, porque é aí que o $Funct_{5:0}$ está ligado.

Tabela de verdade do *Main decoder* para jr : sem modificações.

jr é uma instrução de Tipo-R, com a particularidade de ambos rt e rd serem zero.

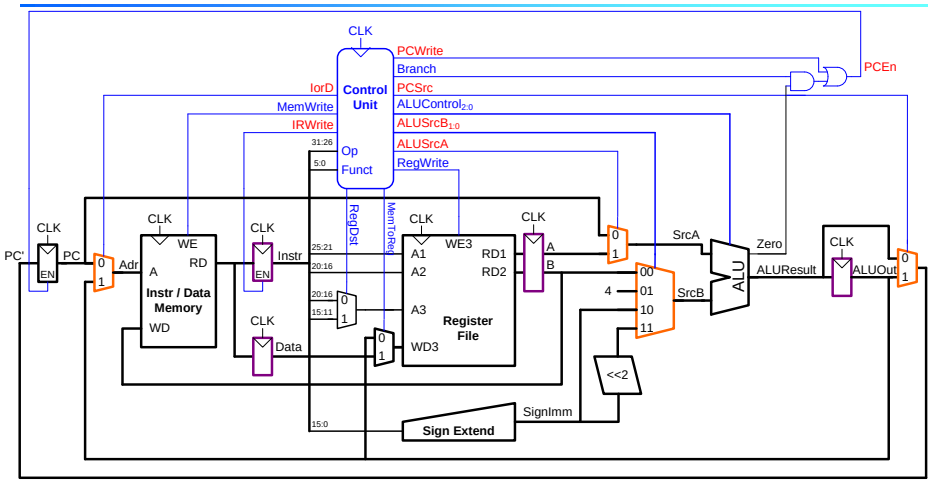
ProbSC (10), P7.4a + P7.4c - JAL + JR: Datapath



Datapath single-cycle modificado para jal + jr
(jal precisa de jr)

Para podermos usar subrotinas, o Datapath do CPU deve suportar ambas as instruções 'jal' e 'jr'.

XX - A seguir: DataPath Multicycle



- Uma única Memória (*Von Neumann*) e uma única ALU.
- Unidade de Controlo mais complexa: FSM (*Finite State Machine*).