VHDL Template for Regular FSM

```
1  ----------------------------------------------------
2  LIBRARY ieee;
3  USE ieee.std_logic_1164.all;
4  ----------------------------------------------------
5  ENTITY <entity_name> IS
6     GENERIC (...);
7     PORT (clk, rst: IN STD_LOGIC;
8           input1, input2: IN <data_type>;
9           output1, output2: OUT <data_type>);
10 END ENTITY;
11 ----------------------------------------------------
12 ARCHITECTURE <archit name> OF <entity name> IS
13    TYPE state IS (A, B, C, ...);
14    SIGNAL pr_state, nx_state: state;
15 BEGIN
16
17    --Lower section of FSM:
18    PROCESS (clk, rst)
19    BEGIN
20       IF (rst='1') THEN
21          pr_state <= A;
22       ELSIF (clk'EVENT AND clk='1') THEN
23          pr_state <= nx_state;
24       END IF;
25    END PROCESS;
26
27    --Upper section of FSM:
27    --Upper section of FSM:
28    PROCESS (all)
29    BEGIN
30       CASE pr_state IS
31          WHEN A =>
32             output1 <= <value>;
33             output2 <= <value>;
34             IF input1=... and ... THEN
35                nx_state <= B;
36             ELSIF input2=... and ... THEN
37                nx_state <= ...;
38             ELSE
39                nx_state <= A;
40             END IF;
41          WHEN B =>
42             output1 <= <value>;
43             output2 <= <value>;
44             IF ... THEN
45                nx_state <= C;
46             ELSIF ... THEN
47                nx_state <= ...;
48             ELSE
49                nx_state <= B;
50             END IF;
51          WHEN C =>
52             ...
53       END CASE;
54    END PROCESS;
```