

```

1  -----
2  LIBRARY ieee;
3  USE ieee.std_logic_1164.all;
4  -----
5  ENTITY <entity_name> IS
6      (same as for regular machines)
7  END ENTITY;
8  -----
9  ARCHITECTURE <archit_name> OF <entity_name> IS
10
11      --FSM-related declarations:
12      (same as for regular machines)
13
14      --Timer-related declarations:
15      CONSTANT T1: NATURAL := <value>;
16      CONSTANT T2: NATURAL := <value>; ...
17      CONSTANT tmax: NATURAL := <value>;
18      SIGNAL t: NATURAL RANGE 0 TO tmax;
19
20  BEGIN
21
22      --Timer:
23      PROCESS (clk, rst)
24      BEGIN
25          IF (rst='1') THEN
26              t <= 0;
27          ELSIF (clk'EVENT AND clk='1') THEN
28              IF pr_state /= nx_state THEN
29                  t <= 0;
30              ELSIF t /= tmax THEN
31                  t <= t + 1;
32              END IF;
33          END IF;
34      END PROCESS;

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35  --Lower section of FSM:
36  (same as for regular machines)
37
38  --Upper section of FSM:
39  PROCESS (all)
40  BEGIN
41      CASE pr_state IS
42          WHEN A =>
43              output1 <= <value>;
44              output2 <= <value>;
45              IF ... AND t>=T1-1 THEN
46                  nx_state <= B;
47              ELSIF ... AND t>=T2-1 THEN
48                  nx_state <= ...;
49              ELSE
50                  nx_state <= A;
51              END IF;
52          WHEN B =>
53              output1 <= <value>;
54              output2 <= <value>;
55              IF ... AND t>=T3-1 THEN
56                  nx_state <= C;
57              ELSIF ... THEN
58                  nx_state <= ...;
59              ELSE
60                  nx_state <= B;
61              END IF;
62          WHEN C =>
63              ...
64      END CASE;
65  END PROCESS;
66
67  --Optional output register:
68  (same as for regular machines)
69
70  END ARCHITECTURE;
71  -----

```