Digital Systems

Memory Elements

1. Complete the temporal diagram of figure 1 for a flip-flop latch SRE. Assume that initial state of the flip-flop is zero. Identify all the states of the flip-flop over the entire diagram.

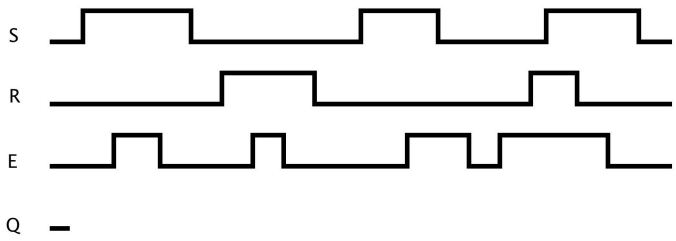

Figura 1: Temporal diagram of the latch SRE flip-flop

2. For the circuits of figures 2 e 3, complete the temporal diagram for Q1 and Q2. Assume that initial state of the flip-flops is zero.

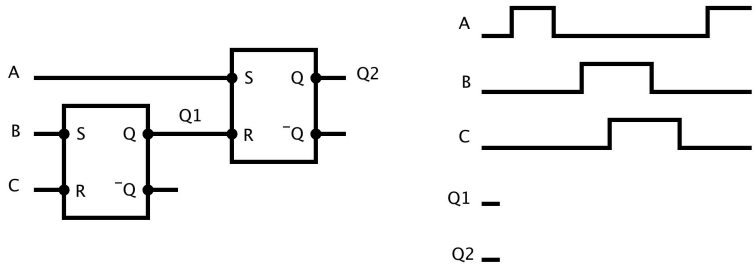

Figura 2: Circuit 1

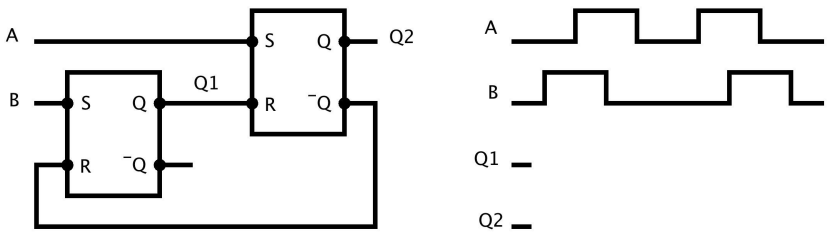

Figura 3: Circuit 2

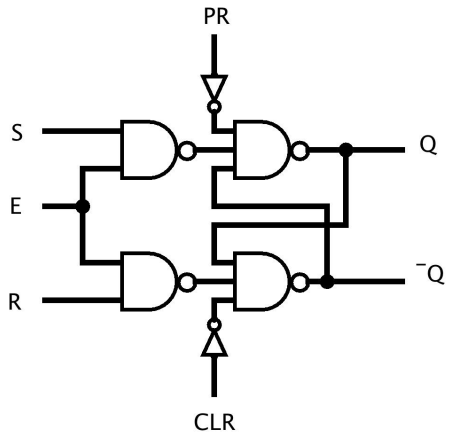

Figura 4: Latch SRE with asynchronous inputs `Preset` e `Clear`

3. Consider the flip-flop latch SRE with the asynchronous inputs `Preset` e `Clear`, represented in figure 4. Show that the behavior of the flip-flop is according to what was presented in the theoretical class.

4. The flip-flop A edge-triggered is obtained by transforming a flip-flop JK as shown in figure 5. Is this flip-flop easily used in practice or does it present any problems.

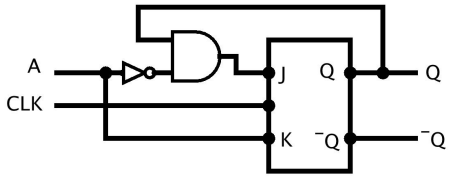

Figura 5: Edge-triggered Flip-flop A circuit