# Power Electronics
## Self Regulating Buck Converter System

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# The Buck Converter

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*Abstract*— **A buck converter was designed that could effectively decrease the output voltage of a circuit, depending on the duty cycle of the system. The converter was able to produce accurate output voltages at varying input voltages and duty cycles. Additionally, a regulator was made out of the buck converter in order for the circuit to be able to account for disturbances. This system used a feedback loop and was effective at maintaining the output of the converter.**

## I. INTRODUCTION

The buck converter that was designed and furthermore analyzed, was composed of an IRF540 power NMOS transistor, a TC1413N MosFET driver chip, and an F15UP20 diode. The passive devices used include a 500$\mu$H inductor, a 47$\mu$F capacitor, and a 10$\Omega$ power resistor. These components were specifically chosen to maintain continuous conduction mode (ccm) and yield a 2.66% voltage ripple with a 10kHz switching speed .

The purpose of this converter was to be able to produce an appropriate output voltage ($V_{out}$) depending on the duty cycle being given to the gate of the power MosFET. The converter circuit was designed on a printed circuit board (PCB) and tested experimentally and with PSPICE to determine the effect that a range of duty cycles has on the output voltage of the converter at different input voltages ($V_{in}$). Based on these experiments, a linear relationship between $V_{out}$ and duty cycle was established. This lead to the creation of a regulator circuit that implemented a feedback loop to adjust the duty cycle of the system to maintain $V_{out}$ at a desired voltage.

The objectives of this project can be seen below.

1) Design Buck Converter
2) Simulate Converter Results
3) Build and Test Converter
4) Design and Implement Regulator Circuit

## II. BACKGROUND

Buck converters are circuits that are very commonly used to deliver a smaller output voltage to the load compared to the input voltage. This is done by a high speed switching transistor that connects the input and output of the circuit. The basic layout of the buck converter can be seen below.

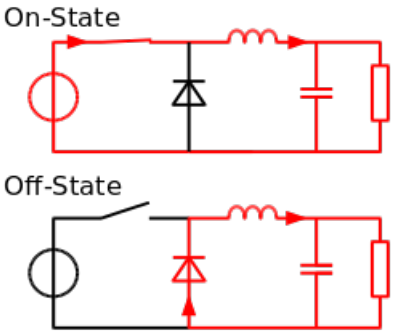


Fig. 1: Buck Converter Layout

As Figure 1 depicts, a buck converter functions in two different modes; Mode 1: On-State (Switch is closed) and Mode 2: Off-State (switch is open). The switching transistor toggles at high frequencies, effectively dropping the input voltage to a value directly correlated to the duty cycle of the switch. For example, if $V_{in}$ equals 7V and the switch has a 50% duty cycle then $V_{out}$ will equal 3.5V. The input voltage and the duty cycle share an inverse relationship, meaning that if one increases the other must in turn decrease to maintain a constant output voltage. The equation for finding the output voltage of a buck converter can be seen below in Equation 1.

$$V_{out} = D * V_{in} \tag{1}$$

Although the input is disconnected from the circuit when the switch is open, the output voltage is able to be maintained by using the energy stored in the inductor when the switch is closed. When the switch is closed, the diode is reverse biased allowing the input voltage to be dropped across the inductor and reach the load. However, when the switch is open, the polarity of the inductor is flipped, allowing current to move in the opposite direction. This current forward bias the diode, completing the circuit and furthermore maintains the output voltage.

The passive components of the buck converter have to be very carefully selected as the inductor has to have a value above a specific critical inductance in order to maintain ccm and the capacitor must be adjusted to provide a desired output voltage ripple. The equation for critical inductance and output voltage ripple can be seen below in Equations 2 and 3 respectively.

$$L_{crit} = \frac{1-D}{2} * T * R \tag{2}$$

$$\frac{\Delta V_{out}}{V_{out}} = \frac{1-D}{8*L*C*f^2} \tag{3}$$

It is important to note that once $L_{crit}$ is determined, the actual inductor value used in the circuit must be larger than the calculated critical inductance. A good rule of thumb is to choose an inductor that is 100 times greater than $L_{crit}$. This inductor value can then be used to find the necessary capacitor value to yield the desired output voltage ripple.

## III. PROCEDURE

The buck converter circuit was designed on a PCB, using the program DipTrace, in order to eliminate the need for wires between the different components. This produced a more condensed and easy-to-examine circuit. Figure 2 below depicts a model of the PCB buck converter circuit.

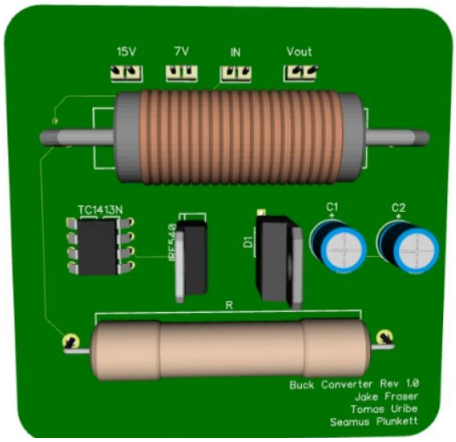


Fig. 2: PCB Buck Converter Circuit

Once the circuit had been designed, the program OrCAD was used to simulate the behavior of the output voltage at varying duty cycles and input voltages. $V_{out}$ was simulated according to a $V_{in}$ ranging from 1-7V while sweeping the duty cycle of the system from 5-95% for each input. The PSPICE model of every component of the buck converter were adjusted to match the exact parts being soldered to the PCB to ensure that all simulations were as accurate as possible. However, the PSPICE model for the TC1413N MosFET driver chip could not be found so a simple low-side MosFET switch was implemented using a RIT4007N NMOS to imitate the behavior of the driver. A schematic of the circuit used for the buck converter simulations can be seen below in Figure 3.

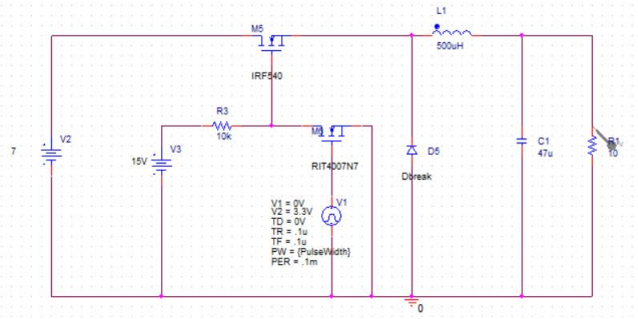


Fig. 3: Buck Converter Schematic

The simulations were used as a point of comparison when the actual buck converter began to be experimentally tested. The tests conducted were performed identically to the set-up of the simulations. The output voltage of the converter was measured for different input voltages and duty cycles. In these tests a two output power supply was used to provide not only the input voltage but to also provide 15V to the supply voltage pin of the mosFET driver. Additionally, a function generator was used to supply the input of the mosFET driver with a square wave. Depending on the duty cycle of the this wave, 15 V would be supplied to the gate of the power mosFET, effectively changing the output of the circuit.

As for the regulator, it was implemented by introducing a feedback loop to the system in order for the duty cycle of the square wave going into the input of the mosFET chip to constantly be adjusted to maintain a desired output voltage. This was achieved by using an MSP430G2553 microcontroller. The output voltage was feed into the analog to digital (A/D) converter of the processor after begin passed through a voltage divider, in order to not damage processor pins. Once the processor read an output voltage reading, an error correcting algorithm was used to adjust the duty cycle of the pulse width modulation (PWM) signal being output to the mosFET driver. This algorithm ensured that the output voltage of the circuit would remain constant, regardless of any disturbances i.e. a change in load resistance. Figures 4 and 5 below depict the schematic of the regulator and the actual experimental implementation of the circuit.

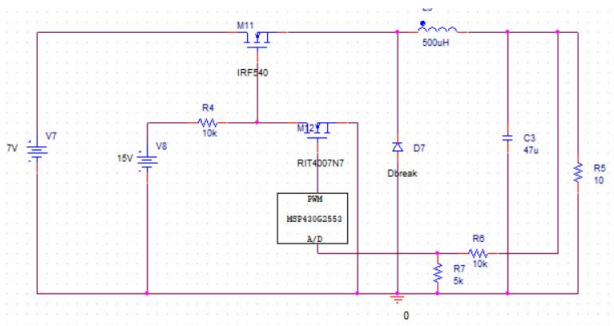


Fig. 4: Regulator Schematic

**NOTE:** The schematic of the regulator does not contain the actual TC1413N mosFET driver as a PSPICE model was not available.

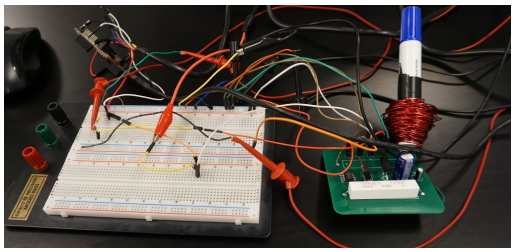

Fig. 5: Buck Converter, Regulator Implementation

## IV. RESULTS & DISCUSSION

**NOTE:** The data presented will reflect input voltages of 2,5,and 7 V. All other data will be available in the Appendix

### A. Simulations

On PSPICE, the circuit seen in Figure 3 was analyzed by using a simulation profile that used a duty cycle sweep. With this sweep the output voltage was measured, given different input voltages, as a function of time. Figures 6-8 depict the simulation results of the buck converter with a 2,5, and 7V input respectively

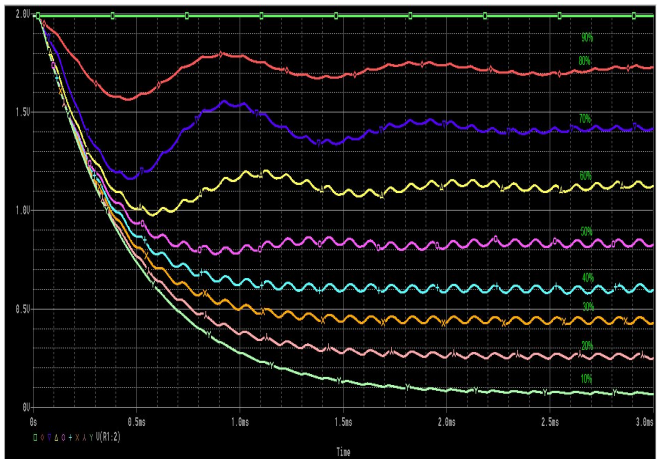


Fig. 6: Output voltage caused by different duty cycles, when $V_{in}$ =2V

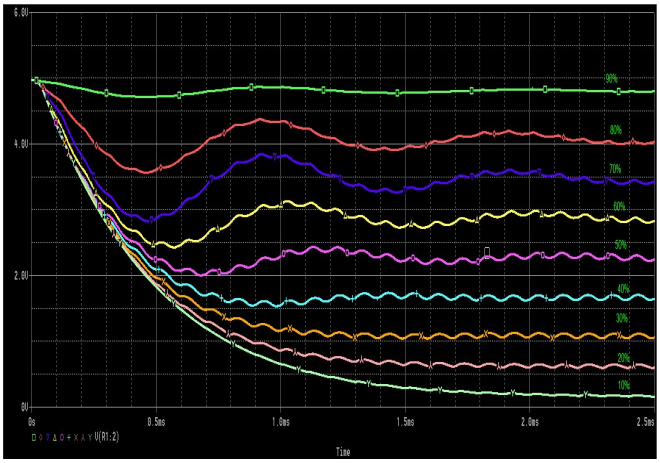


Fig. 7: Output voltage caused by different duty cycles, when $V_{in}$ =5V

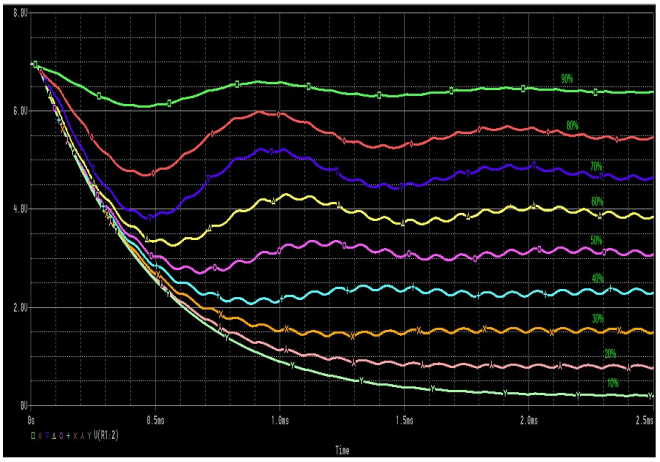


Fig. 8: Output voltage caused by different duty cycles, when $V_{in}$ =7V

Since each line that was produced by the simulation represented a different duty cycle, a relationship between the output voltage and the duty cycle was identified. This was done by extrapolating the steady state $V_out$ corresponding to each duty cycle, and creating tables in Microsoft Excel to relate the duty cycle to the output voltage, at every given input. Additionally the simulated output voltages were compared to the ideal output voltages for each input voltage and duty cycle. These calculations were made using Equation 1. The data below shows the extrapolated $V_{out}$ values for each individual duty cycle at an input of 2,5,and 7V respectively.

| $V_{in}$ = 2V | | |
|---|---|---|
| Duty Cycle (%) | Calculated $V_{out}$ (V) | Simulated $V_{out}$ (V) |
| 5 | 0.1 | 0.005 |
| 10 | 0.2 | 0.069 |
| 20 | 0.4 | 0.259 |
| 30 | 0.6 | 0.44 |
| 40 | 0.8 | 0.599 |
| 50 | 1 | 0.808 |
| 60 | 1.2 | 1.12 |
| 70 | 1.4 | 1.41 |
| 80 | 1.6 | 1.71 |
| 90 | 1.8 | 1.99 |
| 95 | 1.9 | 1.99 |

Fig. 9: Simulated and calculated data comparing $V_{out}$ and duty cycle with an input of 2V

| $V_{in}$ = 5V | | |
|---|---|---|
| Duty Cycle (%) | Calculated $V_{out}$ (V) | Simulated $V_{out}$ (V) |
| 5 | 0.25 | 0.006 |
| 10 | 0.5 | 0.162 |
| 20 | 1 | 0.632 |
| 30 | 1.5 | 1.11 |
| 40 | 2 | 1.68 |
| 50 | 2.5 | 2.28 |
| 60 | 3 | 2.89 |
| 70 | 3.5 | 3.47 |
| 80 | 4 | 4.06 |
| 90 | 4.5 | 4.81 |
| 95 | 4.75 | 4.97 |

Fig. 10: Simulated and calculated data comparing $V_{out}$ and duty cycle with an input of 5V

| $V_{in}$ = 7V | | |
|---|---|---|
| Duty Cycle (%) | Calculated $V_{out}$ (V) | Simulated $V_{out}$ (V) |
| 5 | 0.35 | 0.006 |
| 10 | 0.7 | 0.192 |
| 20 | 1.4 | 0.804 |
| 30 | 2.1 | 1.54 |
| 40 | 2.8 | 2.3 |
| 50 | 3.5 | 3.13 |
| 60 | 4.2 | 3.91 |
| 70 | 4.9 | 4.73 |
| 80 | 5.6 | 5.48 |
| 90 | 6.3 | 6.39 |
| 95 | 6.65 | 6.94 |

Fig. 11: Simulated and calculated data comparing $V_{out}$ and duty cycle with an input of 7V

Lastly, once the data from the simulations had been tabularized, a linear relationship between output voltage and duty cycle was identified by graphing the information.A line of best fit provided a linear equation that could be used to better predict the necessary duty cycle a system needs to produce a desired output.

Figures 12-14 display the $V_{out}$ vs Duty Cycle plots for inputs of 2,5, and 7V

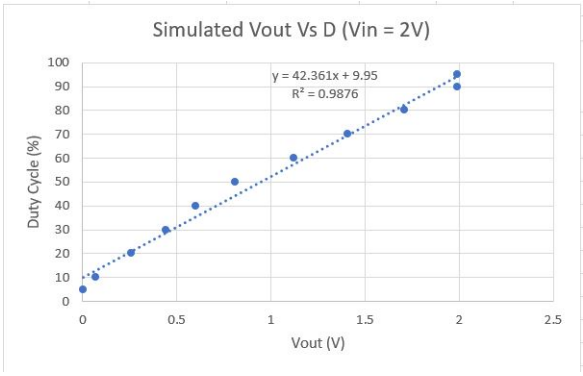


Fig. 12: Simulated $V_{out}$ vs Duty Cycle, $V_{in}$=2V

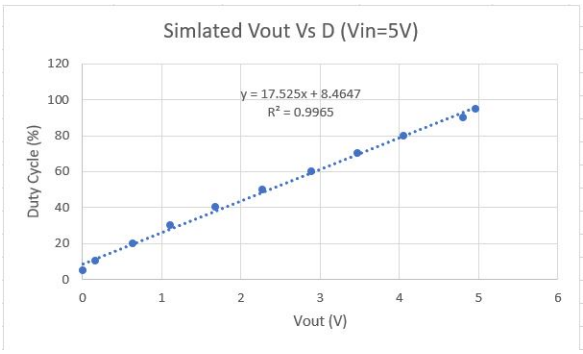


Fig. 13: Simulated $V_{out}$ vs Duty Cycle, $V_{in}$=5V

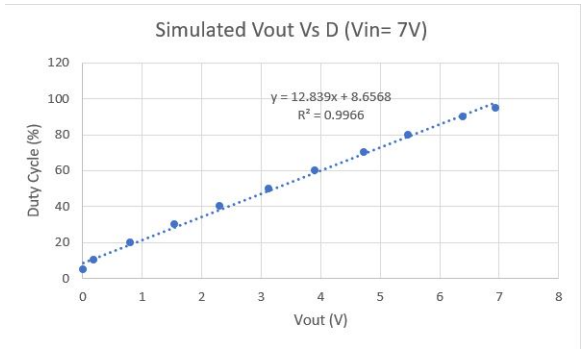


Fig. 14: Simulated $V_{out}$ vs Duty Cycle, $V_{in}$=7V

## B. Experiments

When the physical buck converter was tested, data was extrapolated and organized very similarly to the simulations. For every single input voltage, the output voltage was measured at varying duty cycles. However, additional parameters, such as power efficiency, were also determined in order to establish if the buck converter could even be used as a viable switch. The gathered data can be seen below for corresponding input voltages of 2V,5V, and 7V.

| Vin = 2V | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Duty Cycle | 5% | 10% | 20% | 30% | 40% | 50% | 60% | 70% | 80% | 90% | 95% |
| $I_{in}$ (A) | 0.01 | 0.01 | 0.01 | 0.01 | 0.02 | 0.03 | 0.05 | 0.07 | 0.1 | 0.13 | 0.15 |
| $P_{in}=V_{in}*I_{in}$ (W) | 0.02 | 0.02 | 0.02 | 0.02 | 0.04 | 0.06 | 0.1 | 0.14 | 0.2 | 0.26 | 0.3 |
| $V_{out}$ (V) | 0.0255 | 0.083 | 0.2 | 0.4 | 0.55 | 0.7 | 0.89 | 1.12 | 1.34 | 1.58 | 1.69 |
| $Pout=V^2_{out}/R_L$ | 6.5E-05 | 0.00069 | 0.004 | 0.02 | 0.0303 | 0.05 | 0.08 | 0.12 | 0.18 | 0.25 | 0.29 |
| Describe temperature of load resistor | Warm | Warm | Warm | Warm | Warm | Warm | Warm | Warm | Warm | Warm | Warm |
| η (%) | 0.325125 | 3.4445 | 20 | 78 | 75.625 | 81.7 | 78.3 | 89 | 89.8 | 96 | 95.2 |

Fig. 15: Experimental data comparing $V_{out}$ and duty cycle with an input of 2V

| Vin = 5V | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Duty Cycle | 5% | 10% | 20% | 30% | 40% | 50% | 60% | 70% | 80% | 90% | 95% |
| $I_{in}$ (A) | 0.01 | 0.01 | 0.01 | 0.03 | 0.06 | 0.1 | 0.15 | 0.21 | 0.27 | 0.34 | 0.38 |
| $P_{in}=V_{in}*I_{in}$ (W) | 0.05 | 0.05 | 0.05 | 0.15 | 0.3 | 0.5 | 0.75 | 1.05 | 1.35 | 1.7 | 1.9 |
| $V_{out}$ (V) | 0.122 | 0.311 | 0.729 | 1.13 | 1.51 | 2.01 | 2.52 | 3.03 | 3.53 | 4.03 | 4.28 |
| $Pout=V^2_{out}/R_L$ | 0.001488 | 0.00967 | 0.053 | 0.13 | 0.228 | 0.4 | 0.64 | 0.92 | 1.25 | 1.62 | 1.83 |
| Describe temperature of load resistor | Warm | Warm | Warm | Warm | Warm | Warm | Warm | Warm | Warm | Warm | Warm |
| η (%) | 2.9768 | 19.3442 | 106.3 | 85.1 | 76.003 | 80.8 | 84.7 | 87.4 | 92.3 | 95.5 | 96.4 |

Fig. 16: Experimental data comparing $V_{out}$ and duty cycle with an input of 5V

| Vin = 7V | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Duty Cycle | 5% | 10% | 20% | 30% | 40% | 50% | 60% | 70% | 80% | 90% | 95% |
| $I_{in}$ (A) | 0.01 | 0.01 | 0.02 | 0.05 | 0.09 | 0.14 | 0.21 | 0.29 | 0.38 | 0.48 | 0.53 |
| $P_{in}=V_{in}*I_{in}$ (W) | 0.07 | 0.07 | 0.14 | 0.35 | 0.63 | 0.98 | 1.47 | 2.03 | 2.66 | 3.36 | 3.71 |
| $V_{out}$ (V) | 0.178 | 0.47 | 1.07 | 1.62 | 2.22 | 2.9 | 3.6 | 4.3 | 4.98 | 5.66 | 6 |
| $Pout=V^2_{out}/R_L$ | 0.00317 | 0.02209 | 0.11 | 0.26 | 0.49 | 0.84 | 1.3 | 1.85 | 2.48 | 3.2 | 3.6 |
| Describe temperature of load resistor | Warm | Warm | Warm | Warm | Warm | Warm | Warm | Warm | Warm | Warm | Warm |
| η (%) | 4.52629 | 31.5571 | 81.8 | 75 | 78.2 | 85.8 | 88.2 | 91.1 | 93.2 | 95.3 | 97 |

Fig. 17: Experimental data comparing $V_{out}$ and duty cycle with an input of 7V

As Figures 15-17 depict, the buck converter becomes more efficient, the higher the duty cycle is. In all 3 cases the efficiency of the circuit lies between 80-100% when the duty cycle becomes more than 50%. Although, a switch is supposed to yield 100% efficiency, losses can be attributed to the circuit not being composed of ideal components. Furthermore, this proves that although a switch can theoretically be 100% efficient, it will always have losses whenever it is practically used. As for the large losses when the duty cycle was between 5-10%, this can be attributed to inaccurate measurements of relatively minuscule output voltages.

For the experimental data, $V_{out}$ vs Duty Cycle was also plotted for each input voltage. Like the simulated data this was done to reveal the linear relationship of the data in order to create a line of best fit that would yield an equation for the behavior of the system. These plots can be seen below in Figures 18-20

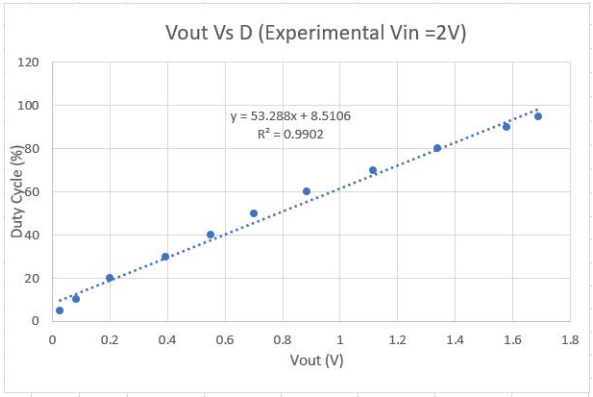


Fig. 18: $V_{out}$ vs Duty Cycle, $V_{in}$=2V

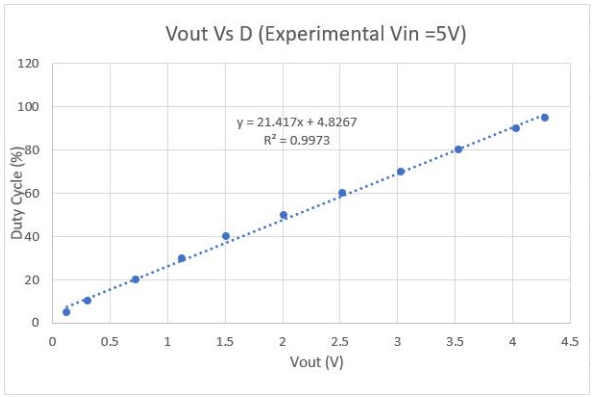


Fig. 19: $V_{out}$ vs Duty Cycle, $V_{in}$=5V

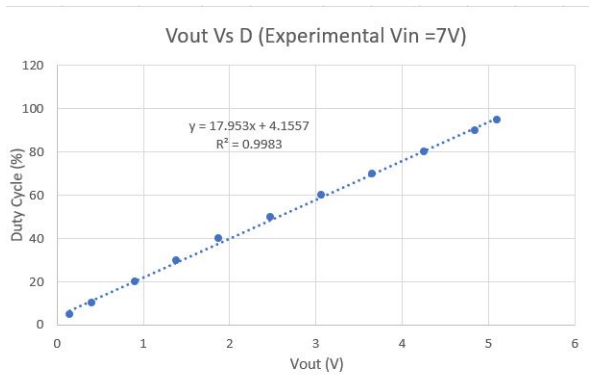


Fig. 20: $V_{out}$ vs Duty Cycle, $V_{in}$=2V

Compared to Equation 1, the equations produced by the plots above could more accurately determine the duty cycle of the converter given an output voltage. The reason these equations were more reliable was because they were personalized for every single input voltage and furthermore accounted for the losses of the system.

### C. Simulated vs Experimental

The percent error between the simulated and experimental data was found for each input voltage in order to determine if the simulations accurately predicted the behavior of the buck converter. The figures below display the percent error between the simulated and experimental output voltage of the converter for $V_{in}$ equal 2,5, and 7V respectively.

| $V_{in}$ = 2V | | | |
|---|---|---|---|
| Duty Cycle (%) | Experimental $V_{out}$ (V) | Simulated $V_{out}$ (V) | Percent Error(%) |
| 5 | 0.0255 | 0.005 | 410.00 |
| 10 | 0.083 | 0.069 | 20.29 |
| 20 | 0.2 | 0.259 | 22.78 |
| 30 | 0.395 | 0.44 | 10.23 |
| 40 | 0.55 | 0.599 | 8.18 |
| 50 | 0.7 | 0.808 | 13.37 |
| 60 | 0.885 | 1.12 | 20.98 |
| 70 | 1.116 | 1.41 | 20.85 |
| 80 | 1.34 | 1.71 | 21.64 |
| 90 | 1.58 | 1.99 | 20.60 |
| 95 | 1.69 | 1.99 | 15.08 |

Fig. 21: Percent error between simulated and experimental data, $V_{in}$=2V

| $V_{in}$ = 5V | | | |
|---|---|---|---|
| Duty Cycle (%) | Experimental $V_{out}$ (V) | Simulated $V_{out}$ (V) | Percent Error(%) |
| 5 | 0.122 | 0.006 | 1933.33 |
| 10 | 0.311 | 0.162 | 91.98 |
| 20 | 0.729 | 0.632 | 15.35 |
| 30 | 1.13 | 1.11 | 1.80 |
| 40 | 1.51 | 1.68 | 10.12 |
| 50 | 2.01 | 2.28 | 11.84 |
| 60 | 2.52 | 2.89 | 12.80 |
| 70 | 3.03 | 3.47 | 12.68 |
| 80 | 3.53 | 4.06 | 13.05 |
| 90 | 4.03 | 4.81 | 16.22 |
| 95 | 4.28 | 4.97 | 13.88 |

Fig. 22: Percent error between simulated and experimental data, $V_{in}$=5V

| $V_{in}$ = 7V | | | |
|---|---|---|---|
| Duty Cycle (%) | Experimental $V_{out}$ (V) | Simulated $V_{out}$ (V) | Percent Error(%) |
| 5 | 0.178 | 0.006 | 2866.67 |
| 10 | 0.47 | 0.192 | 144.79 |
| 20 | 1.07 | 0.804 | 33.08 |
| 30 | 1.62 | 1.54 | 5.19 |
| 40 | 2.22 | 2.3 | 3.48 |
| 50 | 2.9 | 3.13 | 7.35 |
| 60 | 3.6 | 3.91 | 7.93 |
| 70 | 4.3 | 4.73 | 9.09 |
| 80 | 4.98 | 5.48 | 9.12 |
| 90 | 5.66 | 6.39 | 11.42 |
| 95 | 6 | 6.94 | 13.54 |

Fig. 23: Percent error between simulated and experimental data, $V_{in}$=7V

Similar to the efficiency of the converter, the percent error was more agreeable for larger duty cycles. For duty cycles below 10%, the error was, at times, 2 orders of magnitudes greater than larger duty cycles. This discrepancy can be attributed to incorrect measurements as well.

### D. Regulator

The regulator that was created was proven to be able to adjust its duty cycle to maintain a constant output voltage. The desired output voltage could be changed and the system would adjust to meet this voltage. Additionally, the regulator was able to account for disturbances such as a change in its load and input voltage. However, there was some irregularities with the steady state output voltage. For example, if the desired $V_{out}$ was 3V, the system would produce an output of about 3.2V. The reason for this is because there was a lot of oscillation in the system once it reached steady state. This problem could be solved in code by implementing a PI controller to effectively remove the steady state error of the system. A video of the working regulator can be seen in the link below

https://tinyurl.com/Regulator-PWRElectronics

## V. CONCLUSIONS

The buck converter that was designed and built was proven to be able to produce a lower output voltage than its input, based on the duty cycle of the system. Additionally,it was proven that PSPICE simulations could be used to predict the behavior of the circuit before the converter was even built. As a regulator, the buck converter was able to account for disturbances in order to always maintain a desired output voltage. Ultimately, the buck converter was proven to be an effective circuit that can be implemented in many power electronic applications. Future work will include correcting the regulator code in order to produce zero steady state error so the converter always outputs the exact, desired voltage.

## APPENDIX

### A. Simulations

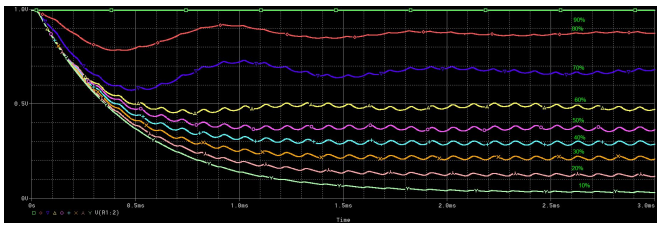

Fig. 24: Output voltage caused by different duty cycles, when $V_{in}$ =1V

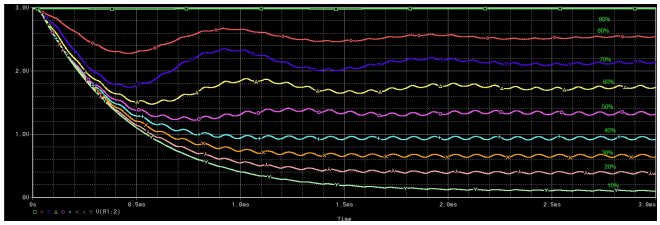

Fig. 25: Output voltage caused by different duty cycles, when $V_{in}$ =3V

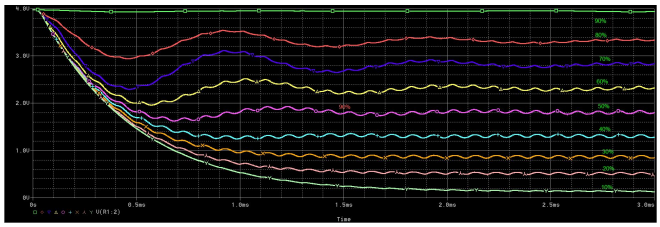

Fig. 26: Output voltage caused by different duty cycles, when $V_{in}$ =4V

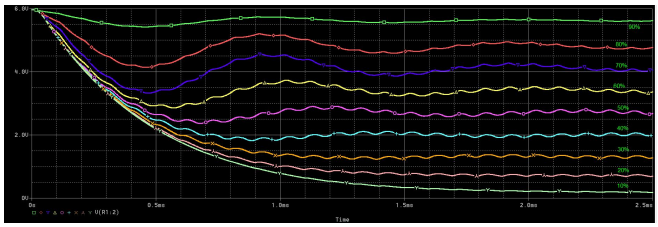

Fig. 27: Output voltage caused by different duty cycles, when $V_{in}$ =6V

| $V_{in}$ = 1V | | |
|---|---|---|
| Duty Cycle (%) | Calculated $V_{out}$ (V) | Simulated $V_{out}$ (V) |
| 5 | 0.05 | 0.003 |
| 10 | 0.1 | 0.033 |
| 20 | 0.2 | 0.123 |
| 30 | 0.3 | 0.216 |
| 40 | 0.4 | 0.293 |
| 50 | 0.5 | 0.377 |
| 60 | 0.6 | 0.482 |
| 70 | 0.7 | 0.672 |
| 80 | 0.8 | 0.873 |
| 90 | 0.9 | 0.994 |
| 95 | 0.95 | 0.995 |

Fig. 28: Simulated and calculated data comparing $V_{out}$ and duty cycle with an input of 1V

| $V_{in}$ = 3V | | |
|---|---|---|
| Duty Cycle (%) | Calculated $V_{out}$ (V) | Simulated $V_{out}$ (V) |
| 5 | 0.15 | 0.006 |
| 10 | 0.3 | 0.105 |
| 20 | 0.6 | 0.396 |
| 30 | 0.9 | 0.662 |
| 40 | 1.2 | 0.939 |
| 50 | 1.5 | 1.35 |
| 60 | 1.8 | 1.72 |
| 70 | 2.1 | 2.14 |
| 80 | 2.4 | 2.53 |
| 90 | 2.7 | 2.98 |
| 95 | 2.85 | 2.98 |

Fig. 29: Simulated and calculated data comparing $V_{out}$ and duty cycle with an input of 3V

| $V_{in}$ = 4V | | |
|---|---|---|
| Duty Cycle (%) | Calculated $V_{out}$ (V) | Simulated $V_{out}$ (V) |
| 5 | 0.2 | 0.006 |
| 10 | 0.4 | 0.137 |
| 20 | 0.8 | 0.525 |
| 30 | 1.2 | 0.882 |
| 40 | 1.6 | 1.31 |
| 50 | 2 | 1.83 |
| 60 | 2.4 | 2.32 |
| 70 | 2.8 | 2.81 |
| 80 | 3.2 | 3.32 |
| 90 | 3.6 | 3.95 |
| 95 | 3.8 | 3.98 |

Fig. 30: Simulated and calculated data comparing $V_{out}$ and duty cycle with an input of 4V

| $V_{in}$ = 6V | | |
|---|---|---|
| Duty Cycle (%) | Calculated $V_{out}$ (V) | Simulated $V_{out}$ (V) |
| 5 | 0.3 | 0.007 |
| 10 | 0.6 | 0.183 |
| 20 | 1.2 | 0.731 |
| 30 | 1.8 | 1.35 |
| 40 | 2.4 | 2.01 |
| 50 | 3 | 2.7 |
| 60 | 3.6 | 3.4 |
| 70 | 4.2 | 4.09 |
| 80 | 4.8 | 4.81 |
| 90 | 5.4 | 5.63 |
| 95 | 5.7 | 5.96 |

Fig. 31: Simulated and calculated data comparing $V_{out}$ and duty cycle with an input of 6V

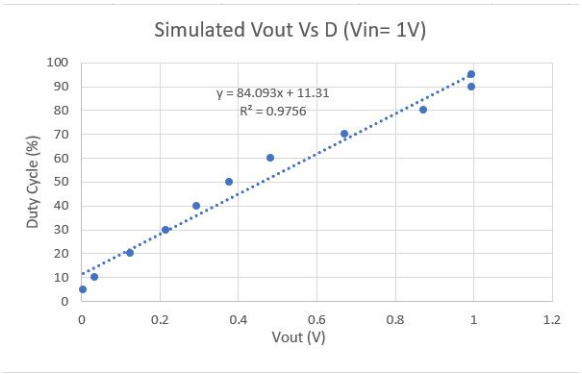


Fig. 32: Simulated $V_{out}$ vs Duty Cycle, $V_{in}$=1V

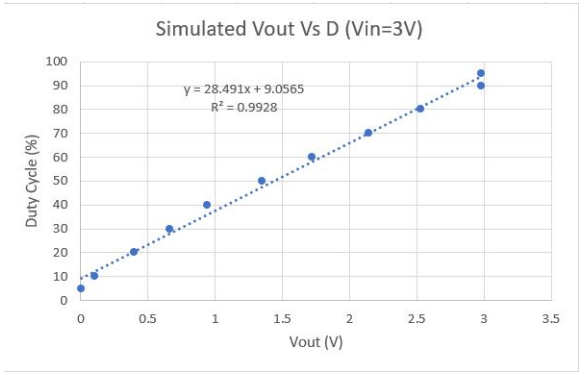


Fig. 33: Simulated $V_{out}$ vs Duty Cycle, $V_{in}$=3V

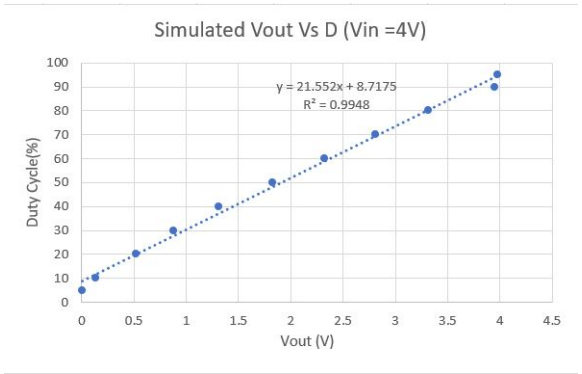


Fig. 34: Simulated $V_{out}$ vs Duty Cycle, $V_{in}$=4V

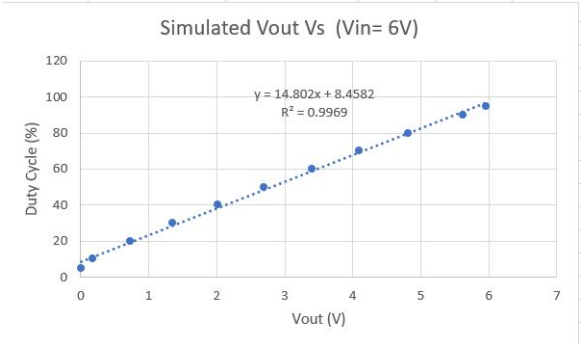


Fig. 35: Simulated $V_{out}$ vs Duty Cycle, $V_{in}$=6V

## B. Experiment

| Vin = 1V | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Duty Cycle | 5% | 10% | 20% | 30% | 40% | 50% | 60% | 70% | 80% | 90% | 95% |
| $I_{in}$ (A) | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.02 | 0.03 | 0.04 | 0.06 | 0.07 |
| $P_{in}=V_{in}*I_{in}$ (W) | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.02 | 0.03 | 0.04 | 0.06 | 0.07 |
| $V_{out}$ (V) | 0.008 | 0.029 | 0.09 | 0.17 | 0.25 | 0.32 | 0.39 | 0.49 | 0.62 | 0.76 | 0.83 |
| $Pout=V^2_{out}/R_L$ | 6.4E-06 | 8.4E-05 | 0 | 0 | 0.01 | 0.01 | 0.01 | 0.02 | 0.04 | 0.06 | 0.07 |
| Describe temperature of load resistor | Warm | Warm | Warm | Warm | Warm | Warm | Warm | Warm | Warm | Warm | Warm |
| η (%) | 0.064 | 0.841 | 8.65 | 28.6 | 60 | 102 | 74.9 | 78.4 | 97 | 97.3 | 98.9 |

Fig. 36: Experimental data comparing $V_{out}$ and duty cycle with an input of 1V

| Vin = 3V | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Duty Cycle | 5% | 10% | 20% | 30% | 40% | 50% | 60% | 70% | 80% | 90% | 95% |
| $I_{in}$ (A) | 0.01 | 0.01 | 0.01 | 0.02 | 0.03 | 0.05 | 0.08 | 0.12 | 0.16 | 0.2 | 0.23 |
| $P_{in}=V_{in}*I_{in}$ (W) | 0.03 | 0.03 | 0.03 | 0.06 | 0.09 | 0.15 | 0.24 | 0.36 | 0.48 | 0.6 | 0.69 |
| $V_{out}$ (V) | 0.049 | 0.15 | 0.39 | 0.64 | 0.86 | 1.11 | 1.42 | 1.75 | 2.07 | 2.4 | 2.56 |
| $Pout=V^2_{out}/R_L$ | 0.0002 | 0.0023 | 0.02 | 0.04 | 0.07 | 0.12 | 0.2 | 0.31 | 0.43 | 0.58 | 0.66 |
| Describe temperature of load resistor | Warm | Warm | Warm | Warm | Warm | Warm | Warm | Warm | Warm | Warm | Warm |
| η (%) | 0.8003 | 7.5 | 51.2 | 67.6 | 82 | 82.1 | 84 | 85.1 | 89.3 | 96 | 95 |

Fig. 37: Experimental data comparing $V_{out}$ and duty cycle with an input of 3V

| Vin = 4V | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Duty Cycle | 5% | 10% | 20% | 30% | 40% | 50% | 60% | 70% | 80% | 90% | 95% |
| $I_{in}$ (A) | 0.01 | 0.01 | 0.01 | 0.03 | 0.05 | 0.07 | 0.11 | 0.16 | 0.21 | 0.28 | 0.31 |
| $P_{in}=V_{in}*I_{in}$ (W) | 0.04 | 0.04 | 0.04 | 0.12 | 0.2 | 0.28 | 0.44 | 0.64 | 0.84 | 1.12 | 1.24 |
| $V_{out}$ (V) | 0.077 | 0.225 | 0.56 | 0.89 | 1.18 | 1.56 | 1.97 | 2.39 | 2.8 | 3.21 | 3.43 |
| $Pout=V^2_{out}/R_L$ | 0.00059 | 0.00506 | 0.03 | 0.08 | 0.14 | 0.24 | 0.39 | 0.57 | 0.78 | 1.03 | 1.18 |
| Describe temperature of load resistor | Warm | Warm | Warm | Warm | Warm | Warm | Warm | Warm | Warm | Warm | Warm |
| η (%) | 1.48225 | 12.6563 | 78.4 | 66 | 69.6 | 86.9 | 88.2 | 89.3 | 93.3 | 92 | 94.9 |

Fig. 38: Experimental data comparing $V_{out}$ and duty cycle with an input of 4V

| Vin = 6V | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Duty Cycle | 5% | 10% | 20% | 30% | 40% | 50% | 60% | 70% | 80% | 90% | 95% |
| $I_{in}$ (A) | 0.01 | 0.01 | 0.02 | 0.04 | 0.07 | 0.12 | 0.18 | 0.25 | 0.33 | 0.42 | 0.47 |
| $P_{in}=V_{in}*I_{in}$ (W) | 0.06 | 0.06 | 0.12 | 0.24 | 0.42 | 0.72 | 1.08 | 1.5 | 1.98 | 2.51 | 2.82 |
| $V_{out}$ (V) | 0.15 | 0.395 | 0.9 | 1.38 | 1.87 | 2.47 | 3.06 | 3.65 | 4.26 | 4.85 | 5.1 |
| $Pout=V^2_{out}/R_L$ | 0.0023 | 0.0156 | 0.08 | 0.19 | 0.35 | 0.61 | 0.94 | 1.33 | 1.81 | 2.35 | 2.6 |
| Describe temperature of load resistor | Warm | Warm | Warm | Warm | Warm | Warm | Warm | Warm | Warm | Warm | Warm |
| η (%) | 3.75 | 26.004 | 67.8 | 79.4 | 83.3 | 84.7 | 86.7 | 88.8 | 91.7 | 93.6 | 92.2 |

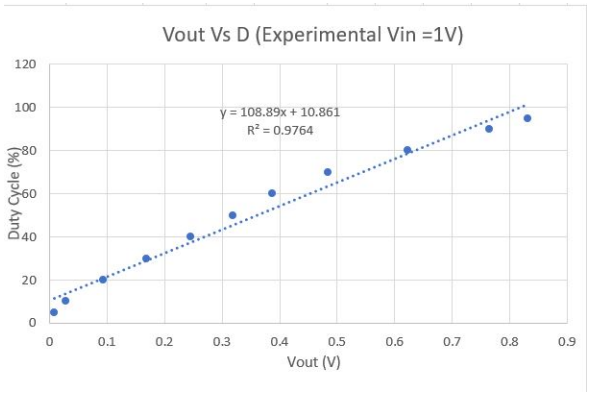


Fig. 40: $V_{out}$ vs Duty Cycle, $V_{in}$=1V

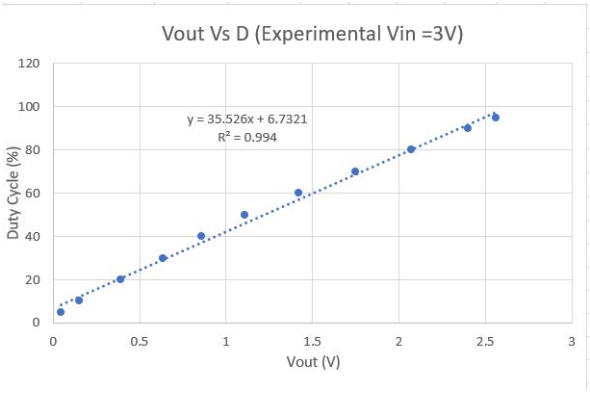


Fig. 41: $V_{out}$ vs Duty Cycle, $V_{in}$=3V

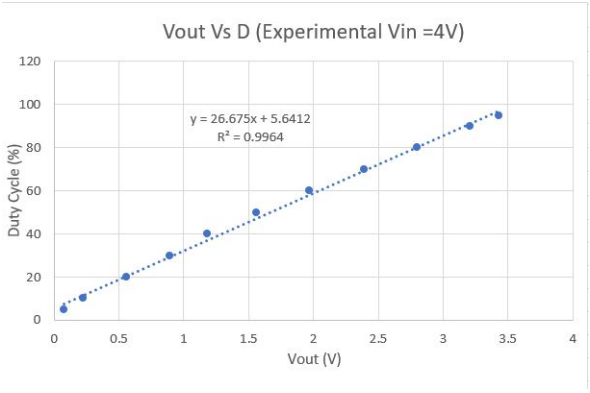


Fig. 42: $V_{out}$ vs Duty Cycle, $V_{in}$=4V

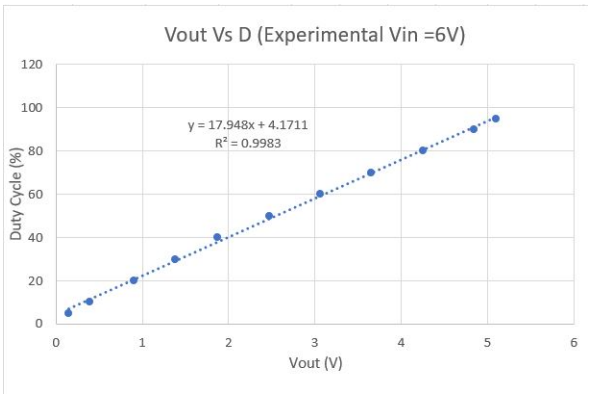


Fig. 43: $V_{out}$ vs Duty Cycle, $V_{in}$=6V

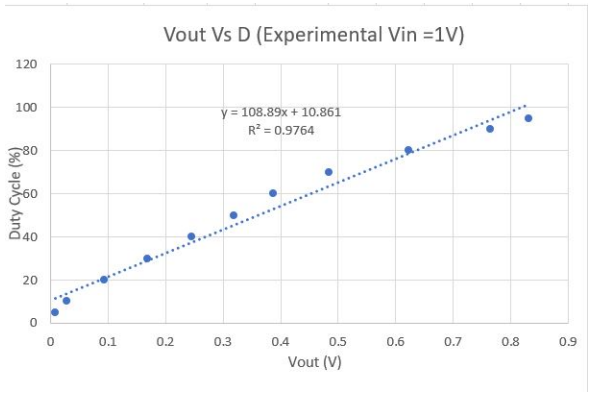


Fig. 44: $V_{out}$ vs Duty Cycle, $V_{in}$=1V

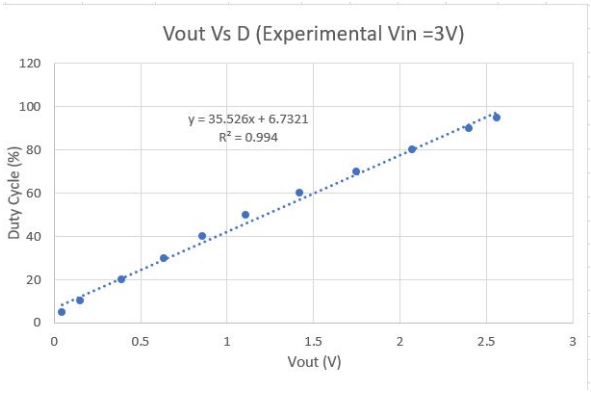


Fig. 45: $V_{out}$ vs Duty Cycle, $V_{in}$=3V

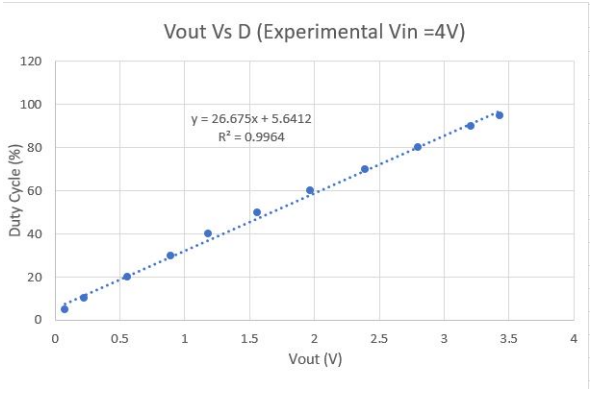


Fig. 46: $V_{out}$ vs Duty Cycle, $V_{in}$=4V

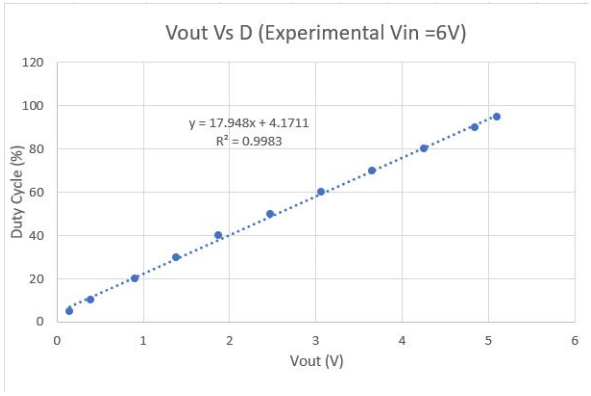


Fig. 47: $V_{out}$ vs Duty Cycle, $V_{in}$=6V

### C. Simulations vs Experimental

| $V_{in}$ = 1V | | | |
|---|---|---|---|
| Duty Cycle (%) | Experimental $V_{out}$ (V) | Simulated $V_{out}$ (V) | Percent Error(%) |
| 5 | 0.008 | 0.003 | 166.67 |
| 10 | 0.029 | 0.033 | 12.12 |
| 20 | 0.093 | 0.123 | 24.39 |
| 30 | 0.169 | 0.216 | 21.76 |
| 40 | 0.245 | 0.293 | 16.38 |
| 50 | 0.319 | 0.377 | 15.38 |
| 60 | 0.387 | 0.482 | 19.71 |
| 70 | 0.485 | 0.672 | 27.83 |
| 80 | 0.623 | 0.873 | 28.64 |
| 90 | 0.764 | 0.994 | 23.14 |
| 95 | 0.832 | 0.995 | 16.38 |

Fig. 48: Percent error between simulated and experimental data, $V_{in}$=1V

| $V_{in}$ = 3V | | | |
|---|---|---|---|
| Duty Cycle (%) | Experimental $V_{out}$ (V) | Simulated $V_{out}$ (V) | Percent Error(%) |
| 5 | 0.049 | 0.006 | 716.67 |
| 10 | 0.15 | 0.105 | 42.86 |
| 20 | 0.392 | 0.396 | 1.01 |
| 30 | 0.637 | 0.662 | 3.78 |
| 40 | 0.859 | 0.939 | 8.52 |
| 50 | 1.11 | 1.35 | 17.78 |
| 60 | 1.42 | 1.72 | 17.44 |
| 70 | 1.75 | 2.14 | 18.22 |
| 80 | 2.07 | 2.53 | 18.18 |
| 90 | 2.4 | 2.98 | 19.46 |
| 95 | 2.56 | 2.98 | 14.09 |

Fig. 49: Percent error between simulated and experimental data, $V_{in}$=3V

| $V_{in}$ = 4V | | | |
|---|---|---|---|
| Duty Cycle (%) | Experimental $V_{out}$ (V) | Simulated $V_{out}$ (V) | Percent Error(%) |
| 5 | 0.077 | 0.006 | 1183.33 |
| 10 | 0.225 | 0.137 | 64.23 |
| 20 | 0.56 | 0.525 | 6.67 |
| 30 | 0.89 | 0.882 | 0.91 |
| 40 | 1.18 | 1.31 | 9.92 |
| 50 | 1.56 | 1.83 | 14.75 |
| 60 | 1.97 | 2.32 | 15.09 |
| 70 | 2.39 | 2.81 | 14.95 |
| 80 | 2.8 | 3.32 | 15.66 |
| 90 | 3.21 | 3.95 | 18.73 |
| 95 | 3.43 | 3.98 | 13.82 |

Fig. 50: Percent error between simulated and experimental data, $V_{in}$=4V

| $V_{in}$ = 6V | | | |
|---|---|---|---|
| Duty Cycle (%) | Experimental $V_{out}$ (V) | Simulated $V_{out}$ (V) | Percent Error(%) |
| 5 | 0.15 | 0.007 | 2042.86 |
| 10 | 0.395 | 0.183 | 115.85 |
| 20 | 0.902 | 0.731 | 23.39 |
| 30 | 1.38 | 1.35 | 2.22 |
| 40 | 1.87 | 2.01 | 6.97 |
| 50 | 2.47 | 2.7 | 8.52 |
| 60 | 3.06 | 3.4 | 10.00 |
| 70 | 3.65 | 4.09 | 10.76 |
| 80 | 4.26 | 4.81 | 11.43 |
| 90 | 4.85 | 5.63 | 13.85 |
| 95 | 5.1 | 5.96 | 14.43 |

Fig. 51: Percent error between simulated and experimental data, $V_{in}$=6V

### D. Netlist

```
* source FINALPROJ
V_V1 N00949 0 7
L_L1 N00989 N01001 500uH
D_D1 0 N00989 Dbreak
R_R1 0 N01001 10 TC=0,0
C_C1 0 N01001 47u TC=0,0
V_V2 N02403 0 15
V_V3 N03654 0
+PULSE 0 3.3 0 .1u .1u PulseWidth .1m
R_R2 N02403 N01700 10k TC=0,0
M_M2 N01700 N03654 0 0 RIT4007N7
M_M3 N00949 N01700 N00989 N00989 IRF540
.PARAM PulseWidth=0.01
```

## REFERENCES


[1] E. Coates, Learnabout electronics, Buck Converters, 03-Sep-2017. [Online]. Available: http://www.learnabout-electronics.org/PSU/psu31.php. [Accessed: 26-Apr-2018].