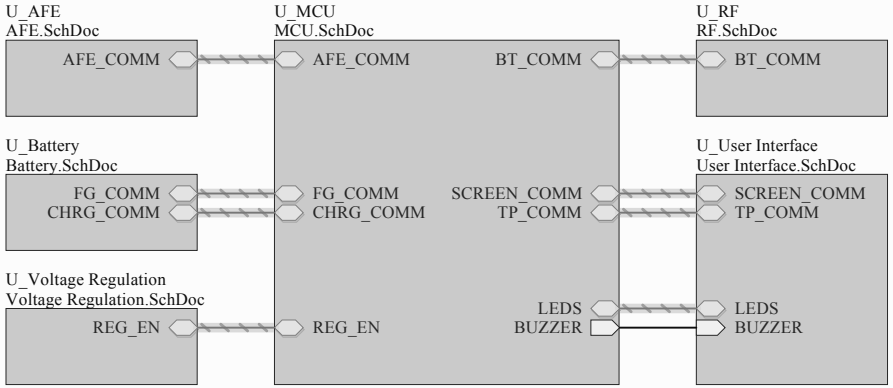
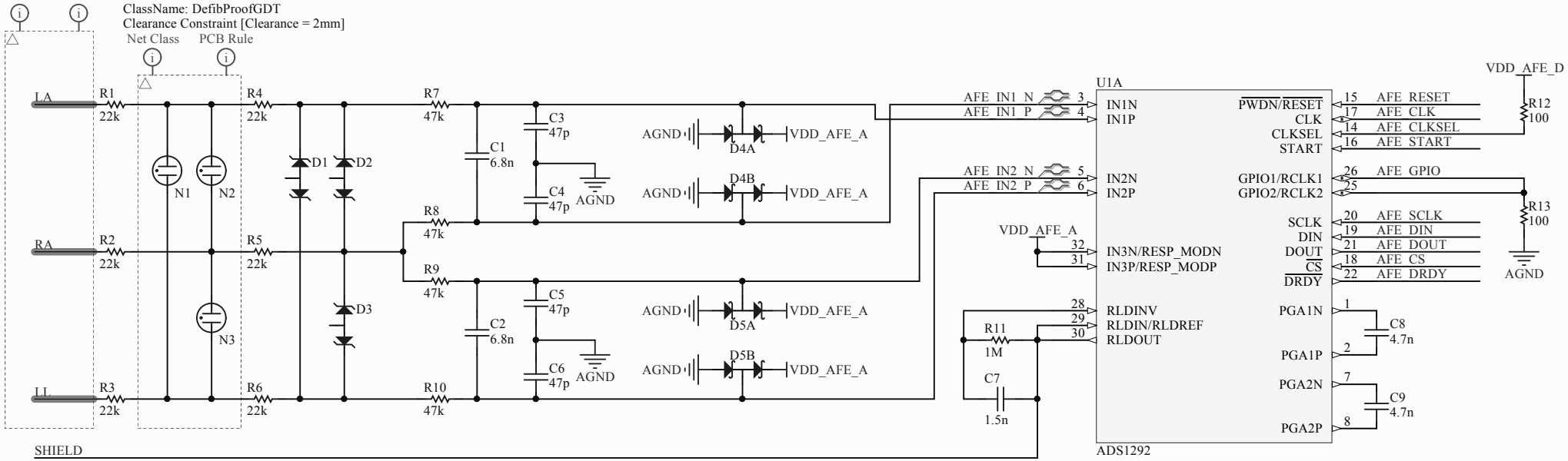


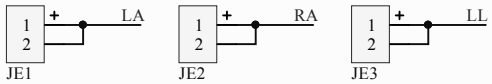
Project: H2H Main Board		Cannot open file C:\Users\Smau\Desktop\IMGs\Eye\Eye.png
Title: Main Board		
Author: Samuel López		
Sheet 1 of 7	Date: 2016/01/06	

ClassName: DefibProof
Clearance Constraint [Clearance = 4mm]
Net Class PCB Rule

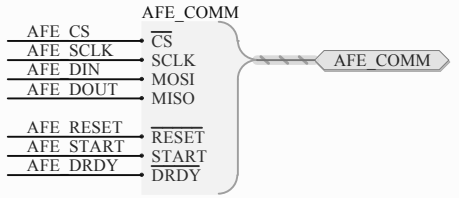
ClassName: DefibProofGDT
Clearance Constraint [Clearance = 2mm]
Net Class PCB Rule



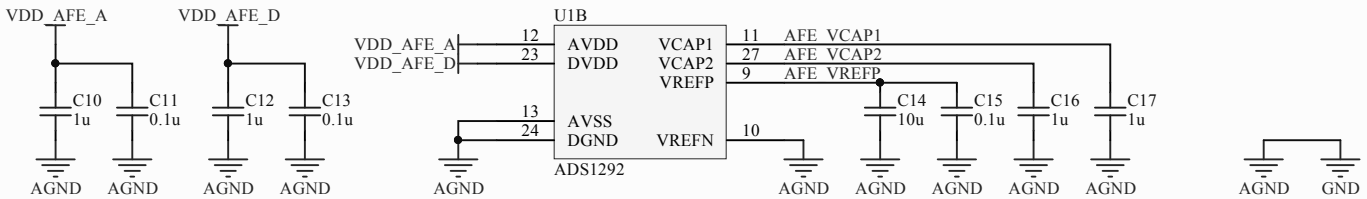
Minimize parasitic capacitance between PGA pins (remove GND plane below caps)



Electrode connectors

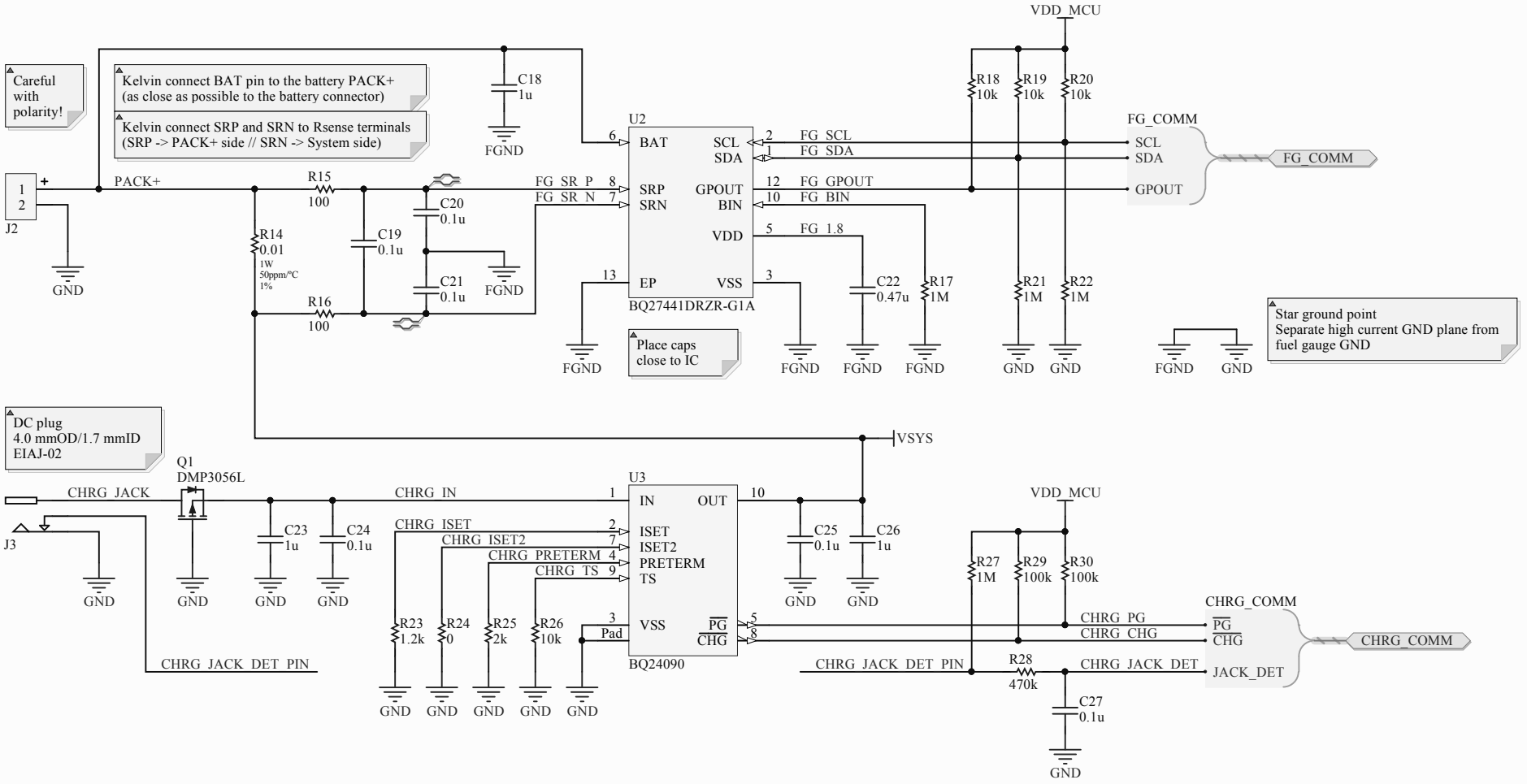


VREFN close to VREFP caps

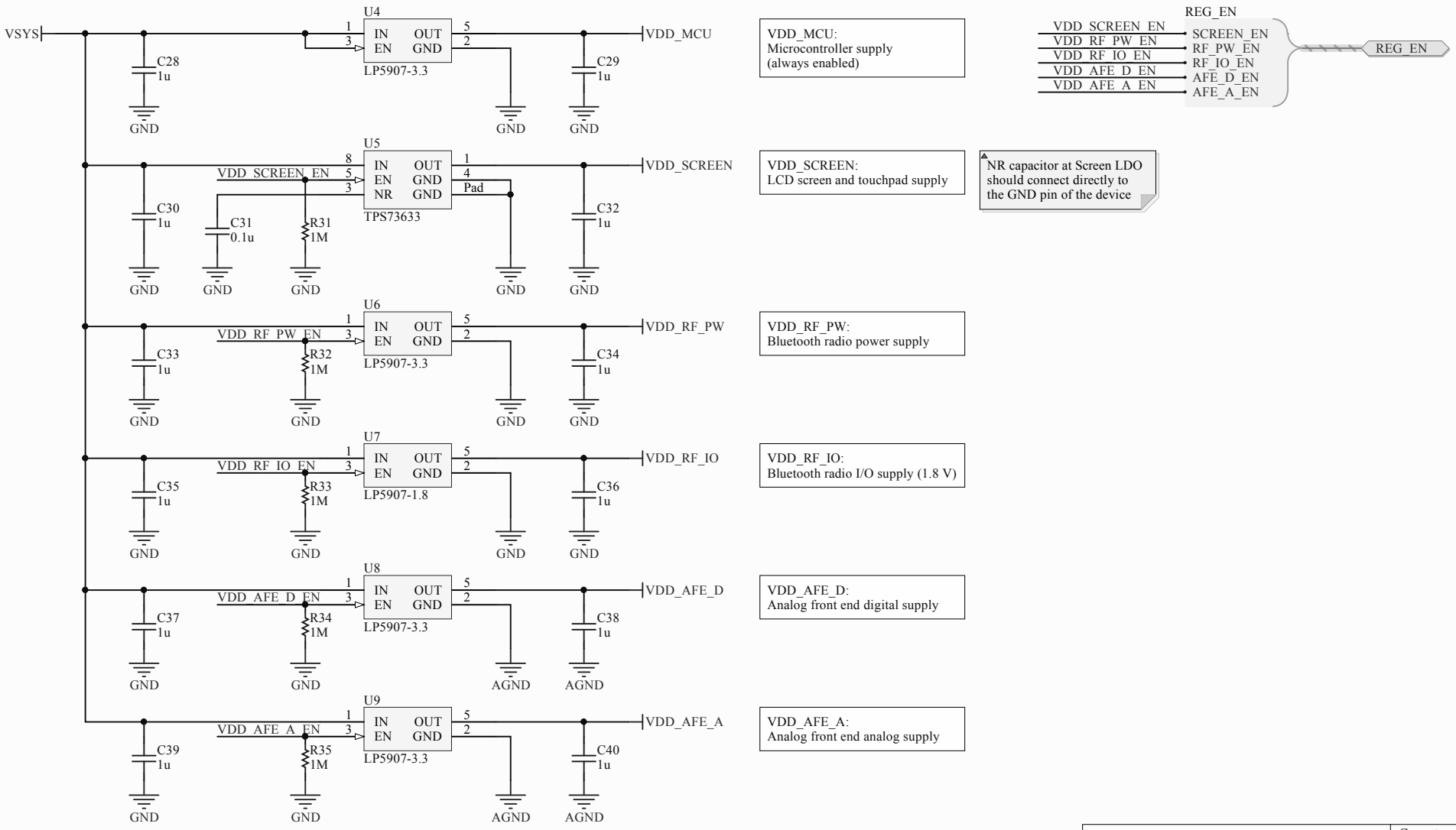


Star ground point
Make connection near AVSS and DGND pins

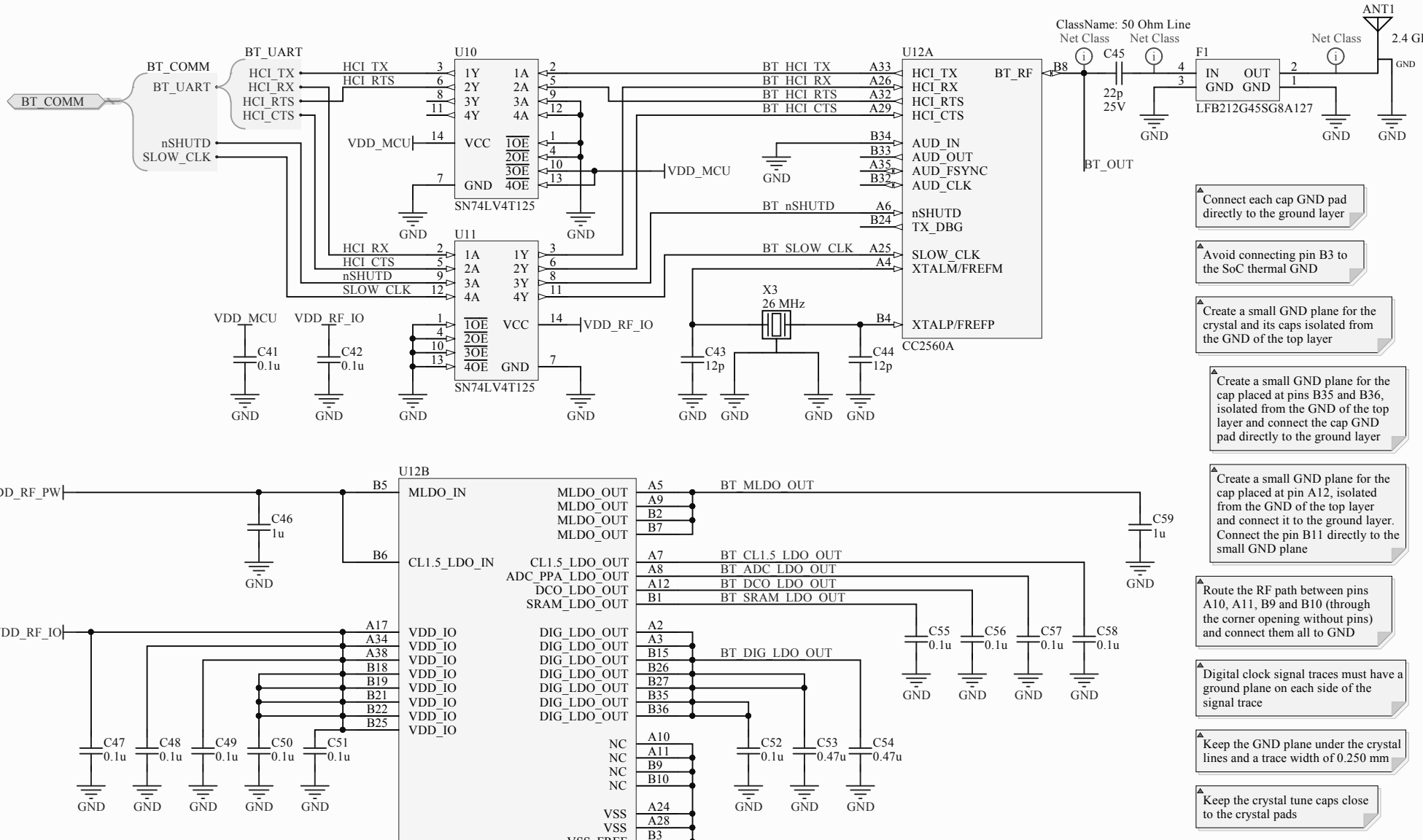
Project: H2H Main Board	Cannot open file C:\Users\Smau\Desktop\IMGs\Eye\Eye.png
Title: Analog Front End	
Author: Samuel López	
Sheet 2 of 7	Date: 2016/01/04



Project: H2H Main Board		Cannot open file C:\Users\Smau\Desktop\IMGs\Eye\Eye.png
Title: Battery		
Author: Samuel López		
Sheet 3 of 7	Date: 2016/01/04	



Project: H2H Main Board	Cannot open file C:\Users\Smau\Desktop\IMGs\Eye\Eye.png
Title: Voltage Regulation	
Author: Samuel López	
Sheet 4 of 7	Date: 2016/01/05


BT_COMM
BT_UART
HCI_TX
HCI_RX
HCI_RTS
HCI_CTS
nSHUTD
SLOW_CLK
U10
SN74LV4T125
U11
SN74LV4T125
VDD_MCU
VDD_RF_IO
C41 0.1u
C42 0.1u
U12A
CC2560A
BT_HCI_TX
BT_HCI_RX
BT_HCI_RTS
BT_HCI_CTS
AUD_IN
AUD_OUT
AUD_FSYNC
AUD_CLK
BT_nSHUTD
TX_DBG
BT_SLOW_CLK
SLOW_CLK
XTALM/FREFM
XTALP/FREFP
BT_RF
BT_OUT
X3
26 MHz
C43 12p
C44 12p
ClassName: 50 Ohm Line
Net Class
C45
22p
25V
F1
LFB212G45SG8A127
ANT1
2.4 GHz F-antenna
GND
U12B
CC2560A
VDD_RF_PW
C46 1u
C59 1u
BT_MLDO_OUT
BT_CL1.5_LDO_OUT
BT_ADC_LDO_OUT
BT_DCO_LDO_OUT
BT_SRAM_LDO_OUT
BT_DIG_LDO_OUT
C47 0.1u
C48 0.1u
C49 0.1u
C50 0.1u
C51 0.1u
C52 0.1u
C53 0.47u
C54 0.47u
C55 0.1u
C56 0.1u
C57 0.1u
C58 0.1u
Connect each cap GND pad directly to the ground layer
Avoid connecting pin B3 to the SoC thermal GND
Create a small GND plane for the crystal and its caps isolated from the GND of the top layer
Create a small GND plane for the cap placed at pins B35 and B36, isolated from the GND of the top layer and connect the cap GND pad directly to the ground layer
Create a small GND plane for the cap placed at pin A12, isolated from the GND of the top layer and connect it to the ground layer. Connect the pin B11 directly to the small GND plane
Route the RF path between pins A10, A11, B9 and B10 (through the corner opening without pins) and connect them all to GND
Digital clock signal traces must have a ground plane on each side of the signal trace
Keep the GND plane under the crystal lines and a trace width of 0.250 mm
Keep the crystal tune caps close to the crystal pads
Project: H2H Main Board
Title: RF
Author: Samuel López
Sheet 5 of 7
Date: 2016/01/05
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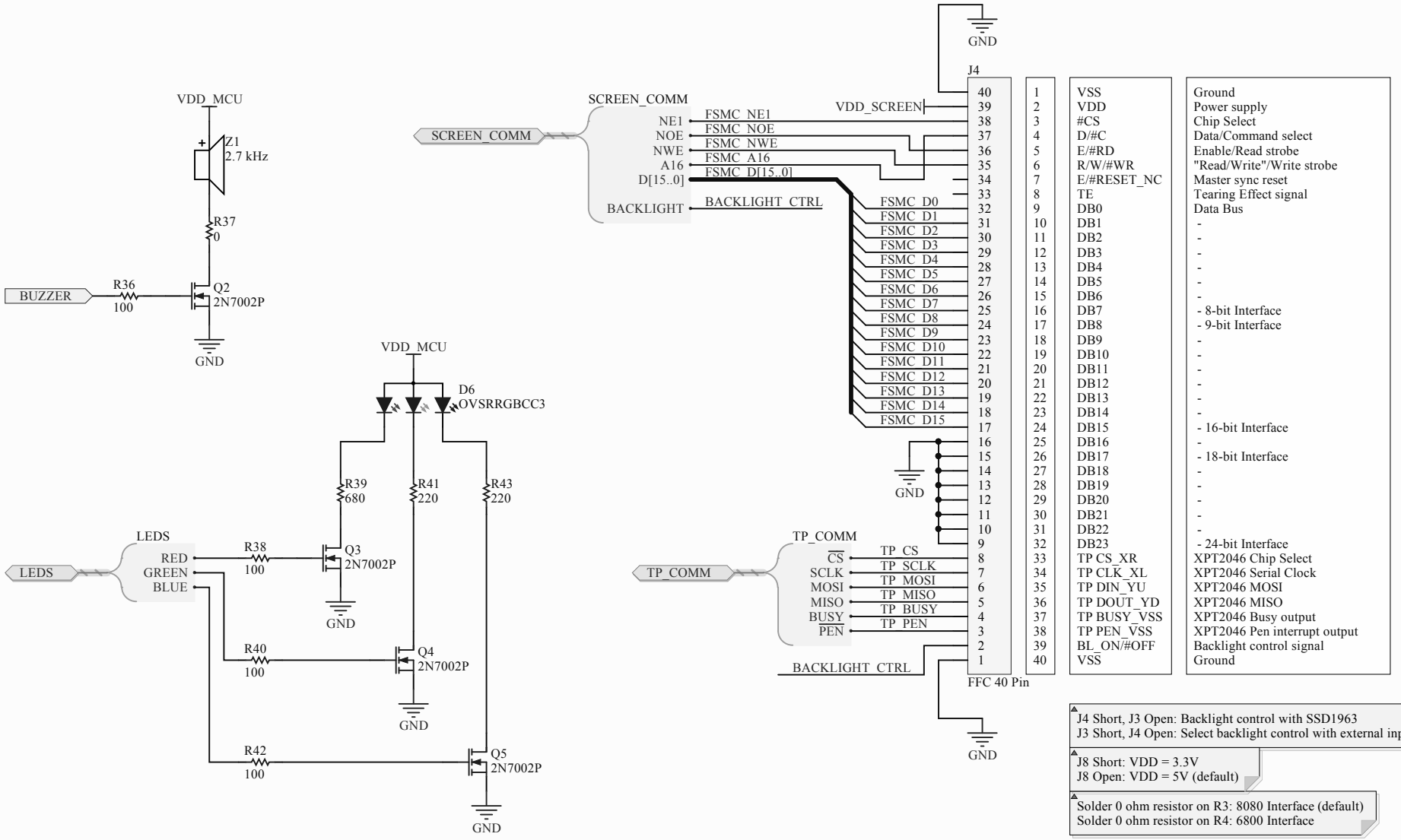
VDD_MCU
Z1
2.7 kHz
R37
0
BUZZER
R36
100
Q2
2N7002P
GND
VDD_MCU
D6
OVSRRGBCC3
R39
680
R41
220
R43
220
LEDS
RED
GREEN
BLUE
LEDS
R38
100
Q3
2N7002P
GND
R40
100
Q4
2N7002P
GND
R42
100
Q5
2N7002P
GND
GND
J4
SCREEN_COMM
NE1
NOE
NWE
A16
D[15..0]
BACKLIGHT
SCREEN_COMM
FSMC_NE1
FSMC_NOE
FSMC_NWE
FSMC_A16
FSMC_D[15..0]
BACKLIGHT_CTRL
VDD_SCREEN
FSMC_D0
FSMC_D1
FSMC_D2
FSMC_D3
FSMC_D4
FSMC_D5
FSMC_D6
FSMC_D7
FSMC_D8
FSMC_D9
FSMC_D10
FSMC_D11
FSMC_D12
FSMC_D13
FSMC_D14
FSMC_D15
GND
TP_COMM
CS
SCLK
MOSI
MISO
BUSY
PEN
TP_COMM
TP_CS
TP_SCLK
TP_MOSI
TP_MISO
TP_BUSY
TP_PEN
BACKLIGHT_CTRL
GND
FFC 40 Pin
40 1 VSS Ground
39 2 VDD Power supply
38 3 #CS Chip Select
37 4 D/#C Data/Command select
36 5 E/#RD Enable/Read strobe
35 6 R/W/#WR "Read/Write"/Write strobe
34 7 E/#RESET_NC Master sync reset
33 8 TE Tearing Effect signal
32 9 DB0 Data Bus
31 10 DB1 -
30 11 DB2 -
29 12 DB3 -
28 13 DB4 -
27 14 DB5 -
26 15 DB6 -
25 16 DB7 - 8-bit Interface
24 17 DB8 - 9-bit Interface
23 18 DB9 -
22 19 DB10 -
21 20 DB11 -
20 21 DB12 -
19 22 DB13 -
18 23 DB14 -
17 24 DB15 - 16-bit Interface
16 25 DB16 -
15 26 DB17 - 18-bit Interface
14 27 DB18 -
13 28 DB19 -
12 29 DB20 -
11 30 DB21 -
10 31 DB22 -
9 32 DB23 - 24-bit Interface
8 33 TP CS_XR XPT2046 Chip Select
7 34 TP CLK_XL XPT2046 Serial Clock
6 35 TP DIN_YU XPT2046 MOSI
5 36 TP DOUT_YD XPT2046 MISO
4 37 TP BUSY_VSS XPT2046 Busy output
3 38 TP PEN_VSS XPT2046 Pen interrupt output
2 39 BL_ON/#OFF Backlight control signal
1 40 VSS Ground
J4 Short, J3 Open: Backlight control with SSD1963
J3 Short, J4 Open: Select backlight control with external input (default)
J8 Short: VDD = 3.3V
J8 Open: VDD = 5V (default)
Solder 0 ohm resistor on R3: 8080 Interface (default)
Solder 0 ohm resistor on R4: 6800 Interface
Project: H2H Main Board
Title: User Interface
Author: Samuel López
Sheet 6 of 7
Date: 2016/01/05
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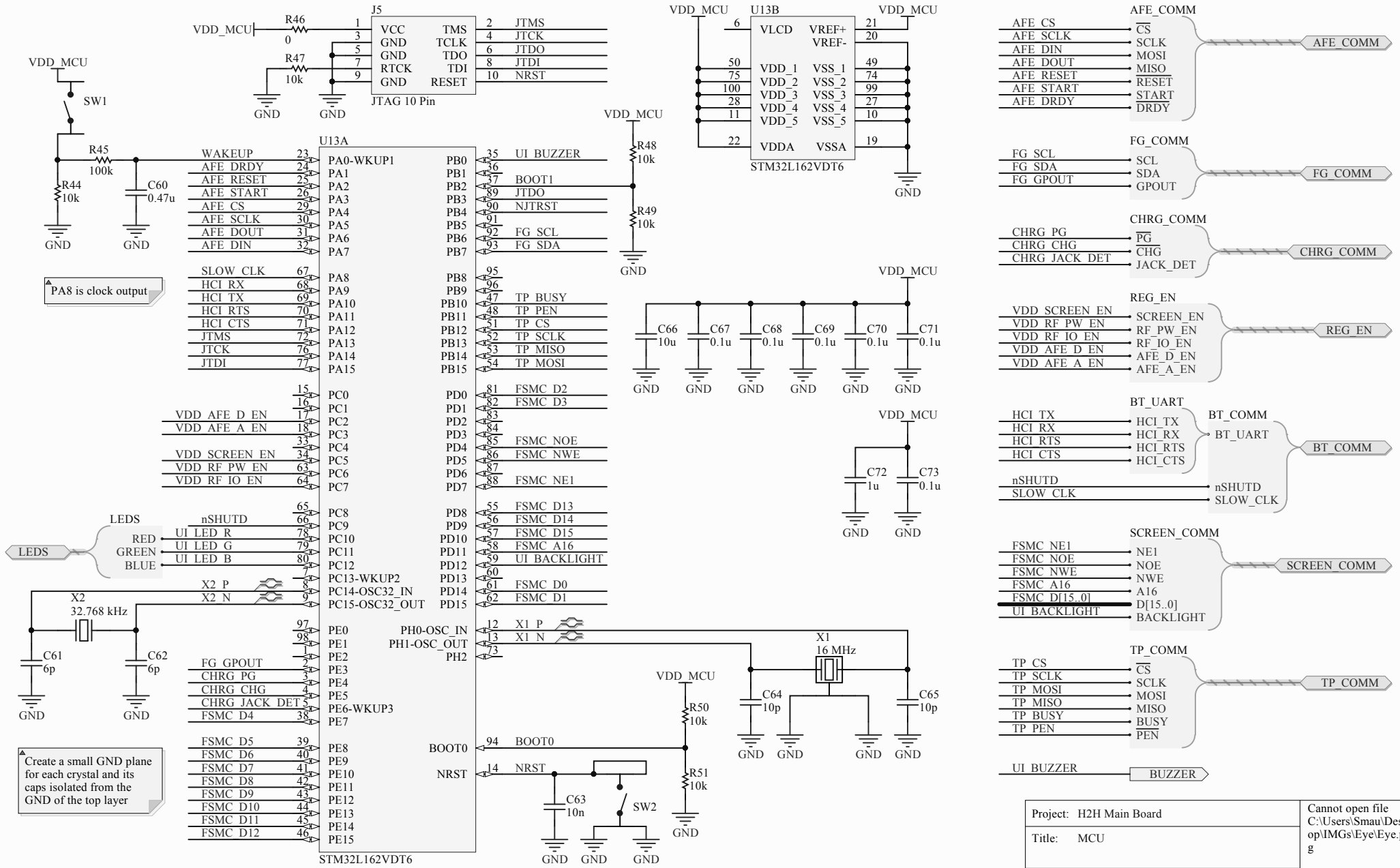
J5
JTAG 10 Pin
U13A
STM32L162VDT6
U13B
STM32L162VDT6
PA8 is clock output
Create a small GND plane for each crystal and its caps isolated from the GND of the top layer
AFE_COMM
FG_COMM
CHRG_COMM
REG_EN
BT_UART
BT_COMM
SCREEN_COMM
TP_COMM
BUZZER
Project: H2H Main Board
Title: MCU
Author: Samuel López
Sheet 7 of 7
Date: 2016/01/06
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