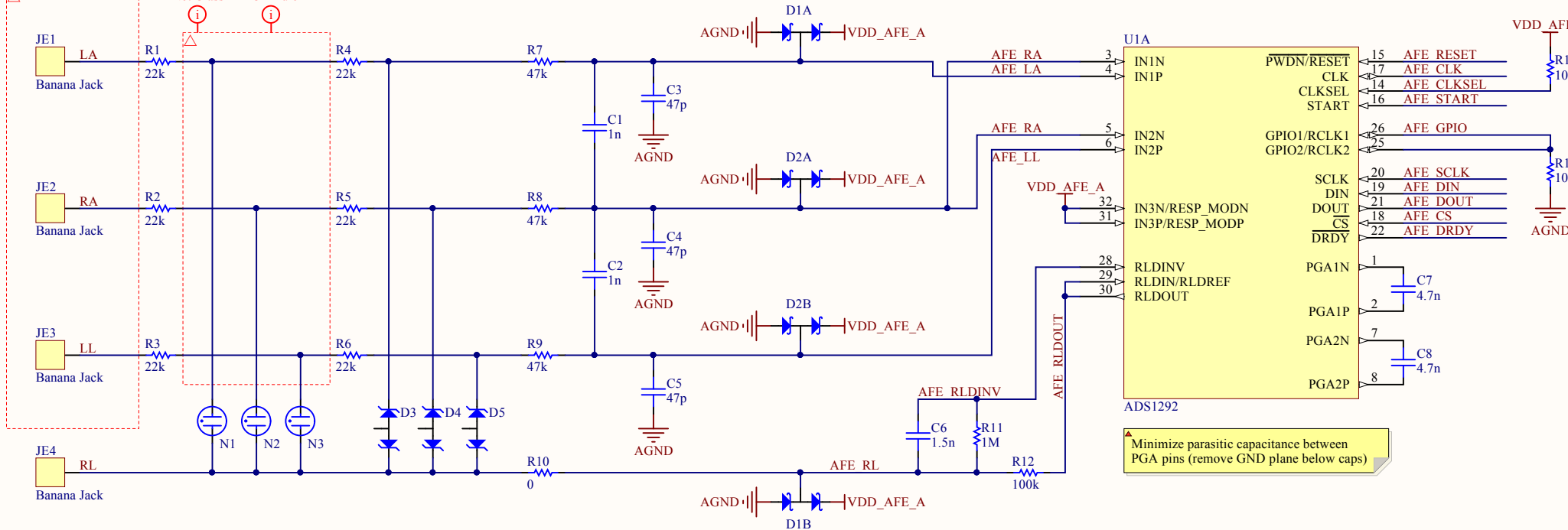


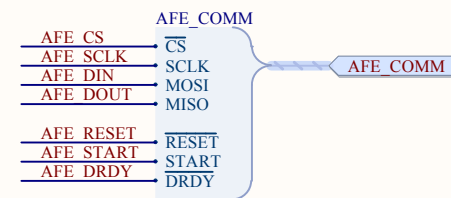
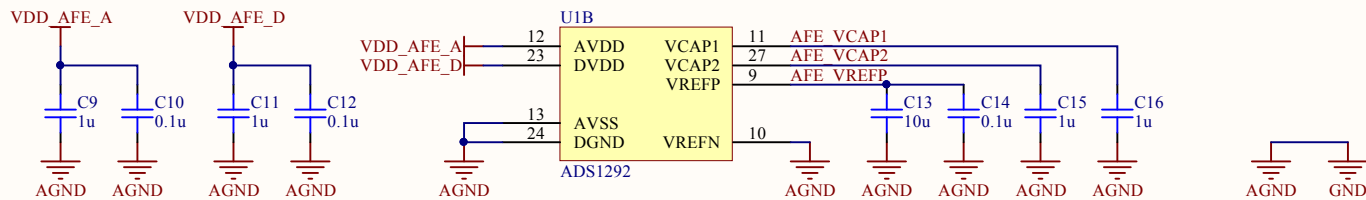
ClassName: DefibProof
Clearance Constraint [Clearance = 4mm]
Net Class PCB Rule

ClassName: DefibProofGDT
Clearance Constraint [Clearance = 2mm]
Net Class PCB Rule

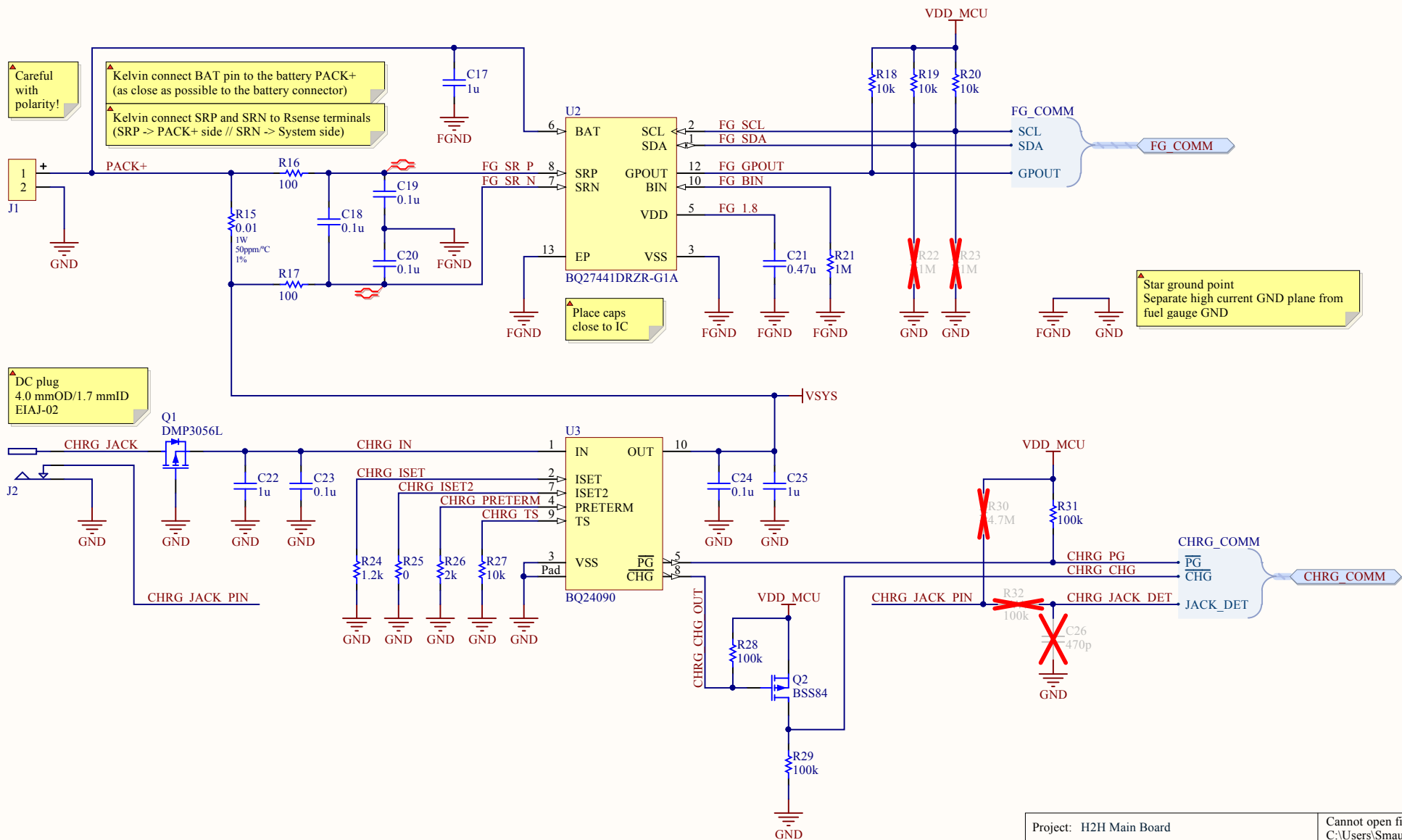


Electrode connectors

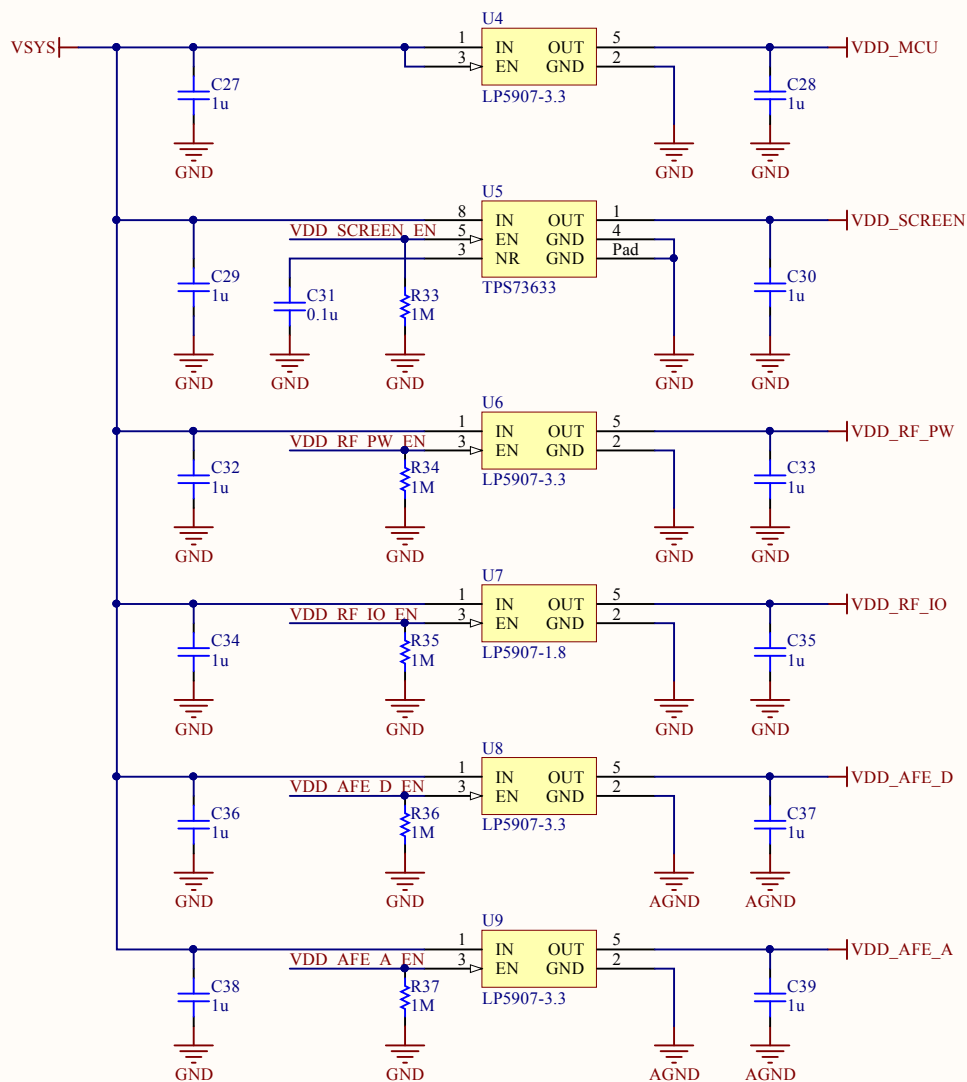
VREFN close to VREFP caps



Project: H2H Main Board	Cannot open file C:\Users\Smau\Desktop\op\IMGs\Eye\Eye.png
Title: Analog Front End	
Author: Samuel López	
Sheet 2 of 7	
Date: 2016/01/04	



Project: H2H Main Board		Cannot open file C:\Users\Smau\Desktop\op\IMGs\Eye\Eye.png
Title: Battery		
Author: Samuel López		
Sheet 3 of 7	Date: 2016/01/04	



VDD_MCU:
Microcontroller supply
(always enabled)

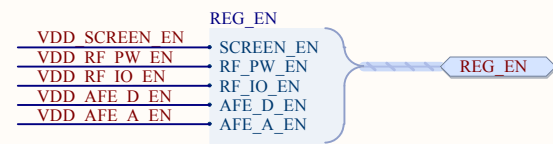
VDD_SCREEN:
LCD screen and touchpad supply

VDD_RF_PW:
Bluetooth radio power supply

VDD_RF_IO:
Bluetooth radio I/O supply (1.8 V)

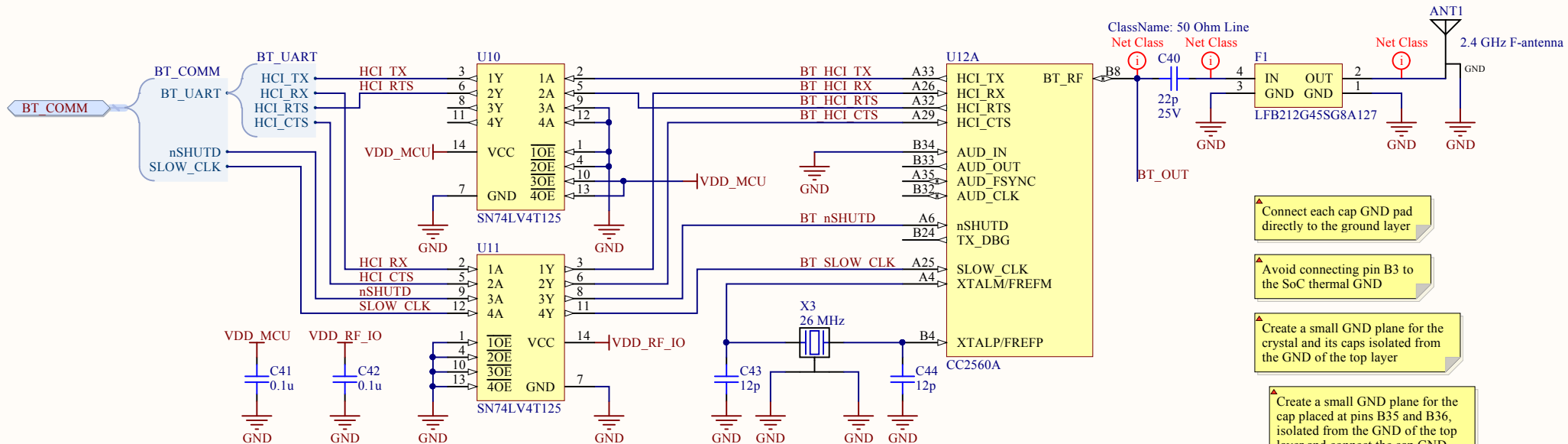
VDD_AFE_D:
Analog front end digital supply

VDD_AFE_A:
Analog front end analog supply



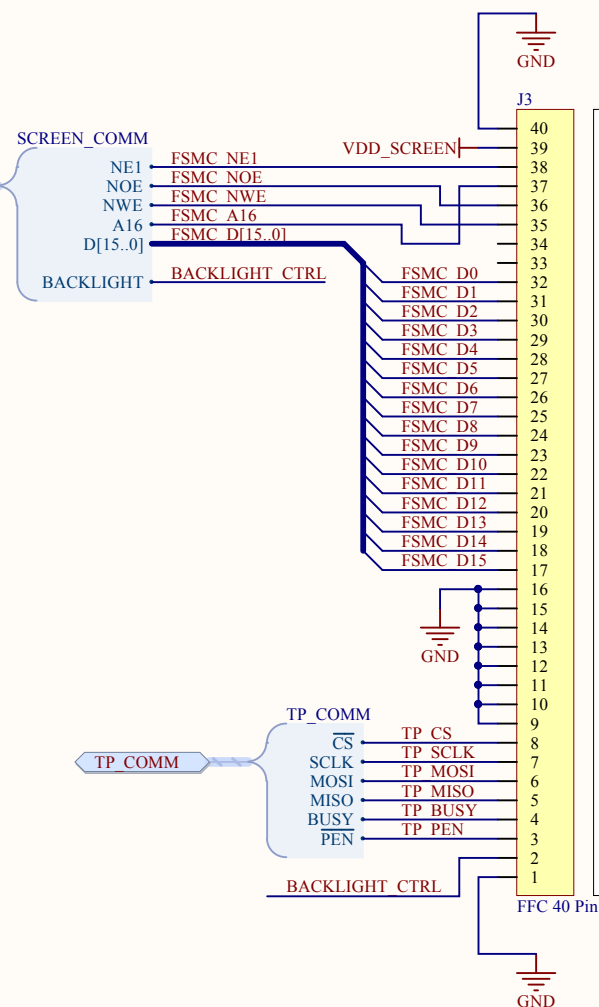
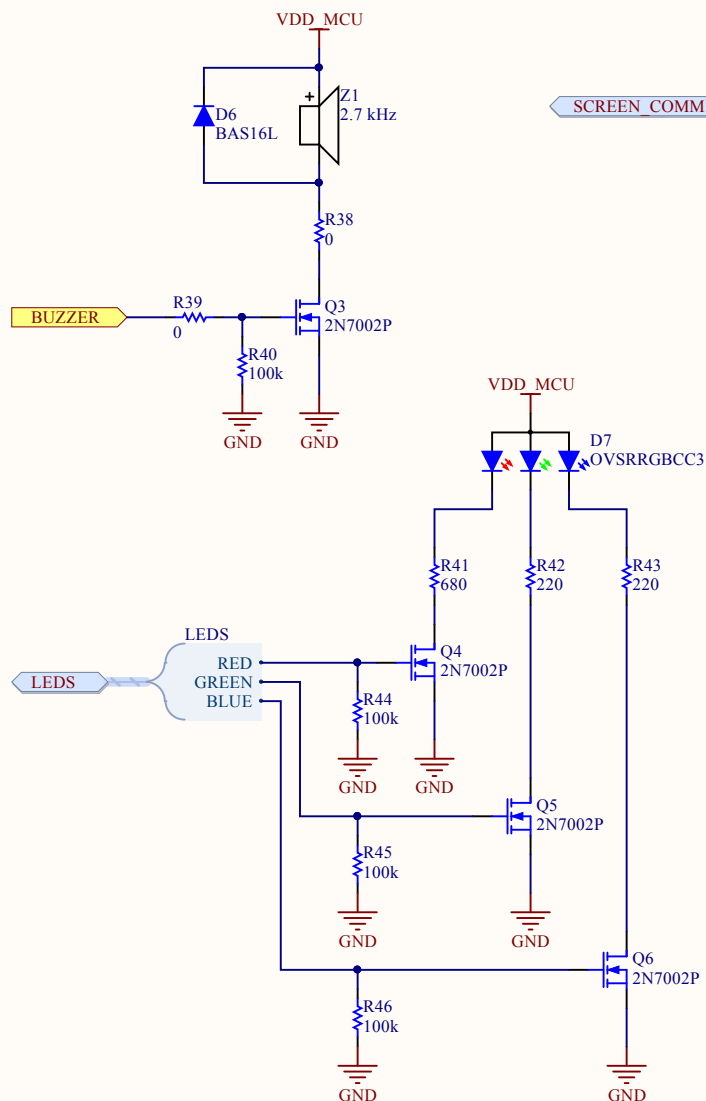
▲ NR capacitor at Screen LDO should connect directly to the GND pin of the device

Project: H2H Main Board	Cannot open file C:\Users\Smau\Desktop\IMGs\Eye\Eye.png
Title: Voltage Regulation	
Author: Samuel López	
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Date: 2016/01/05	



- Connect each cap GND pad directly to the ground layer
- Avoid connecting pin B3 to the SoC thermal GND
- Create a small GND plane for the crystal and its caps isolated from the GND of the top layer
- Create a small GND plane for the cap placed at pins B35 and B36, isolated from the GND of the top layer and connect the cap GND pad directly to the ground layer
- Create a small GND plane for the cap placed at pin A12, isolated from the GND of the top layer and connect it to the ground layer. Connect the pin B11 directly to the small GND plane
- Route the RF path between pins A10, A11, B9 and B10 (through the corner opening without pins) and connect them all to GND
- Digital clock signal traces must have a ground plane on each side of the signal trace
- Keep the GND plane under the crystal lines and a trace width of 0.250 mm
- Keep the crystal tune caps close to the crystal pads

Project: H2H Main Board		Cannot open file C:\Users\Smau\Desktop\op\IMGs\Eye\Eye.png
Title: RF		
Author: Samuel López		
Sheet 5 of 7	Date: 2016/01/05	



1	VSS	Ground
2	VDD	Power supply
3	#CS	Chip Select
4	D/#C	Data/Command select
5	E/#RD	Enable/Read strobe
6	R/W/#WR	"Read/Write"/Write strobe
7	E/#RESET_NC	Master sync reset
8	TE	Tearing Effect signal
9	DB0	Data Bus
10	DB1	-
11	DB2	-
12	DB3	-
13	DB4	-
14	DB5	-
15	DB6	-
16	DB7	- 8-bit Interface
17	DB8	- 9-bit Interface
18	DB9	-
19	DB10	-
20	DB11	-
21	DB12	-
22	DB13	-
23	DB14	-
24	DB15	- 16-bit Interface
25	DB16	-
26	DB17	- 18-bit Interface
27	DB18	-
28	DB19	-
29	DB20	-
30	DB21	-
31	DB22	-
32	DB23	- 24-bit Interface
33	TP CS_XR	XPT2046 Chip Select
34	TP CLK_XL	XPT2046 Serial Clock
35	TP DIN_YU	XPT2046 MOSI
36	TP DOU_T_YD	XPT2046 MISO
37	TP BUSY_VSS	XPT2046 Busy output
38	TP PEN_VSS	XPT2046 Pen interrupt output
39	BL_ON/#OFF	Backlight control signal
40	VSS	Ground

▲ J4 Short, J3 Open: Backlight control with SSD1963
J3 Short, J4 Open: Select backlight control with external input (default)

▲ J8 Short: VDD = 3.3V
J8 Open: VDD = 5V (default)

▲ Solder 0 ohm resistor on R3: 8080 Interface (default)
Solder 0 ohm resistor on R4: 6800 Interface

Project: H2H Main Board	Cannot open file C:\Users\Smau\Desktop\op\IMGs\Eye\Eye.png
Title: User Interface	
Author: Samuel López	
Sheet 6 of 7	Date: 2016/01/05

