FAIRCHILD SEMICONDUCTOR®

September 2010

# FCM8201
# 3-Phase Sinusoidal Brushless DC Motor Controller

## Features

- Supports Space Vector Modulation (SVM)
- Supports Sine-Wave & Square-Wave Solutions
- Built-in Clock Generator
- Built-in Error Amplifier for Torque Loop Control
- Direct Duty Control
- Square-Wave 120°, Sine-Wave 180° Turn-on
- PLL Angle Detection (Hall Sensors)
- Programmable Current Leading Phase
- Serial Interface (SPI)
- Two Operation Modes (Stand-Alone Operation or Controlled through SPI)
- Programmable Soft-Switching (Dead-Time)
- Synchronous Rectifying
- Over-Voltage and Under-Voltage Protections
- Motor & Power Transistor Over-Voltage Protections
- Three Levels of Over-Current Protection (OCP)
- Programmable OC Timer
- Over-Temperature Protection (OTP)

## Applications

- BLDC Motor Control
- Low-Noise Motor Applications
- Fan, Pump, Tools, etc.

## Description

FCM8201 is a three-phase sinusoidal brushless DC (BLDC) motor controller. It comes with the advanced Hall sensor design. Using the Hall sensor signals, the control system is able to execute the PWM commutation by switching the three-phase inverter. There are two PWM modes for selection: Sine-Wave Mode and the Square-Wave Mode. Square-Wave Mode includes PWM-PWM and PWM-ON approaches to improve the efficiency of the motor drive. Protection functions including over-voltage, over-current, over-temperature, and short circuit prevent the control circuits and the motor from being damaged, particularly under stressed applications and demanding environments. Information about voltage, current, and temperature is accessible through the SPI interface.

FCM8201 can be operated stand-alone or worked with microcontrollers for advanced BLDC motor control.

## Ordering Information

| Part Number | Operating Temperature Range | Package | Packing Method |
|---|---|---|---|
| FCM8201QY | -40°c to 85°C | 32-Leadless Quad Flat Pack Package (LQFP) , JEDEC MS-026, Variation BCE, 7mm Square | Tray |

## Typical Application Circuits

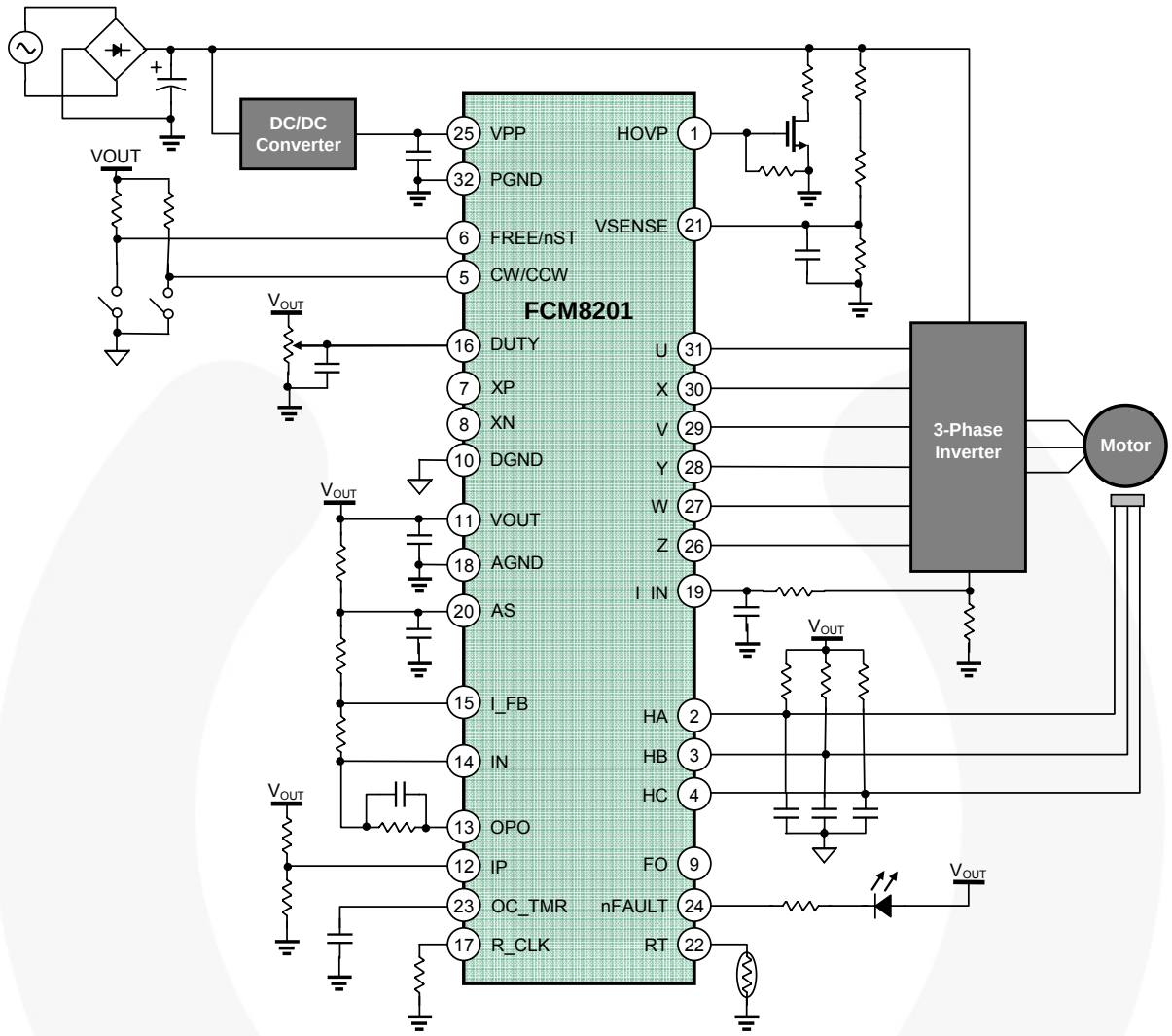



**Figure 1. Stand-Alone Application**

## Typical Application Circuits (Continued)

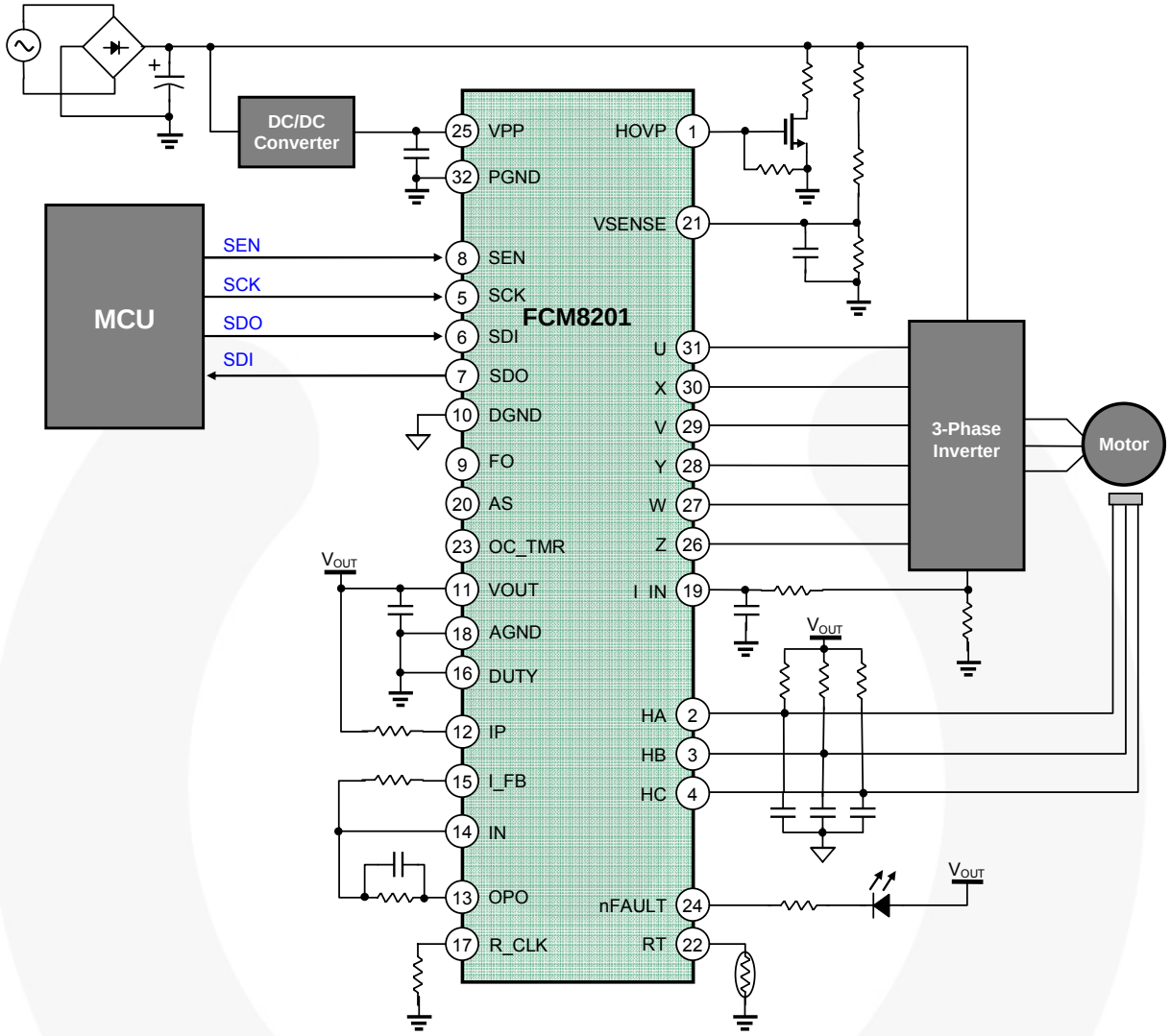



**Figure 2. SPI Application**

## Block Diagram

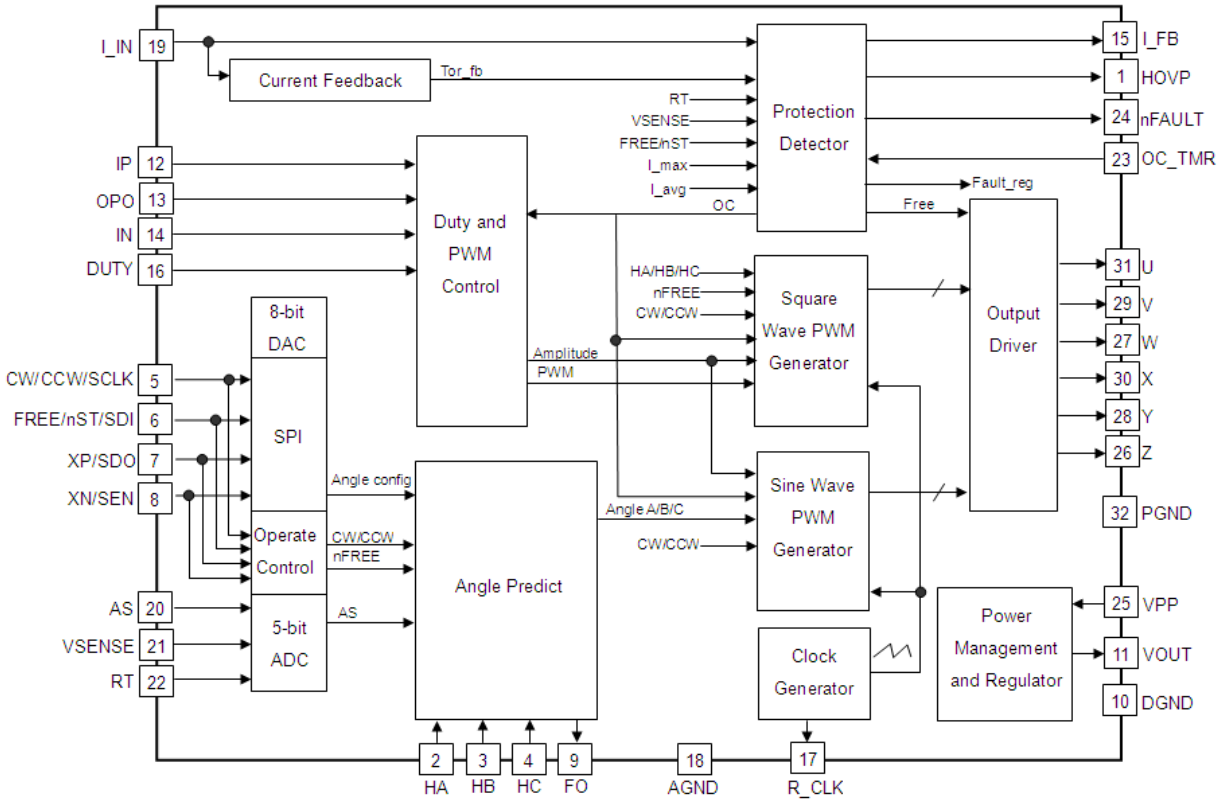
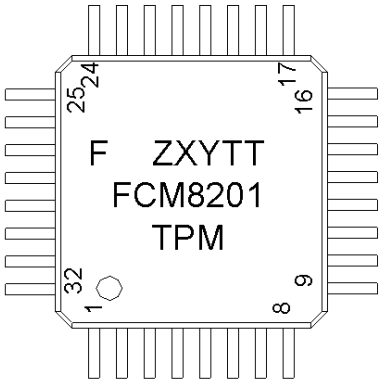



**Figure 3. System Block Diagram**

## Marking Information




*F*- Fairchild Logo
Z- Plant Code
X- 1-Digit Year Code
Y- 1-Digit Week Code
TT: 2-Digit Die Run Code
T: Package Type (Q=LQFP)
P: Y=Green Package
M: Die Run Code

**Figure 4. Top Mark**

## Pin Configuration

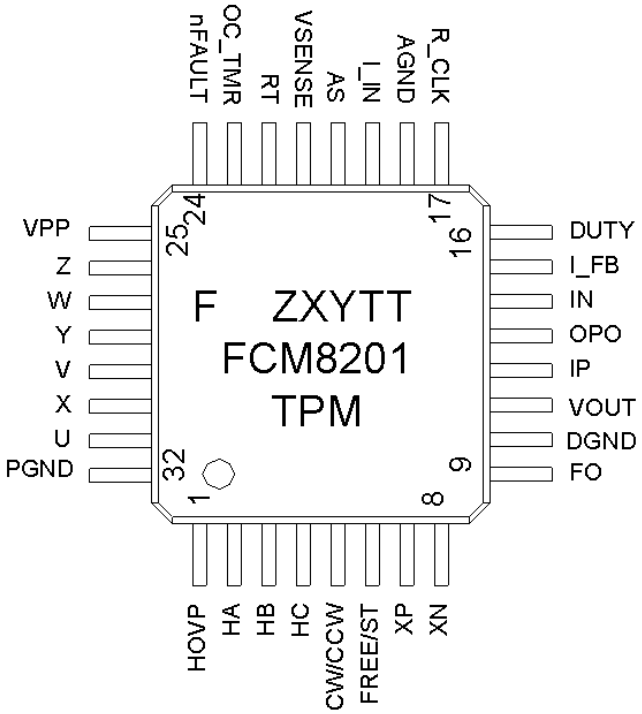



**Figure 5. Pin Configuration**

## Pin Definitions

| Pin # | Name | Description |
|---|---|---|
| 1 | HOVP | **Motor Drive Over-Voltage Protection Output**. It can be connected to an external power transistor for discharging the back EMF. |
| 2 | HA | **Hall A Sensor Input**. Phase-U magnetic field detection. |
| 3 | HB | **Hall B Sensor Input**. Phase-V magnetic field detection. |
| 4 | HC | **Hall C Sensor Input**. Phase-W magnetic field detection. |
| 5 | CW/CCW | **Direction Control Input**. Designed for stand-alone operation. HIGH: CW, LOW: CCW. |
| | SCLK | **Serial Clock Input**. Designed for SPI operation. |
| 6 | FREE/ST | **Free and Start Control Input**. Designed for stand-alone operation. HIGH: Free, LOW: Start. |
| | SDI | **Serial Data Input.** Designed for SPI operation. |
| 7 | XP | **Interface Selection P (Open-Drain)**. Designed to configure the pin #5~8 work on stand-alone or SPI operation. |
| | SDO | **Serial Data Output, (Open-Drain)**. Designed for SPI operation. |
| 8 | XN | **Interface Selection N (Open-Drain)**. Designed to configure the pin #5~8 work on stand-alone or SPI operation. |
| | SEN | **SPI Enable (Open-Drain)**. Designed for SPI operation. HIGH: SPI disable, LOW: SPI enable. |

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## Pin Definitions (Continued)

| Pin # | Name | Description |
|---|---|---|
| 9 | FO | **Revolution Pulse Output**. Pulses per revolution=motor poles ÷ 2 × 3. |
| 10 | DGND | **Digital Ground** |
| 11 | VOUT | **Voltage Regulator Output**. A 0.1μF (minimum) capacitor should be connected between this pin and ground. |
| 12 | IP | **Positive Input of Torque Error Amplifier** |
| 13 | OPO | **Output of Torque Error Amplifier** |
| 14 | IN | **Negative Input of Torque Error Amplifier** |
| 15 | I_FB | **Current Feedback Output** |
| 16 | DUTY | **PWM Duty Control Input.** Designed to directly control the PWM duty cycle in stand-alone operation. |
| 17 | R_CLK | **External Resistor of Clock Generator**. Designed for determining the frequency of the internal clock generator. |
| 18 | AGND | **Analog Ground** |
| 19 | I_IN | **Current Feedback Input** |
| 20 | AS | **Angle Shift Input**. Designed for correcting the lead angle of PWM output signals. The range is from 0° to 60° related to the induced magnetic voltage. |
| 21 | VSENSE | **Motor Drive Voltage-Sensing Resistor**. Designed for determining the voltage level of over-voltage protections. |
| 22 | RT | **Thermistor Voltage Input**. Connect to a NTC (Negative Temperature Coefficient) thermistor for the over-temperature protection. |
| 23 | OC_TMR | **Overload Time-Out Programmable Input**. Connect to a capacitor for determining the time delay of overload protection. |
| 24 | nFAULT | **Fault Flag**. Open-drain output, LOW: system failure. |
| 25 | VPP | **Supply Voltage Input** |
| 26 | Z | **PWM Output of W-Phase Low Side** |
| 27 | W | **PWM Output of W-Phase High Side** |
| 28 | Y | **PWM Output of V-Phase Low Side** |
| 29 | V | **PWM Output of V-Phase High Side** |
| 30 | X | **PWM Output of U-Phase Low Side** |
| 31 | U | **PWM Output of U-Phase High Side** |
| 32 | PGND | **High-Voltage Ground** |

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{VPP}$ | Supply Voltage | 0 | 30 | V |
| ESD | Human Body Model, JESD22-A114 | | 3.00 | kV |
| | Charged Device Model, JESD22-C101 | | 1.25 | |

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $T_A$ | Operating Ambient Temperature | | -40 | | +85 | °C |
| $V_{PP}$ | Supply Voltage | | 10.0 | 12.0 | 17.5 | V |
| $f_{SYS}$ | System Clock | | 0.96 | 1.28 | 1.92 | MHz |
| R_CLK | Clock Generator External Resistor | | | 12 | | kΩ |
| $R_{I\_IN}$ | I_IN Bias Resistor | | | 10 | | kΩ |

## Electrical Characteristics

$V_{PP}$=12V and $T_A$=25°C unless otherwise noted.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| **$V_{PP}$ Section** | | | | | | |
| $V_{VPP\_ON}$ | Turn-On Threshold Voltage | | 8.5 | 9.0 | 9.5 | V |
| $V_{VPP\_OFF}$ | Turn-Off Threshold Voltage | | 7.5 | 8.0 | 8.5 | V |
| $I_{DD\_OP}$ | Operating Supply Current | $V_{PP}$=12V, $f_{SYS}$=1.28MHz | 4.0 | 5.0 | 6.5 | mA |
| **Voltage Regulator Section** | | | | | | |
| $V_{VOUT}$ | Regulator Output Voltage | Output Current 5mA | 4.9 | 5.2 | 5.5 | V |
| $I_{VOUT}$ | Regulator Output Current | $V_{VOUT}$=5.2V | | | 10 | mA |
| $C_{VOUT}$ | Regulator External Capacitor | | 0.1 | | | µF |
| **Digital I/O Section** | | | | | | |
| $V_{IH\_HALL}$ | Hall Signals Input High Level | | 4.0 | | | V |
| $V_{IL\_HALL}$ | Hall Signals Input Low Level | | | | 1.0 | V |
| $V_{HYS\_HALL}$ | Hall Signals Hysteresis Voltage | | 2.0 | 2.5 | 3.0 | V |
| $T_{DEB\_HALL}$ | Hall Signals Debounce Time | | | 5 | | µs |
| $V_{IH\_SPI}$ | SPI Signals Input High Level | | 2.5 | | 5.3 | V |
| $V_{IL\_SPI}$ | SPI Signals Input Low Level | | -0.3 | | 1.0 | V |
| $V_{OH\_SPI}$ | SPI Signals Output High Level | $I_O$=4mA | 4 | | | V |
| $V_{OL\_SPI}$ | SPI Signals Output Low Level | $I_O$=4mA | | | 1 | V |
| $R_{DIO\_UP}$ | Digital I/O Internal Pull High Resistor | | 150 | 200 | 250 | kΩ |
| **High-Voltage I/O Section** | | | | | | |
| $V_{OH\_PWM}$ | PWM Signals Output High Level (U/V/W/X/Y/Z) | $V_{PP}$=12V, $I_O$=4mA | 10 | | | V |
| $V_{OL\_PWM}$ | PWM Signals Output Low Level (U/V/W/X/Y/Z) | $V_{PP}$=12V, $I_O$=4mA | | | 1 | V |
| $V_{OH\_HOVP}$ | HOVP Output High Level | $V_{PP}$=12V, $I_O$=1mA | 10 | | | V |
| $V_{OL\_HOVP}$ | HOVP Output Low Level | $V_{PP}$=12V, $I_O$=1mA | | | 1 | V |
| **PWM Control Section** | | | | | | |
| $V_{fd}$ | Full Duty Voltage of DUTY Pin | | 4.1 | 4.5 | 4.6 | V |
| $V_{zd}$ | Zero Duty Voltage of DUTY Pin | | | 0.7 | | V |
| $t_{PWM\_MIN}$ | PWM Minimum On Time | R_CLK=12KΩ | | 1 | | µs |
| $t_{DEAD0}$ | PWM Dead Time 0 | DT[1:0] / PWM_REG=00 (Default Value) | 2.0 | 2.5 | 3.0 | µs |
| $t_{DEAD1}$ | PWM Dead Time 1 | DT[1:0] / PWM_REG=01 | 1.5 | 2.0 | 2.5 | µs |
| $t_{DEAD2}$ | PWM Dead Time 2 | DT[1:0] / PWM_REG=10 | 3.5 | 4.0 | 4.5 | µs |
| $t_{DEAD3}$ | PWM Dead Time 3 | DT[1:0] / PWM_REG=11 | 3.0 | 3.5 | 4.0 | µs |
| $REG_{zd}$ | Zero Duty Value of DUTY_REG and IP_REG | | 0x00 | | 0x07 | |
| $f_{PWM\_20K}$ | PWM Frequency 20KHz | R_CLK=12KΩ | 18.5 | 20.0 | 21.5 | KHz |
| $I_{SOURCE\_OPO}$ | Current Source Capability of OPO Pin | IP=5V, IN=0V, OPO=0V | 4.5 | 5.0 | 5.5 | mA |
| $I_{SINK\_OPO}$ | Current Sink Capability of OPO Pin | IP=0V, IN=5V, OPO=5V | -4.5 | -5.0 | -5.5 | mA |
| $Av_{ERR}$ | Gain of Torque Error Amplifier | | | 60 | | dB |
| $GBW_{ERR}$ | Unit-Gain Bandwidth of Torque Error Amplifier | | | 10 | | MHz |

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## Electrical Characteristics (Continued)

$V_{PP}$=12V and $T_A$=25°C unless otherwise noted.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| **Sine Wave PWM Generator** | | | | | | |
| $V_{SIN\_ENA}$ | Sine Wave Enable Threshold of DUTY Pin | | | 0.75 | | V |
| $V_{SIN\_DIS}$ | Sine Wave Disable Threshold of DUTY Pin | | | 0.65 | | V |
| $t_{SIN\_ENA}$ | Sine Wave Enable Debounce Time | | | 1 | | ms |
| $t_{SIN\_DIS}$ | Sine Wave Disable Debounce Time | | | 100 | | ms |
| **Over-Current Protections Section** | | | | | | |
| $V_{OCP\_SH}$ | Short-Circuit Current Protection Threshold Voltage | | | 2.5 | | V |
| $V_{OCP\_CYC}$ | Cycle-by-Cycle Current Protection Threshold Voltage | | | 1.5 | | V |
| $V_{OCP\_OL}$ | Overload Current Protection Threshold Voltage | | | 1.4 | | V |
| $V_{OC\_TMR}$ | OC_TMR Threshold Voltage | | | 2.5 | | V |
| $I_{TMR\_CHG}$ | OC_TMR Charge Current | OC_TMR=0V | 30 | 40 | 50 | µA |
| $I_{TMR\_DIS}$ | OC_TMR Discharge Current | OC_TMR=5V | 5 | 10 | 15 | µA |
| $I_{BIAS\_I\_IN}$ | Bias Current of I_IN | $R_{I\_IN}$=10kΩ | 40 | 50 | 60 | µA |
| $I_{O\_I\_FB}$ | I_FB Output Current | | | 0.5 | | mA |
| $G_{I\_FB}$ | I_FB Output Gain | | | 8 | | |
| **Over/Under-Voltage Protections (OVP/UVP) Section** | | | | | | |
| $V_{OV\_VPP}$ | System OVP Threshold Voltage | | | 18 | | V |
| $V_{OV\_VPP\_RLS}$ | System OVP Release Voltage | | | 17 | | V |
| $t_{OV\_VPP}$ | System OVP Debounce Time | | | 100 | | µs |
| $V_{UV\_VPP}$ | System UVP Threshold Voltage | | 7.5 | 8.0 | 8.5 | V |
| $V_{UV\_VPP\_RLS}$ | System UVP Release Voltage | | 8.5 | 9.0 | 9.5 | V |
| $V_{UV\_VOUT}$ | $V_{OUT}$ UVP Threshold Voltage | | | 4 | | V |
| $V_{UV\_VOUT\_RLS}$ | $V_{OUT}$ UVP Release Voltage | | | 4.5 | | V |
| $V_{OV\_MOTOR}$ | Motor Drive Voltage OVP Threshold Voltage | | 4.3 | 4.5 | 4.8 | V |
| $V_{RL\_MOTOR}$ | Motor Drive Voltage OVP Release Voltage | | | 4.0 | | V |
| **Over-Temperature Protection (OTP) Section** | | | | | | |
| $V_{RT}$ | OTP Threshold Voltage | | 0.9 | 1.0 | 1.1 | V |
| $V_{RT\_RLS}$ | OTP Release Voltage | | 1.15 | 1.20 | 1.25 | V |
| $I_{RT}$ | RT Pin Source Current | | 40 | 50 | 60 | µA |
| **Pins Open/Short Protection Section** | | | | | | |
| $V_{SHORT}$ | Pins Short Protection Level | R_CLK Pin | | 0.2 | | V |
| $V_{OPEN}$ | Pins Open Protection Level | R_CLK and RT Pins | 4.6 | 4.8 | 5.2 | V |

## Typical Performance Characteristics

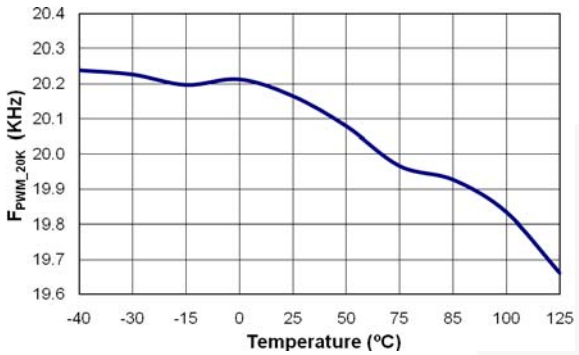



**Figure 6. PWM Frequency 20KHz ($f_{PWM\_20K}$) vs. Temperature**

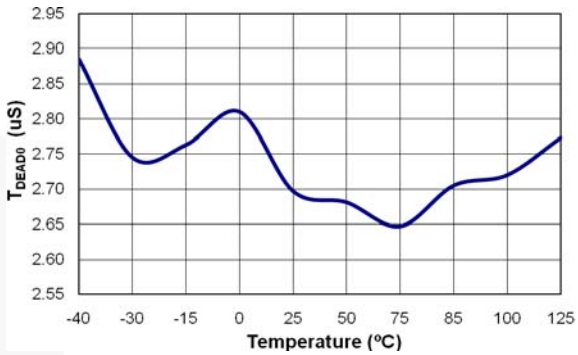



**Figure 7. PWM Dead Time 2µs ($t_{DEAD0}$) vs. Temperature**

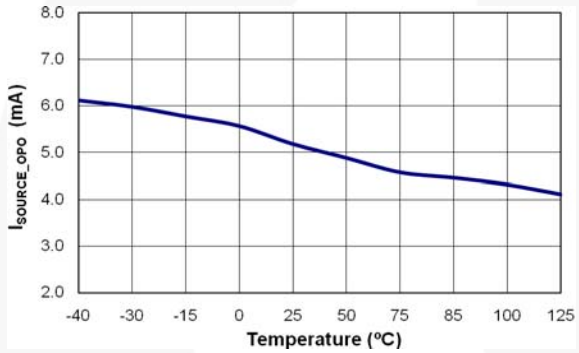



**Figure 8. OPO Current Source ($I_{SOURCE\_OPO}$) vs. Temperature**

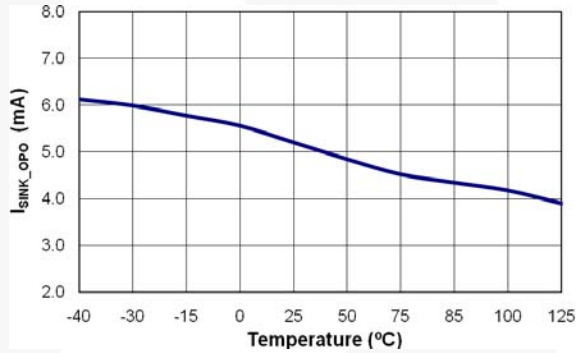



**Figure 9. OPO Current Sink ($I_{SINK\_OPO}$) vs. Temperature**

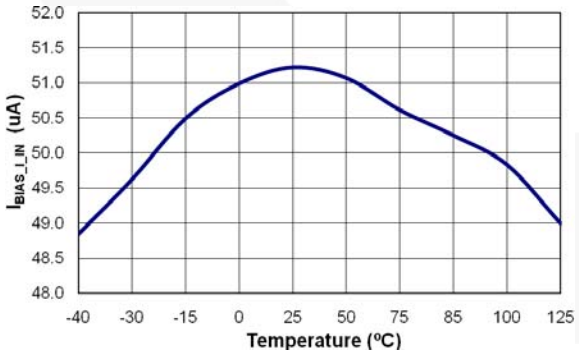



**Figure 10. I_IN Bias Current ($I_{BIAS\_I\_IN}$) vs. Temperature**

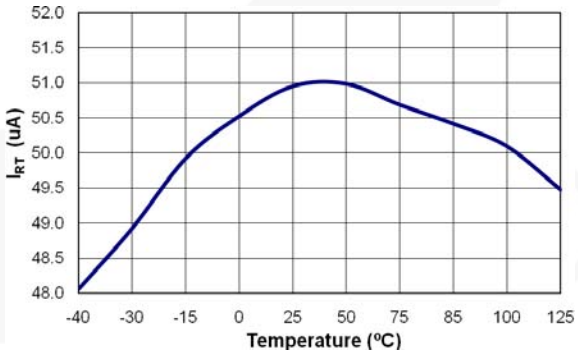



**Figure 11. RT Current Source ($I_{RT}$) vs. Temperature**

## Typical Performance Characteristics (Continued)

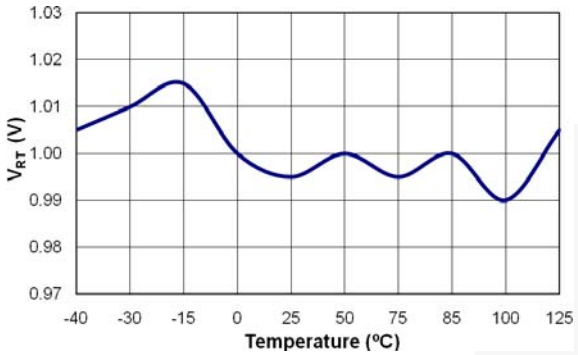



**Figure 12. OTP Threshold Voltage ($V_{RT}$) vs. Temperature**

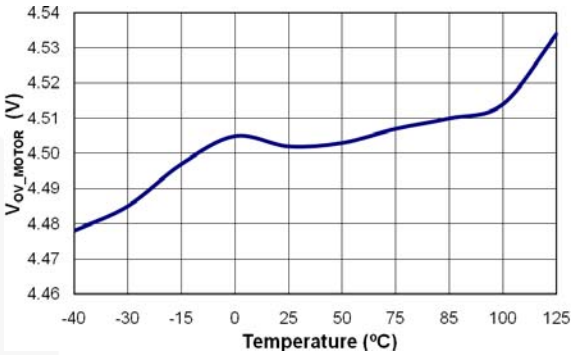



**Figure 13. Motor OVP Threshold Voltage ($V_{OV\_MOTOR}$) vs. Temperature**

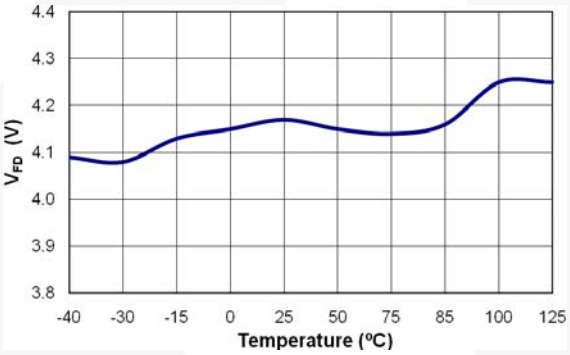



**Figure 14. PWM Full Duty Voltage ($V_{FD}$) vs. Temperature**

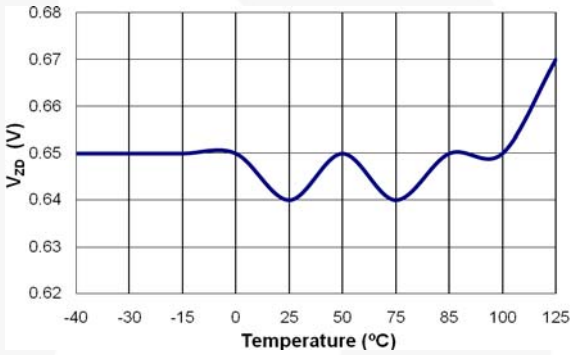



**Figure 15. PWM Zero Duty Voltage ($V_{ZD}$) vs. Temperature**

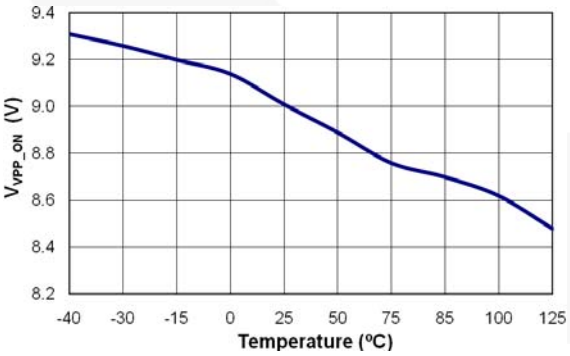



**Figure 16. $V_{PP}$ Turn-On Threshold Voltage ($V_{VPP\_ON}$) vs. Temperature**

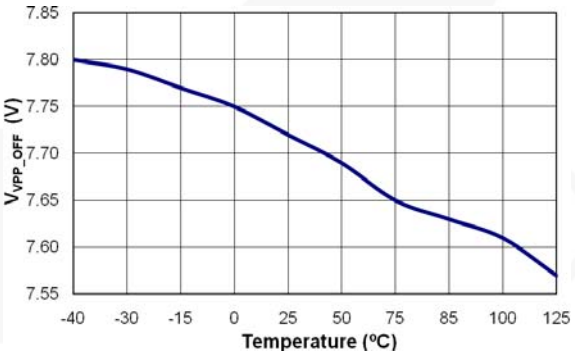



**Figure 17. $V_{PP}$ Turn-Off Threshold Voltage ($V_{VPP\_OFF}$) vs. Temperature**

## Functional Description

### Power Management and Regulator

FCM8201 can be operated in a wide input voltage ($V_{PP}$) range from 10V to 15V. The VOUT pin is the output terminal of an internal voltage regulator. The typical output voltage ranges between 5.0V and 5.2V. To stabilize the $V_{OUT}$ circuit, add an external capacitor connected closely between this terminal and the ground. If the $V_{PP}$ voltage is lower than the 8V threshold, FCM8201 shuts down and all the internal registers are reset.

### Clock Generator

FCM8201 comes with a programmable oscillator. By determining an externally added resistor R_CLK, the system clock can be programmed from 960KHz to 1920KHz. The switching frequency of the PWM signal is equal to 1/64 (divided by ÷64) of the system clock. Therefore, when the system clock is configured as 960KHz, PWM is 960KHz / 64=15KHz. Similarly, if a 20KHz PWM is intended, the system clock has to be set as 1.28MHz.

### PWM Commutation

FCM8201 supports both square-wave and sine-wave PWM for the BLDC motor control. The controller comes with the hall-sensor design used to align the rotor position of the motor. For the Square-Wave PWM Mode, the PWM output commutation (PWM-PWM and PWM-ON) is shown at Table 1 and Table 2. The Square-Wave PWM Modes can be selected by setting an internal control register through the SPI interface. The default value of PWM-PWM commutation is shown in Table 1.

**Table 1. Square Wave PWM-PWM Commutation**

| CW | Hall | Hall | U-V-W | X-Y-Z |
|---|---|---|---|---|
| X | 000 | 0 | 0-0-0 | 0-0-0 |
| X | 111 | 7 | 0-0-0 | 0-0-0 |
| 1 | 001 | 1 | P-0-0 | Pb-1-0 |
| 1 | 011 | 3 | 0-0-P | 0-1-Pb |
| 1 | 010 | 2 | 0-0-P | 1-0-Pb |
| 1 | 110 | 6 | 0-P-0 | 1-Pb-0 |
| 1 | 100 | 4 | 0-P-0 | 0-Pb-1 |
| 1 | 101 | 5 | P-0-0 | Pb-0-1 |
| 0 | 101 | 5 | 0-0-P | 1-0-Pb |
| 0 | 100 | 4 | 0-0-P | 0-1-Pb |
| 0 | 110 | 6 | P-0-0 | Pb-1-0 |
| 0 | 010 | 2 | P-0-0 | Pb-0-1 |
| 0 | 011 | 3 | 0-P-0 | 0-Pb-1 |
| 0 | 001 | 1 | 0-P-0 | 1-Pb-0 |

**Table 2. Square Wave PWM-ON Commutation**

| CW | Hall | Hall | U-V-W | X-Y-Z |
|---|---|---|---|---|
| X | 000 | 0 | 0-0-0 | 0-0-0 |
| x | 111 | 7 | 0-0-0 | 0-0-0 |
| 1 | 001 | 1 | 1-Pb-0 | 0-P-0 |
| 1 | 011 | 3 | 0-0-P | 0-1-Pb |
| 1 | 010 | 2 | Pb-0-1 | P-0-0 |
| 1 | 110 | 6 | 0-P-0 | 1-Pb-0 |
| 1 | 100 | 4 | 0-1-Pb | 0-0-P |
| 1 | 101 | 5 | P-0-0 | Pb-0-1 |
| 0 | 101 | 5 | 0-0-P | 1-0-Pb |
| 0 | 100 | 4 | 0-Pb-1 | 0-P-0 |
| 0 | 110 | 6 | P-0-0 | Pb-1-0 |
| 0 | 010 | 2 | 1-0-Pb | 0-0-P |
| 0 | 011 | 3 | 0-P-0 | 0-Pb-1 |
| 0 | 001 | 1 | Pb-1-0 | P-0-0 |

**Note:**
1. P=PWM, Pb=PWM inverse.

### HALL Signals Input

FCM8201 provides a 3~6μs debounce time for each Hall signal input to reduce the glitch of the Hall signals. When the transition of the Hall signal is slow, a glitch might be produced and an error follow. Through a built-in Hall signal regulation circuit, FCM8201 minimizes the risks of glitches and related errors. This function can be enabled or disabled through a control register via the SPI interface.

The Hall signal's polarity can be configured by setting the levels of HA_INV, HB_INV, and HC_INV. For example, if HA_INV=1, an internal Hall-a signal is the inverse of the HA pin. Otherwise, the internal Hall-a signal is the same as the signal on the HA pin.

### PWM Duty Cycle and Operation

The PWM duty is proportional to the voltage levels on the OPO pin and DUTY pin. A FREE/nST pin is utilized to enable the PWM signals. When FREE/nST pin is set as logic HIGH, the PWM state is in free mode and all PWM outputs (U, V, W, X, Y, Z pins) are logic LOW. Once the FREE/nST pin goes logic LOW, the FCM8201 starts operating the PWM. FCM8201 supports various PWM operation modes to fit different application needs. The detailed description is shown in the Table 6 SPI Register Table.

## Sine Wave Generator

FCM8201 includes space vector modulation (SVM) for the sine-wave PWM. An angle-detect circuit phase-locks the rotor position by using the Hall signals of the motor. The resolution is 32 steps per 60 degrees. Through the PWM operation, the motor current of each phase is sine-wave. The angle shift between phases is 120 degrees.

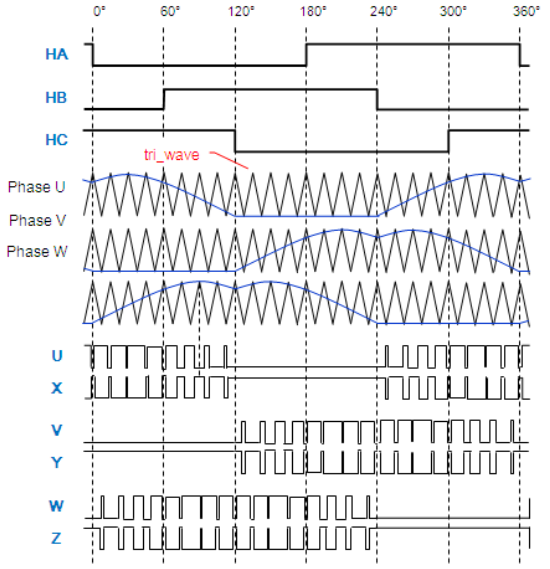



**Figure 18. Sine Wave Output at CW=1**

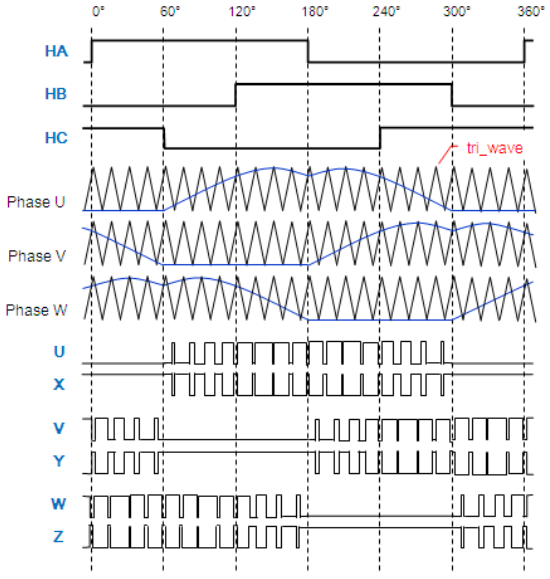



**Figure 19. Sine Wave Output at CW=0**

## Current Feedback and Protections

The current feedback circuit provides two major functions: (1) generating a current feedback signal for the motor control, and (2) supporting over-current protections. The I_IN pin outputs 50μA current to provide a DC bias on the I_IN terminal to prevent a negative voltage, shown in Equation (1) for the I_FB and the I_IN. A 0.5V DC bias on I_IN is recommended. The maximum average current signal is 1V. Using these parameters, the maximum I_FB signal swing is 0.5V~4.5V.

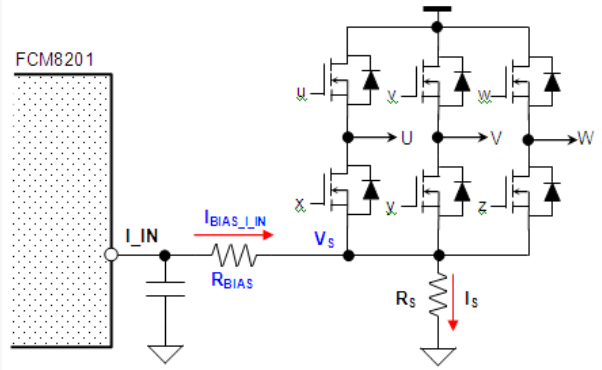



**Figure 20. Current Feedback Flow**

$$V_{I\_FB} = (V_S \times 8) + (I_{BIAS\_I\_IN} \times R_{BIAS}) \quad (1)$$

FCM8201 provides three different levels of over-current (OC) protections. The first level is 1.4V, used for over-load current protection with OC timer delay. If the I_IN is higher than 1.4V, the OC timer is triggered. The OC_Latch is enabled once the timer exceeds its time-out limit. The second level is 1.5V, used for the cycle-by-cycle current limit. The PWM signal is turned off immediately when the I_IN is > 1.5V. The third level is 2.5V, designed for the short-circuit protection. If the I_IN is > 2.5V for over three PWM pulses, all PWM outputs (U, V, W, X, Y, Z pins) are turned off.

## Protections and Faults

**Table 3. Faults Table**

| Type | State | Trigger | Release |
|---|---|---|---|
| $V_{PP}$ OV | Free | $V_{PP}$ > 18V | |
| $V_{PP}$ UV | Free, Reset | $V_{PP}$ < 8V | |
| $V_{OUT}$ UV | Free | $V_{OUT}$ < 4V | |
| $R_T$ | Free | $R_T$ < 1.0V | $R_T$ > 1.2V |
| OS | Free | Open & Short | ↑Run |
| Hall Error | Free | Hall=000 or 111 | |
| HOVP | Free | $V_{SENSE}$ > 4.5V | |
| OC_Latch | Free | I_IN > 1.4V | ↑Run |
| Watch Dog | Free | WDT Time Out | Register |
| SHORT | Free | I_IN > 2.5V | ↑Run |

## Digital-to-Analog Converter

FCM8201 has an 8-bit digital-to-analog converter (DAC) to control the DUTY and IP through the SPI interface.

## Analog to Digital Converter

FCM8201 has a 5-bit analog-to-digital converter (ADC) for the signal on AS, VSENSE, I_FB, and RT pins. Its voltage can be read through the SPI interface.

## I/O Optional Function

The pins 5~8 of FCM8201 are two types of I/O for both stand-alone and microcontroller (SPI mode) applications. FCM8201 uses stand-alone mode by default. The microcontroller should use pin 7 (XP) and pin 8 (XN) to complete the signal toggle procedure shown in Figure 21. In the way, FCM8201 activates SPI operation mode. Afterwards, The pins 5~8 change to SPI function.

To return from SPI mode to stand-alone mode, the microcontroller has to complete the signal toggle procedure shown in Figure 22.

## SPI Interface

The microcontroller can access FCM8201 through the SPI interface. In SPI operation mode, FCM8201 provides more motor control function than in stand-alone operation mode. *Please refer to the Table 6 and Table 7 for the details.*

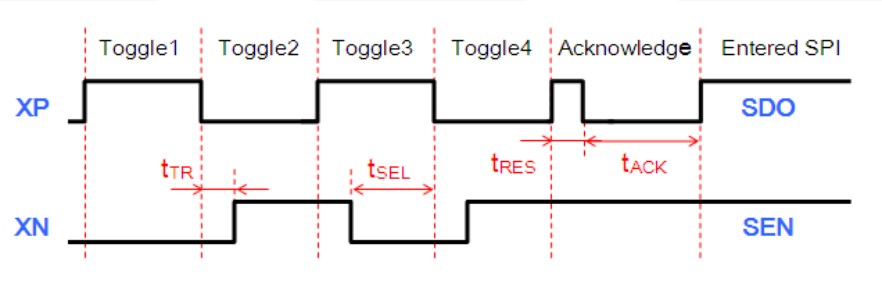



**Figure 21. I/O Select Timing of Entering SPI Mode**

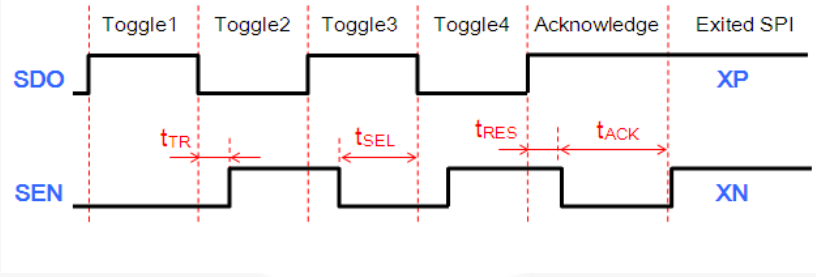



**Figure 22. I/O Select Timing of Exiting SPI Mode**

**Table 4. Timing Specification of I/O Function Selection**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{SEL}$ | Select-Bit Stable Time | $f_{SYS}$=1.28MHz | 12 | | 100 | μs |
| $t_{TR}$ | Select-Bit Transient Time | $f_{SYS}$=1.28MHz | 0 | | 12 | μs |
| $t_{ACT}$ | Acknowledge Bit Pull Low Time | $f_{SYS}$=1.28MHz | | 1 | | ms |
| $t_{RES}$ | FCM8201 Response Time | $f_{SYS}$=1.28MHz | | 4 | | μs |

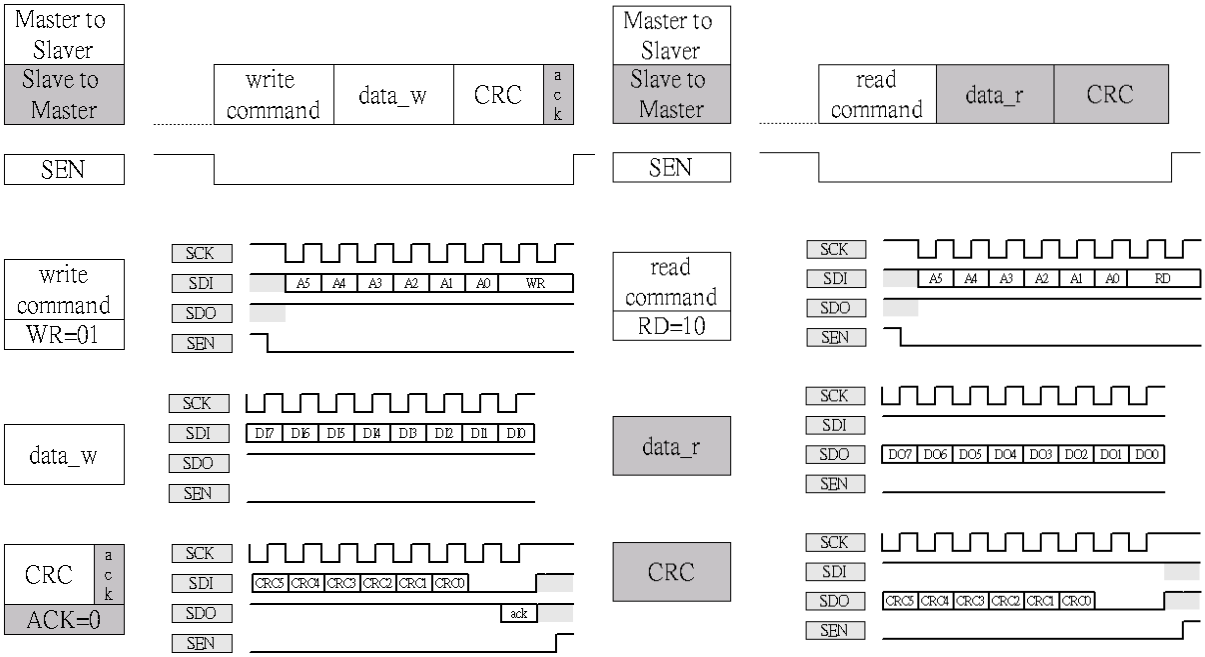



**Figure 23. SPI Bit Definition**

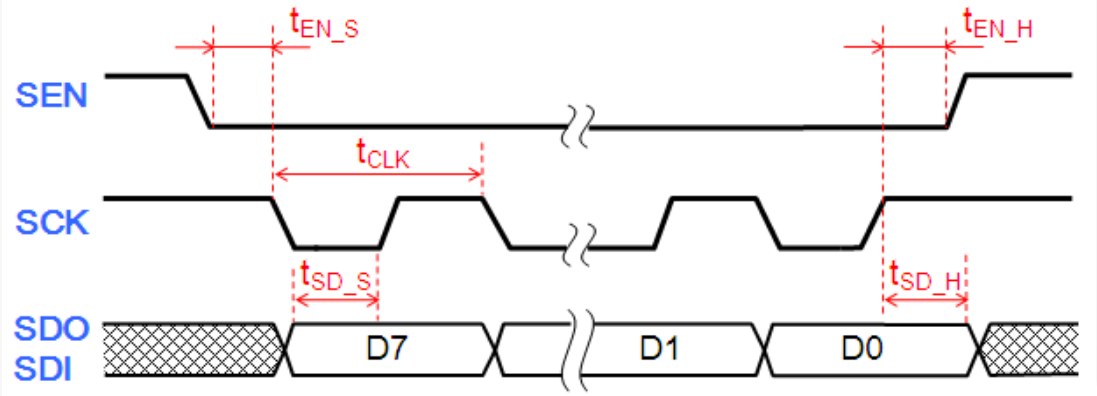



**Figure 24. SPI Timing Specification**

**Table 5. Timing Specification of SPI**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{EN\_S}$ | Setup Time of SEN | $f_{SYS}$=1.28MHz | | 2 | | μs |
| $t_{EN\_H}$ | Hold Time of SEN | $f_{SYS}$=1.28MHz | | 2 | | μs |
| $t_{SD\_S}$ | Setup Time of SDO/SDI | $f_{SYS}$=1.28MHz | | 0 | | μs |
| $t_{SD\_H}$ | Hold Time of SDO/SDI | $f_{SYS}$=1.28MHz | | 2 | | μs |
| $t_{CLK}$ | Maximum Clock Rate of SPI | $f_{SYS}$=1.28MHz | 12.5 | | | μs |
| $t_{TMR\_OUT}$ | SCK Time-Out | $f_{SYS}$=1.28MHz | 90 | 100 | | ms |

**Table 6. SPI Register Table (Read/Write)**

**CNTL_REG: System Control Register**

| Addr. | Name | Type | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x00 | CNTL | W/R | TMR_CLR | OC_TMR2 | OC_TMR1 | OC_TMR0 | IP_EA | DT_EA | CW | FREE/nST |
| | | Reset | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |

| | | | |
|---|---|---|---|
| | b7 | TMR_CLR | OC Timer Clear<br>1=OC timer clear, 0=OC time is normal function |
| | b[6:4] | OC_TMR[2:0] | Overload Current Protection Timer Configuration<br>000=OC timer configure by OC_TMR pin<br>001=OC timer configure to 2^18 ÷ $f_{SYS}$<br>010=OC timer configure to 2^19 ÷ $f_{SYS}$<br>011=OC timer configure to 2^20 ÷ $f_{SYS}$<br>100=OC timer configure to 2^21 ÷ $f_{SYS}$<br>101=OC timer configure to 2^22 ÷ $f_{SYS}$<br>110=OC timer configure to 2^23 ÷ $f_{SYS}$<br>111=OC timer configure to 2^24 ÷ $f_{SYS}$ |
| | b3 | IP_EA | IP_REG Enable<br>1=duty control by IP_REG, 0=duty control by IP pin |
| | b2 | DT_EA | DUTY_REG Enable<br>1=duty control by DUTY_REG, 0=duty control by DUTY pin |
| | b1 | CW | Output Driving Current Direction<br>1=CW, 0=CCW |
| | b0 | FREE/nST | FREE or START<br>1=FREE (PWM outputs disable), 0=START (PWM outputs enable) |

**PWM_REG: PWM Control Register**

| Addr. | Name | Type | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x01 | PWM | W/R | PMOD | n/a | DT1 | DT0 | SEQ_TBL | SYNCOFF | EXT_SYN | LPWM |
| | | Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | | | |
|---|---|---|---|
| | b7 | PMOD | PWM Mode Select<br>0= sine wave PWM drive after angle detector locked<br>1= square wave PWM drive after angle detector locked |
| | b[5:4] | DT[1:0] | Soft Switching Dead Time Setting<br>00=2μs, 01=1.5μs, 10=1μs, 11=0.5μs |
| | b3 | SEQ_TBL | Square Wave Sequencer Table Select<br>0= “PWM-PWM” commutation, 1=“PWM-ON” commutation |
| | b2 | SYNCOFF | Synchronous Rectifier (SR) Disable<br>0= SR enable, 1=SR disable |
| | b1 | EXT_SYN | External Synchronous Rectifier Configure<br>0= SR function control by SYNCOFF bit<br>1= SR function control by OC_TMR pin<br>In this selection, the OC_TMR[2:0] bits of CNTL_REG can’t be set to 0, too<br>OC_TMR pin: HIGH=SR enable, LOW=SR disable |
| | b0 | LPWM | Low-Side Minimum PWM Output Enable. This function is working only on square wave PWM driving<br>0= Low side minimum PWM duty output disable<br>1= Low side minimum PWM duty output enable |

*Continued on the following page…*

**ANG_REG: Angle Shift Control Register**

| Addr. | Name | Type | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x02 | ANG | W/R | ANG_SEL | ARNG1 | ARNG0 | ANG4 | ANG3 | ANG2 | ANG1 | ANG0 |
| | | Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | | |
|---|---|---|
| b7 | ANG_SEL | Angle Shift Control Input Select<br>0=Set by AS pin, 1=Set by ANG[4:0] |
| b[6:5] | ARNG[1:0] | Angle Predictor Working Range Select<br>0,0=Work in 0.8 ~ 80Hz Hall frequency, 48 ~ 4800rpm at 2-pole motor<br>0,1=Work in 0.4 ~ 40Hz Hall frequency, 24 ~ 2400rpm at 2-pole motor<br>1,x=Work in 3.2 ~ 320Hz Hall frequency, 192 ~ 19200rpm at 2-pole motor |
| b[4:0] | ANG[4:0] | Angle Setting of Angle Shift Function<br>0~31=0 ~ 60 degrees |

**SVM_REG: Sine Wave Generator Control Register**

| Addr. | Name | Type | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x03 | SVM | W/R | SIN_MAU | SIN_EA | n/a | n/a | n/a | n/a | n/a | n/a |
| | | Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | | |
|---|---|---|
| b7 | SIN_MAU | Sine Wave Driving Force Active<br>0=Sine wave automatic active<br>1=Sine wave active by SIN_EA bit and ignore AS<0.2V |
| b6 | SIN_EA | Sine Wave Enable (This function only active on while SIN_MAU=1)<br>0=Sine wave disable, 1=Sine wave enable |

**HALL_REG: Hall Signals Control Register**

| Addr. | Name | Type | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x04 | HALL | W/R | n/a | n/a | n/a | n/a | HREG | HC_INV | HB_INV | HA_INV |
| | | Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | | |
|---|---|---|
| b3 | HREG | Hall Signals Regulation Enable<br>0=disable, 1=enable |
| b2 | HC_INV | Hall C Input Invert<br>0=non-invert, 1=invert |
| b1 | HB_INV | Hall B Input Invert<br>0=non-invert, 1=invert |
| b0 | HA_INV | Hall A Input Invert<br>0=non-invert, 1=invert |

*Continued on the following page…*

**WDT_REG: Watch Dog Timer Control Register**

| Addr. | Name | Type | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x06 | WDT | W/R | OSL_DIS | OTL_DIS | n/a | CRC_ON | WDT_EN | CLR | W_TMR1 | W_TMR0 |
| | | Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | | |
|---|---|---|
| b7 | OSL_DIS | Open Short (OS) Fault Latch Disable<br>0=OS protect does not latch<br>1=OS protect does not latch and clear by FREE/nST pin rising edge or FREE/nST bit=1 |
| b6 | OTL_DIS | Over Temperature Fault Latch Disable<br>0=OTP protect does not latch<br>1=OTP protect will latch, and clear by FREE/nST pin rising edge or FREE/nST bit=1 |
| b4 | CRC_ON | SPI CRC Check Enable<br>0=SPI CRC check disable<br>1=SPI CRC check enable |
| b3 | WDT_EN | Watch Dog Timer Enable<br>0=watch dog timer disable<br>1=watch dog timer enable and outputs a faulty when the counter reaches time-out |
| b2 | CLR | Watch Dog Timer Clear (This bit is effective only when WDT_EN=1)<br>1=WDT counter reset, after counter is cleared to zero, this bit auto-resets to 0 |
| b[1:0] | W_TMR[1:0] | Watch Dog Timer Counter Select<br>0,0=0.25s at $f_{SYS}$=1.28MHz<br>0,1=0.5s at $f_{SYS}$=1.28MHz<br>1,0=1s at $f_{SYS}$=1.28MHz<br>1,1=2s at $f_{SYS}$=1.28MHz |

**DUTY_REG: Duty Control Register**

| Addr. | Name | Type | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x08 | DUTY | W/R | DUTY7 | DUTY6 | DUTY5 | DUTY4 | DUTY3 | DUTY2 | DUTY1 | DUTY0 |
| | | Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | | |
|---|---|---|
| b[7:0] | DUTY[7:0] | DUTY Level Configure<br>0 ~ 255=0.5 ~ 4.5V |

**IP_REG: Error Amplifier IP Pin Control Register**

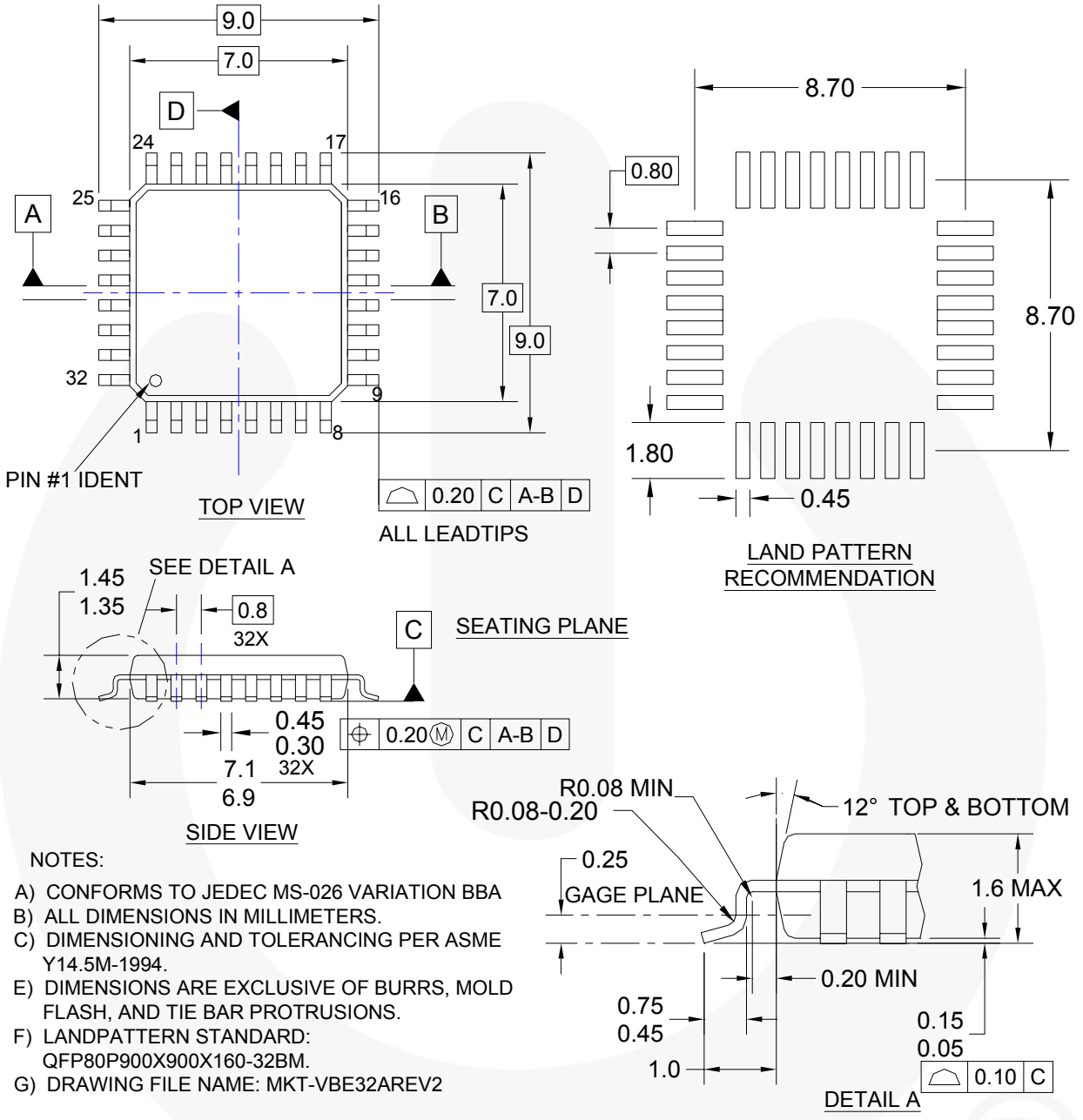
| Addr. | Name | Type | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x09 | IP | W/R | IP7 | IP6 | IP5 | IP4 | IP3 | IP2 | IP1 | IP0 |
| | | Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | | |
|---|---|---|
| b[7:0] | IP[7:0] | IP Pin Level of Error Amplifier Configure<br>0 ~ 255=0.5 ~ 4.5V |

**Table 7. SPI Registers Table (Read Only)**

| **AS_REG: AS Pin Voltage Level Read Register** | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Addr.** | **Name** | **Type** | **B7** | **B6** | **B5** | **B4** | **B3** | **B2** | **B1** | **B0** |
| 0x20 | AS | R | n/a | n/a | n/a | AS4 | AS3 | AS2 | AS1 | AS0 |
| b[4:0] | | AS[4:0] | AS voltage=( AS[4:0] × 0.125 ) + 0.5V | | | | | | | |
| **VSENSE_REG: VSENSE Pin Voltage Level Read Register** | | | | | | | | | | |
| **Addr.** | **Name** | **Type** | **B7** | **B6** | **B5** | **B4** | **B3** | **B2** | **B1** | **B0** |
| 0x21 | VSENSE | R | n/a | n/a | n/a | VS4 | VS3 | VS2 | VS1 | VS0 |
| b[4:0] | | VS[4:0] | VSENSE voltage=( VS[4:0] × 0.125 ) + 0.5V | | | | | | | |
| **I_FB_REG: I_FB Pin Voltage Level Read Register** | | | | | | | | | | |
| **Addr.** | **Name** | **Type** | **B7** | **B6** | **B5** | **B4** | **B3** | **B2** | **B1** | **B0** |
| 0x22 | I_FB | R | n/a | n/a | n/a | IFB4 | IFB3 | IFB2 | IFB1 | IFB0 |
| b[4:0] | | IFB[4:0] | I_FB voltage=( IFB[4:0] × 0.125 ) + 0.5V | | | | | | | |
| **RT_REG: RT Pin Voltage Level Read Register** | | | | | | | | | | |
| **Addr.** | **Name** | **Type** | **B7** | **B6** | **B5** | **B4** | **B3** | **B2** | **B1** | **B0** |
| 0x23 | RT | R | n/a | n/a | n/a | RT4 | RT3 | RT2 | RT1 | RT0 |
| b[4:0] | | RT[4:0] | RT voltage=( RT[4:0] × 0.125 ) + 0.5V | | | | | | | |
| **HPERH_REG: Hall Period Counter HIGH Byte** | | | | | | | | | | |
| **Addr.** | **Name** | **Type** | **B7** | **B6** | **B5** | **B4** | **B3** | **B2** | **B1** | **B0** |
| 0x26 | HPERH | R | HP15 | HP14 | HP13 | HP12 | HP11 | HP10 | HP9 | HP8 |
| b[7:0] | | HP[15:8] | Hall period count HIGH byte, bit [15:8] | | | | | | | |
| **HPERL_REG: Hall Period Counter LOW Byte** | | | | | | | | | | |
| **Addr.** | **Name** | **Type** | **B7** | **B6** | **B5** | **B4** | **B3** | **B2** | **B1** | **B0** |
| 0x27 | HPERL | R | HP7 | HP6 | HP5 | HP4 | HP3 | HP2 | HP1 | HP0 |
| b[7:0] | | HP[7:0] | Hall period count LOW byte, bit [7:0] | | | | | | | |
| **STATUS_REG: System Status Register** | | | | | | | | | | |
| **Addr.** | **Name** | **Type** | **B7** | **B6** | **B5** | **B4** | **B3** | **B2** | **B1** | **B0** |
| 0x28 | STATUS | R | OT | OC | OS | OV | H_ERR | DIR | WDT | SHORT |
| b7 | | OT | 1=Over-temperature protection triggered (RT pin voltage $< V_{RT}$) | | | | | | | |
| b6 | | OC | 1=Overload current protection triggered | | | | | | | |
| b5 | | OS | 1=Open/Short protection triggered | | | | | | | |
| b4 | | OV | 1=Motor drive over-voltage protection triggered (VSENSE pin voltage $> V_{OV\_MOTOR}$) | | | | | | | |
| b3 | | H_ERR | 1=Hall signals error (HA/B/C=1/1/1 or 0/0/0) | | | | | | | |
| b2 | | DIR | 1=Hall direction different from that on the PWM sequencer table | | | | | | | |
| b1 | | WDT | 1=Watch dog time-out triggered | | | | | | | |
| b0 | | SHORT | 1=Short-circuit current protection triggered | | | | | | | |

## Physical Dimensions




NOTES:

A) CONFORMS TO JEDEC MS-026 VARIATION BBA
B) ALL DIMENSIONS IN MILLIMETERS.
C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
E) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR PROTRUSIONS.
F) LANDPATTERN STANDARD: QFP80P900X900X160-32BM.
G) DRAWING FILE NAME: MKT-VBE32AREV2

**Figure 25. 32-Leadless Quad Flat Pack Package (LQFP)**

*Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.*

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FACT®
FAST®
FastvCore™
FETBench™
FlashWriter®*
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F-PFS™
FRFET®
Global Power Resource℠
Green FPS™
Green FPS™ e-Series™
*Gmax*™
GTO™
IntelliMAX™
ISOPLANAR™
MegaBuck™
MICROCOUPLER™
MicroFET™
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MicroPak2™
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Quiet Series™
RapidConfigure™
™
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SmartMax™
SMART START™
SPM®
STEALTH™
SuperFET™
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
SupreMOS®
SyncFET™
Sync-Lock™
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The Power Franchise®
the power franchise
TinyBoost™
TinyBuck™
TinyCalc™
TinyLogic®
TINYOPTO™
TinyPower™
TinyPWM™
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## PRODUCT STATUS DEFINITIONS

### Definition of Terms

| Datasheet Identification | Product Status | Definition |
|---|---|---|
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| Preliminary | First Production | Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design. |
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