Tsi148™ Schematic Review Checklist

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1. Tsi148 Schematic Review Checklist

This checklist discusses the following schematic review topics for the Tsi148:

- "Overview" on page 3
- "PCI/X Signals" on page 6
- "VMEbus Signals" on page 13
- "PLL Signals" on page 29
- "Power Supply Signals" on page 31
- "Miscellaneous Signals" on page 32
- "Tsi148 Typical Applications" on page 36
- "Recommended Reading" on page 47

Revision History

80A3020_CL001_07, Formal, April 2010

Replaced Figure 7 with correct diagram.

80A3020_CL001_06, Formal, October 2009

This version of the document was rebranded as IDT. It does not include any technical changes.

80A3020_CL001_05, Formal, September 2008

The following information has been updated:

- "ACK64_" on page 6

80A3020_CL001_04, Formal, April 2008

Slight formatting and technical changes have occurred throughout the document.

1.1 Overview

The *Schematic Review Checklist* gives a signal by signal termination review for Tsi148 applications. This document is intended for designers that are in the process of completing their Tsi148 board schematics.

For this reason, it is beneficial to review the contents of the checklist before routing a Tsi148-based board.

For more information about Tsi384 hardware and software, refer to the *Tsi148 User Manual.*

1.1.1 Signals

Table 1 describes the signal types found in the Tsi148.

Table 1: Signal Conventions - I/O Type

Signal Type	Definition
Input	Standard input only signal
Output	Standard output only signal, Totem Pole
Output (t/s)	Standard tri-state output only signal
Output (o/d)	Open drain output — allows multiple devices to share as a wire-OR
Bi-direct	Bi-directional, Tri-state input/output signal
Bi-direct (o/d)	Bi-directional, Open drain input/output — allows multiple devices to share as a wired-OR when used as output

Table 2 shows the I/O level conventions used for signal descriptions.

Table 2: Signal Conventions - I/O Level

Symbol	Type
3.3V TTL	3.3V I/O cell, TTL compatible
5Vtlr TTL	3.3V I/O cell, TTL compatible, 5V tolerant
3.3V PCI/X	3.3V I/O cell, PCI/PCI-X compatible
1.8V	1.8V I/O Cell

Table 3 describes the current capabilities (driver impedance) of the I/O cell.

Table 3: Signal Conventions - I/O Drive

Symbol	Type
35 ohm	Nominal impedance 35 ohms
65 ohm	Nominal impedance 65 ohms
PCI/X	For a 3.3V PCI/X I/O cell, the driver impedance for a point-to-point application is 40 ohms. For a 3.3V PCI/X I/O cell, the driver impedance for a multi-point application is 20 ohms. Driver impedance is controlled by the PCIMC pin.

1.1.2 Design Recommendation

It is advantageous to pull power up option signals high and have a jumper option to ground so the option can be changed after board production. Alternatively these can be controlled with a CPLD.

Refer to the Tsi148 *User Manual* for a complete explanation of the power-up options defined for the bridge.

IDT experience has shown that designers who have built either jumpers or a CPLD into their designs have been able to significantly reduce the time it takes to bring their design up.

High Z or Weak pull-up is suggested to be 10K.
Regular pull-ups are suggested to be 4.7K unless otherwise noted. Pull-downs are suggested to be 1K.

1.1.3 Recommended Terminations

The Tsi148 has been designed such that it requires full buffering from the VMEbus signals. Necessary drive current to the VMEbus is provided by the transceivers while at the same time isolating the Tsi148 from potentially noisy VMEbus backplanes. Designers should use higher performance bus transceivers with improved drive current, skew, and tighter receiver thresholds on all address, data and control bus signal lines. IDT recommends the TI SN74VMEH22501 transceivers. The Tsi148 has been designed to work with the TI SN74VMEH22501 transceivers.

All recommended terminations for the VMEbus signals given in this document are from the American National Standard for VME64, VME64x and Vita 1.5 for 2eSST standard.

It is important to note that there are required pull-up terminations for some of the control signals on the PCI/X interface. These pull-ups must exist somewhere in the complete system for PCI/X compliance. The central resource on the PCI/X bus is usually responsible to ensure proper termination of these signals.

All recommendations for the PCI/X signals given in this document are from the *PCI 2.2 Specification*. If you have any questions about signal termination, it is recommended you review the appropriate sections of the latest PCI specification, available at www.pcisig.com.

1.1.4 Checkpoint

A Checkpoint section is included at the end of every signal. This is for the user to track the results of each signal recommendation in the Schematic Review.

- Pass — correct action taken
- Fail — no action or incorrect action taken
- Caution — problem with recommendation
- Help — user requires assistance or additional information

1.2 PCI/X Signals

This section gives recommended terminations for Tsi148 signals that connect to the PCI/X bus.

All of the 3.3V PCI/X signals have an internal 14K pull-up on them which will vary over process. These internal 14K PCI/X pull-ups are disabled by default. In order to enable internal PCI/X pull-ups PCIPUEN must be pulled up on the board. IDT recommends the PCIPUEN pin to be pulled down on the board for PCI/X compliance.

Refer to “Miscellaneous Signals” on page 32 for more information.

1.2.1 ACK64_

Acknowledge 64-bit Transaction: 3.3V PCI/X, Bi-direct

An active low signal. This signal is asserted by a target to indicate the target’s willingness to participate in a 64-bit transaction. Driven by the target; sampled by the master. Rescinded by the target at the end of the transaction.

Recommended Termination:

- When in 64-bit PCI/X mode, the Central Resource on the PCI/X bus must provide a weak 10K pull-up
- When in 32-bit PCI/X mode, the Tsi148 requires that this signal be pulled high with a weak 10K pull-up

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.2.2 AD[63:0]

PCI/X Address/Data Bus: 3.3V PCI/X, Bi-direct

Address and data are multiplexed over these pins to provide a 64-bit address/data bus.

Recommended Termination:

- None, the Central Resource on the PCI/X bus must provide the following:
  - AD[63:32] upper 32-bits — Pull-up
  - AD[31:0] lower 32-bits — None

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.2.3 CBE[7:0]_

Bus Command and Byte Enable Lines: 3.3V PCI/X, Bi-direct

Command and byte enable information is multiplexed over all eight CBE lines.

Recommended Termination:

- None, the Central Resource on the PCI/X bus must provide the following:
  - CBE[7:4]_ — Pull-up
  - CBE[3:0]_ — None

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.2.4 DEVSEL_

PCI/X Device Select: 3.3V PCI/X, Bi-direct

An active low indication from the target of the current transaction. Driven by the target; sampled by the master. Rescinded by the target at the end of the transaction.

Recommended Termination:

- None, the Central Resource on the PCI/X bus must provide a pull-up

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.2.5 FRAME_

Cycle Frame for PCI/X Bus: 3.3V PCI/X, Bi-direct

An active low indication from the current bus master of the beginning and duration of a transaction. Driven by the bus master; sampled by the

selected target. Rescinded by the bus master at the end of the transaction.

Recommended Termination:

- None, the Central Resource on the PCI/X bus must provide a pull-up

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.2.6 GNT_

PCI/X Bus Grant: 3.3V PCI/X, Input

Used by the external arbiter to grant the bus to Tsi148.

Recommended Termination:

- None, the Central Resource on the PCI/X bus must provide a pull-up

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.2.7 IDSEL

PCI/X Initialization Device Select: 3.3V PCI/X, Input

Used as a chip select during Configuration 0 read and write transactions.

Recommended Termination:

- For access to the Tsi148's configuration registers from the PCI/X bus. The central resource should connect the Tsi148's IDSEL to only one unique AD line through a 2K series resistor. Choose from AD[31:16].

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.2.8 INTA_

PCI/X Interrupt A: 3.3V TTL, Output (o/d), 35 ohm

An active low-level indication of an interrupt. This signal is asynchronous to PCLK.

Recommended Termination:

- Although this signal has an internal pull-up it may not be strong enough for a specific application so a pull-up on the board is recommended as well.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.2.9 INTB_

PCI/X Interrupt B: 3.3V TTL, Output (o/d), 35 ohm

An active low-level indication of an interrupt. This signal is asynchronous to PCLK.

Recommended Termination:

- Although this signal has an internal pull-up it may not be strong enough for a specific application so a pull-up on the board is recommended as well.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.2.10 INTC_

PCI/X Interrupt C: 3.3V TTL, Output (o/d), 35 ohm

An active low-level indication of an interrupt. This signal is asynchronous to PCLK.

Recommended Termination:

- Although this signal has an internal pull-up it may not be strong enough for a specific application so a pull-up on the board is recommended as well.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.2.11 INTD_

PCI/X Interrupt D: 3.3V TTL, Output (o/d), 35 ohm

An active low-level indication of an interrupt. This signal is asynchronous to PCLK.

Recommended Termination:

- Although this signal has an internal pull-up it may not be strong enough for a specific application, so a pull-up on the board is recommended as well.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.2.12 IRDY_

PCI/X Initiator Ready: 3.3V PCI/X, Bi-direct

An active low indication of the current bus master's ability to complete the current data phase. Driven by the master; sampled by the selected target**.**

Recommended Termination:

- None, the Central Resource on the PCI/X bus must provide a pull-up)

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.2.13 LRSTI_

PCI/X Bus Reset In: 3.3V TTL, Input

Asynchronous active low reset, when asserted the PCI bus internal logic is reset. This signal should be connected to the boards local bus reset signal.

Recommended Termination:

- This signal has an internal pull-up on it, but it may not be strong enough. The Central Resource on the PCI/X bus must provide a pull-up

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.2.14 LRSTO_

PCI/X Bus Reset Out: 3.3V TTL, Output, 65 ohm

Asynchronous active low reset, when asserted the PCI bus logic on the board should be reset. This signal should be combined with other reset signals on the PCI bus to generate the local bus reset signal.

Recommended Termination:

- None, this signal has an internal pull-up.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.2.15 LSRSTI_

Local System Reset In: 3.3V TTL, Input

This signal allows on board logic to generate a VMEbus system reset. When the LSRSTI_ signal is asserted, an SRSTO signal will be generated.

Recommended Termination:

- Although this signal has an internal pull-up it may not be strong enough for a specific application so a pull-up on the board is recommended as well.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.2.16 M66EN

PCI 66 MHz Enable: 3.3V PCI/X, Input

When pulled low, this signal configures the PLL for operation for 33 MHz. When pulled high, it configures the PLL for operation from 50 to 66 MHz.

Recommended Termination:

- When pulled low, this signal configures the PLL for 33 MHz operation. When pulled high, it configures the PLL for operation from 50 to 66 MHz.

See the *PCI Local Bus Specification Revision 2.2* for more information, including decoupling requirements.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.2.17 PAR

PCI/X Bus Parity: 3.3V PCI/X, Bi-direct

Carries even parity across AD[31:0] and C/BE[3:0]. Driven by the master for the address and write data phases. Driven by the target for read data phases.

Recommended Termination:

- None.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.2.18 PAR64

PCI/X Bus Parity Upper DWORD: 3.3V PCI/X, Bi-direct

Carries even parity across AD[63:32] and CBE[7:4]. Driven by the master for address and write data phases. Driven by the target for read data phases.

Recommended Termination:

- None, the Central Resource on the PCI/X bus must provide a pull-up.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.2.19 PCLK

PCI/X Clock Input: 3.3V PCI/X, Input

Used to generate fixed timing parameters for the PCI/X Interface. PCLK can operate from 33-to-133 MHz.

Recommended Termination:

- None

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.2.20 PERR_

PCI/X Parity Error: 3.3V PCI/X, Bi-direct

An active low indication of a data parity error. Driven by the target receiving data. Rescinded by the target at the end of the transaction.

Recommended Termination:

- None, the Central Resource on the PCI/X bus must provide a pull-up

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.2.21 PURSTI_

PCI/X Power-up Reset In: 3.3V TTL, Input

Asynchronous active low reset, when asserted all Tsi148 circuitry is reset. When PURSTI_ is asserted, the SRSTO and LRSTO_ signals will be asserted.

Recommended Termination:

- Although this signal has an internal pull-up it may not be strong enough for a specific application, so a pull-up on the board is recommended as well.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.2.22 REQ_

PCI/X Bus Request: 3.3V PCI/X, Output (t/s)

Driven low by Tsi148 to request the bus.

Recommended Termination:

- None, the Central Resource on the PCI/X bus must provide a weak pull-up of 10K

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.2.23 REQ64_

Request 64-bit Transfer: 3.3V PCI/X, Bi-direct

An active low indication from the current master of its choice to perform 64-bit transactions. Rescinded by the bus master at the end of the transaction.

Recommended Termination:

- None, the Central Resource on the PCI/X bus must provide a pull-up

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.2.24 SERR_

PCI/X System Error: 3.3V PCI/X, Output (o/d)

An active low indication of address parity error.

Recommended Termination:

- None, the Central Resource on the PCI/X bus must provide a pull-up

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.2.25 STOP_

PCI/X Stop: 3.3V PCI/X, Bi-direct

An active low indication from the target of its desire to stop the current transition. Sampled by the master; rescinded by the target at the end of the transaction.

Recommended Termination:

- None, the Central Resource on the PCI/X bus must provide a pull-up

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.2.26 TRDY_

PCI/X Target Ready: 3.3V PCI/X, Bi-direct

An active low indication of the current target's ability to complete the data phase. Driven by the target; sampled by the current bus master. Rescinded by the target at the end of the transaction.

Recommended Termination:

- None, the Central Resource on the PCI/X bus must provide a pull-up

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3 VMEbus Signals

This section gives recommended terminations for Tsi148 signals that connect to the VMEbus. Refer to “Tsi148 Typical Applications” on page 36 for details on how the Tsi148 should be connected to the external transceivers.

1.3.1 ACFAILI_

VMEbus AC Fail In: 5Vtlr TTL, Input

Warns the VMEbus system of imminent power failure. This gives the modules in the system time to shut down in an orderly fashion before power-down. The VMEbus AC fail is monitored by the Tsi148’s interrupter logic. If enabled, an interrupt is generated on the falling edge of ACFAIL_.

Recommended Termination:

- Connect this signal to the VMEbus through an external buffer.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.2 ADBOUT

Address Transceiver Direction Control: 3.3V TTL, Output, 35 ohm

This signal controls the direction on the external transceivers for VA[31:1] and LWORD_ signals. When Tsi148 is driving these signals on the VMEbus this signal is driven high; when the VMEbus is driving these signals this signal is driven low.

Recommended Termination:

- None, this signal has an internal pull-down

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.3 AM[5:0]

VMEbus Address Modifier Codes: 3.3V TTL, Bi-direct, 35 ohm

These codes indicate the address space being accessed, the privilege level, the cycle type and data type. These signals are monitored by the Tsi148 VMEbus Slave and driven by Tsi148 when it becomes VMEbus master.

Recommended Termination:

- None, these signals have internal pull-ups. These signals are connected to the VMEbus through external bi-directional buffers. WRITE_ and IACK_ should be included on the same external buffer.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.4 AMOUT

AM Code Direction Control: 3.3V TTL, Output, 35 ohm

This signal controls the direction on the external transceivers for the AM[5:0], IACK and WRITE_ signals. When the Tsi148 is driving these signals on the VMEbus this signal is driven high; when the VMEbus is driving these signals this signal is driven low.

Recommended Termination:

- None, this signal has an internal pull-down.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.5 ASI_

VMEbus Address Strobe In: 3.3V TTL, Input

The falling edge of this signal indicates a valid address on the VMEbus. This signal is monitored by the VMEbus master and slave.

Recommended Termination:

- None, this signal has an internal pull-up. This signal is received from the VMEbus with an external buffer.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.6 ASO_

VMEbus Address Strobe Out: 3.3V TTL, Output, 35 ohm

The falling edge of this signal indicates a valid address on the VMEbus. This signal is driven by the Tsi148 when it is VMEbus master.

Recommended Termination:

- None, this signal has an internal pull-up. This signal is connected to the VMEbus through an external tri-state buffer.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.7 ASOE

Address Strobe Output Enable: 3.3V TTL, Output, 35 ohm

This signal is used to enable the address strobe driver. When the Tsi148 is driving the address strobe on the VMEbus this signal is driven high; when the VMEbus is driving the address strobe this signal is driven low.

Recommended Termination:

- None, this signal has an internal pull-down.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.8 BBSYI_

VMEbus Bus Busy In: 3.3V TTL, Input

This signal is monitored by the Tsi148's VMEbus requester and arbiter to see whether the VMEbus is owned by another VMEbus master.

Recommended Termination:

- None, this signal has an internal pull-up. This signal is received from the VMEbus through an external buffer.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.9 BBSYO

VMEbus Bus Busy Out: 3.3V TTL, Output, 35 ohm

This signal is driven by the Tsi148's VMEbus requester.

Recommended Termination:

- None, this signal has an internal pull-down. This signal is connected to the VMEbus through an external inverting open collector buffer.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.10 BCLRI_

VMEbus Bus Clear In: 3.3V TTL, Input

This signal is monitored by the Tsi148's VMEbus master.

Recommended Termination:

- None, this signal has an internal pull-up. This signal is received from the VMEbus with an external buffer.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.11 BCLRO_

VMEbus Bus Clear Out: 3.3V TTL, Output, 35 ohm

When asserted this signal requests that the current owner release the VMEbus. Asserted by the Tsi148 when configured as SCON and the arbiter detects a higher level pending request.

Recommended Termination:

- None, this signal has an internal pull-up. This signal is connected to the VMEbus through an external tri-state buffer.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.12 BDFAIL_

Board Fail: 3.3V TTL, Bi-direct (o/d), 65 ohm

When the BDFAIL bit in the Tsi148's VMEbus Status Register is set the BDFAIL_ signal is asserted. The BDFAIL_ signal is driven by external open drain driver which allows on board logic to also assert the BDFAIL_ signal. When this signal is asserted, the SFAILO signal will be asserted if the SFAILEN bit is set.

Recommended Termination:

- Although this signal has an internal pull-up, it may not be strong enough in specific applications, so a pull-up on the board is recommended as well.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.13 BERRI_

VMEbus Bus Error In: 3.3V TTL, Input

This signal is monitored by the Tsi148's VMEbus master.

Recommended Termination:

- None, this signal has an internal pull-up. This signal is received from the VMEbus with an external buffer.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.14 BERRO_

VMEbus Bus Error Out: 3.3V TTL, Output, 35 ohm

This signal is driven by the Tsi148's VMEbus slave and global time-out timer.

Recommended Termination:

- None, this signal has an internal pull-up. This signal is connected to the VMEbus with an external open collector buffer.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.15 BERROE

Bus Error Output Enable: 3.3V TTL, Output, 35 ohm

This signal is used by the Tsi148 to enable the bus error driver.

Recommended Termination:

- None, this signal has an internal pull-down.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.16 BG[3:0]IN_

VMEbus Bus Grant In: 5Vtlr TTL, Input

The VME arbiter awards use of the data transfer bus by driving these bus grant lines low. The signal propagates down the bus grant daisy chain and is either accepted by the requester (if requesting at the appropriate level) or passed on to the next board in the bus grant daisy chain.

Recommended Termination:

- We recommend these signals be connected to the VMEbus through external buffers.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.17 BG[3:0]INOUT_

VMEbus Bus Grant InOut: 5Vtlr TTL, Output (t/s), 35 ohm

The VMEbus standard requires the board in slot 1 to drive the bus grant in signals as outputs. These outputs are for test purposes only they do not go anywhere.

Recommended Termination:

- We recommend these signals be connected to the BG[3:0]IN_ signals through external tri-state buffers enabled by SCON. IDT recommends the Phillips 74LVT126.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.18 BG[3:0]OUT_

VMEbus Bus Grant Out: 5Vtlr TTL, Output, 35 ohm

Only one output is asserted at a time, according to the level at which the VMEbus is being granted.

Recommended Termination:

- We recommend these signals be connected to the VMEbus through external buffers.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.19 BR[3:0]I_

VMEbus Bus Request In: 5Vtlr TTL, Input

If the Tsi148 is SCON, the arbiter logic monitors these signals and generates the appropriate bus grant signals. These signals are also monitored by the Tsi148's requester.

Recommended Termination:

- We recommend these signals be connected to the VMEbus through external buffers.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.20 BR[3:0]O

VMEbus Bus Request Out: 3.3V TTL, Output, 35 ohm

The VMEbus request signals are driven by the Tsi148's VMEbus requester.

Recommended Termination:

- None, these signals have internal pull-downs. These signals are connected to the VMEbus through external inverting buffers. IDT recommends the Phillips 74LVT126.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.21 DBOE_

Data Bus Output Enable: 3.3V TTL, Output, 35 ohm

Used to control the enable of the data bus, address bus and LWORD_ transceivers. During PURSTI_, DBOE_ will be negated therefore isolating the Tsi148 from the VMEbus. This puts the address and data buses into a high impedance state allowing for pull-ups/pull-downs to be placed on these signals to set power-up options. DBOE_ is asserted after PURSTI_ is negated.

Recommended Termination:

- None, this signal has an internal pull-up.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.22 DBOUT

Data Bus Out: 3.3V TTL, Output, 35 ohm

Used to control the direction of the data bus transceivers. When the Tsi148 is driving these lines on the VMEbus this signal is driven high; when the VMEbus is driving the Tsi148 this signal is driven low.

Recommended Termination:

- None, this signal has an internal pull-down.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.23 DSOE

Data Strobe Output Enable: 3.3V TTL, Output, 35 ohm

Used to control the direction of the data strobe transceivers. When the Tsi148 is driving these lines on the VMEbus this signal is driven high; when the VMEbus is driving the Tsi148 this signal is driven low.

Recommended Termination:

- None, this signal has an internal pull-down.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.24 DS[1:0]I_

VMEbus Data Strobe In: 3.3V TTL, Input

These signals are monitored by the Tsi148's VMEbus Slave logic.

Recommended Termination:

- None, these signals have internal pull-ups. These signals are received from the VMEbus through external buffers.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.25 DS[1:0]O_

VMEbus Data Strobe Out: 3.3V TTL, Output, 35 ohm

These signals are driven by the Tsi148 during VMEbus master cycles.

Recommended Termination:

- None, these signals have internal pull-ups. These signals are connected to the VMEbus through external tri-state buffers.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.26 DTACKI_

VMEbus Data Transfer Acknowledge In: 5Vtlr TTL, Input

This signal is monitored by the Tsi148's VMEbus master. Driven low indicates that the addressed slave has responded to the transfer.

Recommended Termination:

- This signal will normally be driven by a receiver with a totem pole output. A pull-up is not required unless the output of the receiver is tri-stated for some reason like test. This signal is received from the VMEbus through an external buffer.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.27 DTACKO_

VMEbus Data Transfer Acknowledge Out: 3.3V TTL, Output, 35 ohm

This signal is driven by the Tsi148's VMEbus slave.

Recommended Termination:

- None, this signal has an internal pull-up. This signal is connected to the VMEbus through an external tri-state buffer.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.28 DTACKOE

Data Transfer Acknowledge Output Enable: 3.3V TTL, Output, 35 ohm

This signal is used to enable the Tsi148's data transfer acknowledge driver. When the Tsi148 is driving DTACK_ on the VMEbus this signal is driven high; when the VMEbus is driving the Tsi148 this signal is driven low.

Recommended Termination:

- None, this signal has an internal pull-down.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.29 GA[4:0]_

VMEbus Geographic Address: 3.3V TTL, Input

These signals are connected to the geographic address signals on the VMEbus.

Recommended Termination:

- Although these signals have internal pull-ups on them, they may not be strong enough for specific applications, so pull-ups on the board are recommended as well. Since these signals are either grounded or open on the backplane, they can be connected directly to the Tsi148. Pull-ups are placed on the individual board to allow a logic high level to be successfully detected if the signal is not grounded on the backplane.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.30 GAP_

VMEbus Geographic Address Parity: 3.3V TTL, Input

This signal is connected to the geographic address parity signal on the VMEbus.

Recommended Termination:

- Although this signals has an internal pull-up, it may not be strong enough for specific applications, so a pull-up on the board is recommended as well. Since this signal is either grounded or open on the backplane, it can be connected directly to the Tsi148. A Pull-up is placed on the individual board to allow a logic high level to be successfully detected if the signal is not grounded on the backplane.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.31 IACK_

VMEbus Interrupt Acknowledge: 3.3V TTL, Bi-direct, 35 ohm

Indicates that the cycle that is starting is an interrupt acknowledge cycle. This signal is monitored by the Tsi148's VMEbus Slave. This signal is driven when the Tsi148 is VMEbus master.

Recommended Termination:

- None, this signal has an internal pull-up. This signal is connected to the VMEbus through an external bi-directional buffer. IACK_ should be included in the same transceiver as the AM[5:0] and WRITE_ signals.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.32 IACKIN_

VMEbus Interrupt Acknowledge In: 5Vtlr TTL, Input

Input for IACK daisy chain driver. If the interrupt acknowledge is at the same level as the interrupt currently generated by the Tsi148, then the cycle is accepted. If the interrupt acknowledge is not at the same level as the current interrupt or the Tsi148 is not generating an interrupt, then the Tsi148 propagates IACKOUT_. This signal is monitored by the Tsi148's VMEbus interrupter.

Recommended Termination:

- We recommend these signals be connected to the VMEbus through external buffers.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.33 IACKOUT_

VMEbus Interrupt Acknowledge Out: 5Vtlr TTL, Output, 35 ohm

The VMEbus interrupt acknowledge out signal is driven by the Tsi148's VMEbus interrupter. This signal is generated by the Tsi148 if it receives an IACKIN_ and is not currently generating an interrupt at the level being acknowledged.

Recommended Termination:

- We recommend these signals be connected to the VMEbus through external buffers.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.34 IRQ[7:1]I_

VMEbus Interrupt Request In: 5Vtlr TTL, Input

VMEbus Request Interrupts 7 through 1 can be mapped to any of the Tsi148's PCI interrupt outputs. The VMEbus interrupt request signals are monitored by the Tsi148's VMEbus interrupt handler.

Recommended Termination:

- We recommend these signals be connected to the VMEbus through external buffers.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.35 IRQ[7:1]O

VMEbus Interrupt Request Out: 3.3V TTL, Output, 65 ohm

VMEbus Transmit Interrupts 7 through 1 are individually maskable. The VMEbus interrupt transmit signals are driven by the Tsi148's VMEbus interrupter.

Recommended Termination:

- None, these signals have an internal pull-downs. These signals can be connected to the VMEbus through external inverting open collector buffers.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.36 LWORD_

VMEbus Long Word: 3.3V TTL, Bi-direct, 35 ohm

This signal is used in conjunction with the two data strobes DS[1:0] and VA01 to indicate the number of bytes (1-4) in the current transfer. The LWORD_ signal is monitored by the Tsi148's VMEbus slave. The LWORD_ signal is driven by the Tsi148 when it is the VMEbus master. The LWORD_ signal is also used as a data signal during MBLT, 2eVME and 2eSST transfers.

Recommended Termination:

- None, this signal has an internal pull-up. This signal can be connected to the VMEbus through an external bi-directional buffer. LWORD_ should be included in the same buffer group as the VMEbus address signals.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.37 RETRYI_

VMEbus Retry In: 3.3V TTL, Input

This signal used in conjunction with BERR_ can be used to postpone a data transfer. The Tsi148's VMEbus master must then attempt the cycle again at a later time. The retry cycle can be useful in preventing deadlock situations. This signal is monitored by the Tsi148's VMEbus master.

Recommended Termination:

- None, this signal has an internal pull-up. This signal can be received from the VMEbus through an external buffer.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.38 RETRYO_

VMEbus Retry Out: 3.3V TTL, Output, 35 ohm

This signal used in conjunction with BERR_ can be used by the Tsi148's slave to postpone a data transfer. The external VMEbus master must then attempt the cycle again at a later time. The retry cycle can be useful in preventing deadlock situations. This signal is driven by the Tsi148's VMEbus slave.

Recommended Termination:

- None, this signal has an internal pull-up. This signal can be connected to the VMEbus through an external tri-state buffer.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.39 RETRYOE

VMEbus Retry Output Enable: 3.3V TTL, Output, 35 ohm

This signal used to enable the Retry driver.When the Tsi148 is driving RETRY_ on the VMEbus this signal is driven high; when the VMEbus is driving the Tsi148 this signal is driven low.

Recommended Termination:

- None, this signal has an internal pull-up.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.40 SCON

VMEbus System Controller: 3.3V TTL, Output, 65 ohm

This signal is asserted when the system controller function is enabled. This signal is used to enable the BCLR_ and SYSCLK drivers. When the Tsi148 wants to drive these lines on the VMEbus this signal is driven high; when the VMEbus is driving the Tsi148 this signal is driven low.

Recommended Termination:

- None, this signal has an internal pull-down.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.41 SCONDIS_

VMEbus System Controller Disable: 3.3V TTL, Input

This signal is a power-up option used in conjunction with SCONEN_L. When this signal is asserted and the SCONEN_ signal is negated, the Tsi148's system controller functions are disabled. When the SCONEN_ and SCONDIS_ signals are negated, the Auto SCON feature is enabled. The Auto System Controller feature uses the BG3IN_ signal to allow the board to determine if it is in bus slot 1. If the board is in bus slot 1 the BG3IN_ signal will be low and the SCON function will be enabled.

Recommended Termination:

- Although this signal has an internal pull-up, it may not be strong enough for specific applications. We recommend either a pull-up or pull-down on the board.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.42 SCONEN_

VMEbus System Controller Enable: 3.3V TTL, Input

This signal is a power-up option used in conjunction with SCONDIS_. When this signal is asserted and the SCONDIS_ signal is negated, the Tsi148's system controller functions are enabled. When the SCONEN_ and SCONDIS_ signals are negated, the Auto SCON feature is enabled. The Auto System Controller feature uses the BG3IN_ signal to allow the board to determine if it is in bus slot 1. If the board is in bus slot 1 the BG3IN_ signal will be low and the SCON function will be enabled.

Recommended Termination:

- Although this signal has an internal pull-up, it may not be strong enough for specific applications. We recommend either a pull-up or pull-down on the board.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.43 SFAILI_

VMEbus System Fail In: 5Vtlr TTL, Input

This signal is asserted by a VMEbus system to indicate some system failure. This signal is monitored by the Tsi148's interrupter logic. If enabled, an interrupt is generated on the falling edge of SFAILI_.

Recommended Termination:

- We recommend this signal be connected to the VMEbus through an external buffer.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.44 SFAILO

VMEbus System Fail In: 3.3V TTL, Output, 65 ohm

The VMEbus system fail signal is driven by the Tsi148 when the BDFAIL_ signal is asserted and the SFAILEN bit is set.

Recommended Termination:

- None, this signal has an internal pull-down. This signal can be connected to the VMEbus through an external inverting open collector buffer.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.45 SRSTI_

VMEbus System Reset In: 5Vtlr TTL, Input

The VMEbus system reset in signal is used to reset the Tsi148's VMEbus logic. It will also cause the LRSTO_ signal to be asserted which will cause a local bus reset. The VMEbus SYSRESET_ signal is connected to the SRSTI_ input signal. The SRSTI_ reset input will reset all Tsi148 logic which is sensitive to SYSRESET_.

Recommended Termination:

- We recommend this signal can be connected to the VMEbus through an external buffer.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.46 SRSTO

VMEbus System Reset Out: 3.3V TTL, Output, 65 ohm

The VMEbus System Reset Out is driven to reset the VMEbus. The Tsi148's SRSTO signal is normally connected to the VMEbus SYSRESET_ signal through an inverting open collector buffer. When the SRSTO signal is asserted, a VMEbus SYSRESET_ signal is generated.

Recommended Termination:

- None, this signal has an internal pull-down. This signal can be connected to the VMEbus through an external inverting open collector buffer.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.47 SYSCLK

VMEbus System Clock: 3.3V TTL, Output, 35 ohm

The VMEbus System Clock signal is driven by the Tsi148 when the system controller function is enabled. When the PCI/X frequency defined for a specific configuration is at it's maximum the SYSCLK is running at 16MHz.

Recommended Termination:

- None, this signal has an internal pull-up. This signal can be connected to the VMEbus through an external tri-state buffer.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.48 WRITE_

VMEbus Write: 3.3V TTL, Bi-direct, 35 ohm

The VMEbus Write signal indicates the direction of data transfer. The WRITE_ signal is monitored by the Tsi148's VMEbus slave. The WRITE_ signal is driven by the Tsi148 when the Tsi148 is the VMEbus master.

Recommended Termination:

- None, this signal has an internal pull-up. This signal can be connected to the VMEbus through an external bi-directional buffer. The WRITE_ signal should be included in the same buffer as the AM[5:0] and IACK_ signals.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.49 VA[31:1]

VME Address Bus: 3.3V TTL, Tri-state bi-directional, 35 ohm

The VMEbus address signals are monitored by the VMEbus slave, and driven by the VMEbus master. During MBLT, 2eVME and 2eSST transfers, the address lines are used to transfer data.

Recommended Termination:

- These signals have internal pull-ups. These signals are connected to the VMEbus through external bi-directional buffers.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.50 VD[31:0]

VME Data Bus: 3.3V TTL, Tri-state bi-directional, 35 ohm

The VMEbus data signals are used to receive data from the VMEbus during master read cycles and slave write cycles. The VMEbus data signals are driven by the Tsi148 to transmit data during master write cycles and slave read cycles. They are also used to transfer address information during A64 cycles.

Recommended Termination:

- These signals have internal pull-ups. These signals are connected to the VMEbus through external bi-directional buffers.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

Certain power-up configurations for the Tsi148 are obtained by transparently latching the states of the VME data bus signals VD[3:0] at power-up reset. The VMEbus data signals used are between the Tsi148 and the VMEbus buffers.

If your design is using the TI SN74VMEH22501/22501A buffers then 3.3kohm pull-up or pull-down resistors must be placed between the Tsi148 to overcome the bus hold circuitry in the VME buffer.

Refer to the Tsi148 *User Manual* for details on these power-up configurations.

1.4 PLL Signals

This section gives recommended terminations for the Tsi148 PLL signals.

1.4.1 PLL_OUTA

PLL Output: 1.8V Output, 65 ohm

Standard PLL output. This signal may be used to monitor the output of the phase-locked circuits for the PCI/X interface. During normal system operation, this output is in a high-impedance state and should be pulled down on the board.

Recommended Termination:

- Pull-down

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.4.2 PLL_RSTI_

PLL Reset In: 3.3V TTL, Input

This signal resets the Tsi148 PLL. The PLL_RSTI_ has to be asserted until the input clock and power are stable.

Recommended Termination:

- Although this signal has an internal pull-up, it may not be strong enough for specific applications, so a pull-up on the board is recommended as well.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.4.3 PLL_TEN

PLL Tune Enable: 3.3V TTL, Input

When this signal is high PLL_TUNE[9:0] bits are used to tune the PLL.

Recommended Termination:

- Although this signal has an internal pull-down, it may not be strong enough for specific applications, so a pull-down on the board is recommended as well.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.4.4 PLL_TUNE[9:0]

PLL Reset In: 3.3V TTL, Input

When the PLLTEN signal is asserted, these signals are used to tune the Tsi148's PLL. When the PLLTEN signal is negated, the PLL tune bits are internally controlled. The Tsi148's PLL should be internally tuned. IDT does not recommend adjusting these signals.

Recommended Termination:

- The PLL_TUNE[3:0] signals should be grounded on the board. These signals should have pull-up and pull-down resistors very close to the package ball. The pull-up should not be populated and the pull-down should be populated with a zero ohm resistor.
- The PLL_TUNE[9:4] signals should have pull-up and pull-down (1K) resistors placed on the board as well. Since IDT does not recommend tuning the PLL, the pull-up should be populated.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.5 Power Supply Signals

This section gives recommended terminations for the Tsi148 power supply signals.

1.5.1 PLL_VDD

Input Supply

1.8V Analog Vdd for PLL. This input provides clean power to the internal Analog Phase Locked Loop.

Recommended Termination:

- 1.8 V plus filtering

See “Tsi148 PLL Power/Ground Filter Recommendations” on page 46 for filtering recommendations.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.5.2 PLL_VSS

Input Supply

Analog Ground for PLL. This signal provides clean ground to the internal analog Phase Locked Loop.

Recommended Termination:

- Ground

See Section 1.7.1 for filtering recommendations.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.5.3 VDD18

Supply Inputs

The 1.8 V pins provide power for the internal core logic.

Recommended Termination:

- Nominally 1.8 V plus decoupling.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.5.4 VDD33

Supply Inputs

The 3.3 V pins provide power for the I/O buffers.

Recommended Termination:

- Nominally 3.3 V plus decoupling.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.5.5 VSS

Supply Inputs

These pins form the ground connections for all of the input macros, output macros, and core.

Recommended Termination:

- Ground

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.6 Miscellaneous Signals

This section gives recommended terminations for Tsi148 miscellaneous signals.

1.6.1 CEO_TEST

Factory Test: 1.8V, Input

This signal is used for factory test.

Recommended Termination:

- Although this signal has an internal pull-down, it may not be strong enough for specific applications, so a pull-down on the board is recommended as well.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.6.2 HWC_PFU

Float PCI Upper Signals: 3.3V TTL, Input

When the Tsi148 is configured in 32-bit PCI mode and this signal is low, the 64-bit extension signals are driven. When the Tsi148 is configured in 32-bit PCI mode and this signal is high, the 64-bit extension signals are tri-stated. When this signal is asserted it allows the user to test 32-bit capability if wired to a 64-bit bus without bus conflicts.

Recommended Termination:

- Although this signal has an internal pull-down, it may not be strong enough for specific applications, so a pull-down on the board is recommended as well.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.6.3 PCIPUEN

PCI Pull-up Enable: 3.3V TTL, Input

This signal controls whether internal pull-ups are enabled or disabled on all Tsi148 PCI/X signals. When this signal is asserted, the internal PCI/X bus pull-ups are enabled. When this signal is negated, the internal PCI/X pull-ups are disabled.

Recommended Termination:

- Although this signal has an internal pull-down, it may not be strong enough for specific applications, so a pull-down on the board is recommended as well.

All of the 3.3V PCI/X signals have an internal Pull-up on them enabled by PCIPUEN. IDT recommends the PCIPUEN pin to be pulled down on the board for PCI/X compliance.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.6.4 PCIMC

PCI Driver Mode Control: 3.3V TTL, Input

When this signal is asserted, the Tsi148's PCI drivers are configured with a 40 ohm impedance for point-to-point operation. When this signal is negated, the PCI drivers are configured with a 20 ohm impedance for multi-point operation.

Recommended Termination:

- This signal must be either pulled up or pulled down on the board (as described above).

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.6.5 JTAG Signals

As a precaution, the board designer must do their own analysis of the devices on the bus before implementing JTAG. For example, some devices may have signals with pull-ups where the Tsi148 has put-downs. This difference could cause signals to be pulled to an indeterminate logic level.

1.6.5.1 TCK

Test Clock (JTAG): 3.3V TTL, Input

Used to clock state information and test data into and out of the device during IEEE 1149.1 test operation.

Recommended Termination:

- If JTAG is used there is no termination required because this signal has an internal pull-down
- If JTAG is unused this signal can have a pull-up or pull-down

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.6.5.2 TDI

Test Data Input (JTAG): 3.3V TTL, Input

Used (in conjunction with TCK) to shift data and instructions into the Test Access Port (TAP) in a serial bit stream during IEEE 1149.1 test operation.

Recommended Termination:

- This signal has an internal pull-down. However, if boundary scan is not implemented we recommend a pull-down on the board as well.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.6.5.3 TDO

Test Data Output (JTAG): 3.3V TTL, Output, 65 ohm

Used (in conjunction with TCK) to shift data and instructions into the Test Access Port (TAP) in a serial bit stream during IEEE 1149.1 test operation.

Recommended Termination:

- None, this signal has an internal pull-down.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.6.5.4 TMS

Test Mode Select (JTAG): 3.3V TTL, Input

Used to control the state of the Test Access Port Controller during IEEE 1149.1 test operation.

Recommended Termination:

- This signal has an internal pull-down. However, if boundary scan is not implemented we recommend a pull-down on the board as well.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.6.5.5 TRST_

Test Reset (JTAG): Input (5V tolerant)

Used to force the Test Access Port (TAP) into an initialized state. This signal provides an asynchronous initialization of the IEEE 1149.1 compliant TAP controller.

Recommended Termination:

- This signal has an internal pull-down. However, if boundary scan is not implemented we recommend a pull-down on the board as well.
- If boundary scan is implemented, the TRST_ input must be asserted low at the negation of the PURSTI_ input and then held high during boundary scan testing.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.6.5.6 TM_IN

Temperature Monitor In:

This signal is used to measure the die temperature. It is used for test purposes only and not intended for use in an application.

Recommended Termination:

- None

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.6.5.7 TM_OUT

Temperature Monitor Out:

This signal is used to measure the die temperature. It is used for test purposes only and not intended for use in an application.

Recommended Termination:

- None

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.7 Tsi148 Typical Applications

Figure 1: Tsi148 Schematic - Tsi148 Device

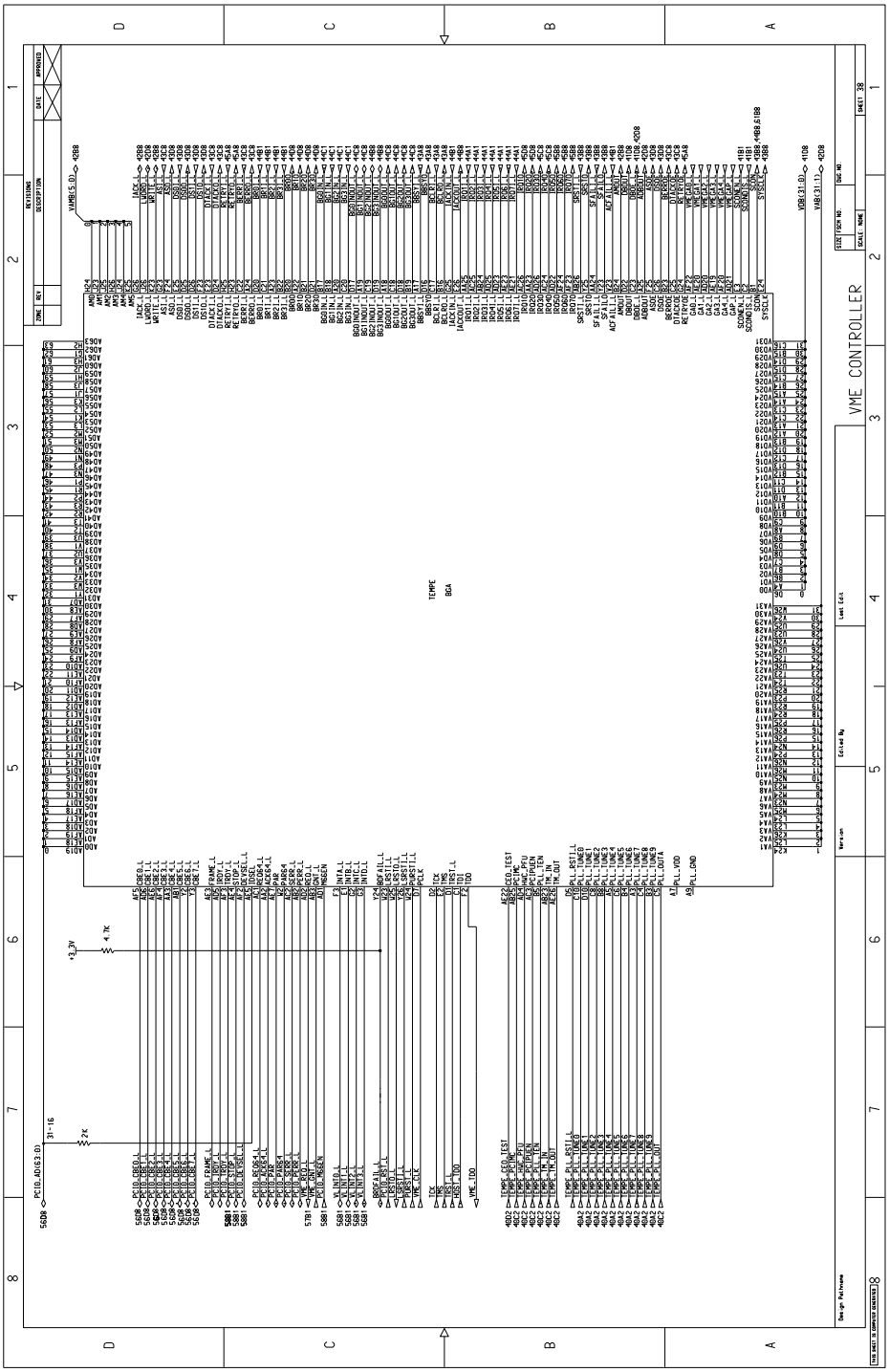


Figure 2: Tsi148 Schematic - Power Pins

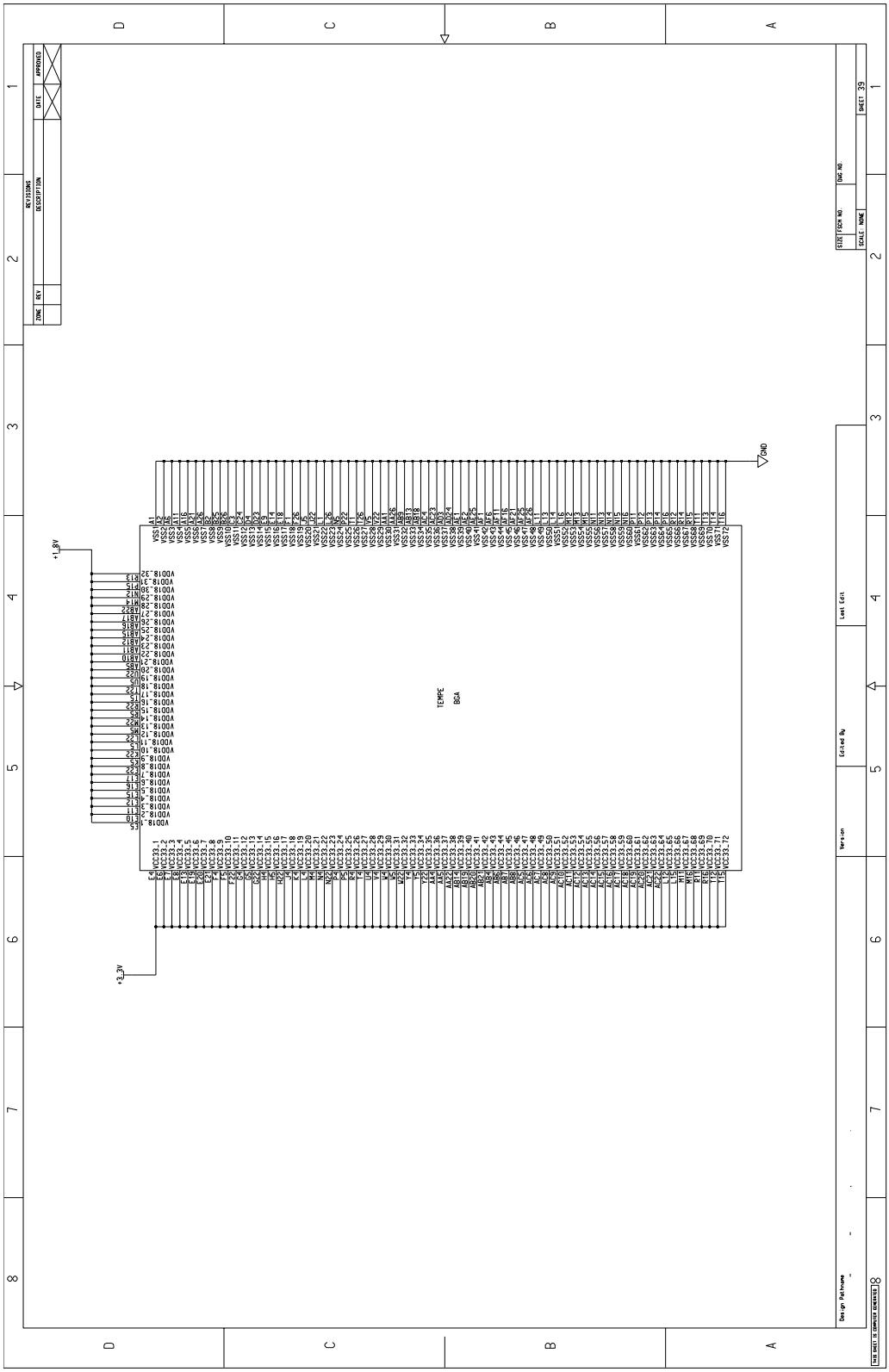
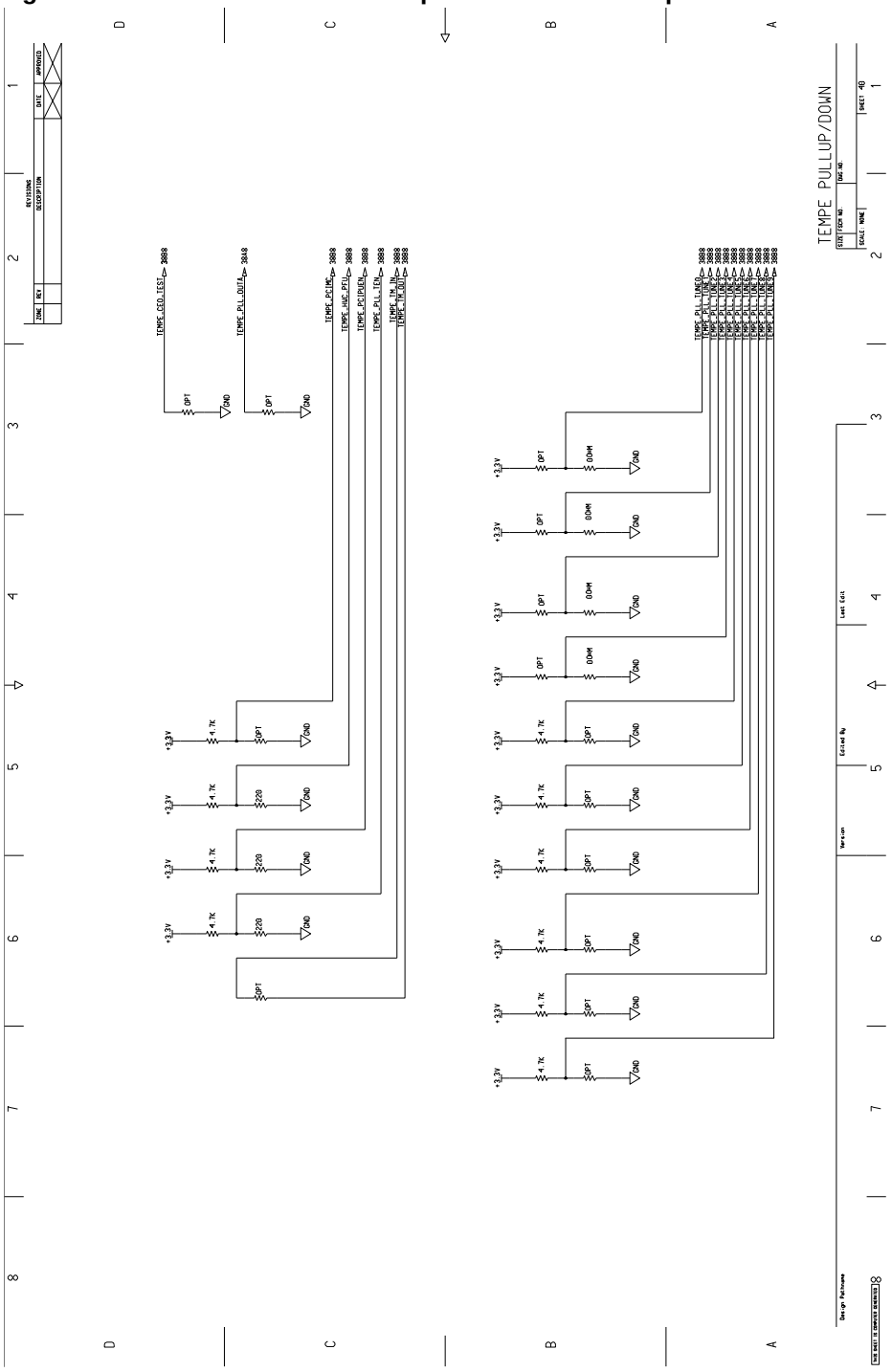


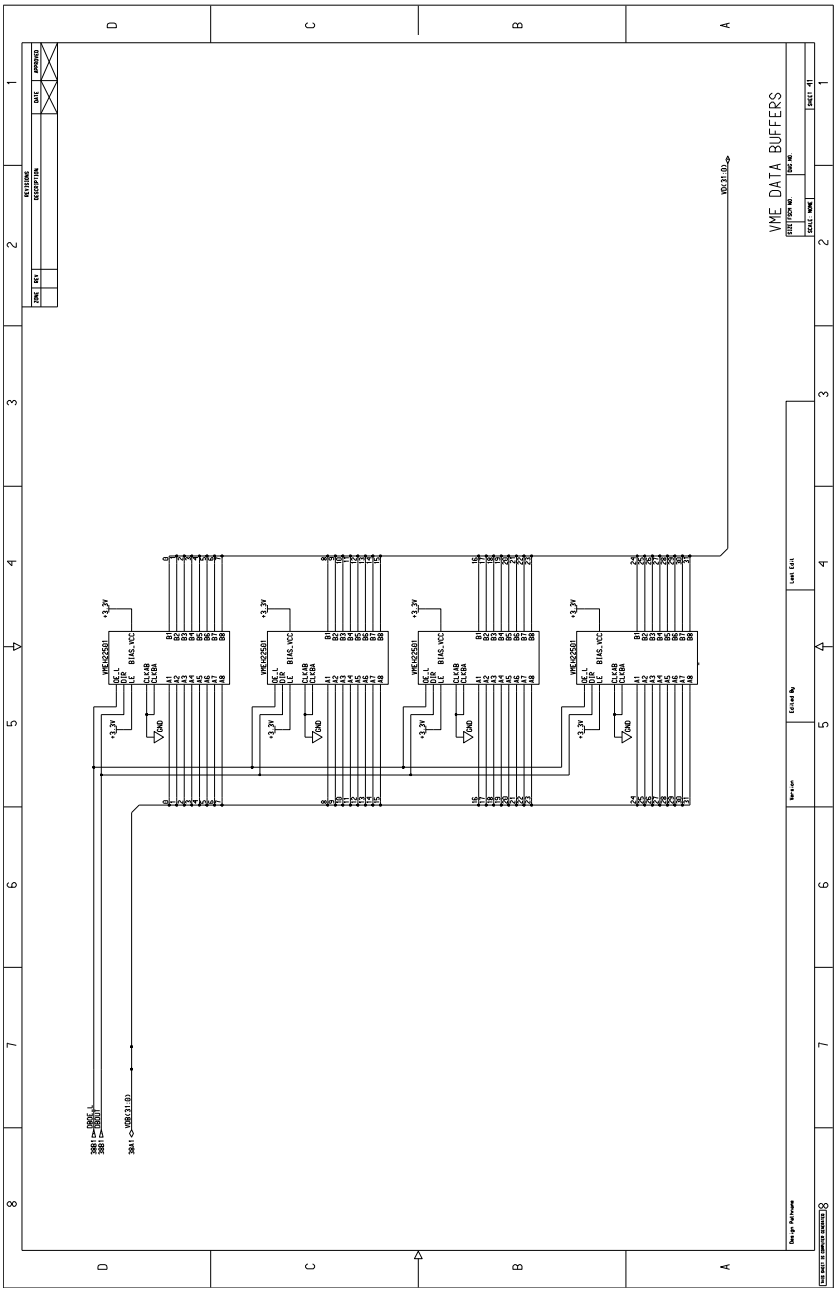
Figure 3: Tsi148 Schematic - Pull-up and Pull-down Requirements



PLL_TUNE[0:3] should be connected to a 0 ohm resistor to ground.

Information in Figure 3 is board dependent. Some boards may not require the pull-up resistors detailed in this schematic.

Figure 4: Tsi148 Schematic - VME Data Buffers



IDT recommends using 3.3kohm pull-up or pull-down resistors to set the desired level on the VME power-up options on the VD[3:0] pins. This resistor value has been determined to work correctly with the bus hold circuitry on the TI SN74VMEH22501/22501A 3A port pins.

Figure 5: Tsi148 Schematic - VME Address Buffers

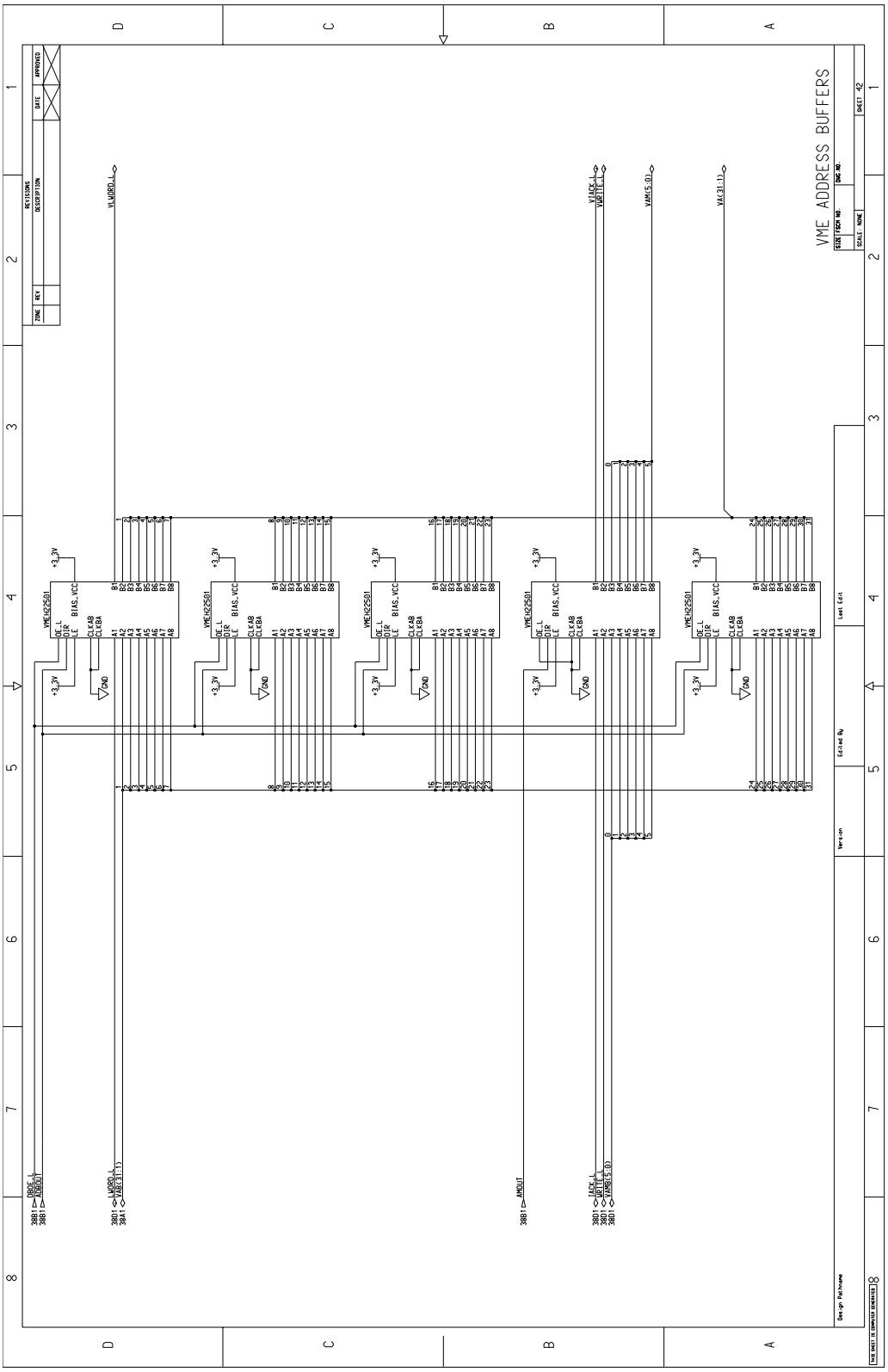


Figure 6: Tsi148 Schematic - VME Control Buffers

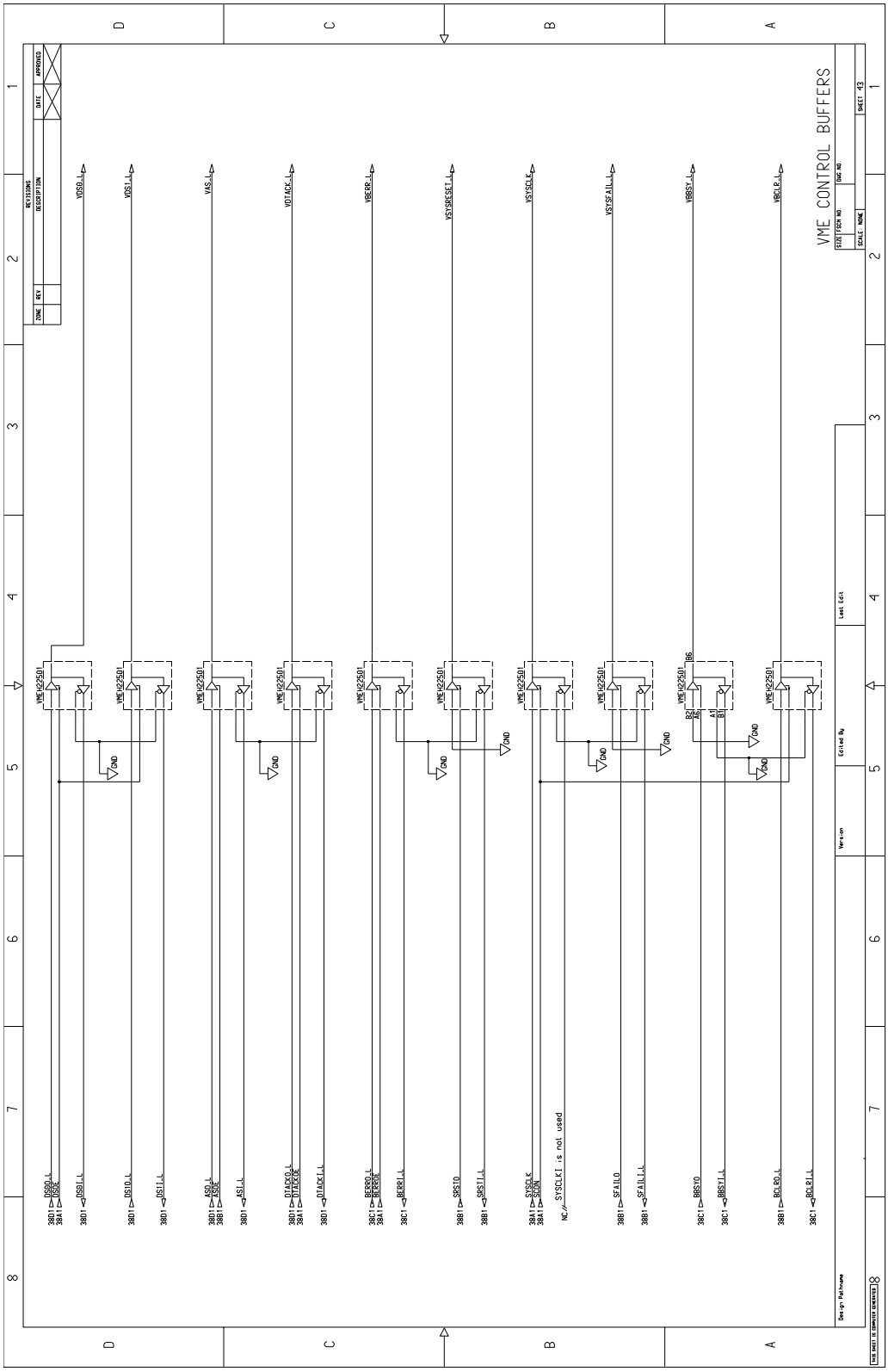


Figure 7: Tsi148 Schematic - VME Transceivers

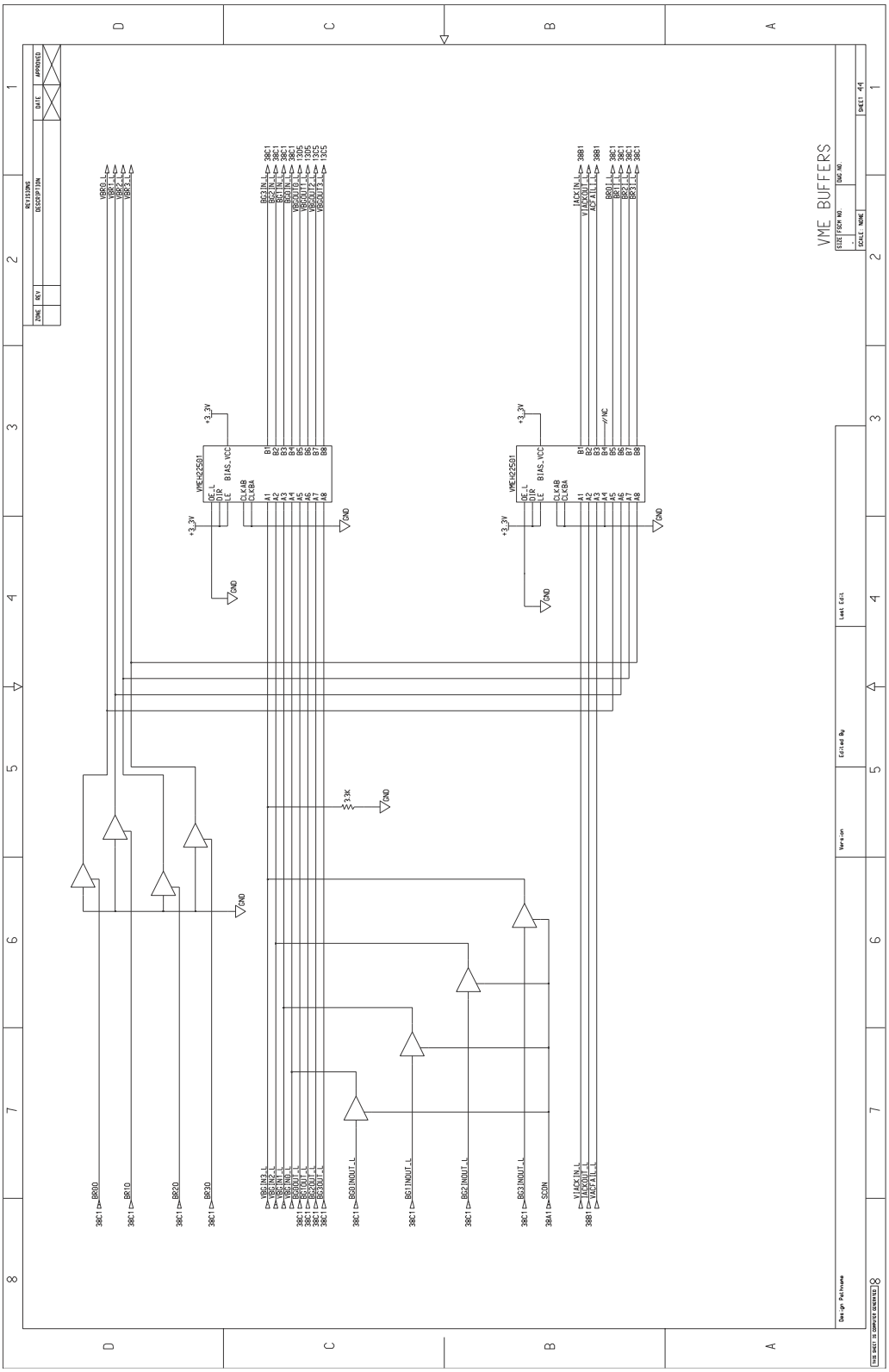


Figure 8: Tsi148 Schematic - VME Transceivers

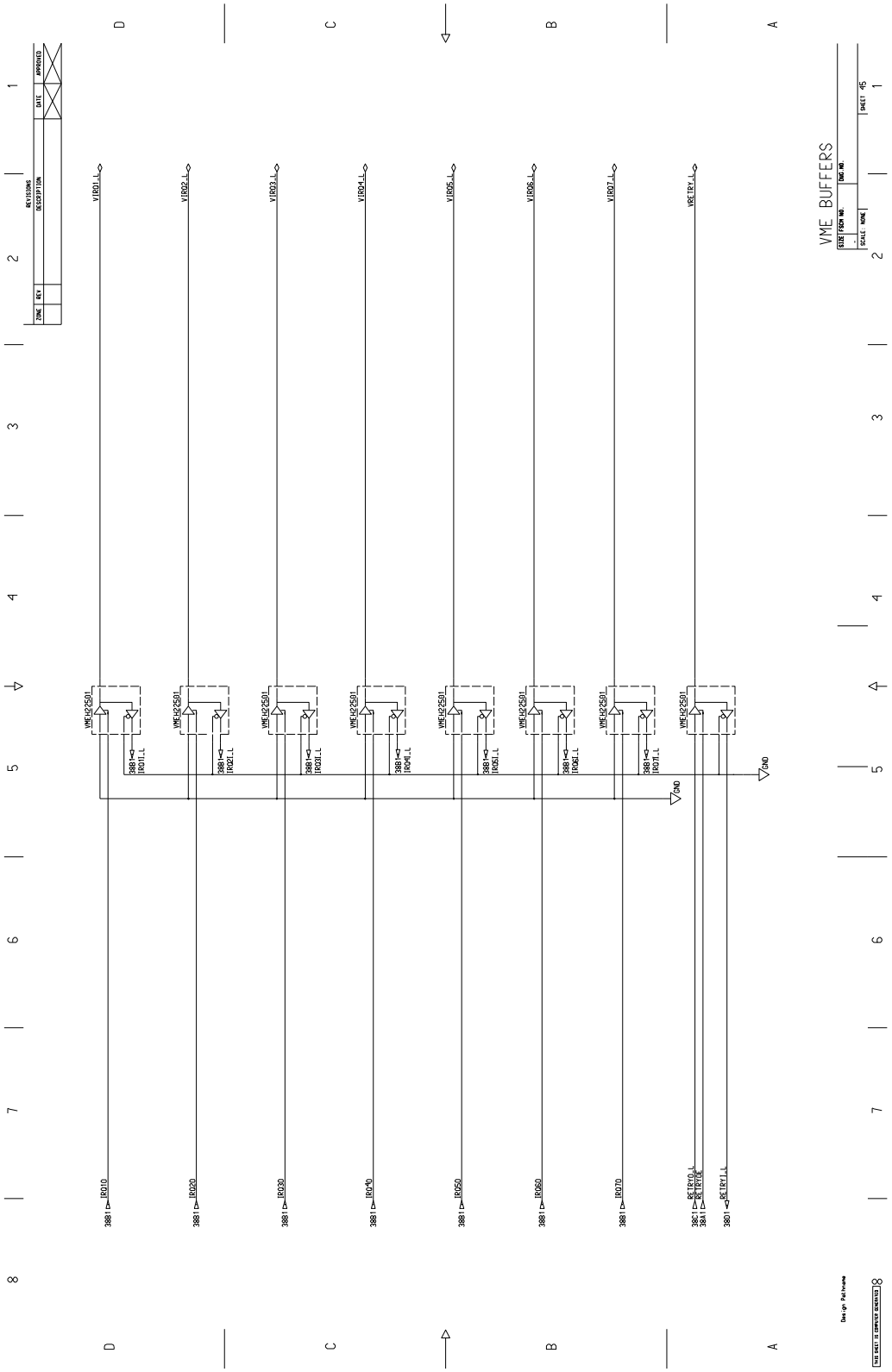


Figure 9: Tsi148 Schematic - PCI Bus 0.0 and 1.0 Pull-ups

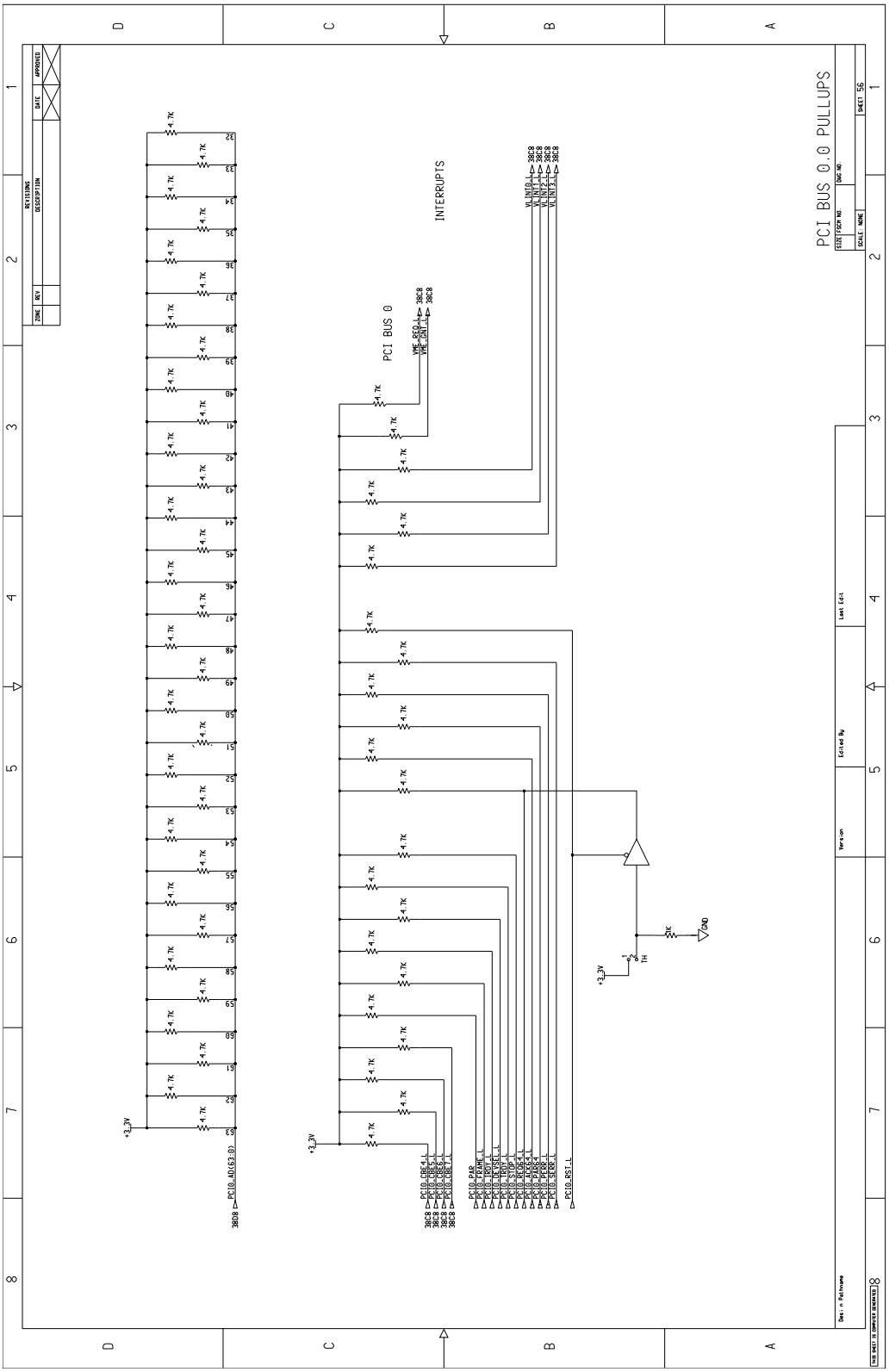
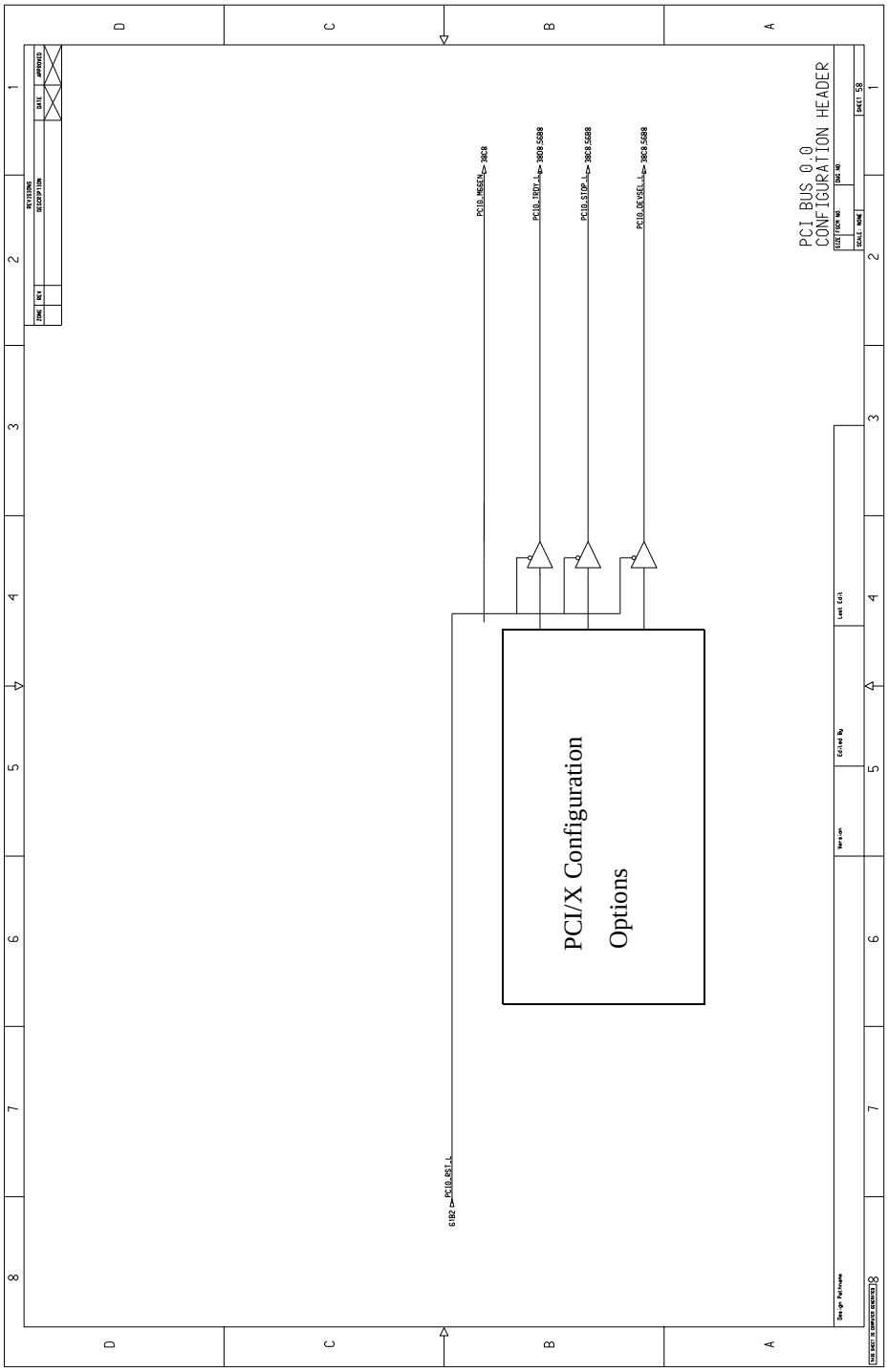


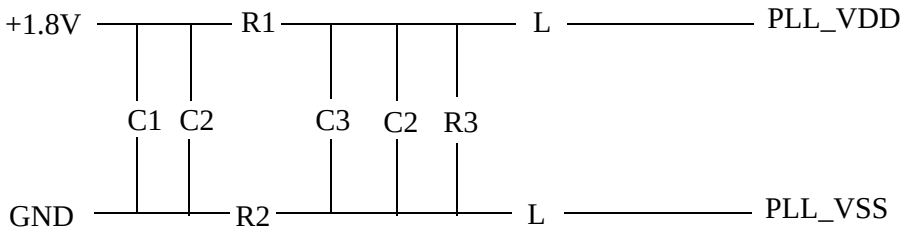
Figure 10: Tsi148 Schematic - PCI Bus 0.0 Configuration Header



1.7.1 Tsi148 PLL Power/Ground Filter Recommendations

Figure 11 shows the recommended power and ground filter for the Tsi148 PLL.

Figure 11: PLL Power/Ground Filter Requirements for Tsi148



The following values should be used for the Tsi148:

- R1 = 2.2 ohm
- R2 = 2.2 ohm
- R3 = not installed
- L = 820 nH
- C1 = 2.2 uF
- C2 = 0.1 uF
- C3 = 10 uF

1.8 Recommended Reading

1. *PCI-X System Architecture*

   (Tom Shanley, Don Anderson) Mindshare Inc. ISBN 0-201-72682-3

2. *PCI System Architecture, 4th edition*

   (Tom Shanley, Don Anderson) Mindshare Inc. ISBN 0-201-30974-2

3. *PCI Local Bus Specification Rev. 2.2*

   (Available from www.pcisig.com)

4. *PCI-X Specification Rev 1.0b*

   (Available from www.pcisig.com)

5. *American National Standard for VME64*

   (Available from www.vita.com)

6. *American National Standard for VME64 Extensions*

   (Available from www.vita.com)

7. *VITA 1.5-2003 2eSST Specification*

   (Available from www.vita.com)

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