International Journal of Production Research

Publication details, including instructions for authors and subscription information:
http://www.tandfonline.com/loi/tprs20

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Version of record first published: 22 Feb 2007.

To cite this article: N. Kumar, K. Kennedy, K. Gildersleeve, R. Abelson, C. M. Mastrangelo & D. C. Montgomery (2006): A review of yield modelling techniques for semiconductor manufacturing, International Journal of Production Research, 44:23, 5019-5036

To link to this article: http://dx.doi.org/10.1080/00207540600596874

International Journal of Production Research,
Vol. 44, No. 23, 1 December 2006, 5019–5036

Review article

A review of yield modelling techniques for semiconductor manufacturing

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(*Revision received January 2006*)

Semiconductor manufacturing is a complex multistage manufacturing process, and wafer fabs use complex processes involving billions of dollars worth of equipment to produce integrated circuits. The level of complexities associated with an integrated circuit is increasing in terms of feature size and number of devices. Companies use several performance metrics such as defectiveness, yield, and cycle time to improve manufacturing performance. Maintaining high yield through reliable and accurate quality control measures is one of the key performance criteria used by companies. The intent of this paper is to provide a review of the literature dealing with critical aspects of yield modelling. A review of many topics from simple probabilistic yield models to the incorporation of critical features such as spatial defects and radial yield losses will be provided. We will also assess empirical techniques used to model variations associated with complex interrelated wafer manufacturing processes. We emphasize that yield modelling should not be considered in isolation and system-wide aspects are necessary for integrated yield modelling and analysis.

Keywords: Yield modelling; Semiconductor manufacturing

1. Introduction

Semiconductor manufacturing is a complex multistage manufacturing process and requires monitoring a number of inter-related critical process parameters from the initial stages of production to the packaging of final product (Chung and Sang 2000). The wafer fabs use complex processes involving billions of dollars worth of equipment. With rapid advances in technology, semiconductor manufacturing companies strive to achieve defect-free products by adopting sophisticated manufacturing technology and thereby lowering defect densities. Performance metrics such as line yields, normalized defect rates, equipment utilization, cycle time, and on-time delivery are used to improve manufacturing performance

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International Journal of Production Research
ISSN 0020–7543 print/ISSN 1366–588X online © 2006 Taylor & Francis
http://www.tandf.co.uk/journals
DOI: 10.1080/00207540600596874

(Leachman 1993). Although it is difficult to achieve defect free products using state-of-the-art technology and maintaining the best performance metrics (Koren and Koren 1998), it is important to identify and measure critical process parameters, to understand the interrelationships among them, and to model their impact on the final product quality and performance measures.

Yield is a widely used performance metric in semiconductor manufacturing. Improving yield significantly reduces manufacturing cycle time (Gardner *et al*. 2000), improves product quality, facilitates timely product delivery (Radojcic and Rencher 2000) and helps in making decisions about yield targets for new processes. Therefore, maintaining high yield through reliable and accurate quality control is a key performance measurement. However, it is a challenging task to quantify and model yield due to the huge amount of data generated as well as the complicated processes associated with semiconductor manufacturing. The large amount of data makes data acquisition, management and analysis a very exhaustive and challenging task (Tobin and Karnowski 2000). In addition, there are hundreds of critical process parameters, and it is a challenging task to determine the patterns and relationships that exist among the parameters. Stapper (1989) provides a comprehensive review of yield modelling techniques. The yield models reviewed are developed from the standpoint of product design and hence are useful to product designers. Critical parameters related to wafer design and chip architecture are very well considered in these models. This paper emphasizes the need to develop integrated yield models from the operational modelling viewpoint, i.e. models which account for the fluctuating nature of the manufacturing processes. In our view, the state-of-the-art yield modelling techniques are equally important from an operational modelling viewpoint.

The intent of this paper is to provide a review of the literature dealing with critical aspects of yield modelling. Yield models were developed in the 1960s and have been growing in complexity due to the incorporation of different types of process variability. In this paper, we will provide a review of many topics from simple probabilistic yield models to the incorporation of critical features such as spatial defects and radial yield losses. We will also assess empirical techniques used to model variations associated with complex interrelated wafer manufacturing processes. Due to the complicated nature of semiconductor manufacturing, yield modelling should not be considered in isolation. The system-wide aspects necessary for integrated yield modelling and analysis will also be evaluated.

This paper is organized as follows: section 2 provides a brief overview of the semiconductor manufacturing processes. Section 3 emphasizes the significance of yield modelling techniques in terms of technical and economic growth. Section 4 introduces the concept of yield followed by a review of yield-modelling techniques useful from product design viewpoint. Section 5 emphasizes the need to characterize variability in yield modelling. Different approaches to characterize variations are discussed in this section. Section 6 provides a discussion of screening methodologies and techniques used for capturing and modelling defects affecting yield. Section 7 provides a detailed review of process modelling techniques used for modelling complex manufacturing processes. Section 8 emphasizes on integrated yield modelling using system approach to interconnect different levels associated with semiconductor manufacturing hierarchy, followed by conclusion in section 9.

Figure 1. Operations sequence required on wafers (Chung and Sang 2000).

2. Overview of semiconductor manufacturing processes

Before covering the various aspects of yield modelling in detail, a brief overview of semiconductor manufacturing processes is provided. Semiconductor manufacturing processes can be broadly classified into four basic processes (Chen *et al*. 1988): wafer fabrication, wafer probe, assembly or packaging and functional test and burn-in.

The basic processing unit is called a wafer, which is a disk of silicon. Wafers are produced in a facility known as wafer fab or fab. In the fab, wafers are processed and different layers and patterns of metals are constructed on them. Figure 1 shows a typical operations sequence required on wafers in a fab (Chung and Sang 2000). This sequence of operations is repeated for each layer of circuit on the wafer. There are many critical process parameters associated in a wafer fabrication process, and these critical process parameters tend to be very dynamic in nature due to the variability associated with the complex nature of the processes.

Wafer probe, also known as wafer sort, provides key information about the performance of the wafer fabrication process. It involves testing of individual die for functionality using different electrical probes. Bin code numbers are assigned to wafers based on the output of the test; in particular, wafers with defective die are assigned a bin code number as per the specification of defect type (Quirk and Serda 2001: 556). Following wafer probe/wafer sort, the wafers are cut into individual die. Functional die are connected to leads and placed in ceramic shells known as packages. Packaged chips are then sent for final functional test and burn-in. Refer to Quirk and Serda (2001), Van Zant (2004), and Wolf (2003) for a more detailed description of different manufacturing processes associated with wafer manufacturing.

3. Significance of yield modelling

In today's rapidly changing technological environment, formulating a model to predict yield is equally as important as measuring and monitoring yield. An accurate model helps in understanding the deviation between planned and actual yield and can also help in making recommendations for potential improvements in the entire wafer production process (Peikert *et al*. 1998). Actual yield can be compared to predicted yield and corrective actions can be taken to correct a process producing wafers with low yield (Cunningham 1990). New products are launched in a fairly short period of time due to intense competition among leading semiconductor manufacturing companies, and yield losses dominate the early stages of production due to variations associated with the processes. Therefore, it becomes a challenging task to monitor and predict yield accurately for new products at early stages of products. For established products, it is easier to predict yield with a high degree of certainty (Horton 1998).

Processes used in semiconductor wafer processing are usually very dynamic and short in duration. If one process goes out of control, very soon many non-conforming wafers will be produced, thereby lowering the final yield significantly. An accurate yield prediction model would serve as an alert for proactive measures; thereby preventing the production of non-conforming wafers before a malfunction is detected in the process.

An accurate yield prediction model also helps in estimating and readjusting the burn-in time of the final product. For example, if the yield predicted by the model is very high then a short testing time of a specific semiconductor process can be set. On the other hand, if the predicted yield is determined to be very low, then the burn-in time can be set for longer duration.

Yield models are a tool for making more accurate yield projections (Balasubramaniam *et al*. 1997). Moreover, accurate yield models help in predicting the manufacturing cost of a product still under development (Cunningham 1990). Various cross-functional departments such as production control and material management can manage their resources more accurately. In certain cases, it is difficult to maintain expected delivery date due to inevitable process variations. Delivering products as per the agreed due date is a critical business performance measure for customer satisfaction and in surviving today's highly competitive semiconductor industry. Meeting due dates can be greatly assisted with the use of an accurate yield prediction model.

Effective yield management also plays an important role in establishing a partnership between wafer foundries and fabs. The very first step in writing a contract between the partners includes detailed study, estimation and prediction of yield, and Chatterjee *et al*. (1997) provide models to quantify the benefits related to having a good yield improvement system.

Yield modelling also requires modelling of the processes involving complex design features, equipment characteristics and human learning. In semiconductor wafer manufacturing, product and process specifications change at an unprecedented rate. Therefore, predicting yield with high degree of certainty becomes a challenging task and depends heavily on the accuracy of yield modelling and process specification methods. It is important to consider significant microscopic design features that affect yield and are critical in wafer manufacturing while developing a yield model. Various yield models covering critical design features are available and vary in complexity. For example, yield models to model die yields are based on Poisson statistics or the generalized negative binomial distribution, which accommodate effects such as defect clustering.

In the next section, we will review yield models starting from the elementary level to the one with increasing level of complexities.

4. Yield modelling

As previously mentioned, yield is one of the most important performance indices. In general terms, it is defined as the fraction of total input transformed into shippable output. In a typical semiconductor manufacturing environment, variability is associated with the wafer as well as the die level, with additional variability associated with the wafer-die interaction. Semiconductor industries use yield as

a performance metric at different stages of processing to evaluate their process performances at different levels of hierarchy such as wafer, die, or package level (Uzsoy *et al*. 1992). Typically, the yield of a semiconductor manufacturing component is divided into three categories: line yield, wafer sort yield, and final test yield. The total yield of a process is the product of these yields (Cunningham *et al*. 1995). The first two types, i.e. line and wafer sort yields, are used as major product cost determining factors (Cunningham 1990). Accurate modelling and prediction of these two yields facilitate high yield at the final stage and saves money and resources. However, ignoring line and wafer yields significantly affects packaging yield and may prove very costly to the companies. For example, 1% assembly yield losses for the Intel Pentium microprocessor cost $42 million annually (Thompson 1996). Therefore efforts should be focused on improving line and die yields.

4.1 *Line yield*

Line yield, synonymous with wafer yield and process yield, is used to measure the performance of wafer fabs. It is defined as the fraction of wafers reaching the wafer-level electrical test in wafer fabrication process. Losses at line yield occur due to factors such as wafer breakage and faulty processing. Horton (1998) defined line yield as a fraction of unprocessed wafers into processed wafers reaching the final electrical test in a wafer fab. Horton's definition of line yield does not consider the varying nature of in-process inventory or work in process (WIP). Cunningham (1990) incorporated the effects of WIP on the line yield:

$$Y_{\text{line}} = \frac{\text{wafers out rate} - \text{change from normal out rate}}{\text{wafers start rate} - \text{change from normal start rate}} \tag{1}$$

where normal or expected start rate and out rate can be calculated as:

$$\text{Normal out rate} = (\text{WIP}) \times \left(1 + Y_{\text{lineavg}}\right)/(\text{cycle time})$$
$$\text{Normal start rate} = (\text{WIP})\left(1 + Y_{\text{lineavg}}\right)/(\text{cycle time})\ Y_{\text{lineavg}}$$

Parameter Y_{lineavg} is simply the best average line yield available at the time. The cycle time, in days, can be estimated by dividing the total yielded line inventory or WIP by the average, daily, ship rate of wafers.

Cunningham (1990) also accounted for the effect of rework in his line yield computational formula:

$$Y_{\text{line}} = \left[\frac{\text{Total wafer moves in the line}}{\text{moves} + \text{scrap or discarded wafers} - \text{reworked wafers}}\right]^n \tag{2}$$

where n is the number of process steps of a wafer.

There are many advantages cited in the literature about considering line yield in wafer manufacturing (Peikert *et al*. 1998). Directing resources to analyse line yield is useful as problems at an early stages in wafer manufacturing require less effort and resources to detect and resolve.

4.2 *Die yield*

The wafer sort process involves testing of individual die using different electrical probes. Because the wafer sort process follows the wafer fabrication process, high yield on wafer sort reflects the stability and efficiency of wafer fabrication process indirectly. Die yield, also known as wafer sort yield, probe yield, or chip yield, is defined as the fraction of dice on yielding wafers that are not discarded in a wafer probe test.

Losses due to die yield can be classified into two categories: functional yield loss and parametric yield loss (Cunningham *et al*. 1995). A die is lost with respect to functional yield if it fails to perform its intended function. The functional yield loss may occur due to defects such as open or short circuits, scratches, contamination, etc. On the other hand, parametric yield loss occurs when a die performs its functions but does not meet the specifications. Examples of parametric yield losses include factors such as lower frequency and low speed.

4.3 *Yield modelling techniques*

Stapper (1989) provided a comprehensive review of probabilistic wafer sort yield models. However, in this review article, we provide a brief review of some of the commonly used yield models described in the literature.

4.3.1 Poisson model. According to the Poisson yield model:

$$Y_{\text{wafer sort}} = \exp(-A_{\text{die}} \times D) \tag{3}$$

where $Y_{\text{wafer sort}}$ is the wafer sort yield, D the defect density, and A_{die} the die surface area (a ratio of total device area to chip area).

The Poisson model assumes that the defect density across wafers remains constant. Also, it is assumed that defects are uniformly distributed over the entire wafer area and that a defect will affect wafer sort yield irrespective of its location on the wafer (Murphy 1964). However, yield is affected by the generation of defects on the critical areas. The critical area is defined as the area on a die where a defect, if it occurs, produces a short and causes functional yield losses (Nurani *et al*. 1998). The limitation of the early-developed Poisson model is that it considers die surface area but does not incorporate the effect of critical areas on yield losses.

4.3.2 Stapper model. Extending Poisson yield model theory, Stapper (1976) proposed computing partial wafer sort yield for each defect category using the critical area of die. Partial wafer sort yield for defect of nth category ($Y_{\text{partial wafer sort},\,n}$) is given by:

$$Y_{\text{partial wafer sort},n} = \exp(-A_{\text{die},n} \times D_n) \tag{4}$$

where D_n is the defect density for nth type of defect, and $A_{\text{die},\,n}$ the die critical surface area for nth type of defect.

Total wafer sort yield (functional yield) for all layers (N) on a die can be computed as follows:

$$Y_{\text{wafer sort}} = \prod_{n=1}^{N} Y_{\text{partial wafer sort},n} \tag{5}$$

4.3.3 Murphy's yield model. Murphy (1964) proposed a yield model in which he considered defect density D to be a random variable and assumed that the defect densities vary across die, wafers and lots. A yield model was developed as a function of defect density, in which he proposed summing defect density over die and wafer using an appropriate defect density distribution function:

$$Y = \int_0^{\infty} \exp(-DA) f(D)\, dD \tag{6}$$

where $f(D)$ describes the distribution of defect density.

The above formula was used as a base for deriving yield models for defects of different distributions. The expression could not be integrated for the Gaussian distribution; therefore Murphy used the triangular distribution as an approximation and obtained:

$$Y = \left[\frac{\left(1 - e^{-D_0 A}\right)}{D_0 A}\right]^2 \tag{7}$$

4.3.4 Seeds's yield model. Like Murphy's model, Seeds (1967) assumed that the defect densities vary across wafers and from wafer to wafer. He used the exponential distribution to estimate the defect density function $f(D)$: $f(D) = [(\exp(-D/D_0))/D_0]$. Substituting density distribution function $f(D)$ in the yield formula gives

$$Y = \frac{1}{(1 + D_0 A)} \tag{8}$$

where D_0 is average number of defects per unit area and A is critical area.

4.3.5 Price's yield model. Price (1970) used Seed's yield model for proposing a generic yield model, which took into account defect densities at different processing steps:

$$Y = \prod_{n=1}^{N} (1 + D_n \times A) - 1 \tag{9}$$

where D_n is the defect density per process step as wafers pass through the line.

4.3.6 Okabe's model. Okabe *et al.* (1972) proposed a yield model in which a number of different processing steps were taken into account while developing

the model. It was assumed that critical areas and defect densities are the same for all layers:

$$Y = \frac{1}{(1 + D_0 A/n)^n} \tag{10}$$

where D_0 is average number of defects per unit area and n is a number of processing steps.

4.3.7 Negative binomial yield model The negative binomial distribution is commonly used when the number of successes is fixed and we are interested in the failure probabilities for different numbers of faults/die before reaching the fixed number of successes.

$$Y = \frac{1}{(1 + D_0 A/\alpha)^\alpha} \tag{11}$$

where Y represents the defect-limited yield, D_0 is the defect density, and α is a cluster parameter.

The cluster factor α represents the bunching or clustering of the failure causing defects on a die and is roughly proportional to the complexity of the process. It increases as the variance of the defect distribution decreases. Different statistical techniques to determine α are presented in Cunningham (1990). Horton (1998) pointed out the shortcomings of negative binomial yield model for yield prediction when applied to devices that contain a mixture of different types of circuitry. He proposed a method for predicting die yield in a piecewise manner that takes into consideration a mixture of circuitry, different geometries, and unused area.

The yield modelling techniques described in this section are very useful from the product design viewpoint. These models are probabilistic in nature and help designers understand circuit design parameters such as critical die area, defect density, and number of layers in order to produce the optimal product yield. However, it should be kept in mind that even with the best designed product, it is difficult to obtain the expected yield results unless the processes producing the products are in control or exhibit minimal variability. The yield models mentioned in this section do not offer any potential to characterize variation and incorporate the effect of process parameters and variability onto yield.

5. Characterizing variation in yield modelling

One of the challenges associated with semiconductor yield modelling is to account for variation and its possible sources. Variability is generally classified into two categories: systematic and random. It is important to separate systematic and random causes of variation in order to have a clear understanding of possible sources of variations. Wong (1996) proposed a methodology to identify systematic and random components of yield loss. Systematic yield is modelled using statistical correlation analysis and multiple regression modelling techniques. A function is generated for the response and input variables considering all significant electrical test parameters that are identified by the statistical correlation analysis.

Probe yield wafer maps, electrical test data, process defect monitoring data, and product design databases are used in the analysis. Lee *et al*. (1995a) described a defect signature analysis technique to identify random and systematic defects in a manufacturing line.

In variation analysis, it is important to understand the effect of variation on the performance of critical parameters in wafer manufacturing. Covariance between the wafer and die is of clear concern for the process control. Any process modifications made in an attempt to improve or control the wafer level variation may also have an unintentional effect on the die-level pattern dependencies. Therefore, an interaction between wafer and die can correspond to a perturbation in the die pattern as a function of position on the wafer. Boning *et al*. (1997) decomposed the overall variation into wafer, die, and wafer-die interaction levels. Wafer level variation represents variation of critical parameters across wafers. Die level variation represents variation associated with critical quality characteristics on different die on each wafer. An additive model is used in which variation at the three levels of wafer, die, and wafer-die interaction are summed up to represent the overall systematic variation.

Boning and Chung (1998) proposed a systematic approach to measure and model process variation. In figure 2, a five-stage methodology consisting of variation identification methods, variation modelling, semi-physical model calibration, circuit

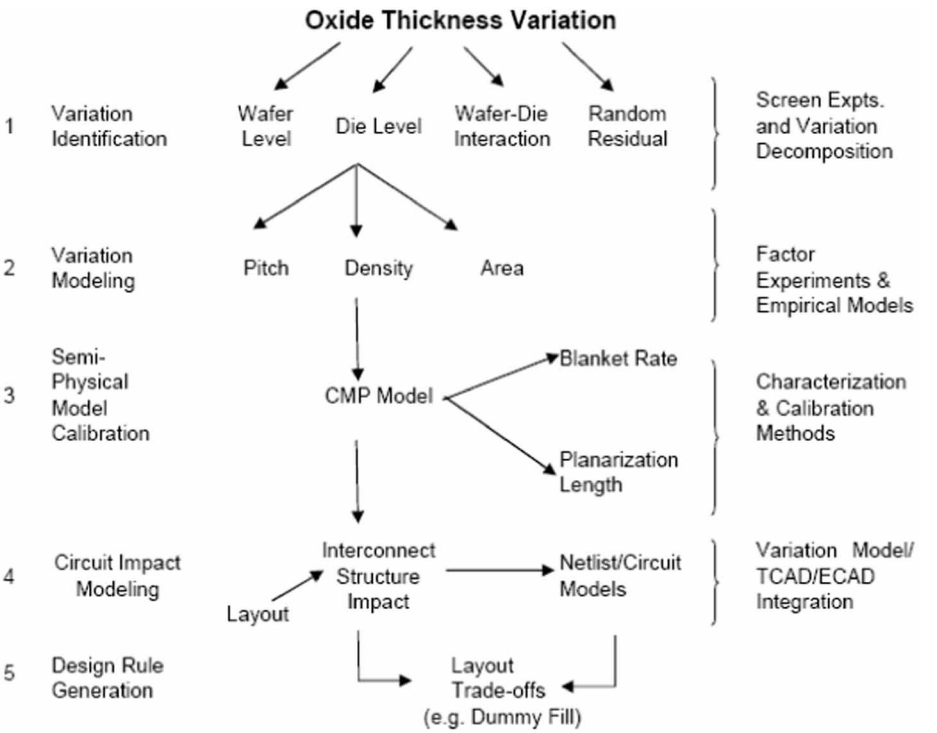

Figure 2. A five-step variation measurement and modelling approach (Boning and Chung 1998).

impact modelling, and design rule generation has been developed. In variation decomposition methods, it is proposed to use hierarchical models where residuals from one estimate become the input for the next estimation.

Due to the complex nature of semiconductor manufacturing, it is a challenging task to identify the critical parameters affecting wafer sort yield. Design features such as wafer diameter, die size, number of processing steps, and feature size affect wafer sort yield. With large wafer diameters, small numbers of die are near the edges and are likely to be non-functional, while the majority of die are away from the edges and are more likely to be functional. Wafer sort yield also shows a downward trend as number of processing steps increases. One of the possible causes is that the chance of wafer contamination increases as number of processing steps increases. A review of different modelling techniques accounting for critical parameters affecting wafer sort yield will be presented in the next sections.

6. Chip screening methods and yield modelling approaches

Yield is affected by the generation of defects on the critical areas. Critical area analysis is used to quantify the sensitivity of a design to defects based on the layout. The critical area is calculated by defect type and size. According to Wong (1996), a defect is defined as any extra or missing material caused by any unwanted particle or droplet of liquid that falls on the wafer during processing. Defects that result in yield loss are called fatal defects or faults. Examining the defect variation on wafer provides insight into the possible causes of defective chips. Mallory *et al*. (1983) used graphical presentations to model the spatial distributions in order to identify the location of killer defects. Longtin *et al*. (1996) incorporated a Markov random field model to capture spatial clustering effects of failed chips. Also, different screening strategies were proposed to capture factors affecting yields such as radial effects, and variation by chip locations. Harvey *et al*. (2005) provided a review of spatial modelling techniques. Spatially homogenous Bernoulli process (SHBP) and Markov random field (MRF) techniques were used to analyse the spatial relationship between chips on the wafer.

Radial yield loss is responsible for a higher probability of failure for die closer to the edge of a wafer. With an increase in wafer size, the effect of radial yield loss becomes more prominent as more defects are generated near the border of the wafer. Therefore, the radial yield degradation effect should be incorporated into the traditional yield models. Ferris-Prabhu *et al*. (1987) reported the effect of radial defects on the dropping yield at the periphery of wafer. Maynard *et al*. (1999) described modelling techniques to characterize and optimize the radial yield loss component of the wafer final test yield. Teets (1996) developed an expression for radial yield degradation as a function of chip size. Gupta *et al*. (1974) considered the effects of defects such as radial and angular defects for the optimal placement of chips on wafer to improve yield. Stapper and Rosner (1995) emphasized the role of circuit design and layout on yield analysis. Hess and Weiland (1999) proposed an algorithm using wafer maps and micro density distribution to predict yield.

The performance of yield models depends significantly on the defect size distributions as well as the spatial distribution of critical defects (Ferris-Prabhu 1992). Stapper (1985) proposed a Gamma distribution function as a compound

distribution function with negative binomial yield model to account for clustering behaviour in the defect distributions. Ferris-Prabhu (1992) proposed scaling rules with the simple Poisson model and compares its performance with the compound Poisson model. Murphy (1964) proposed a triangular distribution function as a compound distribution function to account for clustering behaviour. Stapper (1991) proposed a truncated Gaussian distribution function as a compound distribution function. Flack (1985) altered the negative binomial yield model and generated a defect distribution model to account for clustering effect. Gandemer *et al*. (1988) developed a circuit design to determine the critical area for each circuit layer, and a mixed Poisson statistic was used to fit the data. Walker (1987) used a simulation approach to calculate the yield after accounting particle size distribution and different layouts.

7. Process modelling techniques (including empirical modelling)

As semiconductor technology becomes more and more advanced, specifications on critical parameters become tighter. Statistical methods have been applied extensively on various semiconductor processes to analyse and monitor critical parameters associated with different processes and sub processes. These methods play a key role in the overall yield monitoring of semiconductor wafer manufacturing. Different techniques such as statistical process control (SPC), design of experiments, cluster analysis, and rule-based models are used to monitor the processes.

By the late 1980s and early 1990s, SPC had gained widespread usage as a means of monitoring critical process variables. Spanos (1992) provided an overview of application of SPC techniques such as $\overline{X}$-R chart, and cumulative sum of deviation chart in a semiconductor manufacturing. SPC techniques are useful in monitoring critical process parameters and help in the timely detection of a process shift. Control charts are primarily used to detect changes in the process mean, also known as excursion, caused by the generation of assignable sources of variation (Nurani *et al*. 1996). The implementation of SPC techniques resulted in improved process capability and subsequently improved yields. As wafer manufacturing processes involve simultaneous monitoring of several critical parameters, Spanos (1992) discussed the applications of advanced statistical techniques, such as Hotelling T^2 chart, regression chart, and time series analysis for multivariate data collected from sensors.

However, there are inherent limitations associated with the use of SPC. Semiconductor wafer manufacturing involves producing wafers in large quantities at a high manufacturing rate. Process shifts or excursions at a very high manufacturing rate require quick signals to ensure high product and process quality. If there is a significant time delay between the actual process shift and signal detected on the control chart, bad product may be produced which will lead to additional scrap and yield losses. Another limitation of applying SPC techniques in semiconductor manufacturing is that the critical process observations are typically dependent, non-stationary, auto-correlated and cross-correlated across the wafers due to dynamic nature of the processes. This type of observations behaviour may lead to excessive false alarms. Therefore, the direct observations, in the form of raw data from the processes, may not be used directly as input for standard Shewhart

control charts (Lee *et al*. 1995b). Therefore, the data needs to be transformed first. Also, using stand-alone SPC methods requires manual adjustments of the processes, which are dynamic in nature. Often the adjustments are not made quickly enough and the processes are often out-of-control more than they are in-control.

Guo *et al*. (1991) used a combination of multivariate statistical process control methods, Hotelling T^2 statistics and time series models, known as seasonal ARIMA, to compensate for non-stationary, auto-correlated, cross-correlated, and seasonal variation found in sensor data to control critical parameters in the plasma etching process.

Lee and Spanos (1995) reported developing empirical models using real-time data collected from sensors to predict critical parameters of wafers such as etch rate during and after the plasma processing stage. Techniques such as ordinary least squares regression (OLSR), principal component regression (PCR), partial least squares regression (PLSR), and feed forward error back propagation neural networks were used and compared while modelling the behaviour of critical parameters. Ordinary least squares regression was outperformed by the other techniques.

The wafer-manufacturing process involves hundreds or thousands of critical process parameters and their possible interactions. Design of experiments (DOE) is another statistical technique that can be used to monitor process parameters. Significant insight and engineering intuition can be developed about the processes using a DOE approach. However, application of DOE methodology becomes very time consuming as the number of experiments required increases rapidly with an increase in the number of process parameters included. This is demonstrated by the experiments, which took five years, to determine the causes of leakage in a specific process using DOE tools such as process comparison, split lot experiments, and failure analysis (Gardner *et al*. 2000).

Wang and Spanos (2001) used neural network modelling techniques to model the lithographic process. Cluster maps were used to identify critical parameters responsible for causing poor yield from normally collected wafer manufacturing data. In addition, rule-based induction methods were used to explore the complex relations in wafer manufacturing data. The accuracy of these methods depends on how extensively rule-based methods capture the information about different process parameters and about their interrelationship. Inverse predicting modelling technique was used as a diagnostic technique to estimate the input parameters from the critical output parameter. A library of input–output pairs of parameters was created. For a new output critical parameter, an extensive search in the library was performed using a neural network algorithm to find the association between inputs and corresponding output parameters. In addition, a cost function was used to relate the output parameter with input parameters just in case corresponding match between output and input parameters did not take place. This approach has performance limitations when the input parameters are numerous for a given output parameter. Moreover, only a single process was considered in this study.

Gardner *et al*. (2000), proposed a combination of self-organizing neural networks to find the significant variables affecting yield in a wafer manufacturing data. Rule induction, an unsupervised data-mining algorithm, was used to form clusters and identify characteristics that discriminate between clusters. Skinner *et al*. (2002)

recommended using classification and regression trees (CART) to analyse yield using probe data. The probe data was found to fit the data adequately and provide a recipe for avoiding low wafer yield.

Recently, there has been an emerging focus on model-based control techniques. Automatic process control is widely implemented to deal with the increasing demands of rapidly maturing semiconductor industry. Automatic process control (APC) techniques such as run-to-run control and adaptive process control techniques deal with making adjustments in the process recipe. A recipe is a collection of information such as process flow, device type, and the desired output or target values and the relevant control methods required to obtain the desired output (Butler 1995). The adjustment in the process is made based on the relationship between input and output parameters.

Run-to-run control is considered to be very useful in controlling the long-term drift of a wafer manufacturing processes (Moyne *et al*. 1995). In run-to-run control, product recipe with respect to a particular process parameter is modified between runs so as to reduce drift and variability. Khan *et al*. (1998) used run-to-run control-to-control critical parameters of the ITO deposition process such as optical transmission and resistivity. Moyne *et al*. (2000) is an excellent source about the theory and applications of run-to-run control techniques in semiconductor manufacturing. A review of control algorithms and related implementation challenges involved is provided with several case studies. See Del Castillo (2002) for details about control theory and statistical process adjustment methods and their relationship with the traditional process monitoring techniques such as control charts.

Edgar (1999) used a model-based predictive control approach with multivariate run-to-run control technique to control chemical mechanical planarization (CMP) process. However, techniques such as run-to-run control are primarily used for process control and adjustments rather than predicting the critical process parameters. Other approaches such as decision trees, Bayes theory, and neural networks offer a good potential in the area of semiconductor wafer modelling and yield prediction and need to be exploited. Chung and Sang (2000) used a combination of memory-based reasoning (MBR) and neural network learning techniques to model the dynamic behaviour of processes.

Boning and Chung (1998) proposed a methodology including techniques to identify, model and predict variations associated with ILD thickness in a chemical mechanical planarization process. The impact of variation on circuit performance was followed by generation of design rules to minimize variation and its impact has been reported in this study.

Traditional statistical methods are very difficult to apply especially when large numbers of complex processes are under consideration. In a typical semiconductor wafer manufacturing process, thousands of wafers are produced in a day and there are thousands of critical parameters involved in fabricating a single wafer (Chung and Sang 2000). In such a complex environment, traditional statistical approaches have limitations when used for quality improvement. They are neither feasible nor efficient in analysing the vast amount of data in a modern semiconductor wafer manufacturing. Moreover, the majority of the applications of statistical methods have been reported in the literature in the area of process improvements for discrete manufacturing processes rather than for the entire system.

8. Integrated yield modelling

Integrated yield modelling is a challenging task in wafer manufacturing environment due in part to the huge amount of data collected. There are many complex problems and defects associated with the yield modelling of wafer manufacturing environment due to a high degree of automation and interdependent process steps (Nurani *et al*. 1996). These problems should not be addressed in isolation for different processes and sub-processes, but analysed from the system viewpoint. Integrated yield models should have the capability to link defect and parametric data to its original source of origin so that the root causes of a specific problem can be determined. Then corrective actions can be taken and overall wafer yield can be improved (Nurani *et al*. 1996).

Doniavi *et al*. (1996, 2000) discussed adopting a systems approach to solving manufacturing problems. This is an approach that optimizes the whole of the system while optimizing discrete subsystems as well. It involves a series of steps accomplished in a logical manner and directed toward the development of an effective and efficient model. A system approach for integrated yield modelling needs to be formulated for modelling an entire system as well as its discrete subsystems. Tobin and Karnowski (2000) and Sack (1998) emphasized the need to have an integrated yield management system to determine the effect of process attributes on the final product yield at different steps such as the probe test and evaluation step.

Semiconductor manufacturing is a complicated process consisting of hundreds of processes, steps, equipment settings and flow hierarchies (Durbeck *et al*. 1993). It is important to simplify the system and relate different processes with each other. Durbeck *et al*. (1993) introduced a process specification system based on the concept of an object-oriented system to decompose process specifications into appropriate equipment, step, process and flow hierarchies. The proposed system is used for defining, reviewing or updating process steps and flows. Kristoff *et al*. (1995) also used a hierarchical object-oriented data structure to specify process flows, number of processes and steps at different level of nesting. Chaudhry *et al*. 1998 developed software, called active controller, for multistep control in wafer manufacturing facility.

Literature related to yield modelling focuses on specific processes and sub-processes such as lithography, CMP and does not present an integrated approach to predict the overall system yield. Therefore, there is a tremendous potential for linking the processes and sub-processes at different levels and producing an integrated yield model in a wafer-manufacturing environment.

8.1 *System Approach*

Newnes *et al*. (2001) used a three-phase approach to generate a model to analyse, control, and optimize various sub-processes involved in semiconductor wafer manufacturing. The system-modelling phase uses an IDEF0 model (a model used to relate the decisions, actions, and activities of a system) to identify the state of the existing system. The analysis and control phase uses techniques such as process characteristic charts, process capability ratios, and failure mode and effect critical analysis to identify potential areas where analysis and control is required. Finally, the optimization phase use techniques such as experiment design and response

surface models to optimize various sub-processes. Boning and Chung (1998), proposed an integrated methodology using tools such as modified ANOVA and empirical models to identify, model and predict variation; and after determining the impact of variation, developed design rules to minimize variation in a CMP process. Radojcic and Rencher (2000) proposed a feature-based methodology which includes understanding failure mechanism, building model, characterizing process and synthesizing yield using bottom up approach. However, literature is lacking in offering a systematic system approach towards integrating sub-processes at various levels in semiconductor manufacturing hierarchy.

We emphasize using a systems approach to understand the influence and contributions of sub-systems output on the product performance characteristics such as yield and defectivity. Systems approach will help decision makers and process engineers to compare and assess competing models. For example, some process engineers believe the Gate Contact (GC) layer is the most critical layer; others say that lithography is the most important process; neither have the tools to assess the impact of process deviations or corrections on yield. One of the approaches might be to use a systems level hierarchical modelling approach to develop a methodology to characterize process variability and identify the impact of critical sub-processes variables on the system output such as defectiveness. One of the unique features of systems level hierarchical approach is that we can use well established modelling techniques such as normal, Poisson, and logistic regression to estimate parameters, and to model and predict intermediate data and system output performance measures. Using a systems approach to characterize the relationships at the operational level will also improve productivity, identify and validate quality control parameters, and enable evaluation of competing process models.

9. Conclusions

The wafer manufacturing process involves hundreds of processing steps. In each step, multiple pieces of equipment are used to process wafers. Each piece of process equipment could cause variability. One possible way to capture variability is to test the effect of every variable and its possible interaction with other variables to understand the correlation of input variables with the output variable such as yield. However, the caveat is the complex nature of the processes and huge amount of data generated. The computation time required to analyse even one sub-process may be very high. A robust system should be developed that can correlate the different critical process parameters from different sources, and from that information critical output parameter such as yield could be predicted. Without using a system approach, it is difficult to integrate and utilize numerous data-related information obtained from different sources, and the gains from working on processes independently could result in yield loss from other processes that were affected by the changes.

Acknowledgement

This work was supported by NSF/SRC/ISMI grants DMI-0432484 and DMI-0432395.

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