Semiconductor Yield Improvement: Results and Best Practices

Sean P. Cunningham, Costas J. Spanos, *Member, IEEE*, and Katalin Voros, *Member, IEEE*

Abstract— **The results of a world-wide study on yield improvement are presented. Die yields collected from 21 fabs are transformed via a logit formula and compared. The die yields and die yield improvement rates of the fabs are compared, and manufacturing yield improvement practices are evaluated. Preliminary results of this continuing study indicate that die yield improvement is a function of computer-aided manufacturing practices and statistical process control practices in addition to commonly cited practices such as particle control and advanced manufacturing technology.**

I. Introduction

THE RESULTS of a world-wide study on yield improvement in 21 semiconductor manufacturing facilities are presented in this report. Each factory included in this study has completed an extensive factory performance questionnaire, providing information about the major processes in the factory, the clean room environment and equipment in the factory, and monthly or quarterly yield figures. In addition, an extensive fab tour and interview sessions between our study team and fab engineering staffs cover organizational and technical issues, and allow the study team to assess yield improvement practices.

To place yield improvement in context, *yield* is defined as the fraction of total input transformed into shippable output. (This is the typical semiconductor industry use of the term yield: other industries refer to this quantity as *yield rate*, reserving the term yield for the total quantity shipped.) The yield of the manufacturing facility is subdivided into components. *Line yield* is the fraction of wafers that are not discarded before reaching final wafer electrical test. *Die yield* is the fraction of dice on yielding wafers that are not discarded before reaching assembly and final test. *Final test yield* is the fraction of devices built with yielding dice that are deemed acceptable for shipment.

The total yield for the process is the product of these three terms. Wafer fabrication facilities have direct control over the line yield and the die yield, and decisions made in wafer fabrication may influence the final test yield. The economics of assembly and final test suggests strategies in which bad dice are discovered at wafer electrical test or wafer probe; i.e., packaging and final test of bad dice are becoming prohibitively expensive, especially since wafer electrical test can indicate which dice will fail at final test.

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The authors are with the Department of Electrical Engineering and Computer Sciences, University of California at Berkeley, CA 94720 USA.

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Similar economics may apply within wafer fabrication. Strategies in which potentially low-yielding wafers are discovered during wafer fabrication may be preferred owing to the capacity and material resources conserved in fabrication, and the capacity saved in wafer electrical test. However, two factors discourage strategies in which line yield is reduced to realize potential gains in die yield. First, the die yield of a specific wafer cannot be known until wafer electrical test, and thus causes for the failure of a specific die are unknown unless that die has been fully fabricated. Failure analysis methods in industry are typically geared toward the analysis of fully fabricated dice; consequently, information about dice obtained at wafer electrical test is perceived as more informative than information about dice obtained as wafer scrap in-line. Second, the line yield is often an important factor in the appraisal of the manufacturing organization, and there may be a disincentive for manufacturing to scrap product during wafer fabrication regardless of perceived product quality.

Die yield loss may be decomposed into functional yield loss and parametric yield loss. Functional yield loss consists of dice which do not function, whereas parametric yield loss consists of dice which do function, but not according to specification. Functional yield losses are caused primarily by particulate defects, scratches, and contamination that cause an otherwise correctly manufactured device to fail; functional losses may also result from severe processing variations that cause the device to be manufactured incorrectly and fail. Parametric losses are caused primarily by less severe processing variations that cause the die to behave differently from specification, e.g., lower frequency, slower speed, incompatible voltage range, etc.

Line yield loss is not an overwhelming concern in the semiconductor industry, although there are exceptions. Improvements to the die yield typically require few additional physical resources and few additional consumable materials, while the benefit from a small increase is large. During the early phases of product life, functional yield losses dominate parametric yield losses, and the severe process variation component of functional yield loss dominates the particulate component. The rate of improvement of yield, therefore, tends to be influenced by the capability of the manufacturing organization to eliminate severe processing variations quickly. The rate of improvement is also influenced by the quality of the product upon transfer from development.

This introduction is intended to illustrate why the comparison of yield performance across a sample of semiconductor manufacturing facilities is a challenging task subject to judg-

TABLE I
CANDIDATE FACTORS FOR THE STATISTICAL MODEL RELATING YIELD AND MANUFACTURING FACTORS

PROCESS/PRODUCT	FACILITY	PRACTICE
Die area	Clean room class	Automated SPC practices
Minimum feature size	Clean room size	Commitment to SPC
Number of mask layers	Facility age	Automated CAM practices
Type of technology	Facility region	Paperless CAM practices
Wafer size	Make/model of photo equipment	Organizational practices
Process age	Linking of photo equipment	Yield modeling practices

ment and interpretation. Some manufacturers may emphasize line yield at the expense of die yield in the hope that better information about fully processed failed dice will allow for a higher rate of yield improvement. Some may have tighter specifications at wafer electrical test which cause their die yields to be lower, but their final test yields to be higher. Some manufacturers may have applications for devices of a lesser specification such as memories with slower access speeds. Some may introduce products to market long before the severe parametric issues are resolved, trading low yield for increased market presence in cases where the technology is new and the potential customers are many. In summary, the analysis of this data requires qualitative explanations in addition to quantitative models.

The remainder of this report is organized as follows. A linear statistical model regresses die yield against technological product-related and facility-related factors. The residuals of this model are used to derive a qualitative model using manufacturing practices as factors. This model is extended and applied to individual fabs to determine which fabs improve yield fastest. In this context we study the qualitative factors that lead to strong performance in yield improvement. Some concluding remarks are made recommending future areas for study in yield improvement.

II. MODELING ABSOLUTE YIELD

In comparing die yields across a number of different manufacturing facilities, technological and organizational factors influencing the yields of different manufacturing processes must be considered. It is convenient to group these factors into three broad categories: process/product, facility, and manufacturing practice.

Table I contains the candidate factors modeled for this analysis. Many of these variables are true qualitative variables, e.g., SPC extent, a qualitative entity that represents our judgment regarding the strength of the facility's approach to executing SPC. Some of these variables have been expressed as qualitative variables in the interest of protecting fab confidentiality, e.g., facility size and facility age. Table II contains a sample of the 72 processes included in our analysis; only the most advanced process from each fab is included in Table II.

The model used here is a linear model relating a transformation of die yield with the collection of manufacturing variables. The die yield of each process is taken as the most recent for which data has been supplied by the participants. We have restricted the analysis to include a single die type for each process in each facility. We apply the following logit

TABLE II
PROFILE OF SEMICONDUCTOR MANUFACTURING PROCESSES AND FACILITIES

		PROCESS/PRODUCT			FACILITY			LITHOGRAPHY	
Fab	Yield[a]	Technology[b]	Age[c]	Size[d]	Size[e]	Class[f]	Age[g]	Equipment[h]	Link[i]
P1	0.89	2.5μm Bipolar	15	0.21	Small	3	Old	PE (align)	No
P2	0.91	2.0μm Bipolar	45	0.03	Med	2	Old	NSR-g	Yes
P3	0.80	1.5μm CMOS	36	0.20	Large	1	Old	Ultratech	Yes
P4	0.48	1.2μm CMOS	9	0.36	Small	2	Mid	Canon	No
P5	0.71	1.1μm CMOS	27	0.73	Med	2	Mid	ASM-2500	No
P6	0.49	1.0μm CMOS	12	0.80	Small	2	Old	NSR-g	No
P7	0.70	0.9μm CMOS	57	1.31	Med	0	Mid	NSR-g	Yes
P8	0.48	0.9μm CMOS	36	1.61	Large	3	Old	NSR-i	Yes
P9	0.75	0.8μm CMOS	30	0.42	Small	0	Mid	ASM-2500	No
P10	0.74	0.8μm CMOS	3	0.42	Med	3[j]	New	ASM-5000	Yes
P11	0.78	0.7μm CMOS	18	0.82	Large	2	Mid	NSR-g	Yes
P12	0.62	0.7μm CMOS	15	1.40	Small	2[j]	Old	NSR-i	Yes
P13	0.60	0.7μm CMOS	24	0.83	Large	2	Mid	NSR-i	No
P14	0.57	0.7μm CMOS	7	0.76	Med	1	Mid	NSR-g	Yes
P15	0.23	0.7μm CMOS	24	1.91	Med	1	Mid	NSR-g	No
P16	0.76	0.6μm CMOS	9	0.69	Large	1	New	NSR-i	Yes
P17	0.71	0.5μm CMOS	4	0.40	Med	1	New	NSR-i	Yes
P18	0.83	0.6μm CMOS	23	0.14	Med	1	Mid	NSR-i	Yes
P19	0.75	0.8μm CMOS	44	0.82	Med	2	Mid	NSR-g	Yes
P20	0.32	1.5μm CMOS	69	0.52	Small	1	Mid	PE (align)	No
P21	0.61	0.9μm CMOS	27	0.70	Med	1	Mid	NSR-i	No

a. *Yield* is given for the most recent time period for the process listed.

b. *Technology* refers to the most advanced process in production in the facility. The minimum feature size is shown in microns ($1\mu m = 10^{-6}$m).

c. *Process age* refers to the time span in months between the first and last yield data point supplied for the technology listed.

d. *Product size* refers to the area of the representative die type in cm^2.

e. *Facility size* refers to the physical size of the cleanroom in ft^2. Fabs smaller than 20,000 ft^2 are defined as small; fabs larger than 60,000 ft^2 are defined as large.

f. *Class* is the clean room cleanliness class as reported by the facilities. The value for class is x where the reported clean room class is 10^x.

g. *Facility age* refers to the vintage of the fab. Old fabs are those built before 1985; mid fabs are those built between 1985 and 1990; new fabs are those built after 1990.

h. *Equipment* refers to the most recent lithographic technology introduction into the facility. NSR refers to Nikon Step and Repeat systems, and PE refers to Perkin Elmer aligners.

i. *Link* refers to the existence of a physical link among the coat/expose/develop equipment in photolithography operations; such links may be robotic, track, or other conveyance automation. A positive response indicates the existence of at least one such linked system.

j. Both P10 and P12 use standard mechanical interface (SMIF) technology, in which the cleanliness class of the equipment is typically one or two orders of magnitude less than the clean room itself. The class reported is that of the cleanroom.

transformation:

$$\boldsymbol{W} = \log\left(\frac{y}{1-y}\right). \tag{1}$$

To relate yield to any or all of the manufacturing parameters, we apply a linear model of the following form:

$$\boldsymbol{W} = \boldsymbol{X}\beta + \varepsilon \tag{2}$$

where $\boldsymbol{X}$ is a design matrix. The actual yield y may be expressed as follows:

$$y = \frac{\exp(\boldsymbol{X}\beta)}{1+\exp(\boldsymbol{X}\beta)} \tag{3}$$

which has the appealing property that, as y approaches one, the derivative with respect to any particular regressor variable is decreasing, i.e., it is more difficult to achieve large gains in yield with a high-yielding process than with a low-yielding process.

The original design matrix $\boldsymbol{X}$ of this linear regression included the process and facility related variables listed in Table I. After some statistical analysis, we discovered three significant process and facility variables: *dieSize* is the total area of the device expressed in cm^2; *processAge* is the time span from the oldest to the most recent die yield data point given in months; and *photoLink* is a binary factor variable

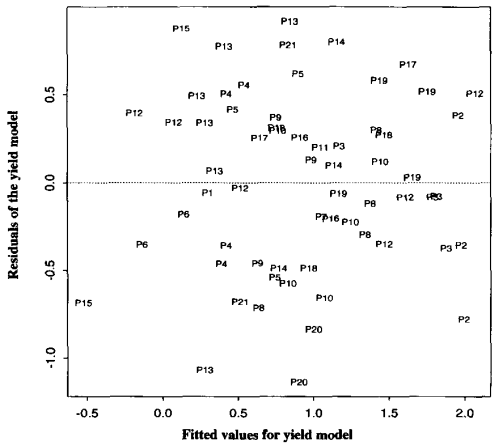

Fig. 1. Residuals of the model fit in (4). Points above the line reflect those die types which outperform the yield model. For this model, $R^2 = 0.60$.

which is 1 if the photolithography system is linked and -1 otherwise. We obtained the model

$$W = 0.33 - \underset{(\pm 0.13)}{0.80} \cdot dieSize + \underset{(\pm 0.08)}{0.34} \cdot \log(processAge) + \underset{(\pm 0.07)}{0.39} \cdot photoLink. \quad (4)$$

In building this model, seven of our 72 data points were removed as outliers from a standard Cook's distance residual analysis. The parenthetical values below the coefficients indicate the standard errors of the coefficients. This is a statistically significant linear model, and each of the coefficients is also highly significant.

That these regressors appear in the linear model is not surprising: the dependence of die yield on die area is well documented [2]; the yield learning rate for a new process may be approximated by a logarithmic function, and linked photolithography systems are often associated with improved equipment and practice leading to improved yield. What is surprising is the absence of other factors such as technology type, minimum feature size, and the number of mask layers. However, these factors may be confounded with factors appearing in the model, and the inclusion of the factors in (4) reduces the additional explanatory power of the excluded factors. While the creation of a technology complexity index which accounts for these additional factors was considered, we chose to maintain model simplicity and include only the three primary terms.

The residuals from the statistical model in (4) are shown in Fig. 1. These residuals are independently and identically normally distributed. While our statistical model explains over half of the variance in yield scores, more detailed information unavailable to us such as robustness of the circuit design and other issues discussed in the introduction might account for additional systematic variance in these residuals.

III. Assessment of Manufacturing Practice

Qualitative manufacturing practice factors may explain some of the additional model variance, i.e., having corrected for process and facility factors outside the domain of the manufacturing facility, we may assess the effect of manufacturing practice on the residuals of the foregoing model. Table III lists manufacturing practice factors assessed here.

While we were able to include 72 yield data points in deriving (4), our analysis of manufacturing practices is qualitative owing to the smaller sample size of 21 facilities, since each of the manufacturing practices listed in Table III is assumed to be a facility-wide practice. To assess the independence of each of the manufacturing practice factors, we have developed contingency tables for each pair of factors suspected to be associated in some way, e.g., extent of SPC practice and automation of SPC practice. While there are statistical tests appropriate for analyzing the results of contingency tables, e.g., the χ^2 test for independence, the sample size of 21 is too small for classical statistics to be meaningful. Table IV is a contingency table for the SPC factors under evaluation.

Factories which have automated the rote plotting task of SPC are able to benefit from advanced control procedures and increased numbers of control charts in their fabs. Table V is a contingency table for the CAM factors under evaluation.

TABLE III
Profile of Semiconductor Manufacturing Practice

		CAM		SPC		ORGANIZATION	
Fab	Yield Model[a]	Recipes[b]	Paperless[c]	Auto[d]	Extent[e]	Group[f]	Goals[g]
P1	Seeds	Manual	No	No	Low	Yes	Historical
P2	Empirical	Full-auto	No	Yes	Medium	Yes	Corporate
P3	Murphy	Manual	No	No	Low	Yes	Corporate
P4	Empirical	Manual	No	Yes	Medium	Yes	Historical
P5	Murphy/Seeds	Semi-auto	No	Yes	Medium	Yes	Historical
P6	Murphy/Price	Manual	No	Yes	Low	Yes	Corp/hist
P7	Moore	Semi-auto	Yes	Yes	Medium	Yes	Historical
P8	Empirical	Semi-auto	No	Yes	High	Yes	Corporate
P9	Moore	Semi-auto	No	Yes	Medium	Yes	Corporate
P10	Seeds	Full-auto	Yes	Yes	High	Yes	Corporate
P11	Empirical	Full-auto	Yes	Yes	High	No	Corporate
P12	Moore	Manual	No	Yes	Medium	No	Corp/sister
P13	Empirical	Manual	No	No	Medium	No	Corporate
P14	Moore	Manual	No	Yes	Medium	Yes	Corporate
P15	Murphy/Binomial	Semi-auto	Yes	Yes	Medium	Yes	Corp/sister
P16	Murphy	Full-auto	No	Yes	High	No	Corporate
P17	Seeds	Manual	No	No	Medium	Yes	Historical
P18	Empirical	Semi-auto	No	Yes	Medium	Yes	Historical
P19	Murphy	Full-auto	Yes	Yes	Low	No	Historical
P20	Poisson	Semi-auto	No	No	Medium	Yes	Corp/hist
P21	Empirical	Full-auto	Yes	Yes	High	Yes	Historical

a. *Yield model* refers the specific formula used by that organization to predict the yield of the process as a function of a measure of defect density.

b. *Recipes* refer to the capacity of the facility to automatically download recipes via a computer-aided manufacturing system into the equipment. Full-auto indicates a fab in which a majority of operations have auto-recipe download; semi-auto indicates a fab in which a minority of operations have auto-recipe download; manual indicates a fab without auto-recipe download.

c. *Paperless* is an indicator of the extent of computer-aided manufacturing in the fab. Only fabs P11, P15, and P10 are fully paperless, *i.e.*, no lot travellers or run cards accompanying production lots.

d. *SPC Auto* is an indicator of whether the SPC control charting function is automated.

e. *Extent* of SPC practice is our subjective rating of each facility's commitment to and execution of SPC. This index is more fully described in the Process Control section of this report.

f. *Group* refers to the existence of a yield engineering group at the facility. In nearly every case where there is a yield group, their efforts are supplemented by product engineering and other entities within the fab.

g. *Goals* indicate the mechanism for setting yield targets. Corporate indicates the existence of a central corporate body which determines yield goals, usually after some negotiation with the fab. Historical indicates the reliance of yield goals on historical performance. Sister refers to cases where two fabs within the same firm produce the same products and derive yield goals based on the performance of the sister fab.

TABLE IV
Contingency Table for SPC Automation and SPC Extent Rating

	SPC EXTENT		
	High	Medium	Low
Automated SPC charts	4	10	1
Manual SPC charts	0	4	2

TABLE V
CONTINGENCY TABLE FOR PAPERLESSNESS AND CAM AUTOMATION

	CAM AUTOMATION		
	Full	Semi	Manual
Paperless	4	2	0
Not paperless	2	5	8

TABLE VI
CONTINGENCY TABLE FOR SPC AUTOMATION AND CAM AUTOMATION

	CAM AUTOMATION		
	Full	Semi	Manual
Automated SPC charts	6	6	4
Manual SPC charts	0	1	4

TABLE VII
CONTINGENCY TABLE FOR REGION AND LINKED PHOTOLITHOGRAPHY

	LINKED PHOTO	
	Yes	No
Europe	0	2
Asia	6	1
U.S.	6	6

CAM automation is a measure of the extent to which factories have automated the recipe download to their equipment. Such automation efforts are typically expected to improve yields. Table VI is a contingency table for the automation of SPC and CAM.

The bottom row of Table VI indicates that some fabs are technologically limited, but the top row indicates that it may be easier to implement an SPC automation system than an automated recipe download system.

Finally, Table VII is a contingency table evaluating the association of region and linked photolithography; this table shows that the link factor in (4) may be confounded with region.

Having an understanding of some of the associations among the manufacturing practice factors, we assess the effect of these practices on yield through an analysis of the residuals of (4). Fig. 2 is a plot of the model residuals for each facility; facilities primarily above the centerline are outperforming the other fabs relative to the model, whereas facilities below the centerline are underperforming relative to the model prediction. Factor plots of this type are useful in assessing the performance of factories with respect to the other manufacturing practice factors.

Fig. 3 shows factor plots for SPC automation and extent. While neither result is statistically significant, there appears to be some small advantage to using SPC to more than a cursory extent. Whether SPC automation is undertaken or not does not appear to make a difference; however, the significance of this plot is very low owing to the vast majority of facilities which automate SPC.

Fig. 4 shows factor plots for CAM automation and paperlessness of the factory. The results for Fig. 4 are not statistically significant, although the trend seems to be as expected in both plots. Factories which have adopted automated recipe downloading in a significant number of factory operations tend to score better in yield than factories with few or no automated operations. Paperless factories tend to score better in yield, but this plot is based on 15 processes in paperless factories from the 72 process sample; the paucity of the data sample of nonpaperless factories reduces the significance of the results.

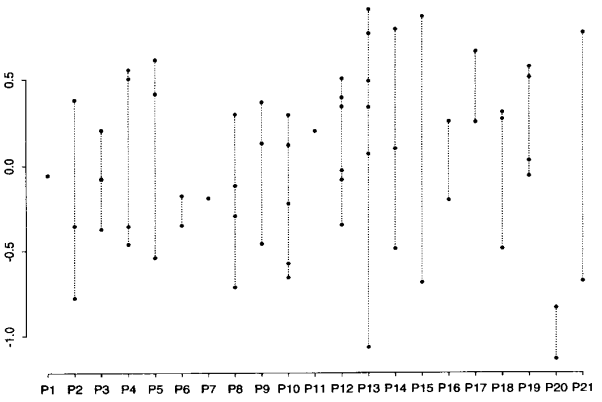

Fig. 2. Plot of residuals by facility.

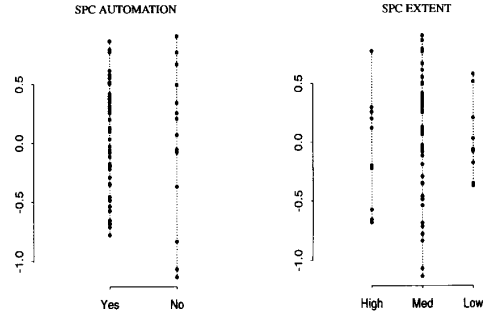

Fig. 3. Plots of residuals by SPC automation and SPC extent.

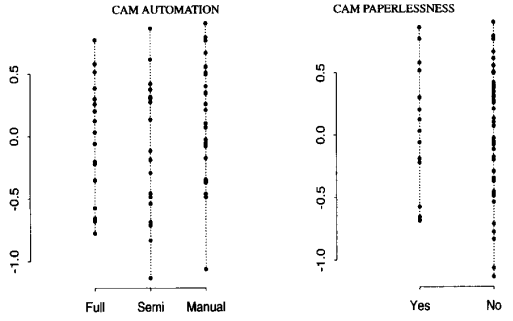

Fig. 4. Plots of residuals by CAM automation and CAM paperlessness.

Fig. 5 shows the factor plot by yield model and yield group. The yield models have been condensed to those developed on-site and those developed off-site. The yield group indicator measures the existence of a central yield group. The development of homegrown yield models appears advantageous, and this result is intuitive given that homegrown yield models can respond to the specifics of the processes and products within each fab. The yield group result is not intuitive, and is most likely the result of having only four fabs working

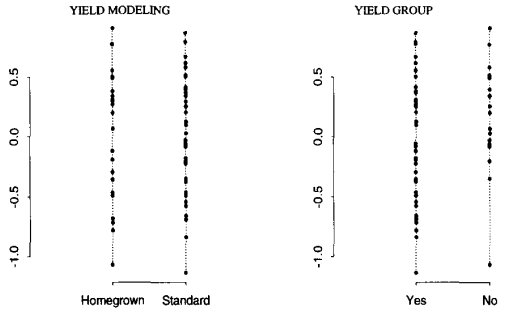

Fig. 5. Plots of residuals by yield model and yield group.

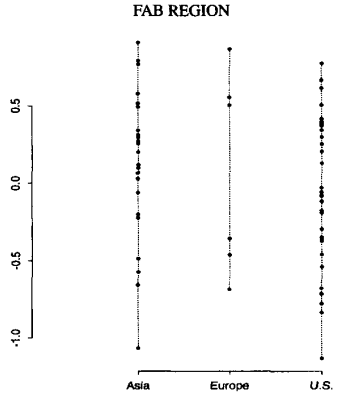

Fig. 6. Plot of residuals by facility region. Asian facilities include Japanese and Taiwanese sites.

without yield groups in the sample. Also, this is one of the more subjective measures among the manufacturing practices analyzed; the extent to which these yield groups are involved in yield improvement is difficult to determine during a site visit.

Fig. 6 shows the residuals by regions in which the facility is located. Asian fabs, including Japanese and Taiwanese sites, score higher than both U.S. and European factories; however, this may be an artifact of the sampling strategy used to select study participants. Site visits are more likely to include low-yielding U.S. factories than low-yielding Asian or European factories, and as a result there may be some bias in the results.

We have created a yield model incorporating process and facility factors intended to correct for existing conditions outside the control of the factory. We have analyzed the residuals of this model with respect to manufacturing practices which are controllable by manufacturing. While the sample size of 21 facilities is still small from which to draw statistically valid conclusions, the trends combined with some judgment and intuition reveal some practices which factories have used to improve yields. In the next section, we use similar methods to analyze the rate of improvement of die yield.

IV. Modeling Yield Improvement Rate

In the previous analysis, we have used the most recent yield data from 72 die types in separate processes to develop the yield model of (4). Using a similar analysis, we can study the yield improvement rate. We may interpret the coefficient of (4) such that for every additional month the process is in existence, the transformed yield value is expected to rise 0.36 per month. We interpret this as an aggregate learning rate for the industry.

Applying a similar model to data from each factory individually, we may investigate the learning rate in individual factories. This model is the same as that in (4) with the *linkPhoto* term removed; because each factory takes a single value for this variable, this term is essentially part of the intercept in the analysis of a single factory; the model is shown here:

$$W_j = \alpha_{0j} + \alpha_{1j}\, dieSize_j + \alpha_{2j} \log (processAge)_j \quad (5)$$

where a different model is created for each factory j. We restrict these models to contain only data points from the most recent 18 months from our receiving the factory performance questionnaire; this was done to compare the factory in its current state with other factories in their current states. For each fab, data points from multiple processes may appear; for this additive model, the *dieSize* term acts as a scaling term intended to account for the differences in processes, and α_{0j} acts as an intercept. Our interest in these models is the coefficient α_{2j}, which is a measure of the individual rate of improvement in yield by factory. Table VIII lists the models computed for each of the factories.

These fabs are rated according to their performance into three categories based on their α_{2j} coefficients in cases where the yield model we have imposed on the fabs fits well. Similar

TABLE VIII
Individual Factory Yield Models

FAB		COEFFICIENTS			DIAGNOSTICS	
Name	Rating[a]	α_0	α_1	α_2	R^{2b}	df
P1	Low	2.09	-3.41	0.19	0.98	22
P2[c]	?	-8.91	64.75	2.31	0.60	37
P3[d]	Low	-2.02	16.19	0.16	0.68	28
P4	?	0.86	-2.80	0.16	0.30	17
P5	?	-0.17	0.01	0.39	0.43	39
P6	Low	-0.26	-0.53	0.19	0.31	18
P7	Medium	0.00	-1.52	0.71	0.73	4
P8	High	-2.63	-1.34	1.27	0.91	32
P9	High	-2.60	-2.46	1.29	0.91	73
P10	Medium	0.86	-1.84	0.41	0.61	19
P11[e]	Low	0.00	0.56	0.18	0.56	5
P12	Medium	0.47	-0.61	0.31	0.80	72
P13	Low	3.15	-4.48	0.17	0.76	37
P14	?	2.66	-2.22	0.17	0.21	51
P15	Medium	0.54	-1.58	0.41	0.69	17
P16	Medium	3.38	-4.28	0.49	0.96	29
P17	?	-3.68	9.15	1.09	0.76	17
P18	Medium	0.43	-0.27	0.44	0.54	27
P19	Medium	1.65	-2.54	0.41	0.91	69
P20	Low	1.30	-0.84	-0.37	0.60	44
P21	High	-1.22	-2.75	1.07	0.90	33

TABLE IX
Contingency Tables for Yield of Improvement Against SPC Factors

	SPC AUTOMATION	
	Yes	No
High	3	0
Med	6	0
Low	2	4

	EXTENT OF SPC		
	High	Med	Low
High	1	2	0
Med	2	3	1
Low	1	3	2

TABLE X
CONTINGENCY TABLES FOR YIELD OF IMPROVEMENT AGAINST CAM FACTORS

	PAPERLESS FAB	
	Yes	No
High	1	2
Med	3	3
Low	1	5

	CAM AUTOMATION		
	Full	Semi	Manual
High	1	2	0
Med	3	2	1
Low	1	1	4

TABLE XI
CONTINGENCY TABLES FOR YIELD OF IMPROVEMENT AGAINST ORGANIZATIONAL FACTORS

	YIELD MODEL	
	Home	Away
High	2	1
Med	1	5
Low	2	4

	YIELD GROUP	
	Yes	No
High	3	0
Med	3	3
Low	4	2

to the analysis of the previous section, associations between manufacturing practices and yield improvement ratings are revealed.

Table IX shows the relationship between yield improvement and SPC automation and the extent of SPC.

While the results of Table IX are not statistically conclusive, poor performance in automation and extent of SPC practice appears to impede yield improvement efforts. Table X shows the relationship between yield improvement and CAM practices.

As in Table IX, it appears that an investment in sensible fab automation pays dividends in yield improvement.

Table XI shows the relationship between yield improvement and yield modeling, and yield improvement group activity. The yield modeling results are difficult to interpret owing to the scarcity of homegrown models in the contingency table; the yield group results show a small tendency toward favoring yield groups.

Table XII shows the relationship between yield improvement and fab region. While this result may be initially surprising, the three U.S. fabs rated highest have sustained steady yield improvement over a long period of time. The high rating for fab P9 owes much to a poor starting point for yields and the need for a great deal of improvement. However, fabs P8 and P21 have maintained steady yield improvement over a long span of time, and are clearly the top yield improvement performers in the study. Of the medium rated Asian fabs, fab P10 has a short time history and might be expected to develop a high rating if it is able to sustain steady improvement; despite some well documented difficulties in product design, fab P16 has shown good yield improvement.

V. CONCLUSIONS

Through statistical analysis and qualitative modeling, we have shown that the yield of products from different semiconductor manufacturing facilities can be analyzed and compared through a common yield model. By accounting for the differences in processes, facilities, and equipment sets using an appropriate model, we may analyze the residuals of such a model to determine the effect of manufacturing practice on yield performance. In this section, we report some general conclusions of our study.

TABLE XII
CONTINGENCY TABLE FOR YIELD OF IMPROVEMENT AGAINST FAB REGION

	FAB REGION		
	U. S.	Asia	Europe
High	3	0	0
Med	1	4	1
Low	4	2	0

As indicated by Fig. 5, we have found much qualitative evidence that the use of homegrown yield models is beneficial. Traditional semiconductor yield modeling, i.e., the normalization of yield into some quantity usable across all products within the fab, is useful for prioritizing engineering effort, obtaining yield forecasts for financial planning, and making decisions regarding yield targets for new process introductions. Factories which invest their effort in understanding the causes of low yield, and which capture this specific knowledge in detailed yield models tend to outperform those factories which consult the widely available yield models and fit parameters based on a small data sample.

We have also found evidence that the class of clean room is not a critical factor in determining yield. Clearly, semiconductor manufacturing requires a clean ambient environment free from contamination and airborne particulates. However, we have observed a convincing number of cases where particles generated during certain processes, e.g., metallization sputtering, tungsten chemical vapor deposition, and plasma etching, have a much greater effect on the yield of the process. Although the clean room practices maintained by the factories we have visited vary greatly, it seems that the effect of these practices are not detectable in the yields.

Finally, sensible factory automation appears to be a prerequisite for yield improvement. Detailed data analysis is required for continuing yield improvement, and large data sets are only manageable using computer-aided manufacturing. Improved automation of SPC allows more control charts to be maintained, and the automated upload of data from equipment to database is an emerging trend for increased process control. In addition to this computer-aided manufacturing effort, we have observed advances in physical automation such as robotics, automatic guided vehicle systems, and overhead conveyors. This type of automation is effective not only because of improved material handling, but also because of the streamlining of operations that usually accompanies automation efforts.

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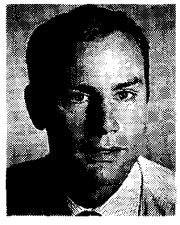

Sean P. Cunningham received the B.S. degree in industrial engineering from the State University of New York, Buffalo, in 1989, and the M.S. degree in industrial engineering from the University of California at Berkeley, in 1990. He is currently earning the Ph.D. degree in industrial engineering and operations research at the University of California at Berkeley.

Since 1992, he has worked with the Competitve Semiconductor Manufacturing Program. He has held summer positions with Harris Semiconductor and Eastman Kodak Company.

Mr. Cunningham is a member of the Operations Research Society of America, the Institute of Industrial Engineers, and Tau Beta Pi. In 1993, he was awarded the Robert N. Noyce Memorial Fellowship from the Intel Foundation.

Costas J. Spanos (S'81–M'85), for photograph and biography, please see p. 25 of the February 1995 issue of this TRANSACTIONS.

Katalin Voros (S'83–M'84) received the B.S. degree in physics from the Drexel Institute of Technology, Philadelphia, PA, in 1966, and the M.S. degree in electrical engineering and computer sciences from the University of California, Berkeley, in 1984.

In 1984, she became a process engineer at the Microfabrication Laboratory of the University of California, Berkeley; she has been its manager since 1986. She worked on bipolar IC's as a process engineer for Philco–Ford Microelectronics, on RF transistors and CMOS circuits for Solid State Scientific, Inc., and high frequency power transistors for the Microwave Semiconductor Corporation. She joined RCA's David Sarnoff Research Center, Princeton, NJ, in 1980 as an associate member of technical staff in the high density bulk CMOS (SRAM) development group.

Ms. Voros is a member of the Electrochemical Society. She is a recipient of the University of California at Berkeley, Administrative and Professional Staff Distinguished Achievement Award, 1991.