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Variability-Aware DTCO Flow: Projections to N3 FinFET and Nanosheet 6T SRAM

M. Karner, G. Rzepa, O. Baumgartner, G. Strof, F. Schanovsky, F. Mitterbauer, C. Kernstock, H.W. Karner, and Z. Stanojevic
Global TCAD Solutions, Vienna, Austria

***Abstract*—Variability increases with downscaling, making it a vital component in the assessment of upcoming technologies. We use a variability-aware DTCO flow, which seamlessly integrates accurate TCAD simulations with industry-proven SPICE solutions. The impact of local variability sources on SRAM KPIs is analyzed for N3 FinFET and nanosheet technologies. Assuming typical process parameters, the geometrical variations due to LWR, STI recess, and epitaxial growth significantly affect the SRAM variability. However, the main contributor to variability for N3 technologies is MGG, highlighting the crucial role of metal grains size reduction for technology optimization.**

I. Introduction

Decreasing device dimensions of advanced technologies inherently lead to increased device variability [1]. *Global variability* sources induce a performance spread across the wafer and are controlled through processing. *Local variability* however can be more fundamental and needs to be assessed systematically to evaluate the achievable performance of a technology. Main contributors to local variability are random discrete dopants (RDD) [2], metal gate granularity (MGG) [3–5], oxide defects [6], and geometrical variations such as line edge roughness (LER) [7], line width roughness (LWR) [8], and height variations due to STI recess and epitaxial growth. Experimental studies of individual contributions to local variability in advanced technologies are challenging. The advantage of TCAD simulations can be fully leveraged here, since the physics of these variability sources are well understood. However, these simulations are limited by the computational effort required to obtain large sample sizes for statistical analysis. To overcome this limitation, we present a variability-aware design technology co-optimization (DTCO) [9, 10] flow, which combines TCAD simulations with SPICE [11].

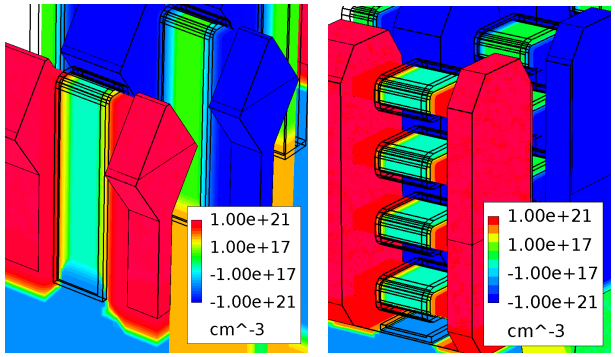

Fig. 1: Net doping (donor: +, acceptor: −) of N3 FinFETs (left) and nanosheets (right) in a 6T SRAM cell. The same doping profile is assumed for both technologies (channel doping of 10^{16}cm^{-3}). The full SRAM cell with interconnects is shown in Fig. 2.

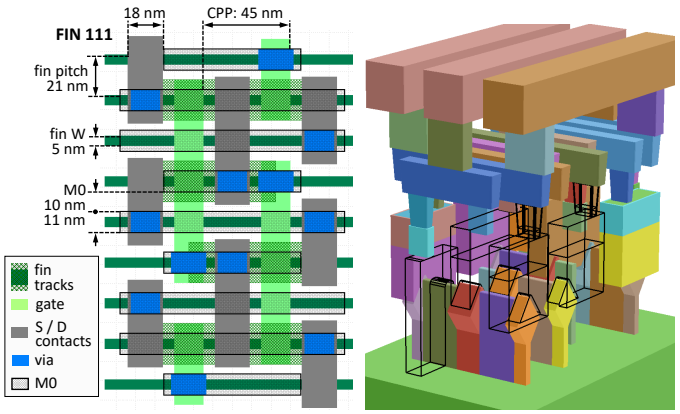

Fig. 2: Layout (left, shaded area of fin tracks mark fin cuts, M1 not shown) and corresponding structure (right) of a SRAM cell in N3 FinFET technology with symetrical n/pFET effective widths (111 configuration with 1 fin track for pull-up, pull-down, and pass-gate FETs).

II. Technologies

The two main contestants for N3 are FinFET and gate-all-around (GAA) horizontal nanosheet (NS) technologies [12–14]. Inherent to NS are better short-channel control and more room for design optimization with planar-like non-digital n/pFET balancing [15–17]. FinFET SRAM designs are limited to conventional 111 or 122 configurations but processing is well established.

Thus, with a focus on N3 variability projections in this work, a 111 SRAM in FinFET technology and a NS SRAM design with 16 nm widths for both nFET and pFET are investigated. Their key design and technology specifiactions are listed below.

	N3 Fin	N3 NS
gate L [nm]	15	15
channel W x H [nm]	5 x 55	16 x 5
number of channels [1]	1	4
channel doping [cm^{-3}]	10^{16}	10^{16}
SiO_2 / HfO_2 [nm]	0.5 / 1.5	0.5 / 1.5
contact poly pitch [nm]	45	45
spacer L [nm]	8	6

The NS technology has 4 stacked nanosheets per FET, resulting in a comparable but slightly larger effective channel area as the FinFET technology (see **Fig. 1**). 3D SRAM cells are generated for both technologies with a M0-pitch of 21 nm [18]. **Fig. 2** shows the FinFET 111 SRAM structure as an example.

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III. Simulation Framework

A two-stage simulation approach is used that separates a) TCAD simulation of FETs, including variability through the impedance field method (IFM) [1], from b) accurate SPICE simulation of cells based on integrated 3D parasitics extraction (PEX) of full cells [19] (see **Fig. 3**). PEX extracts complete circuits with all resistors, capacitors, and FETs from 3D cell models. BSIM-CMG [20] model cards of the FETs are extracted from the TCAD simulations, allowing to run the circuits in SPICE simulators. Simulation times can be further substantially reduced also for single FET variability by only simulating about 100 statistical samples of FETs with TCAD and then extrapolating them to obtain a very large number of FET model cards using the following procedure.

(i) The nominal BSIM-CMG model card is fitted to TCAD (see **Fig. 4**).
(ii) Based on the nominal model cards, the BSIM-CMG variabilitiy parameters are extracted from variability TCAD simulations (see **Fig. 5**).
(iii) The number of model cards acquired in step II is still limited by the computational costs of TCAD simulations. This is resolved by extrapolating the BSIM-CMG variability model cards from an representative set of model cards to much larger numbers considering the parameter correlations accurately (see **Fig. 6**) [9].

IV. Variability Sources

RDD and MGG is simulated with TCAD while the geometrical variability sources are simulated with SPICE models. The RDD model is free of parameters and for the MGG model two grain orientations are assumed with equal probability and a difference in work function of $\Delta E_W = \pm 0.1$ eV. As the grain sizes are strongly process dependent, two different sizes are simualted as reported in literature for TiN contacts [3, 5]. The parameters for the variability models are listed in the table below [21].

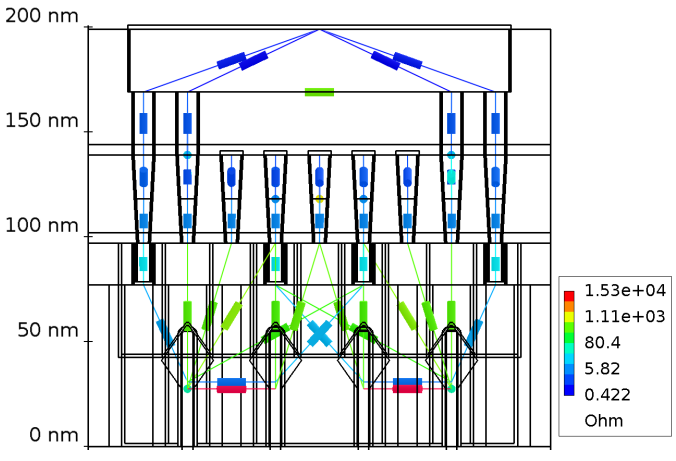

Fig. 3: Extracted resistances of the SRAM cell in Fig. 2 shown in a transversal parallel-projection of the 3D structure.

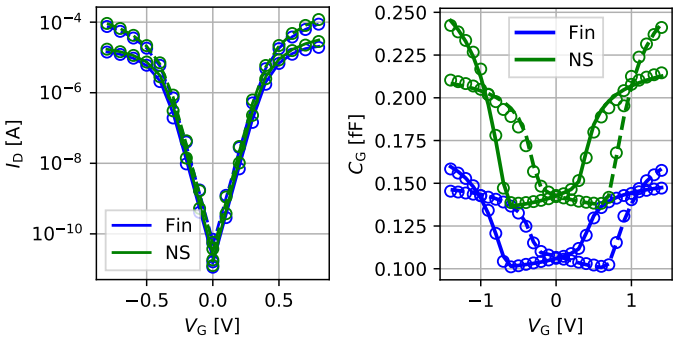

Fig. 4: **Step (i)** of TCAD-to-SPICE: Nominal TCAD simulations (circles) are fitted by SPICE (lines). Shown are $I_D V_G$ (left, solid line: linear, dashed: saturation regime, $V_D = 0.8$ V) and $C_G V_G$ (right, solid line: nMOS, dashed: pMOS).

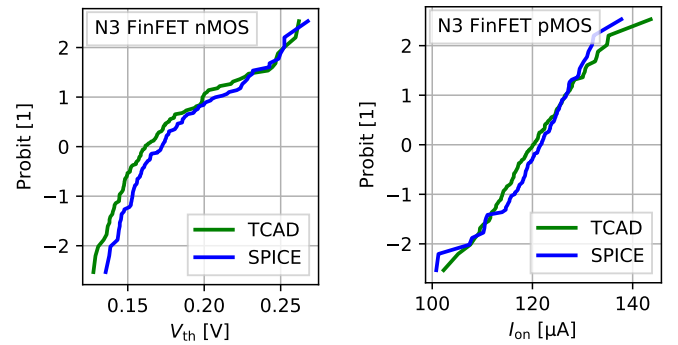

Fig. 5: **Step (ii)**: Variability from TCAD IFM [1] is fitted with SPICE based on nominal parameterization. Shown as examples are the distribution of V_{th} for nMOS (left) and I_{on} for pMOS (right).

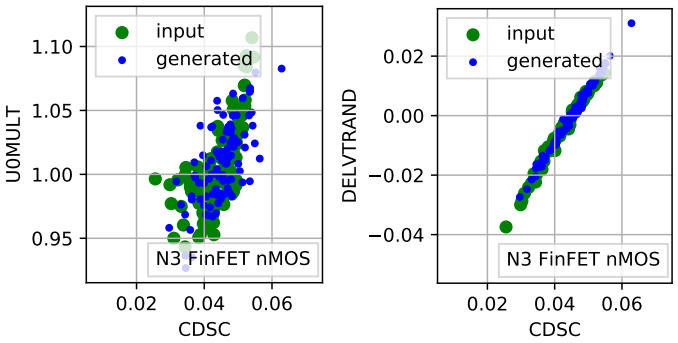

Fig. 6: **Step (iii)**: The BSIM-CMG variability model cards obtained in step (ii) from TCAD simulations are boosted to a large number of model cards for broad statitical analysis through extrapolation considering the parameter correlations [9].

RDD	doping based
small MGG	avg. grain size: 10 nm, $\Delta E_W = \pm 0.1$ eV
large MGG	avg. grain size: 22 nm, $\Delta E_W = \pm 0.1$ eV
channel H	Fin: STI recess, $\sigma = 1.5$ nm, NS: epi. growth, $\sigma = 0.133$ nm
channel W & L	LWR, $\sigma = 0.167$ nm

For the NS technology, the geometrical variations can be correlated within a stack, depending on the process. These correlated geometrical variations are expected to increase the variability of a technology and are thus analyzed as well, denoted by "cor" where applicable.

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V. Results

Using the simulation framework described above, FinFET and NS variability is simulated for room temperature. The results are discussed in the following on FET and SRAM level.

A. FET Variability

The resulting distributions of V_{th} and the subthreshold slope (SS) are shown in **Fig. 7** for selected NS and FinFET variability sources. NS show better mean SS compared to FinFETs and approximately normally distributed parameters are confirmed. Their relative standard deviations are listed in **Fig. 8**. This analysis shows that MGG is the dominant source for local variability in these technologies while RDD plays a minor role. For the NS technology, the geometrical variability is more pronounced assuming correlated variations but is still small compared to MGG. The impact of the geometrical variations on the FinFET technology is slightly larger compared to the NS technology.

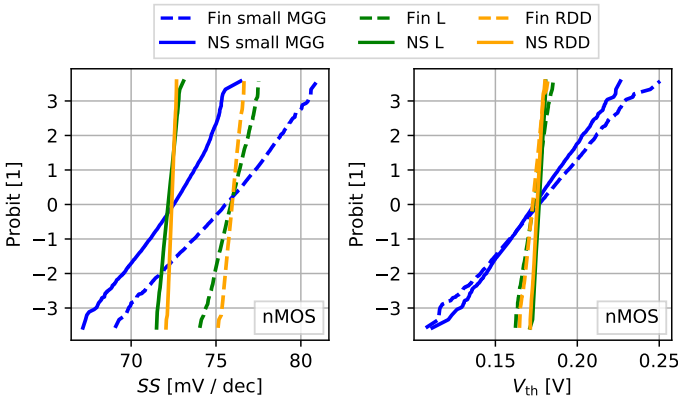

Fig. 7: Probit plots showing approximately normally distributed V_{th} and SS of 4000 nMOS FinFET and NS. The impact of the selected variability sources on the FET performance is shown separately: Small MGG (average metal grain size: 10 nm), RDD, and geometrical variation of the channel L due to LWR. For the NS, the latter is shown for correlated geometry variations where each nanosheet within a FET has the same L.

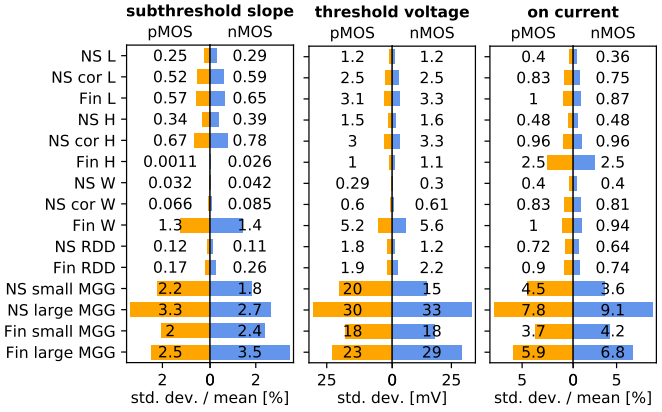

Fig. 8: Standard deviations of FET parameters (4000 nMOS, 2000 pMOS) shown separately for each variability source. Geometrical variations due to LWR, STI recess, and epitaxial growth affect the variability more severly than RDD, but MGG is the leading variability contributor.

B. SRAM Variability

BSIM-CMG model cards that accurately reproduce the variability simulated with TCAD are integrated into the PEX circuit representation of the 6T SRAM cells (111 topology). This enables high-throughput SRAM simulations with SPICE including local variability sources. As a reference, the nominal SRAM butterfly curve was simulated with both full TCAD and the TCAD-to-SPICE flow, demonstrating excellent agreement, see **Fig. 9**. The computationally expensive SRAM variability simulations were done using the TCAD-to-SPICE flow, showing approximately normally distributed static noise margins (SNM) across technologies and variability sources, see **Fig. 10**. A broad range of these SRAM simulations were conducted and the write-trip-points (WTP) as well as the SRAM read currents determined. The resulting distributions are given in **Fig. 11**. As expected from the study of the individual FET variability sources, MGG with large grains significantly affects the SRAM performance by increasing the variability of all key performance indicators (KPIs). This effect is more pronounced for NS SRAMs, which show a larger increase in variability with increasing grain sizes compared to FinFET SRAMs.

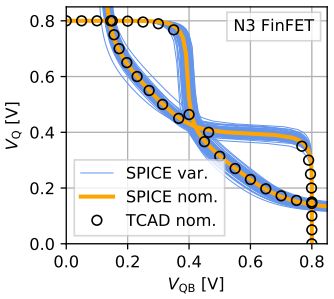

Fig. 9: Butterfly curves of 6T SRAM cells in N3 FinFET technology with $V_{\text{DD}} = 0.8$ V. Nominal simulations are compared for full TCAD (circles) and the TCAD-to-SPICE flow (thick orange line). The latter is also used for the variability simulations (thin blue lines).

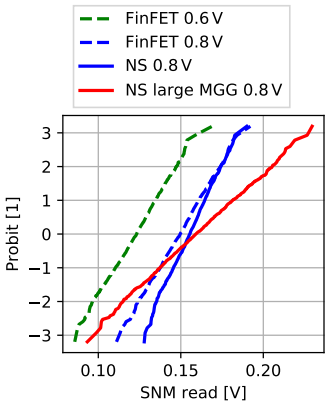

Fig. 10: Probit plot showing normally distributed SNMs of N3 SRAM cells simulated with SPICE based on TCAD variability.

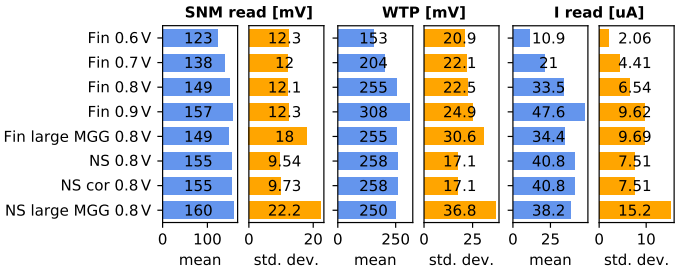

Fig. 11: Mean (blue) and standard deviation (orange) of N3 SRAM KPIs in 111 topology simulated with SPICE based on TCAD variability. V_{DD} as indicated in the labels. All variability sources (RDD, MGG, geometrical variations from LER, STI recess, epitaxial growth) are considered in each row. "cor" denotes correlated geometrical variations of all nanosheets within the same FET and "large MGG" is for average grain size of 22 nm, all others being with 10 nm. Compared to N3 NS, the FinFET SRAMs are slightly less affectey by MGG-induced variability for large grains while the opposite is true for small grains.

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VI. Conclusions

A TCAD-enabled high-throughput DTCO flow has been applied for the accurate study of SRAM statistics under various local variability sources. Based on N3 process assumptions for FinFET and NS technologies, the impact of RDD, MGG, as well as geometrical variations due to LWR, STI recess, and epitaxial growth was analyzed for FETs and SRAM cells. Given the low channel doping, RDD has a small impact compared to the other variability sources. MGG is the overall dominant source of variability for grain sizes as reported for standard TiN processes and the reduction of metal gate grain sizes is crucial to reduce variability at N3 for both FinFET and NS technologies.

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