The Device and Circuit Level Benchmark of Si-Based Cold Source FETs for Future Logic Technology

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***Abstract*— Si-based cold source field-effect transistor (CSFET) combines the benefits of sub-60-mV/dec steep-slope switching, high I_{ON} current, and compatibility with current Si CMOS process technology. Therefore, it is a promising candidate for future energy-efficient logic technology. For the first time, we present device and circuit benchmark of Si-based gate-all-around (GAA) CSFET versus conventional GAA MOSFET. The device's characteristics are first generated using a calibrated multiscale TCAD framework. Then a novel SPICE device compact model based on neural network is created to capture the unique CSFET $I-V$ and $C-V$ data with high precision. This SPICE model further enables the circuit benchmark simulations. Through this approach, it is identified that compared with GAA MOSFET, Si-based GAA CSFET shows up to 67% performance/power gain for a supply voltage (V_{dd}) below 0.43 V in an ideal gate-loaded ring oscillator circuit. It is 70% more energy-efficient in the capacitive-loaded fan-out of 4 (FO4) inverter circuit. Finally, the comparisons of GAA CSFETs with different nanosheet widths are accomplished for design technology cooptimization (DTCO) purpose.**

***Index Terms*— Circuit benchmark, device compact model, gate-all-around (GAA) MOSFET, Si-based GAA cold source field-effect transistor (CSFET), TCAD simulations.**

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I. Introduction

FASTER speed and better energy efficiency (EE) are always desired for future logic technology. This requires continuous scaling of V_{dd} while maintaining low leakage and high I_{ON} of transistor. Current MOSFET is subjected to the thermal limit of 60 mV/dec subthreshold swing (SS), restricting V_{dd} scaling; tunneling field-effect transistor (TFET) is advantageous for steep SS but usually suffers from low I_{ON} and higher operation variability [1]–[4]. Recently, a specialized field-effect transistor (FET) with energy filtering mechanism, namely, cold source FET (CSFET), appears to be a promising candidate to break Boltzmann's limit and keeping relatively high drive current [5]–[7]. Multiple types of CSFETs have been theoretically predicted or fabricated, in which notable subthermionic switching is obtained by source engineering to cut off the Boltzmann tail of carrier distribution [5]–[7]. Nevertheless, the development of CSFET is still in its early stage, and nonideal factors including in-elastic phonon scatterings of carriers and trap-assisted leakage still need further considerations. To our knowledge, all works to date still stay in the material and single device level. To identify its potential for future logic technology, it is appealing to quickly benchmark the CSFET with the corresponding MOSFET not only in the device level but also in the CMOS circuit level.

To this end, we design and characterize complementary pair of Si-based gate-all-around (GAA) CSFET (CSFET for short) using full quantum mechanical transport calibrated TCAD. Then a novel SPICE compact device model based on multi-gradient neural network (MNN) is developed to accurately capture the device electrical properties, e.g., unique $I-V$ and $C-V$, attributed to special band alignment and energy filtering in CSFET. Using this model, logic circuit simulations have been accomplished to benchmark GAA CSFET with

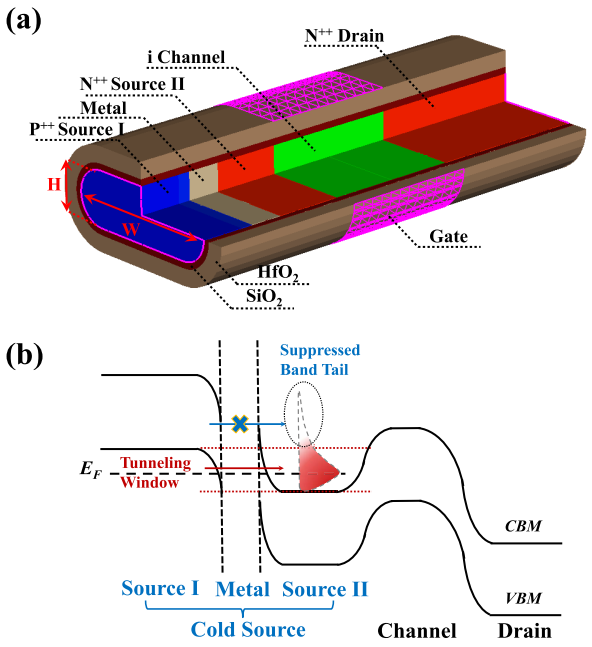

Fig. 1. (a) Schematic of GAA CSFET. (b) Energy band diagram of Si GAA-CSFET with energy filtering effect in the source.

conventional GAA MOSFET. Finally, CSFET with different nanosheet widths are also studied to demonstrate further device and circuit optimization opportunities.

II. Device-Level Benchmark

We focus on the Si-based CSFET compatible with the mainstream process technology. In a Si GAA-CSFET, the energy filtering source is presented as a sandwich structure composed of p^{++}Si/metal/n^{++}Si (n^{++}Si/metal/p^{++}Si) for nMOS (pMOS) as shown in Fig. 1(a). Heavily n-type-doped (3×10^{20} cm^{-3}) and p-type-doped (3×10^{20} cm^{-3}) regions are required to achieve broken-gap-like band alignment. The injected carriers from *Source I* distribute in the tunneling window, and therefore high energy tail is filtered out as shown in Fig. 1(b). The metal layer is inserted so as to enhance the cold carrier injection efficiency with lower and thinner tunneling barrier compared with TFET [7]. To prevent rethermalization of cold carriers in the metal and Source II, the phonon-limited mean-free path (MFP) in the cold source is investigated using molecular dynamic Landauer (MDL) approach [8] implemented in QuantumATK [9], [10]. It is verified that the phonon-limited MFPs of electrons are 21 and 36 nm in silicon and metal Au nanowire structures, respectively, in consistency with previous reports [8], [11]. Therefore, the cold source is carefully designed with metal of 3 nm and Source II of 6 nm, both well below their respective MFPs, ensuring ballistic transport of cold carriers in the source region. Note that TiN with MFP >40 nm is also a possible candidate to be used to replace the inserted metal.

The overall TCAD model framework used here is similar to our previous works [12], [13], including a key in-house effective cold carrier distribution model. The Philips unified mobility model with degradation at the interface is

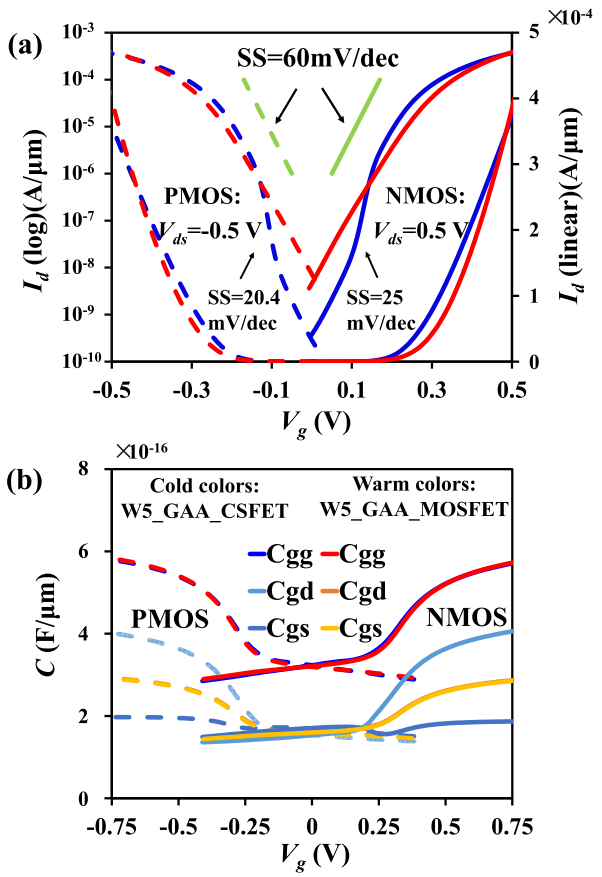

Fig. 2. (a) $I_d - V_g$ transfer characteristics of W5-GAA-CSFET (blue) compared with conventional GAA FETs (red). Green lines indicate SS = 60 mV/dec for reference. (b) C–V_g of CSFETs (cold colors) with conventional GAA FETs (warm colors).

implemented. The driven force of the high-field mobility is the electric field parallel to the closest interface. This framework is systematically calibrated with Nonequilibrium Green's Function—Tight Binding (NEGF-TB) package of Nanoskim [14]. GAA-CSFETs with a gate length L_g of 12 nm, a channel thickness H of 5 nm, and a channel width W of 5 nm/10 nm/15 nm are investigated, referred as W5/W10/W15-GAA-CSFET, respectively. The lengths of Source I/metal/Source II are 5 nm/3 nm/6 nm, and the gate dielectric thickness of SiO_2/HfO_2 is designed to be 0.6 nm/1.5 nm [15]. All devices' data are normalized by their electrical gate width for comparison. The conventional GAA counterparts are under the same structure with homogeneous source.

Fig. 2(a) shows the representative $I_d - V_g$ transfer characteristics of W5-GAA-CSFET compared with the conventional GAA MOSFET of same width, both in linear and logarithmic scales. As V_g decreases, the barrier in the channel becomes higher than the maximum energy of injected cold carriers [see Fig. 1(b)]. The current drops rapidly, since the hot carriers in the high-energy Boltzmann tail are effectively filtered out by the cold source. As V_g keeps lowering, the thermal current has already been effectively suppressed and the SS recovers. This mechanism exhibits a unique sharp slope around band alignment between valence band maximum (VBM) of *Source*

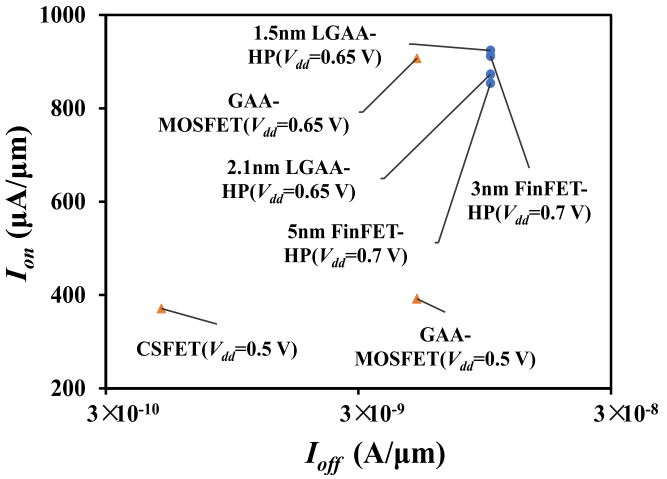

Fig. 3. Comparison of key parameters (ON-state current versus OFF-state current) between our TCAD data (orange triangle) and 2020 IRDS prediction (blue circle) for devices in different technology nodes.

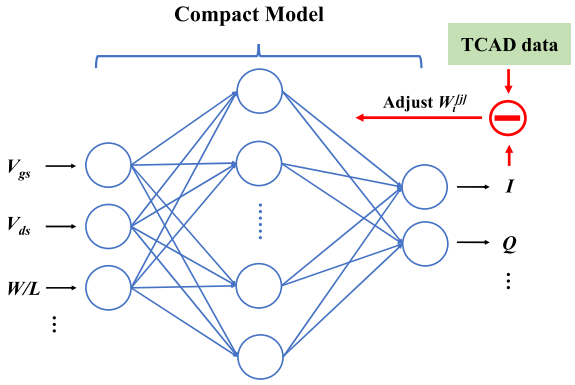

Fig. 4. Illustration of the feed-forward neural network compact device model.

I and conduction band minimum (CBM) of *Source II*, with a minimum SS of ~24 mV/dec and an average SS of 49 mV/dec. Fig. 2(a) further shows that I_{ON} of W5-GAA-CSFET is 3.62 × 10^{-4} (A/μm)/3.71 × 10^{-4} (A/μm) for pMOS/nMOS, and that of W5-GAA-MOSFET is 11.66%/5.61% higher. I_{OFF} of W5-GAA-CSFET is 2.19 × 10^{-10} (A/μm)/3.66 × 10^{-10} (A/μm) for pMOS/nMOS, while I_{OFF} of MOSFET is more than one order of magnitude higher at similar V_{th}. The $C-V$ characteristics (V_{ds} = 0 V) of both the devices are shown in Fig. 2(b). C_{gd} and C_{gs} of W5-GAA-CSFET are asymmetric due to their unique source structure, while the difference in C_{gg} between CSFET and MOSFET is small due to the similar device geometry. Similar to TFET devices, the asymmetry between the source and the drain of the CSFET ($C_{gd} > C_{gs}$) could introduce additional effects in the circuit operations such as the overshoot and undershoot in the ring oscillator (RO) operation, similar to that in TFET [16].

The key device parameters of our device are compared with the 2020 IRDS predictions for future GAA technology [17] (see Fig. 3). Our GAA MOSFET data match well with that of high-performance (HP) lateral GAA (LGAA) and FinFET predicted in 2020 IRDS for V_{dd} of 0.65 V, as the ON-state current is almost equal, while the OFF-state current differs only by 4.89 nA, demonstrating the validity of our TCAD methodology and results. Fig. 3 shows that the ON-state current of CSFETs is close to that of GAA-MOSFETs at V_{dd} of 0.5 V, while the OFF-state current of CSFETs is almost an order of magnitude lower than GAA-MOSFETs. Finally, it is possible to integrate cold source structure to lateral nanosheet process flow by replacing the standard source/drain epitaxy module with cold source/drain formation module [18]. Further work is needed to address the detailed material and interface processing issues in CSFET larger scale manufacture.

III. SPICE Device Compact Model Creation

Section II explained the mechanism and the unique electrical characteristics of the CSFET devices qualitatively and quantitatively, using simplified band diagrams, Fermi distributions, and calibrated TCAD simulation results.

Furthermore, inspired by a pioneering work [19], dense $I-V$ and $C-V$ data generated by TCAD are used to construct an accurate MNN-based device compact model (MNNDCM) for circuit simulation [20]. Fig. 4 shows a schematic of model architecture and fitting principle. An improved back-propagation algorithm with an automated procedure developed in-house was used for model parameter extraction. The extracted MNNDCM was then implemented in Verilog-A for the Synopsys HSPICE simulator to enable circuit simulations. This approach conveniently links the novel device performance and circuit simulations without the need to invent various sophisticated compact CSFET models for different devices and their required manual fitting.

MNNDCM is demonstrated to precisely capture $I-V$ and $C-V$ of all the devices. Fig. 5 illustrates an example of MNNDCM fit to W10-GAA-CSFET TCAD data. Only linear and saturation I_d-V_g are shown in Fig. 5(a); in reality, all I_d-V_g with V_{ds} step of 0.05 V were fitted from 0 V to V_{dd}. Fig. 5(a) depicts the fitting results of the MNNDCM from linear and logarithmic coordinates, and it is easy to find that even in the subthreshold region where I_d is very small, MNNDCM can quite accurately fit the TCAD data. Fig. 5(b) shows the fitting results for I_d-V_{ds}. Overall, the $I-V$ data over seven orders of magnitude are fitted with the largest error smaller than 5%, among all biases including the near-threshold voltage transition and subthreshold region. To obtain a more accurate compact model, it is not only necessary to fit the $I-V$ characteristics of the transistor but also to accurately fit its transconductance G_m and conductance G_{ds}. Among them, G_m is the differential of I_{ds} to the gate bias V_{gs}, and G_{ds} is the differential of I_{ds} to the drain voltage V_{ds}. MNNDCM is also fully differentiable, Fig. 5(c) and (d) are the model play-back of G_m and G_{ds} compared with data, and they are also well-captured. The accurate fitting of G_m and G_{ds} will be very helpful for the designs of analog and RF circuits. Fig. 5(e) shows the $C-V$ model fit to data; note that C_{gd} and C_{gs} of CSFET are separately modeled due to the device asymmetry, and the largest error is also within 5%.

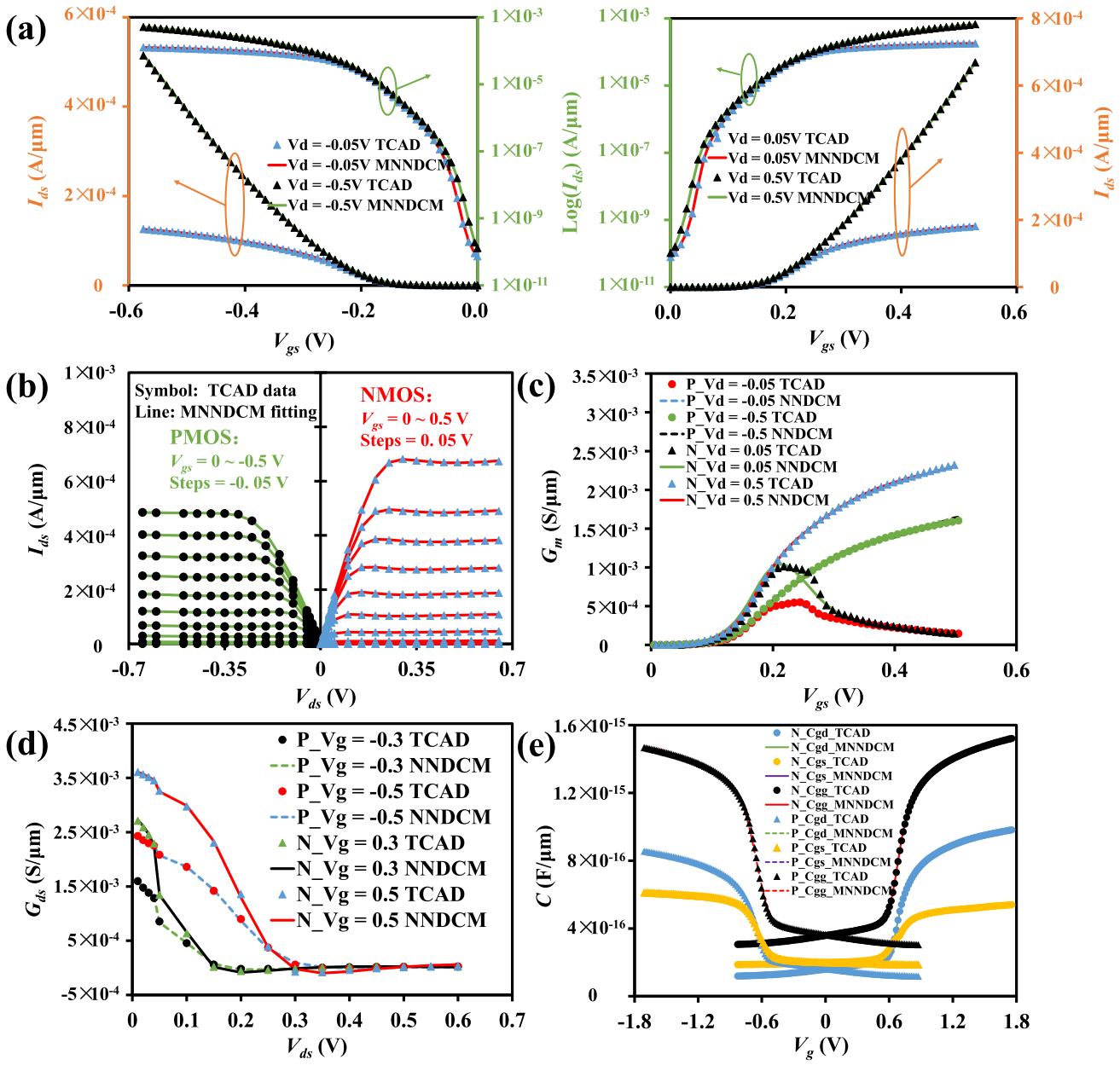

Fig. 5. MNNDCM SPICE model fitting example of CSFET TCAD data (a) $I_d - V_{gs}$ data fitting shown in linear and logarithm scale for N and P devices at linear and saturation conditions, (b) $I_d - V_{ds}$ fitting results, and (c) and (d) G_m and G_{ds} model play-back versus data. (e) $C - V$ data fitting results.

The MNNDCM SPICE models are created for all four devices in the same fashion for the circuit benchmark simulations.

IV. Circuit-Level Benchmark Results

The inverter circuit composed of 5-nm p-CSFET and n-CSFET is first studied for dc simulation, as shown in Fig. 6(a). Different from the case of TFET, V_{out} of the CSFET inverter shows no degradation in voltage transfer characteristics (VTCs) as exhibited in Fig. 6(b), due to negligible ambipolar effect of CSFET [13]. In addition, the CSFET-based inverter shows a high voltage gain $\Delta V_{out}/\Delta V_{in}$, the highest gain of 100 is obtained at $V_{dd} = 0.6$ V, and a gain of 5 is still achieved at $V_{dd} = 0.1$ V.

Furthermore, 19-stage RO is simulated for both W5-GAA-CSFET and W5-GAA-MOSFETs to examine the device characteristics' impact on the gate-loaded ideal circuit. Fig. 7(a) shows the RO circuit schematic, and the simulation benchmark results are shown in Fig. 7(b) and (c). Different from the traditional TFET [21]–[23], the performance of CSFET benefits from both steeper SS and high I_{ON}. Fig. 7(b) gives the delay versus V_{dd} comparison. The CSFET shows performance benefit for V_{dd} between 0.18 and 0.43 V, with a maximum gain of ~67% at 0.25–0.3 V. For $V_{dd} > 0.43$ V, MOSFET is advantageous attributed to slightly larger I_{ON}, and CSFET current is too weak for circuit operation in the deep subthreshold regime for $V_{dd} < 0.18$ V. Fig. 7(c) shows the power versus delay tradeoff; W5-GAA-CSFET exhibits lower power consumption than that of the corresponding MOSFET for

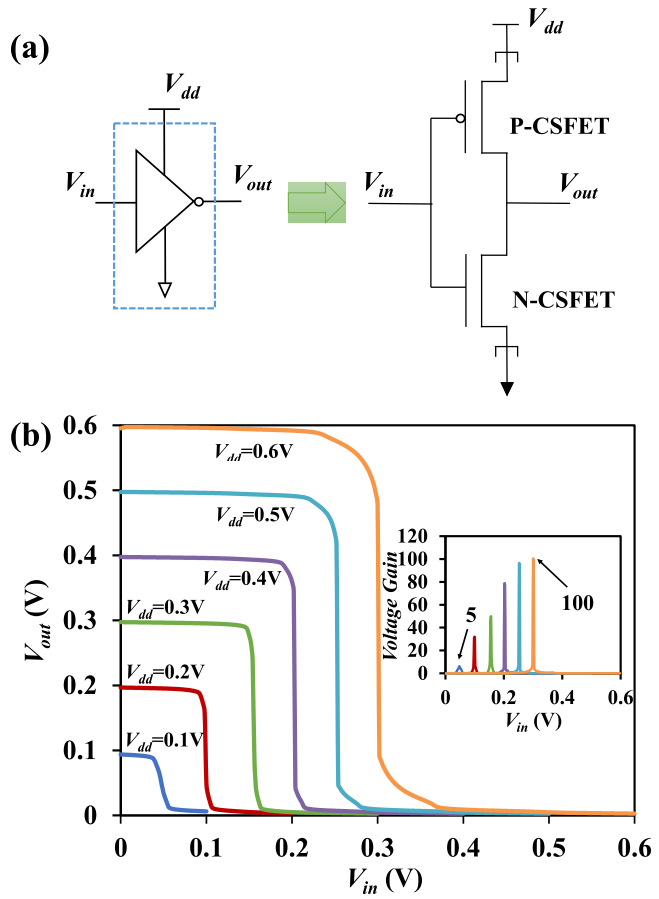

Fig. 6. DC simulation of an inverter. (a) Inverter circuit schematic. (b) VTC and voltage gain for W5-GAA-CSFET.

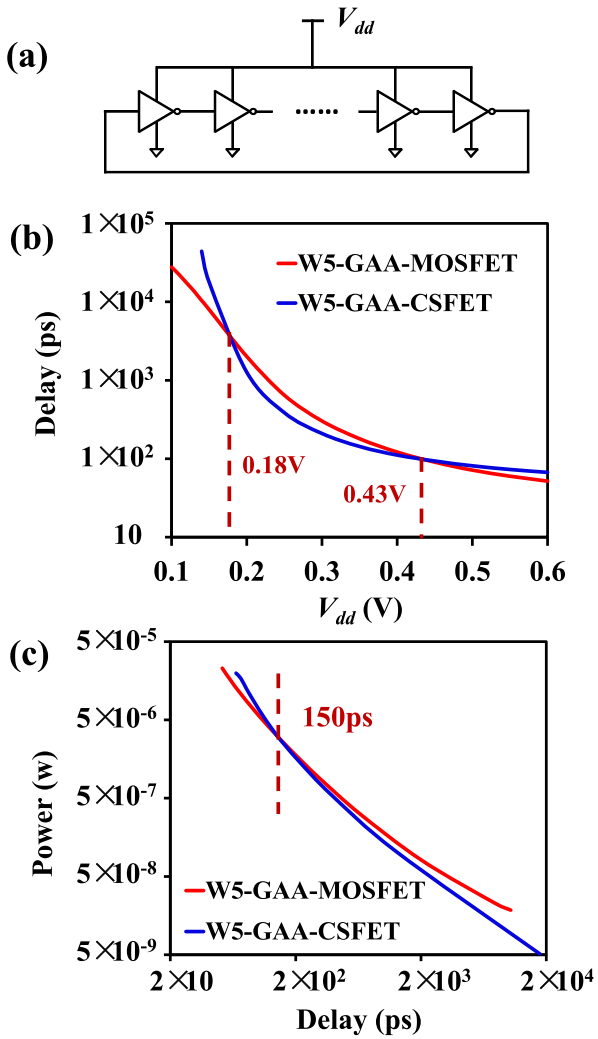

Fig. 7. Nineteen-stage gate-loaded RO simulation. (a) RO circuit schematic. (b) Delay at different V_{dd}. (c) Power versus delay.

delay above 150 ps. In the faster operation regime of such ideal RO, MOSFET shows better performance due to large I_{ON} for large V_{dd} above 0.43 V. While the results shown in Fig. 7 are assumed of RO with a duty cycle of 10%, the trend is largely unchanged for duty cycle of 50%.

To better mimic the real logic circuit usage case, fan-out of 4 (FO4) inverter with capacitive load is also simulated [24], [25]. Taking local interconnect wire cap into consideration, a 10-fF capacitive load C_L is chosen for the FO4 circuit as shown in Fig. 8(a). Fig. 8(b)–(d) are the simulation benchmark results. The total energy is defined as the sum of the static energy and the dynamic energy, the latter of which is proportional to the logic activity factor (AF). Both 1% and 20% AF are simulated to represent different product usage scenarios. While Fig. 8(b)–(d) mainly focuses on the 1% AF case, the conclusions are largely unchanged for 20% AF case. The delay under different V_{dd} is shown in Fig. 8(b). When the supply voltage is more than 0.2 V, W5-GAA-CSFET has an advantage over W5-GAA-MOSFET in delay. When the supply voltage is less than 0.2 V, because the drain current of W5-GAA-CSFET decreases rapidly, it is difficult to drive the capacitive load, and the delay of device presents a sharp increase.

In this work, the EE is defined as the performance/watt, where "performance" is characterized by the inverse of delay in the FO4 circuit, and "watt" is characterized by the power consumption. The performance/watt is obtained by the following equation:

$$\frac{\text{performance}}{\text{watt}} = \frac{1}{\text{delay} * \text{power}}. \quad (1)$$

As shown in Fig. 8(c), the EE for CSFET is about 70% higher than that of MOSFET with the same geometrical dimension for relevant V_{dd} around 0.4 V, due to its lower leakage and better I_{ON}, while EE of CSFET drops quickly for V_{dd} smaller than V_{th} since the steep SS causes CSFET current too small to drive the capacitive load for the subthreshold circuit operation. Fig. 8(d) shows that W5-GAA-CSFET can be ~40% faster at the same energy consumption or consume ~35% lower energy at the same speed than that of W5-GAA-MOSFET in the FO4 circuit, referenced at the relevant V_{dd} between 0.4 and 0.5 V. This result demonstrates the practical advantage of CSFET in the future low-power logic operations.

In addition, to further demonstrate the device and circuits' cooptimization opportunities for CSFET, we have also done device and circuits' evaluations for CSFETs with different widths. The results are summarized in Table I. I_{ON} shows an

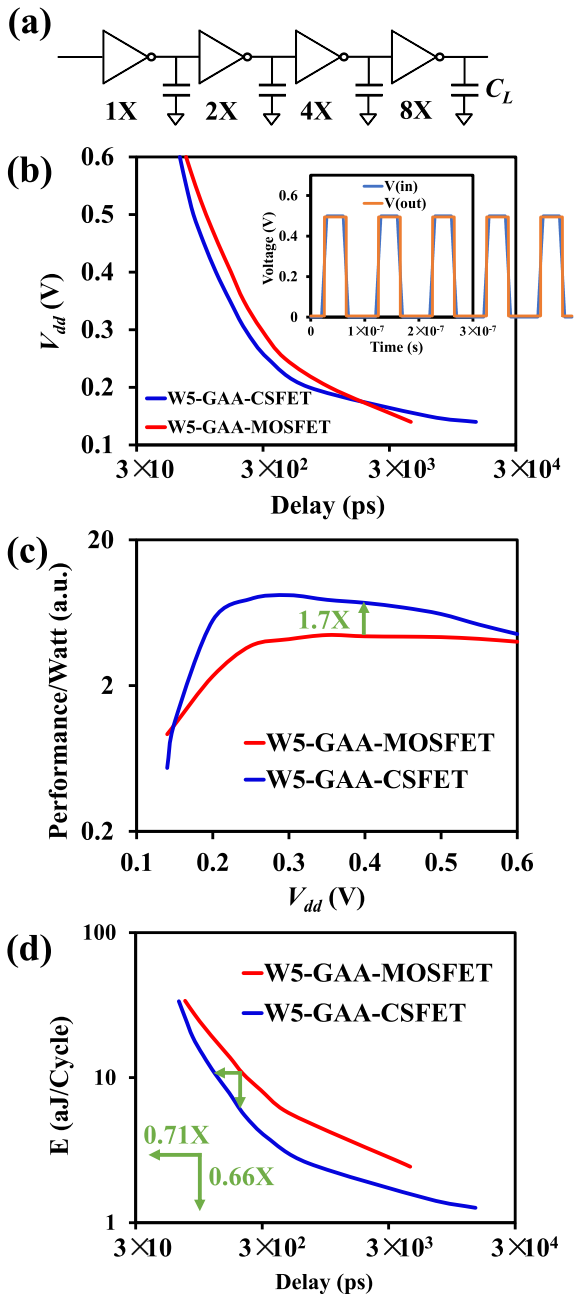

Fig. 8. Capacitive-loaded FO4 inverter simulation. (a) FO4 circuit schematic. (b) V_{dd} versus delay relationship, example waveform shown in the inset. (c) EE benchmark. (d) Energy versus delay tradeoff.

TABLE I
COMPARISON OF W5-GAA-MOSFET AND W5/W10/W15 GAA-CSFET

Device	W5-MOSFET	W5-CSFET	W10-CSFET	W15-CSFET
I_{on}[uA/μm] (P/N)	198/178	206/211	271/306	294/340
I_{off}[nA/μm] (P/N)	5.32/3.49	0.28/0.38	1.35/2.48	1.97/3.37
C_{gg}[aF/μm] (P/N)	0.49/0.47	0.51/0.51	0.46/0.45	0.44/0.43
SS(min)[mV/dec] (P/N)	63.8/63.3	20.4/24.9	25.4/31.6	26.2/30.6
FO4 Perf./Watt[a.u.] *	4.35/0.67	7.40/1.05	8.28/0.97	8.51/0.98
* FO4 EE numbers are for 1% activity factor/20%activity factor.				

improvement from 5- to 15-nm width for GAA CSFETs, by a percentage of 42.71%/61.14%; while I_{OFF} also increases by 6.03×/7.87×. Overall, FO4 EE improves as the device width enlarges. This shows that the optimization can be done to further improve the CSFET circuit performance with device geometry fine-tuning.

V. CONCLUSION

We present device and circuit benchmark of Si-based GAA CSFET versus conventional GAA MOSFET. The results show that Si-based CSFET could achieve higher EE, faster speed, and lower energy consumption in gate-loaded and capacitive-loaded logic circuits in scaled V_{dd} for future lower power operations, rendering it a promising candidate in the future logic technology road map. GAA CSFETs with different nanosheet widths are also evaluated for further optimization opportunity.

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