Design Enablement: The Challenge of Being Early, Accurate, and Complete

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Abstract

Progress evidenced by Moore's Law has driven increased performance at decreased cost per function. Often, the price of this progress is balanced against complexity and time-to-market (both directly impacting cost). Design enablement teams must mitigate these cost factors by delivering accurate process design kits (PDKs) that predict both process and device performance at production on a schedule that supports time-to-market goals. Here, we examine some key technology issues affecting the critical relationship between process, device, design and products.

Introduction

Over time, semiconductor device and product complexity have risen sharply. Market demands (Fig. 1) have increased significantly; 100M gate ASICs are common. Meanwhile, design teams face aggressive product life cycles that are the shortest of any industry [1]. Future requirements are clear: designers must deliver increasingly complex low cost-per-function chips to market faster.

One way to enable earlier product delivery with shorter design cycles is to provide PDKs to design teams earlier in the design cycle, and improve the accuracy of those kits. This allows for less design rework. Since the PDK essentially represents a contract between manufacturing and design, early delivery can be problematic. Fig. 2 illustrates the tradeoff between development uncertainty and design rework risk as a function of time.

Innovation and Uncertainty

Semiconductor process and device innovation are critical for cost-per-function improvements, but they have inherent risk. Uncertainty in device performance and process parameters means model accuracy is a function of time [2]. From a design perspective, kit inaccuracy and design rework inevitably lead to time-to-market delays. When considering future technology nodes (e.g. 14nm), several interesting examples are apparent. Four of many possible examples are highlighted here by way of illustration.

Lithographic Challenges

Lithography technology has always had a direct impact on "node timing" and delivery. For the 14nm node, it may be necessary to transition to Extreme Ultra-Violet (EUV) lithography to avoid the potentially prohibitive costs of triple patterning [3]. However, significant challenges remain for EUV regarding mask defects and source power, with the latter being approximately one order of magnitude short of the needed flux for production [4]. As a result, the lithography solution for 14 nm production remains unclear (delayed at best), and generally unavailable for process development [5]. Uncertainty results, impacting process development, modeling, design kit accuracy and delivery.

Noise Challenges

Since noise generally scales inversely with device area, noise modeling will be an increasing challenge at 14 nm and beyond. For example, Fig. 3 shows the noise spectral density variation across three bias values for a given gate area WL = 0.01 mm^2 for multi-die. Noise variability of > 500X is observed across all biases, indicating higher 3-sigma/mean values for noise. This variation is seen both for SiON and high-K metal gate (HKMG) planar technologies. A dynamic SPICE model with statistical distribution is required to capture this effect, again impacting model and kit complexity [6].

Another well-known phenomenon is the discretization of 1/f noise to $1/f^2$ (known as Random Telegraph Signal or RTS). This is mainly due to the presence of single interface traps. Fig. 4 shows the time domain signal of the drain current which has a clear bimodal distribution of the amplitude. This aspect of noise becomes critical for SRAMs where extreme RTS is known to cause failing bits, resulting in yield issues. How process engineers will minimize this effect and how design kits will model this behavior are questions that impact design kit availability.

Scaling Impact On ESD

Choices made at the device level can have profound impact at the circuit level. For example, technology scaling has dramatically reduced the available ESD Design Window for Human Body Model (HBM), especially in high-speed designs [7]. Fig 5 illustrates that as technology moves towards the 22nm node, the reduction in both the ESD-domain gate oxide breakdown voltage and the metal current density have a combined impact on the ESD circuit design margin. This consequently reduces the ESD HBM levels to 1kV and lower. As a result, scaling-related ESD challenges may impact kit availability.

Context Dependence Challenges

The sensitivity of transistors to nearby geometries has been increasing with each node. These variations are a function physical design, which allows them to be modeled. Area scaling brings actives into closer proximity, resulting in increased interaction between stressor (e.g. isolation, SiGe, etch liners, etc.) Fig 6 illustrates the effect of nearby wells on the drive current of standard core CMOS transistors node over node. Comprehensive equations are required to model the various interactions of the stronger context effects as dimensions scale down in future nodes.

Summary

Early delivery of accurate design kits is critical for design. However, introduction of new materials, observation of new phenomena and delays in availability of production technology make that goal increasingly challenging.

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Moore's Law – SoC Trends

Technology	65nm	40nm	28nm	20nm	14nm
Scale from 65nm	100%	62%	43%	31%	22%
Route Pitch	210	126	90	~70	~50
Raw Mgates/mm^2	0.7	1.8	3.6	5.9	12.6
20x20 die gates (10^9)	0.3	0.7	1.4	2.3	5.0
mid-size ASIC target Mgates	32	82	167	270	580
Block K-Instances	1	3	7	11	23

Fig 1. Design trends from 65nm to 14nm showing almost an order of magnitude increase in complexity as measured by number of gates, critical dimensions, and other design metrics. 12 billion gates on 20mm x 20mm die.

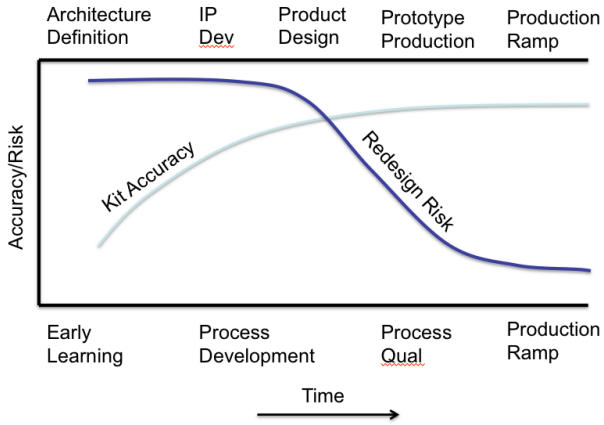

Fig 2. Relationship between kit accuracy (a function of process maturity) and redesign risk. Earlier kits are critical to enable short time to market. Adapted from Mansfield, et. al [2]

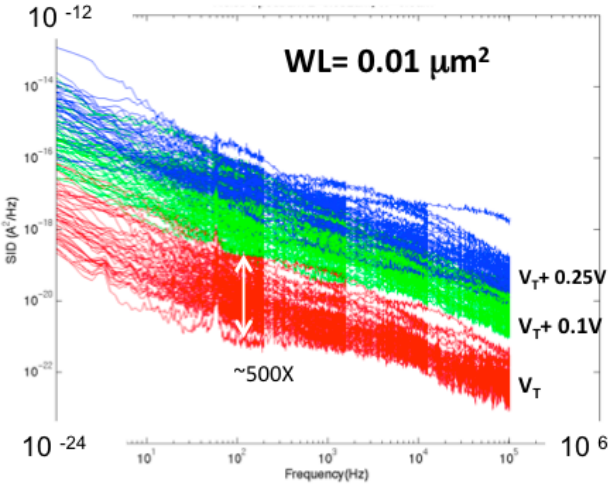

Fig 3. The noise spectral density variation across three bias values for a given area WL = 0.01 µm^2 for multi-die. Noise variability of > 500X is observed.

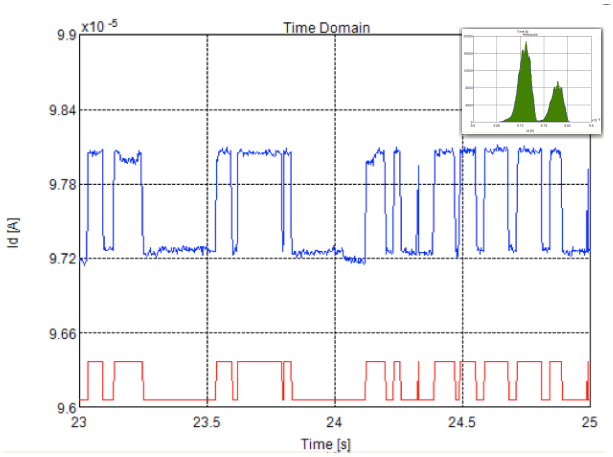

Fig 4. Time domain signal of the drain current, showing the bimodal distribution of the amplitude (inset). This is classic Random Telegraph Signal (RTS) noise. A 28nm-class short channel device data is shown.

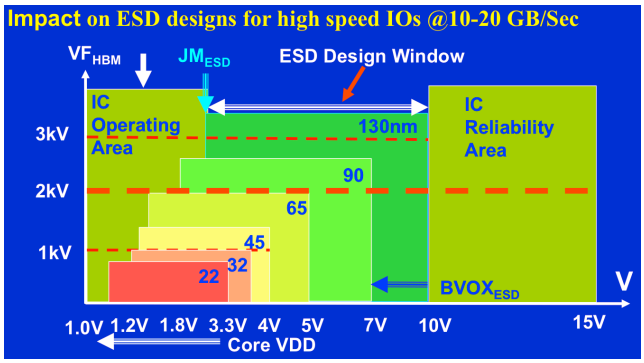

Fig 5. Shrinking ESD design window for HBM in high speed IOs. Gate oxide breakdown and metal current density constraints are making the design window vanishingly small.

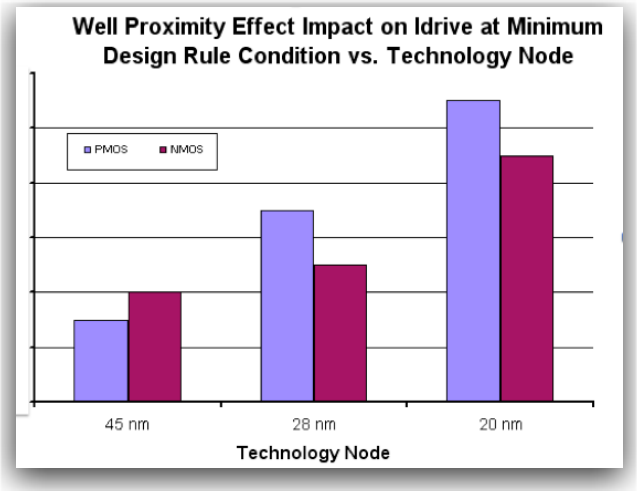

Fig 6 Well proximity effect impact on Idrive has doubled over the last two nodes. Relative percent Idrive error is plotted in the y-axis for a minimum transistor at each node from 45nm thru 28nm.