Towards Physics-Based DTCO for Performance of Advanced Technology Nodes

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***Abstract*—We present a case study which shows the path towards design-technology co-optimization (DTCO) based on physical device modeling as opposed to simulation based on empirical mobility models. This allows for more accurate and robust predictions of device performance, and allows to assess novel process options found in 7 nm and 5 nm technology nodes. A more than ten-fold increase in computational efficiency brings turn-around times down sufficiently to make physical models suitable for the DTCO process.**

I. Introduction

Current work flows for design-technology co-optimization (DTCO) rely on the use of classical device simulation. As such they suffer from the same problem as classical device simulation: poor accuracy and predictive power. Typically, an entirely empirical, geometry-dependent mobility [1, 2] needs to be used in order to maintain the required accuracy. For new technology nodes, it becomes increasingly difficult for empirical mobility modeling to keep up with shrinking device dimensions and new technological approaches. We thus propose the integration of *physical device modeling* [3] into the DTCO process to resolve this problem.

II. Stress-Enhanced 7 nm Nodes

The 7 nm node uses a common channel stressing technique for both NMOS and PMOS transistors [4]. The idea is to use a SiGe strain-relaxed buffer (SRB), with moderate Ge-fraction, on which the fin is formed. A pure-Si (NMOS) fin will be tensely stressed, while a SiGe (PMOS) fin with higher Ge-fraction the SRB will be compressively stressed, thus achieving mobility enhancement in both device types simultaneously. This technique presents a completely novel technology option and is also likely to be crucial for the 5 nm node [5].

Stress values of 1.6 GPa have been reported for a $Si_{0.75}Ge_{0.25}$ SRB [4]. Such high stresses are beyond the range of validity for empirical piezo-resistivity models, mandating a physical device modeling approach.

III. Stress Simulation

Realistic 7 nm NMOS and PMOS FinFET model devices were constructed, shown in Fig. 1, with a physical gate length of 14 nm and ⟨110⟩-oriented channels. An analytical doping profile was used and a linear elasticity simulation was performed to obtain the static stress in the device due to semiconductor lattice mismatch.

The *reference NMOS* device is of pure unstrained silicon, while the *enhanced NMOS* device has a $Si_{0.9}Ge_{0.1}$ SRB, applying around 1 GPa tensile stress to the fin (Fig. 2).

The *reference PMOS* device has a pure silicon fin stressed by SiGe raised source and drain, while the *enhanced PMOS* device has a $Si_{0.9}Ge_{0.1}$ SRB and a $Si_{0.8}Ge_{0.2}$, which is compressively stressed to around 1 GPa (Fig. 3). Compared to stressing from raised S/D, the SRB-based solution is more effective and produces an almost uniform uniaxial stress field.

IV. Device Simulation

Device simulations have been performed for NMOS and PMOS using our physical-model-based GTS Nano-Device Simulator (NDS) [3, 6, 7], at the core of which lies a subband Boltzmann transport equation (SBTE) solver. A two-band $\mathbf{k}\cdot\mathbf{p}$ model was used for the NMOS devices, while a six-band $\mathbf{k}\cdot\mathbf{p}$ model with SiGe-composition dependent parameters was used for the PMOS devices. The material composition was also included in the parameters for the scattering models, which included phonons (acoustic, optical intra and inter-valley), roughness, charged impurities and alloy disorder.

The SBTE was solved in the active region of the device designated in Fig. 4, which is then fitted to the drift-diffusion/density-gradient (DD/DG) simulation of the entire device using an effective mobility [3] in each iteration step. The raised S/D resistance and leakage across the SRB are covered by the DD/DG simulation. Figure 5 shows the solution of the SBTE, i.e. the electron spectrum, for the NMOS reference device in on-state. The emission of LO phonons (dominant inter-valley process) can be seen in the spectrum.

Figure 6 shows the transfer characteristics for all four devices (NMOS/PMOS, reference/enhanced). The enhanced NMOS device shows a 33 % drain current increase w.r.t. its reference device. For the enhanced PMOS device the drain current increase amounts to 16 %; however, it must be noted, that the reference PMOS device is also strained, albeit not as effectively as the enhanced PMOS device.

The most computational effort by far is spent on the solution of the SBTE. Heavily optimized algorithms were developed that speed up the computation by more than an order of magnitude without sacrificing accuracy. This keeps the turn-around time for 7 nm transistors computations below 10 h enabling simulation of simple logic cells such as single inverters withing the same time frame, thus paving the way towards physics-based DTCO.

V. Conclusion

We demonstrated that physical device modeling is a feasible approach for current technologically relevant devices. The approach was used on the the very recent 7 nm technology node, which features a novel unified stressing technique for both NMOS and PMOS channels. The more than ten-fold enhancement in computational efficiency makes physical device modeling a viable approach for design-technology co-optimization.

Acknowledgment

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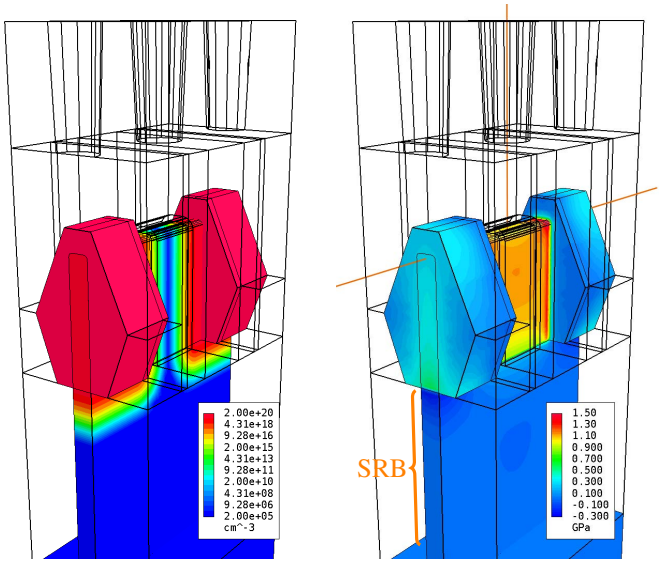

Fig. 1. Structural view of a NMOS FinFET model with doping profile (left) and axial stress (right) due to lattice mismatch between fin and SRB

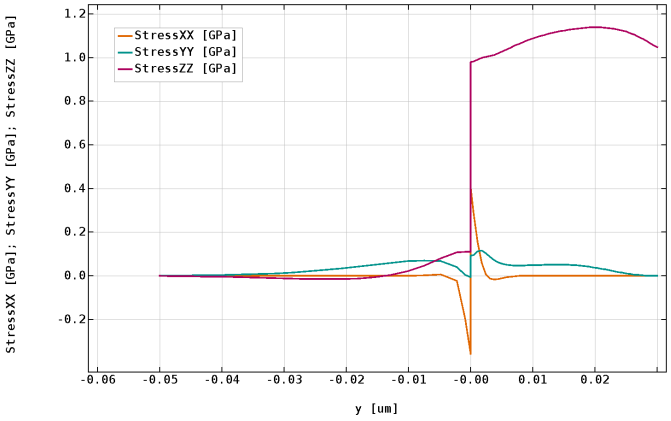

Fig. 2. Vertical stress profile in the device center for a NMOS device with pure Si grown on a $Si_{0.9}Ge_{0.1}$ SRB

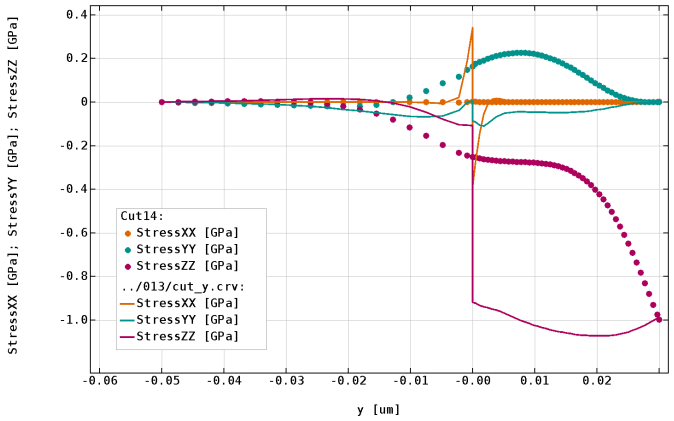

Fig. 3. Vertical stress profile in the device center for a PMOS device with pure $Si_{0.8}Ge_{0.2}$ grown on a $Si_{0.9}Ge_{0.1}$ SRB (solid line); for comparison, the stress profile for a pure Si PMOS with SiGe raised S/D is shown (dots).

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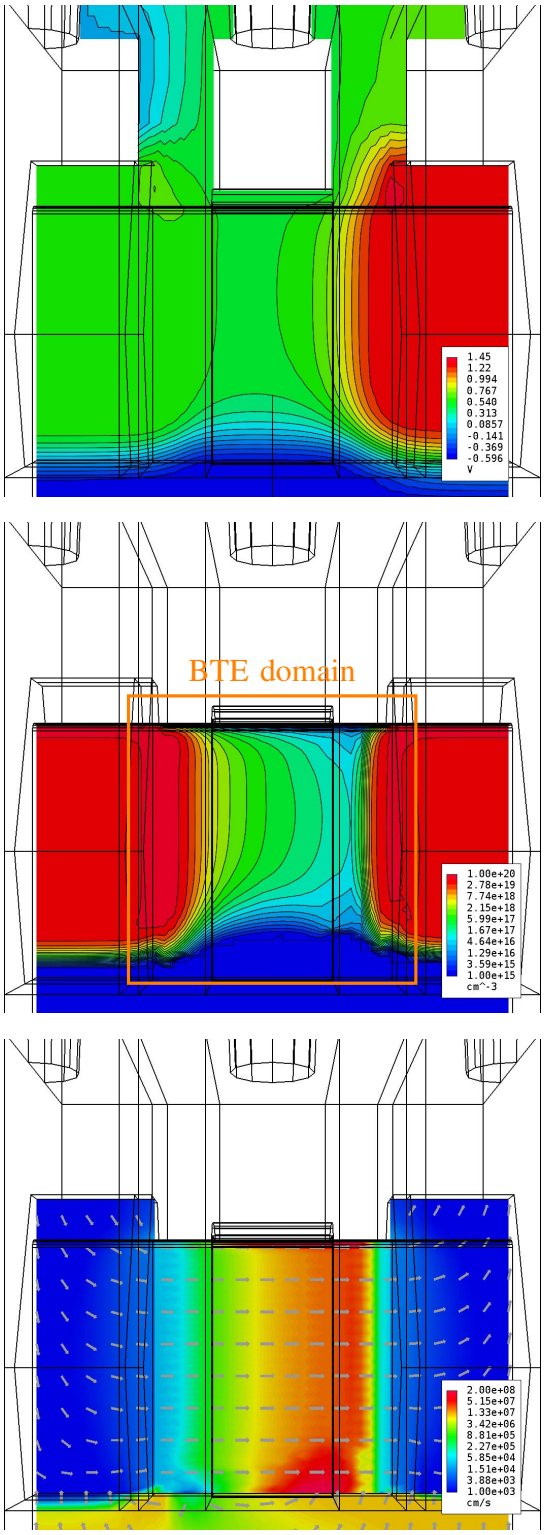

Fig. 4. Cut though the NMOS device along the fin showing electrostatic potential (top) electron concentration (middle) and average electron velocity (bottom) at $V_{GS} = 0.5\,V$ and $V_{DS} = 0.7\,V$; the orange rectangle indicated the region where the SBTE is solved, the remainder of the device being simulated with drift-diffusion/density-gradient.

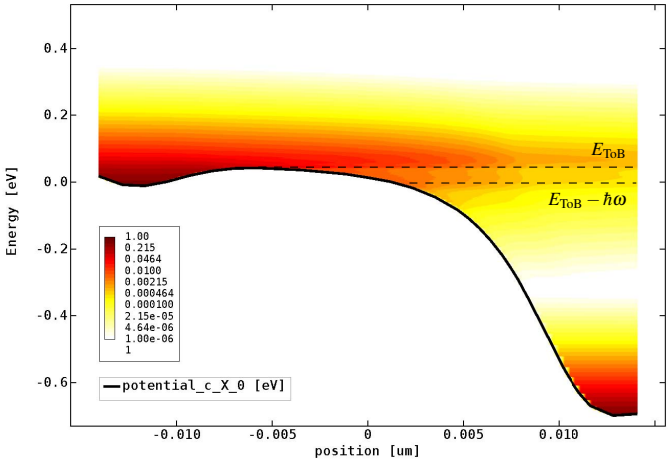

Fig. 5. Band edge profile along the NMOS device, with electron distribution shown in colors, at $V_{GS} = 0.6\,V$ and $V_{DS} = 0.7\,V$; the dashed lines indicate the top of the barrier, E_{ToB} and the energy after emission of one LO-phonon $E_{ToB} - \hbar\omega$.

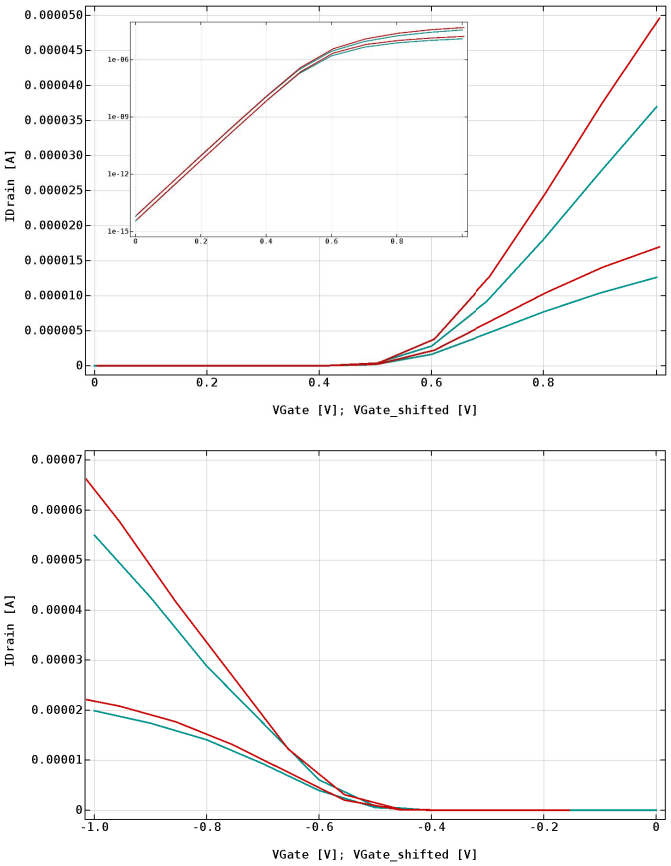

Fig. 6. Transfer characteristic for NMOS (top) and PMOS (bottom) at $|V_{DS}| = 0.05\,V$ and $0.7\,V$ enhanced device with $Si_{1-x}Ge_x$ SRB (red) and reference device (blue); the enhanced characteristics are shifted to match the respective reference devices' off-current; the enhanced devices show a 33 % (NMOS) and 16 % increase in on-current compared to their respective reference devices.