Investigation of Novel Hybrid Channel Complementary FET Scaling Beyond 3-nm Node From Device to Circuit

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***Abstract*— Complementary FET (CFET) is a promising candidate for CMOS scaling beyond 3-nm technology node. In this article, a novel hybrid channel CFET (HC-CFET) is proposed, which takes advantage of the vertical structure and simultaneously co-optimizes the preferred high-electron/hole-mobility surface of NMOS/PMOS on one substrate. The flexible combination of nanowires (NWs) and nanosheets (NSs) in the HC-CFET allows NMOS to have (100) channel surface orientation, while PMOS has (110) channel surface orientation without increasing the footprint of CFET pillars. Parasitic-aware device to circuit design-technology co-optimization (DTCO) analysis of the HC-CFET is performed based on advanced TCAD simulation of the device and comprehensive HSPICE simulation with TCAD-calibrated compact model. At the device level, the optimization of the channel surface orientation in the HC-CFET enables both NMOS and PMOS to obtain a current gain of more than 20%. By adjusting the wafer orientation and stacking type, HC-CFET exhibits higher frequency gain and comparable energy consumption in ring oscillator (RO) than multiscreen CFET (MS-CFET) and multibridge CFET (MB-CFET). After fully considering the impact of the stacking type on the static random access memory (SRAM) cell structure, (110) wafer together with n-NW on top of p-NS stack is the preferable approach to manufacture HC-CFET, which helps balance the speed, stability, and area of the SRAM cell.**

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***Index Terms*— Beyond 3-nm node, channel surface orientation, CMOS, complementary FET (CFET), gate-all-around FET (GAA FET), hybrid channel CFET (HC-CFET), ring oscillator (RO), static random access memory (SRAM).**

I. Introduction

WHEN the manufacturing process develops beyond 3-nm node, the development of the integrated circuits along with the famous "Moore's Law" encountered a series of challenges. Gate-all-around FETs (GAA FETs) have been proven to be one of the most promising successors of the FinFET to achieve better electrostatics and device performance [1]–[6]. However, the N/P spacing limits the aggressive scaling of the CMOS area. The scope of improvement in the integration density has been extended from ground rule scaling to stack devices in the vertical direction. The complementary FET (CFET) that vertically stacks NMOS and PMOS can theoretically reduce the area of CMOS by 50%. By driving on important structural parameters, CFET is proven to have application prospects at future 3-nm node and is deemed as an ultimate device architecture of CMOS scaling [7]–[11].

The state-of-the-art CFET can be classified into two categories: monolithic-CFET and sequential-CFET, which are distinguished according to the manufacturing sequence of the two-layer devices. Tighter N/P gate connections, free from thermal budget constraints, and lower cost per wafer make monolithic-CFET more attractive [12]–[14]. Benefiting from the reduction of total gate capacitance and parasitic resistance between gate contact, monolithic-CFET exhibits higher frequency of ring oscillator (RO) over standard CMOS and even sequential-CFET [15]. Feasible process flow of vertical channel stacking, vertical source-and-drain stacking, separated top and bottom contact eliciting, and also threshold regulating has been successively developed [12], [14]–[17]. To tap the advantage brought by vertical structure, there is a lot of research on the configurations of CFET, such as FinFET on top of FinFET, nanosheet (NS) FET on top of NS FET, FinFET on top of NS FET, and NS FET on top of FinFET [18], [19]. Nevertheless, those structures are based on sequential-CFET. It is very interesting to tap the advantages of vertical structure in monolithic-CFET. Until now, fin-based configuration (FBC) and sheet-based configuration (SBC) have been studied for the structure of monolithic-CFET [31], [32],

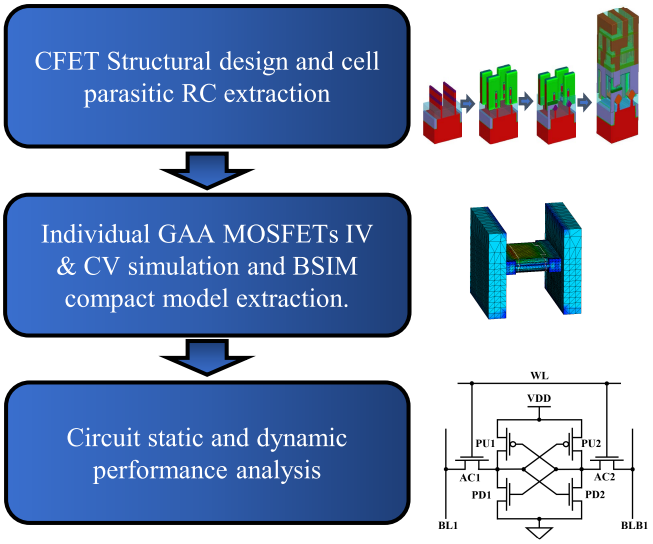

Fig. 1. Device and circuit performance evaluation methodology with parasitic-aware device to circuit design-technology co-optimization.

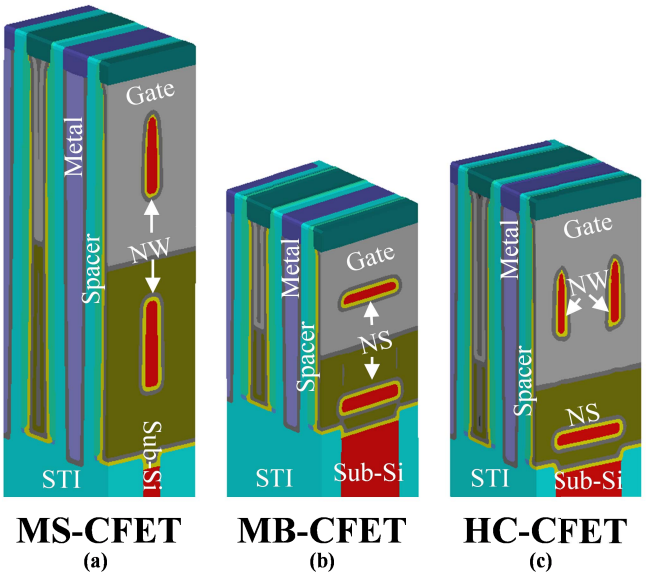

Fig. 2. Schematic of fully processed 3-D transistor structure that are (a) MS CFET, (b) MB CFET, and (c) HC-CFET.

[40]. However, they all face the problem that the channel surface orientation of NMOS and PMOS cannot be optimized at the same time, which seriously hinders the improvement of the overall performance of monolithic-CFET.

This article explores the structural advantages of monolithic-CFET and reports, for the first time to the knowledge of the authors, a novel hybrid channel CFET (HC-CFET) architecture. We propose a set of key manufacturing processes suitable for the integration of HC-CFET, which are emulated by the virtual fabrication techniques. Characteristics of devices are simulated through 3D-TCAD. By properly choosing the wafer orientation and notch direction, we have achieved (100) and (110) channel surface orientation in NMOS and PMOS, respectively. Therefore, the carrier mobility in NMOS and PMOS can be optimized to their preferable channel surface orientation at the same time. In order to evaluate the advantages of the novel HC-CFET, we simulate the 17-stage RO and the classic 6T-SRAM with parasitic. Different substrates and different stack types are considered. Based on the simulation results, we propose the optimal substrate and stack type for manufacturing HC-CFET and tap the prospects of HC-CFET in high-speed and low-power integrated applications.

II. Simulation Environment Setting

The actual manufacturing process and silicon verification are very time-consuming and costly. As inspired by design-technology co-optimization (DTCO) flow [20]–[24], we evaluated the process flow, device performance, parasitic parameters, and corresponding circuit for different structures of monolithic-CFETs, using the simulation flow shown in Fig. 1. In our work, the process probability and complexity of three different CFET pillars are taken into consideration using the virtual fabrication techniques—SEMulator3D [27]–[32]. Lateral-gate-all-around (LGAA) devices can be identified in all these CFET pillars. Those LGAA devices are simulated as common LGAA devices in bulk or silicon-on-insulator (SOI) substrate. The electrical characteristics of devices are simulated by Synopsys Sentaurus TCAD software. Taking into account the quantum effect of the beyond 3-nm node device, the drift-diffusion model is self-consistently solved by the Poisson and carrier continuity equations. To describe carrier distribution in nanowire (NW) and NS, quantum correction is carried out through the density-gradient model. Philips unified mobility, Enormal, thin-layer, and inversion and accumulation layer are used to simulate the mobility degradation. At the same time, the velocity saturation model is implemented for high gate and drain bias. Moreover, the influence of stress is considered, and Shockley–Read–Hall (SRH) recombination and band-to-band-tunneling model are also applied to account for gate-induced-drain-leakage (GIDL) current. These models are validated with the experimental data of the NS transistors [4]. Taking full use of the TCAD electrical data of all the devices, TCAD-calibrated compact models are generated by fitting the physical parameters in Berkeley short-channel insulated-gate field effect transistor model—common multi-gate (BSIM-CMG). The parasitic parameters in RO and static random access memory (SRAM) cells are accurately solved by numerical calculation in SEMulator3D. A netlist with parasitic *RC* is added to the circuit cell netlist for HSPICE simulation. HSPICE simulation is performed to give both transient and static performance of circuits. In the circuit netlist, the MOS device is represented by our TCAD-calibrated compact models. Other current sources, voltage sources, capacitances, and resistances are constructed with HSPICE internal components.

III. Novel HC-CFET Design and Device Performance Analysis

Multiscreen CFET (MS-CFET), multibridge CFET (MB-CFET), and HC-CFET are evaluated (see Fig. 2). In this article, we use "NW" to denote a vertical sheet with all-around gate and "NS" to denote a horizontal sheet with

TABLE I
DEVICE PARAMETERS FOR THE MS-CFET, MB-CFET, AND HC-CFET

Parameter	Value
Gate length (L_G)	16 nm
Effective gate oxide thickness (t_{ox})	0.808 nm (0.6nm SiO_2 + 1.2nm HfO_2)
Channel projection width (W_{ch})	30 nm
Effective channel width per sheet (W_{eff})	66.85 nm
Channel thickness (t_{ch})	6 nm
Work function (WF)	4.44(n), 4.85(p) eV

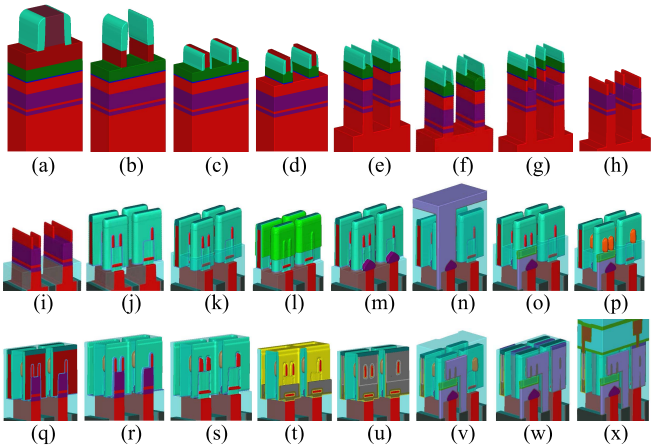

Fig. 3. Detailed HC-CFET process flow includes channel formation, fin-cut, NP/work function metal vertical integration, S/D epitaxy in monolithic way, S/D contact eliciting, and BEOL.

all-around gate. In the MB-CFET, both the top layer (TL) and bottom layer (BL) devices are NS. However, in the MS-CFET, both the TL and BL devices are NW. For HC-CFET, the TL device is NW and the BL device is NS. The proposed process flow of HC-CFET is similar to the process flow of MS-CFET and MB-CFET. In these three monolithic-CFET structures, TL devices are SOI-like devices and BL devices are bulk devices. The LGAA device's parameters are shown in Table I. Both NW and NS devices are with the gate length (L_G) of 16 nm, effective gate oxide thickness (t_{ox}) of 0.808 nm, channel projection width (W_{ch}) of 30 nm, and channel thickness (t_{ch}) of 6 nm.

A. HC-CFET Structure Design and Parasitic Parameter Analysis

The structure of HC-CFET is similar to that of the MB-CFET and MS-CFET, so that it can be fabricated using the compatible process flow that changes the channel formation steps. Fig. 3 presents the detailed process flow of HC-CFET. In the formation of Si/GeSi stacks, the thickness of the lower Si layer is defined as the lower device's channel thick, whereas the thickness of the upper Si layer is defined as the upper device's channel height, so that the upper Si layer is thicker than the lower one. Drawing on the process flow of self-aligned quadruple patterning (SAQP) [33], SiN_x hard mask (HM) is partially etched before α-Si core 2 been removed and the Si/GeSi stacks are partially etched to form the bottom channel pattern (see Fig. 3, steps 1–5). Then, top channel is formed by HM second etching and final Si/GeSi stacks etching (see Fig. 3, steps 5–8).

Buried power rail (BPR) is carried out before SD epitaxy (see Fig. 3, step 9). In order to protect the top channel during bottom SD epitaxy, it is first necessary to fill and etch the dielectric to the middle of the upper and lower layers of the channel, and then, the sidewalls that protect the top channel are made (see Fig. 3, steps 10–12). After removing the dielectric surrounding the bottom channel, the bottom SD epitaxy process can be performed without epitaxial the top channel (see Fig. 3, steps 12 and 13). The bottom self-aligned Ti silicidation step and SD contact (CNT) are then carried out followed by dielectric fill to isolate the bottom metal (see Fig. 3, steps 14 and 15). Then, the protective spacers of the top channel are removed and the top channel SD epitaxy and contact can be performed with the standard silicide-last process of NiPt (see Fig. 3, steps 16, 22, and 23) [11], [16].

After the polysilicon dummy gate was etched away using a conventional TMAH solution at 70 °C, the replacement metal gate (RMG) was performed (see Fig. 3, steps 17–21). The vertical integration of N/P work function metal (WFM) can be achieved by first depositing the WFM of the BL device, then removing the metal around the channel region of the TL device, and then depositing the WFM of the TL device [14]. The remaining processes of the BEOL are the same as the MB-CFET and MS-CFET, refer to FBC and SBC.

This process flow is easy to integrate. The top and bottom devices have channel self-alignment characteristics, which reduces the difficulty of the formation of the gate stacks. When etching the Si/GeSi stack, a slight vertical overetching can be tolerated; thus, designers can accurately control the height and thickness of the channel. Meanwhile, the effective channel widths of TL and BL devices can be adjusted separately by modulating the Si/GeSi stacks, which is very useful in device performance balancing. Moreover, in the HC-CFET pillar, the TL device naturally has two NWs within an NS, but the number of NW can be adjusted to one NW through the fin-cut process (steps 5–8 in Fig. 3). Through one step of photolithography, the top sidewall can be partially etched away, leaving a figure with two side walls in specific area and only one sidewall in another area. Then, according to the morphology of the top sidewalls to etch the SiN_x and Si channels, we can adjust the number of NWs in some areas from two to one. This flexibility and processability make great sense for SRAM designers to increase read and write performance together with noise margin.

As shown in Fig. 4, MS-CFET has the highest cell parasitic resistance, while HC-CFET has the lowest. This trend can be attributed to the change in contact resistance. Since MS-CFET and MB-CFET have the same top and bottom channel structures and need to control the lateral etch in the fine contact to a very low level, the bottom device has a limited via contact area. As a result, the larger contact area of the bottom device in the HC-CFET and the lower parasitic resistance in HC-CFET over MS-CFET and MB-CFET are expected. On the other hand, the lengthening of the wires

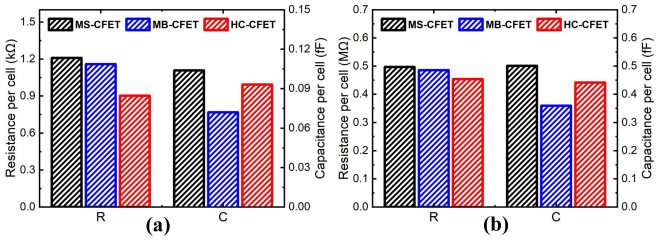

Fig. 4. Parasitic resistance and capacitance in (a) INV cell and (b) SRAM cell.

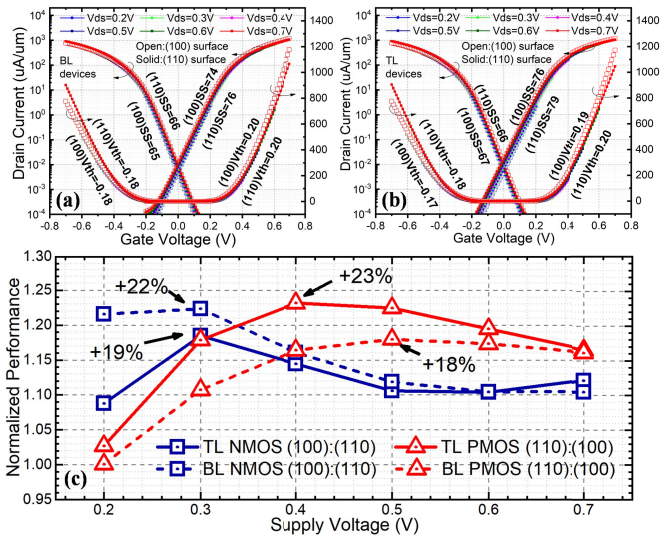

Fig. 5. I_d–V_g characteristic of (a) top-layer (TL) devices and (b) bottom-layer (BL) devices. (c) Current gain of TL and BL devices. For NMOS, the current gain is (100) ratio (110). For PMOS, the current gain is (110) ratio (100).

caused by the increase of the cell height will also increase the parasitic resistance. The difference in parasitic capacitance in Fig. 4 can be attributed to the influence of the different stack heights of the active layers. Since the stacking height of the active area of the MS-CFET, HC-CFET, and MB-CFET is decreasing, the parasitic capacitance is also decreasing.

B. Device Performance Analysis

3D-TCAD simulation was performed to get the NMOS and PMOS characteristics in different CFET pillars. The wafer surface orientation is changed to (100) and (110), but the device channel direction is maintained at <110>. In (100) and (110) substrates, the channel surface orientation of the device is dominated by (100) and (110) surfaces separately. For silicon, (100) surface provides higher electron mobility than (110) surface; meanwhile, (110) surface provides higher hole mobility [34]–[39].

According to our simulation, NMOS possess higher drive currents with (100) channel surface orientation, while PMOS possess higher drive current with (110) orientation, both for TL and BL devices [see Fig. 5(a) and (b)]. At the same time, the extracted values of the subthreshold swing (SS) and drain-induced barrier lowering (DIBL) keep almost the same. It means that the increase of the drive current due to channel surface orientation optimization will not affect the short channel effect (SCE). Fig. 5(c) shows the drive current gain of NMOS and PMOS as a function of the supplied voltages. It shows that (110) PMOS exhibits 24% (at 0.4 V) larger drive current than (100) PMOS for TL devices and 16% (at 0.5 V) larger drive current than (100) PMOS for BL devices. However, this drive current gain decreases when the supply voltage goes higher and lower. For BL NMOS, the (100) surface provides 10% (at 0.7 V) larger drive currents than (110) surface, and the drive current gain goes higher when supply voltage decreases but decreases at 0.2 V. TL NMOS exhibits the same trend as BL NMOS. For the performance change for NMOS and PMOS with the change in position as TL or BL, the parasitic channel of the BL devices can affect the performance gain from the channel surface orientation change. Under the traditional CMOS process, the shallower junction depth of NMOS and the deeper junction depth of PMOS also cause the difference between NMOS and PMOS affected by crystal orientation changes. As can be seen from Fig. 5(c), TL devices and BL devices have a similar change trend affected by the crystal orientation. This trend may support the best supply voltage range for the HC-CFET.

IV. Ring Oscillator Performance Advantage

Neither MS-CFET nor MB-CFET can optimize the channel surface orientation of NMOS and PMOS at the same time, in any type of wafer and any type of NP stack. Due to the novel structure of the HC-CFET, the channel surface orientation of NMOS and PMOS can be selected as (100) and (110) surface separately, which results in the maximum drive current of the NMOS and PMOS on the selection of the channel surface orientation. A larger drive current in RO circuits means lower charge and discharge time between the stages and thus higher frequency. We performed the 17-stage RO simulation through HSPICE.

A. RO Performance Evaluation

The impact of the different wafers and different types of the monolithic-CFET on the frequency of the 17-stage ROs performance is shown in Fig. 6, and the situation of devices' channel surface orientation is shown in Table II. In the cases of (100) wafer with NMOS on top of PMOS (N-on-P) and (110) wafer with PMOS on top of NMOS (P-on-N), HC-CFET has no advantage over MS-CFET and MB-CFET because HC-CFET shows the worst devices' channel surface orientation against MS-CFET and MB-CFET. When CFET is fabricated on (110) wafer, staking NMOS on top of PMOS is beneficial to the HC-CFET to obtain the optimal devices' channel surface orientation. Comparing to MS-CFET and MB-CFET, HC-CFET gains 12.2% (at 0.5 V) and 7.0% (at 0.3 V) improvement in frequency, respectively. For (100) wafer, the PMOS needs to be stacked on the NMOS to show benefits. In this situation, HC-CFET gains up to 16.1% (at 0.2 V) and 10.5% (at 0.5 V) improvement in frequency, compared with MS-CFET and MB-CFT separately. However, the HC-CFET does not show obvious frequency gain at all supply voltages. This is because the frequency is highly

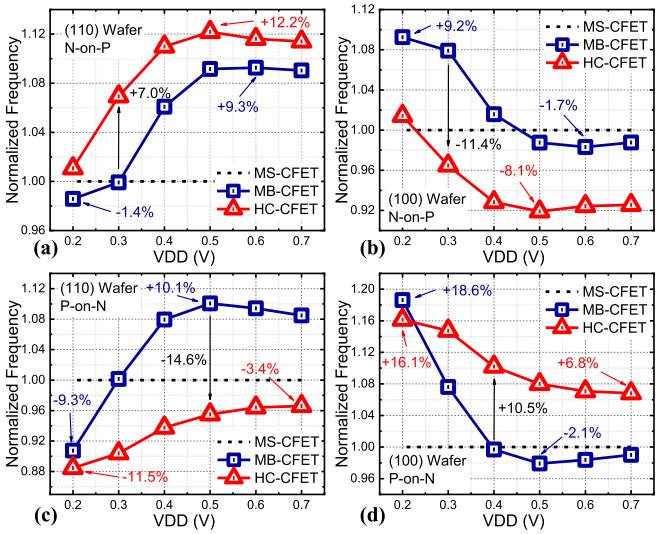

Fig. 6. Normalized frequency versus VDD of MS-CFET, MB-CFET, and HC-CFET fabricated on (a) (110) wafer with N-on-P stack, (b) (100) wafer with N-on-P stack, (c) (110) wafer with P-on-N stack, and (d) (100) wafer with P-on-N stack.

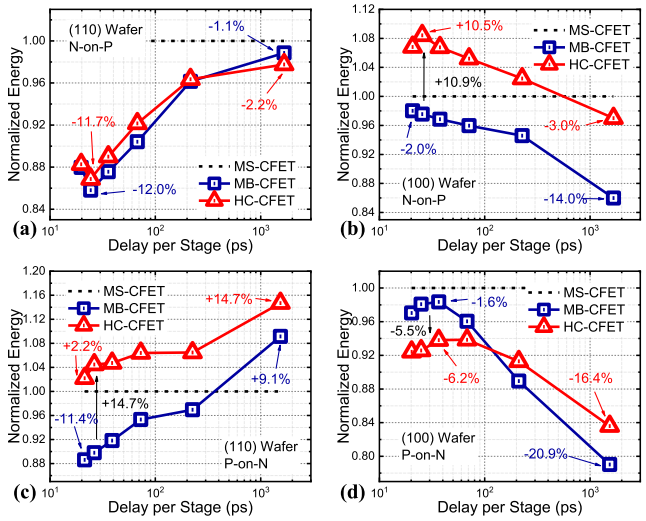

Fig. 7. Normalized energy versus delay per stage of MS-CFET, MB-CFET, and HC-CFET fabricated on (a) (110) wafer with N-on-P stack, (b) (100) wafer with N-on-P stack, (c) (110) wafer with P-on-N stack, and (d) (100) wafer with P-on-N stack.

TABLE II
CHANNEL SURFACE ORIENTATION OF THE DEVICE IN MS-CFET, MB-CFET, AND HC-CFET

Channel Surface Orientation		MS-CFET	MB-CFET	HC-CFET
(110) Wafer N-on-P	NMOS	(100)	(110)	(100)
	PMOS	(100)	(110)	(110)
(100) Wafer N-on-P	NMOS	(110)	(100)	(110)
	PMOS	(110)	(100)	(100)
(110) Wafer P-on-N	NMOS	(100)	(110)	(110)
	PMOS	(100)	(110)	(100)
(100) Wafer P-on-N	NMOS	(110)	(100)	(100)
	PMOS	(110)	(100)	(110)

The optimal channel surface orientation for NMOS and PMOS is marked in red.

related to the device current. The current gain caused by the optimization of channel surface orientation will vary with the change of the supply voltages. For (110) wafer N-on-P stack, the channel surface orientation of PMOS in the HC-CFET is optimized compared with that of MS-CFET. The frequency gain goes lower at lower supply voltage. This trend is due to the small drive current gain of the (110) BL PMOS relative to (100) BL PMOS at low voltage [see Fig. 5(c)]. Compared with the MB-CFET, the TL NMOS in the HC-CFET is optimized, so the trend of frequency gain is highly matched with the drive current gain of the TL NMOS shown in Fig. 5(c). For (100) wafer P-on-N stack, since the drive current gain of the BL NMOS goes higher at lower supply voltage, it can be observed that the frequency gain of the HC-CFET relative to the MS-CFET is higher at low supply voltage. When compared with the MB-CFET, the frequency gain of HC-CFET becomes largest around 0.5 V and fades at 0.2 V, which also matches the drive current gain of the TL PMOS. For the other two cases, the reasons are similar to the above two cases and can also be analyzed from Fig. 5(c). After the above analysis, (100) wafers with P-on-N stack and (110) wafers with N-on-P stack are suitable for HC-CFET to reach higher performance beyond 3-nm node.

B. Power Consumption Analysis

In addition to the considerable RO's frequency gain, the HC-CFET also shows great improvement in energy saving under careful design. We compared the energy under the same delay. Fig. 7 compares the energy consumption of the MS-CFET, MB-CFET, and HC-CFET under different substrates and stack types. Under the situation of (100) substrate with N-on-P stack and (110) substrate with P-on-N stack, due to the degraded device's performance in HC-CFET, higher energy consumption in HC-CFET is observed. By contrast, significant energy saving is observed under the situation of (110) substrate with N-on-P stack and (100) substrate with P-on-N stack. Under the situation of (100) wafer with P-on-N stack, the HC-CFET exhibits a 16.4% lower energy consumption relative to the MS-CFET at the delay of about 2000 ps. Due to the higher frequency gain at lower voltages [see Fig. 5(c)], the lower voltage is required to maintain the same delay, hence the lower energy consumption. When compared with the MB-CFET, energy reduction can be observed at lower delays, since lower voltage is needed to keep the same delay with MB-CFET. The increase in energy at the higher delay of HC-CFET over MB-CFET can be attributed to the disappeared frequency gain at low supply voltage [see Fig. 5(c)] and increased parasitic capacitance (see Fig. 4) of HC-CFET over MB-CFET. Similarly, the HC-CFET also provides good energy reduction in the situation of (110) substrate with N-on-P stack but a bit lower than the above case. According to the above analysis, both (100) wafer with P-on-N stack and (110) wafer with N-on-P stack are suitable for HC-CFET to apply to the low-power application.

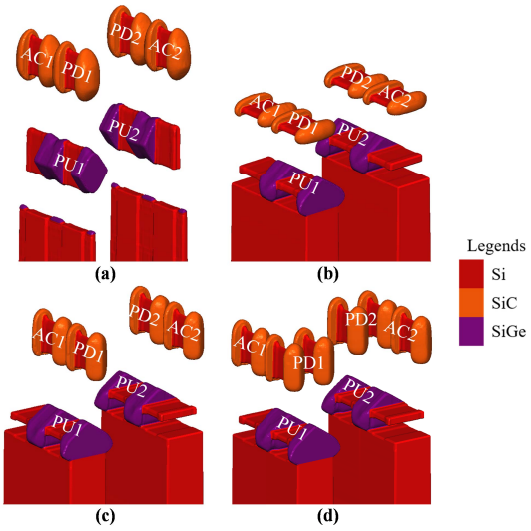

Fig. 8. 6T-SRAM cell 3-D structure of (a) MS-CFET with PU:AC:PD = 1:1:1, (b) MB-CFET with PU:AC:PD = 1:1:1, (c) HC-CFET with PU:AC:PD = 1:1:1, and (d) HC-CFET with PU:AC:PD = 1:1:2.

V. SRAM Structure Design and Performance Analysis

The 6T-SRAM cell includes pull-up (PU), access (AC), and pull-down (PD) devices. The bit-cell area of 6T-SRAM is kept the same in our work. In MS-CFET and MB-CFET, the number of NW/NS in devices is controlled as one NW/NS. In HC-CFET SRAM with PU:AC:PD = 1:1:2, the number of NW/NS in devices is the same as that of the MS-CFET and MB-CFET. By taking advantage of the vertical structure, the HC-CFET SRAM is optimized to have PU:AC:PD = 1:1:2. The 6T-SRAM circuit is simulated under 0.7-V supply voltage.

A. Structure Design

By choosing (110) substrate with N-on-P stack and (100) substrate with P-on-N stack, HC-CFET shows a great advantage in drive current for both NMOS and PMOS. In addition to the overall current improvement, the drive current configuration of different functional devices is very important. In monolithic-CFET architecture, NMOS is vertically separate from PMOS. The PU devices of SRAM are vertically stacked with AC and PD devices. Benefiting from the advantages of the relative separation of the upper and lower two-layer processes, the drive ability of PU and PD functions can be decoupled to some extent, but the coupling of PD and access function remains as usual. In the MS-CFET structure, the NW number of PU devices and PD devices is limited to be the same, as shown in Fig. 8(a). In the MB-CFET structure, the NS number of PD and AC devices is limited to be the same, as shown in Fig. 8(b). By comparison, the NW/NS number of each device in the HC-CFET can be adjusted flexibly. In HC-CFET, the top NW number can be adjusted using the fin-cut process; at the same time, the bottom NS number can be adjusted by Si/GeSi stacks. In the P-on-N structure, the NS number of PD and AC devices cannot be adjusted separately. Instead, in the N-on-P structure, the NW number of PD and AC devices can be adjusted using the fin-cut process, and the NS number of PU devices is independent of the top NW number. Thus, when the HC-FET is fabricated on (110) substrate with N-on-P stack, device number of PU, AC, and PD devices can be optimized to 1:1:2, which is helpful to improve 6T-SRAM read operation. The structure of SRAM using HC-CFET with PU:AC:PD = 1:1:1 is shown in Fig. 8(c). The optimized case, that is HC-CFET with PU:AC:PD = 1:1:2, is shown in Fig. 8(d). Moreover, the NS thickness and NS width of PU devices can be adjusted without changing the physical parameter of the AC and PD devices. Also, the NW height and NW thickness of AC and PD devices are independent of PU devices. The uncoupling properties of HC-CFET provide many benefits to designers. Meanwhile, the cell area of them is kept the same (0.168 μm $\times$ 0.084 μm), as shown in Fig. 9.

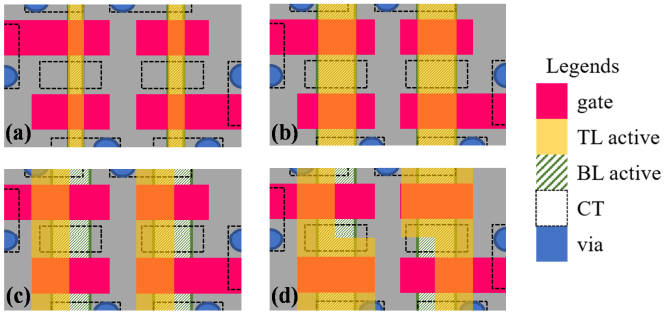

Fig. 9. 6T-SRAM cell layout of (a) MS-CFET with PU:AC:PD = 1:1:1, (b) MB-CFET with PU:AC:PD = 1:1:1, (c) HC-CFET with PU:AC:PD = 1:1:1, and (d) HC-CFET with PU:AC:PD = 1:1:2.

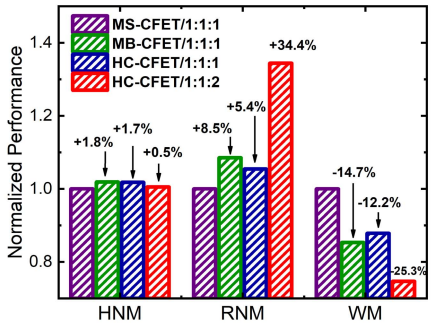

Fig. 10. Performance of MS-CFET SRAM with PU:AC:PD = 1:1:1, MB-CFET SRAM with PU:AC:PD = 1:1:1, HC-CFET SRAM with PU:AC:PD = 1:1:1, and HC-CFET SRAM with PU:AC:PD = 1:1:2 normalized to MS-CFET SRAM with PU:AC:PD = 1:1:1.

B. Performance Analysis

In view of the balanced design parameters of the SRAM cell, the stability, read and write speed, and area of the SRAM cell are the focuses of our discussion. Fig. 10 shows the noise margin of MS-CFET SRAM with PU:AC:PD = 1:1:1, MB-CFET SRAM with PU:AC:PD = 1:1:1, HC-CFET SRAM with PU:AC:PD = 1:1:1, and HC-CFET SRAM with PU:AC:PD = 1:1:2. Those four monolithic-CFETs are fabricated on (110) wafers and have N-on-P stacks. The hold noise margin (HNM) is only affected by PU and PD devices. When compared to MS-CFET, the drive ability of PU devices in HC-CFET is promoted, which provides a stronger "1" node,

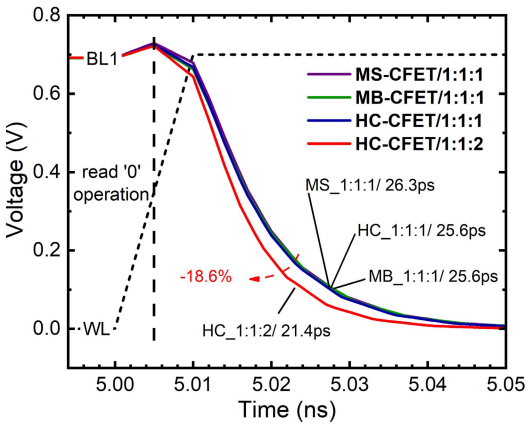

Fig. 11. BL and WL waveform of MS-CFET SRAM with PU:AC:PD = 1:1:1, MB-CFET SRAM with PU:AC:PD = 1:1:1, HC-CFET SRAM with PU:AC:PD = 1:1:1, and HC-CFET SRAM with PU:AC:PD = 1:1:2, while reading "0."

thus leading to higher HNM. Similarly, when compared with MB-CFET, promoted drive ability of PD devices in HC-CFET gives SRAM a stronger "0" node and higher HNM. However, the HNM of SRAM is already excellent, and there is not much room for optimization. Even if the NW number of the PD device is doubled, it will only cause a change within ±2%. Although doubled NW number of PD decreases write margin (WM), at the beyond 3-nm technology node, read noise margin (RNM) is most vulnerable. Stronger PU makes the storage nodes more stable and partly increases RNM. It is worth mentioning that, after optimizing the PD device number to two, due to the increased PD drive strength against AC, HC-CFET SRAM with PU:AC:PD = 1:1:2 shows over 30% increase in RNM. The optimized HC-CFET SRAM also provides a path for high-speed SRAM. When AC is turned on, stronger PD discharges the bitline faster, resulting in an 18.6% drop in read time (RT; see Fig. 11). Larger RNM, as well as smaller RT, mitigates the requirements for sense amplifiers. Those improvements are at the expense of increasing leakage, which makes more sense to gain high-speed and robust SRAM by optimizing the system operation and peripheral circuit. Using HC-CFET to achieve a ratio of PU:AC:PD = 1:1:2 does balance the performance of SRAM cell, so that SRAM cells are more robust in large-scale array integration.

VI. Conclusion

In summary, we report a novel HC-CFET starting from one substrate, which can effectively co-optimize the NMOS and PMOS drive currents through the preferred channel surface orientation, without degrading the SS and DIBL characteristics. The high-speed and low-energy 17-stage RO is demonstrated, with a significant-increased frequency and comparable energy consumption compared with that of MS-CFET and MB-CFET. Benefiting from the structure flexibility of HC-CFET, a robust 6T-SRAM is validated with more than 30% increase in RNM and 18.6% decrease in RT. The results demonstrate that when started from (110) substrate with NMOS stack on top of PMOS, HC-CFET has the optimal performance and flexible structural operability.

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