DTCO including Sustainability: Power-Performance-Area-Cost-Environmental score (PPACE) Analysis for Logic Technologies

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Abstract— Driven by concerns on climate change, resources depletion, local and global pollution, sustainability is becoming an integral component of business and of regulations. The progress of Design Technology Co-Optimization (DTCO) methodologies and tools, building transversal knowledge from manufacturing to design, provides an opportunity to develop a framework for early sustainability assessments of logic technologies. Environmental scores can be derived together with the established Power, Performance, Area, Cost (PPAC) metrics. To demonstrate this approach, we evaluate the energy and water consumption as well as the greenhouse gas emissions trends from processing logic nodes from iN28 to iN3 with different scaling scenarios.

I. INTRODUCTION

Semiconductor manufacturing is resource intensive in energy, water, chemicals and raw materials, and generates different classes of emissions, including greenhouse gases (GHG) [1-5]. The semiconductor industry has a long running expertise in environment, health and safety (EHS) control, and efforts are made by foundries, equipment suppliers and design companies towards greener IC manufacturing. Through the years, some initiatives emerged to bring environmental considerations into the technology definition phase and to develop dedicated methods to assess the sustainability of integrated circuits [6-9]. Meanwhile, Life Cycle Assessment (LCA), a methodology to evaluate the environmental impact of products from material sourcing to end-of-life, has become a standard used extensively in different disciplines [10,11].

Yet, the pathfinding phase of upcoming CMOS technologies is still disconnected from sustainability considerations and the environmental impacts are not monitored when optimizing the PPAC metrics of future nodes. Moreover, the mass balances and energy flows needed to conduct quality LCA for integrated circuits is scarce and discontinued (the latest published data collection is for the 32 nm node [2]), leading to errors and variability in the LCA of electronics products and to a strong demand for updated information [12-14]. The increasing complexity of the technologies in terms of number of process steps, scaling boosters, new materials, new equipment such as Extreme Ultraviolet lithography (EUV), the amount of data and access to this data, complicate this task. This increase in complexity makes also more crucial to evaluate sustainability ahead of high-volume production. A holistic approach is also required to conduct correct evaluations. For instance, EUV tools consume approximately *10x* more power per tool than traditional Deep Ultraviolet (DUV) lithography but replace multiple processing steps in the fabrication.

The DTCO frameworks contain process flows that can be coupled to the information on process steps and manufacturing equipment. They constitute thus an interesting base for a comprehensive and parametric analysis of environmental indicators, that can be monitored in parallel to the PPAC metrics. To demonstrate this, we first review some of the technological transitions that support logic circuits scaling from iN28 down to iN3 with different scenarios for most recent nodes (Table 1). We then present wafer processing metrics corresponding to this scaling roadmap, focusing on three aspects: *(1)* energy consumption from processing (and equivalent CO_2 footprint), with attention for the transition to EUV *(2)* water consumption, with attention for Ultra Pure Water (UPW), and *(3)* GHG emissions. We also discuss the growing importance of raw minerals.

II. TECHNOLOGY SCALING FOR AREA AND PERFORMANCE

Multiple innovations have allowed to continue reducing the logic cells area (Fig.1) while increasing the operating frequency node-to-node (Fig.2) [15-17]. To print tighter pitches, lithography techniques have evolved from DUV 193nm ArF-dry to immersion 193nm (ArFi) exposure, then to EUV. Before the enablement of EUV, pitches smaller than 40nm were already achieved using double, triple or quadruple patterning repeating Litho-Etch sequences (LE2, LE3, LE4), or using Self-Aligned Double or Quadruple Patterning (SADP, SAQP) that require litho, deposition and etching steps. The enablement of EUV allowed to strongly reduce the number of processing steps and masks needed (Fig.3). EUV was mature for iN8, but its adoption varies between foundries as multiple processing routes are possible for the same pitches (Fig.4). As single exposure EUV reaches its limits at 30nm pitch, EUV LE2 is needed beyond iN7.

The number of interconnect layers in the Back-End-Of-Line (BEOL) increases node to node to maintain routing (Fig.3). From iN8, the complexity of the densest BEOL metal lines has also increased: block layers are needed to cut the metal lines, adding litho and etching steps. The metallization scheme changes, moving from Tungsten to Cobalt then Ruthenium to achieve low resistivity in the densest layers. From iN8, area scaling is obtained reducing also the standard cells number of metal tracks, which forces the introduction of scaling boosters in the Front-End and Middle-Of-Line (FEOL, MOL): local interconnect, Self Aligned Gate Contact (SAGC) at iN8, Metal Gate Cut (MGC) at iN6, Buried Power Rail (BPR) at iN5. At device level, besides multiple enhancements, planar FETs were replaced by FinFETs at iN14, then Lateral NanoSheets (NSH) at iN5 for improved short channel control.

From these gradual changes, the number of steps for the entire process flows assumed here has been multiplied by 2.6 between iN28 and iN3 (Fig.5).

III. MANUFACTURING METRICS

A. Electrical energy consumption

Energy consumption for a full process flow is derived summing the electrical energy usage of individual process steps, calculated from the utilities real average power multiplied by tool times (standby and engineering times are not included) [18]. Fig.6 shows the distribution of power and throughputs (TPT) in wafers per hour (wph) considered. The power ranges from 10 to 100 kW for most tools but is significantly larger for EUV utilities: 1MW input power is required, 10 times higher than for DUV. The lowest TPT are for EPI, atomic layer deposition (ALD), annealing, and chemical mechanical polishing (CMP). The TPT of an EUV scanner is generally lower than for DUV but has improved significantly in recent years. It is tied to the photoresist dose which defines the resolution: in latest machines, a TPT of 170 wph at low resolution and down to 65 wph at high resolution is expected, leading to an energy of 6 to 14 kWh/wafer for a single EUV step (Fig.7). A median TPT 110 wph will be assumed here for all EUV scanners steps. With this value, the energy required to process a metal layer at pitch 32nm with EUV LE is close to the energy used for SAQP ArFi (Fig.8). This value is thus the minimum throughput needed for the transition to EUV to be energy neutral for manufacturing.

The energy consumption increases in the three parts of the process across nodes (Fig.9). This increase comes from the addition of MOL interconnect and scaling boosters (MGC, BPR), increase in number of metal layers in the BEOL, increase of steps with multiple patterning, and an increase in low throughput steps such as ALD and CMP. The pitch scaling is particularly penalizing on energy at iN6 and iN3 in the BEOL (Fig.10) because of the EUV LE2 steps needed first for blocks and vias, then for trenches. Note that immersion based octuple patterning (SAOP) would have given similar results.

To get a first estimate of the total manufacturing energy (Fig.11), the electrical consumption of the facility equipment supporting the process (cooling water, dry air, vacuum,..) is assumed to contribute to 40% of the total energy [19]. A total of 1 kW/cm^2 for iN28 to 3.5 kWh/cm^2 to iN3 is obtained. The tools energy is distributed between process areas, with dominance of PVD in the FEOL and lithography and dry etch in the BEOL on scaled nodes (Fig.12). The equivalent CO_2 emissions depend on the sources used for electricity generation (Table 2). As foundries transition from fossil fuel-based electricity generation mixes to renewable energies, the potential important node-to-node growth of the electricity carbon footprint per wafer could be compensated (Fig. 13). The growth in number of wafers produced will also need to be counterweighted.

B. Ultra Pure Water consumption

UPW is used to rinse the wafer in wet benches and CMP. As UPW is contaminated after use and purification systems are cost and energy intensive, recycling is challenging, but reclaimed UPW can be reinjected towards cooling and scrubber towers of the facility (up to 88% of the process water can be reclaimed [5]). UPW production also uses chemicals and energy and about twice its volume of water. The higher number of CMP and wet steps led to an increase of UPW consumption from 6 l/cm^2 at iN28 to 14 l/cm^2 at iN3 in our analysis (Fig.14).

C. Greenhouse gases emissions

High Global Warming Potential (GWP) GHGs, including fluorinated compounds (e.g. SF_6, NF_3, CF_4, CHF_3), are used for dry etching, cleaning CVD chambers and epitaxial growth. We evaluated the CO_{2eq} emissions based on the process flows, tool time and average input gas flows for each tool, corrected by the abatement and utilization factors following the Tier 2b method of the Intergovernmental Panel on Climate Change (Table 3) [20,21]. SF_6 and NF_3 are the two major contributors due to their high GWP (Fig.15). EUV helps reduce the GHGs by replacing some deposition and etching steps. The increase in CVD steps across nodes increases NF_3 consumption. By changing the abatement factor for NF_3 from 95% to 99% announced for latest abatement systems [22], the total GHG emissions for the process flows considered would stay close to the ITRS target of 0.22 kgCO_{2eq}/cm^2 [19].

D. Raw materials

Minerals extraction and refinement consume large amounts of energy. LCA datasets (Fig.17) suggest that adopting Ruthenium as local and BEOL interconnect as motivated by its excellent electrical properties could increase the total CO_{2eq} footprint of ICs. Further analysis based on efficiency in the tools and recycling options is needed. Some minerals used for IC fabrication are also listed as critical, meaning the relation between stocks, supply and demand is considered at risk (e.g., Germanium, Ruthenium, Cobalt, Tungsten). Tungsten is also a conflict mineral. IC are difficult to recycle compared to other components of electronics systems, but initiatives to start recycling from scrap of the fabrication line have started.

IV. PPACE

Our analysis shows a significant increase in electricity (*x3.46*) and UPW (*x2.3*) consumption, and GHG emissions (*x2.5*) per wafer from iN28 to iN3. Together with a delay improvement, the standard cell area is still scaling (Fig.18), so the environmental metrics normalized per transistor still reduce but are shown to saturate for the projected nodes iN5 and iN3.

V. CONCLUSIONS

The higher complexity of scaled logic nodes leads to an increase of energy, water and GHG emissions per wafer. Design Technology Co-Optimization frameworks can be used to estimate these metrics in an early phase of technology definition as for the PPAC metrics. This approach allows to benchmark different integration schemes, identify key process steps, or draw a sensitivity analysis to specific parameters.

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Technology	iN28	iN20	iN14	iN10	iN8	iN7	iN6	iN5	iN3
Transistor structure	Planar	Planar	FF	FF	FF	FF	FF	FF or NSH	NSH
# Tracks standard cell	9T	9T	9T	7.5T	6.5T	6T	6T	5T	5T
# Fins per active	4	4	4	3	3	2	2	1	1
Gate Pitch [nm]	120	90	90	64	56	48	45	45	42
Metal Pitch [nm]	90	64	64	48	40	28	21	21	16
Scaling boosters	-	-	-	-	SAGC	SAGC	SAGC + MGC	SAGC+BPR + MGC	SAGC+BPR + MGC
S/D EPI scheme	DEC	DEC	DEC	DEC	DEC	DEC	WAC	WAC	WAC

Abbreviations : FF: FinFET. NSH: NanoSheet. SAGC: Self Aligned Gate Contact. BPR: Buried Power Rail. MGC : Metal Gate Cut. DEC: Diamond Epitaxial Contact. WAC: Wrapped Around Contact.

Table.1- Technology assumptions: device structure, number of metal tracks per standard cell, gate and metal pitches, scaling boosters and source/drain contacting schemes used for this work (imec nodes). Three Vts are used for both N- and P-FETs.

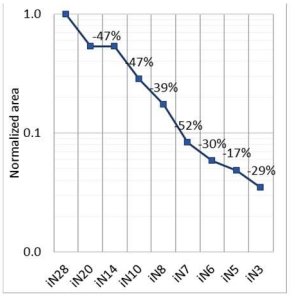

Fig.1- Node to node standard cell area scaling normalized to iN28 area.

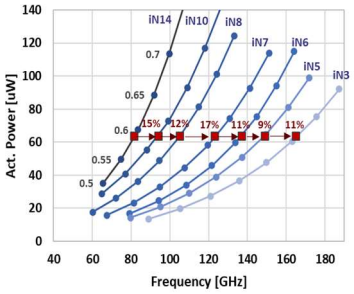

Fig.2- Frequency gain from iN14 FinFETs to iN3 NanoSheets based on simulations using pathfinding compact models and including interconnect parasitics [15].

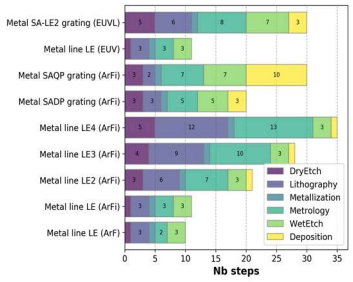

Fig.3- Process complexity in number of steps for different lithography options. Direct EUV allowed to reduce the number of steps to a third compared to SAQP.

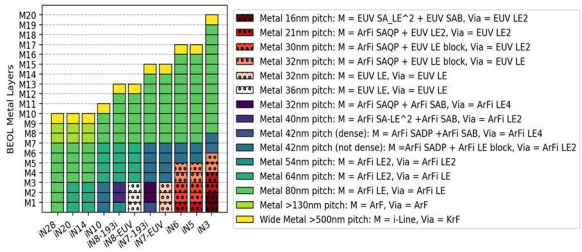

Fig.4- BEOL metal layers patterning assumptions. At iN8 and iN7, two options are considered, immersion multiple patterning and EUV direct print (for trenches, blocks and vias). At iN5 (pitch 21nm), 193i SAQP can still be used with EUV LE2 for blocks and vias. At iN3 (pitch 16 nm), self-aligned double patterning EUV is used also for the metal lines.

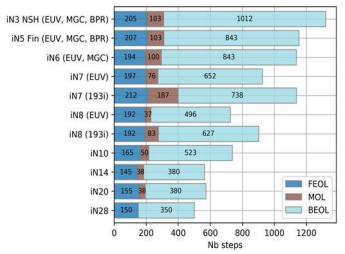

Fig.5- Manufacturing complexity in number of process steps from processing for FEOL, MOL and BEOL, from iN28 to iN3. Three Vts are assumed in the FEOL. The BEOL contributes for 70 to 76% of the total.

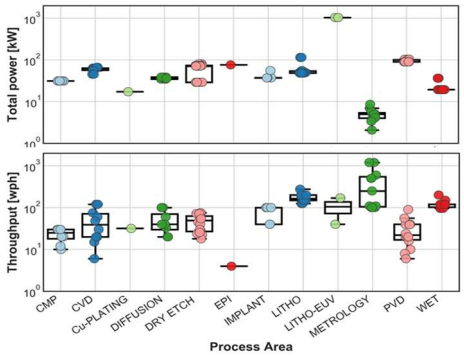

Fig.6- Power and throughput used for the process tools/steps considered, per process category. Annealing steps are under CVD and diffusion. Slowest CVD and PVD steps are based on atomic layer deposition or for thick layers (e.g. STI fill).

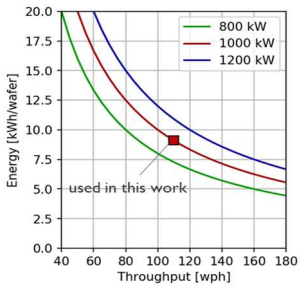

Fig.7- The electrical energy needed per wafer for a EUV scanner step as function of throughput (TPT decreases with higher photoresist dose and resolution), for different tool power. 110 wph is used for the process flows analysis.

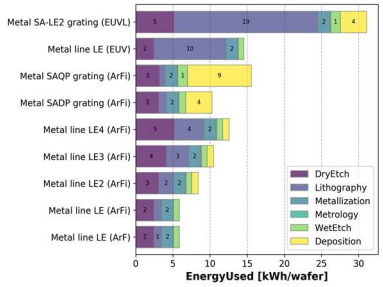

Fig.8- Electrical energy used per wafer for different lithography options. Assuming EUV throughput 110wph, EUV LE results in a total energy close to SAQP grating due to the simultaneous reduction of number of processing steps and increase in power per step. The consumption doubles when going to EUV LE2.

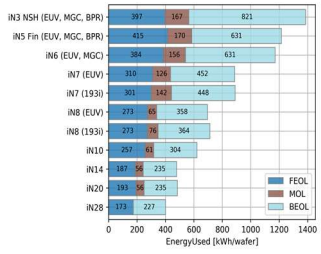

Fig.9- Manufacturing energy per 300mm wafer equivalent from processing for FEOL, MOL and BEOL, from iN28 to iN3 (1 kWh = 3600 kJ). Facility energy not included. The BEOL contributes to 57 to 59% of the total.

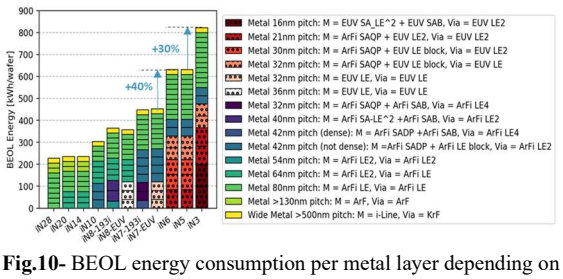

Fig.10- BEOL energy consumption per metal layer depending on patterning options. The energy increase is due to the increase in the number of metal layers, in complexity (i.e, introduction of block layers to cut metal lines), and multiple patterning for tight pitches. EUV at 110wph does not penalize energy compared to SAQP. The energy consumption increases strongly at iN6 and iN3 due to processing blocks, vias then trenches with EUV LE2..

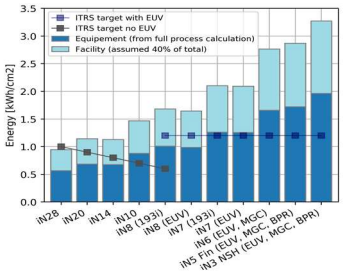

Fig.11- Total manufacturing electricity per cm^2 for full process flows (300mm wafer=706cm^2). Facility energy is projected assuming 40% of the total energy. ITRS guideline is added for reference [19]. Previous estimates of total energy for the 32nm node was 1.6 kWh/cm^2 [1].

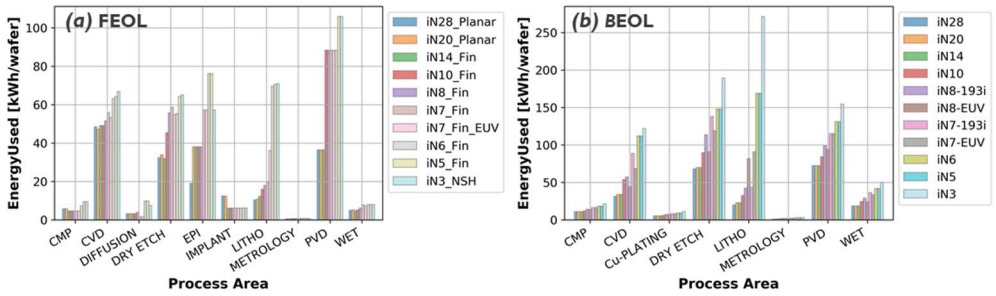

Fig.12- Energy per process area across nodes (a) for FEOL (b) for BEOL. In the FEOL, PVD steps are used to fabricate the gate stacks with different metal work functions. EPI growth is needed for S/D stressors. The contribution of litho increases from iN6 with the 45nm gate pitches. In the BEOL, dry etch and PVD dominate until iN6, where the lithography effort protrudes.

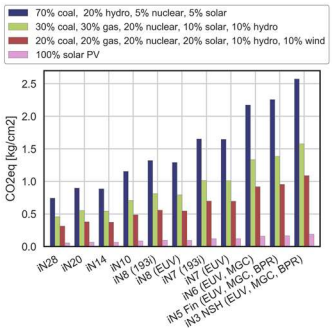

Fig.13- Comparison of the $CO_{2,eq}$ of electricity generation estimation for wafer processing per wafer cm^2, per node, for different typical energy mixes, with increasing contribution of renewable energy.

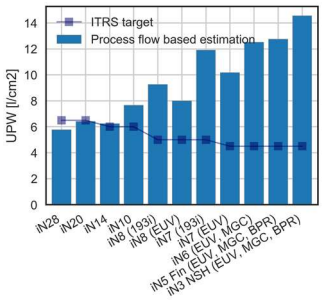

Fig.14- Total Ultra Pure Water (UPW) usage in liters per cm^2 for full process flows from iN28 to iN3 for 300mm wafer equivalent. ITRS guidelines shown as reference.

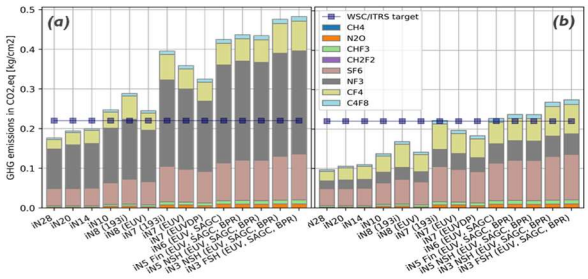

Fig.15- GHGs emissions in kg CO_{2eq} per cm^2 of wafer, per node, for the full processes, calculated using the GHG protocol for electronics industry of IPPC [21]: assuming NF_3 abatement factor of *(a)* 95% as in [21]; *(b)* 99% as announced in [22]

Source	gCO2eq/kWh
Coal	820
Gas	490
Solar PV	48
Hydropower	24
Wind	12
Nuclear	12

Table 2- Life cycle CO_2 equivalent per kWh of electricity production from selected supply technologies used in Fig.13, from [20].

$$CO_{2eq} = GWP \cdot \sum_{p} \sum_{i} m_i \cdot (1 - U_{i,p}) \cdot (1 - d_i)$$

GHG	GWP [kg/kg]	$(1\text{-}U_i)$ for dry etch	$(1\text{-}U_i)$ for CVD ent	Abatem d_i
CO2	1			
CH4	28	40%	40%	90%
N2O	265	40%	40%	90%
CH2F2	677	60%	60%	90%
CF4	6630	70%	90%	90%
C4F8	9540	90%	90%	90%
C2F6	11100	40%	60%	90%
CHF3	12400	40%	40%	90%
NF3	16100	20%	20%	95%
SF6	23500	20%	20%	90%

Table 3- Equivalent CO_2 emissions estimation for the greenhouse gases emitted by processing tools. The standard input rates from the tools and the specific tool time of each process step is used to calculate the input gas mass m_i. The GWP in CO_{2eq} per emitted mass is taken from IPCC AR5 [20], the fraction not used in the process $(1\text{-}U_i)$ and destruction efficiency d_i of the abatement systems from [21].

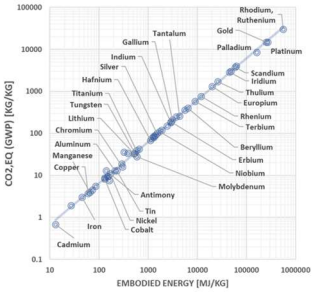

Fig.17- Embodied energy and Global warming potential in CO_{2eq} of the extraction and refinement of standard industrial grade raw materials [23].

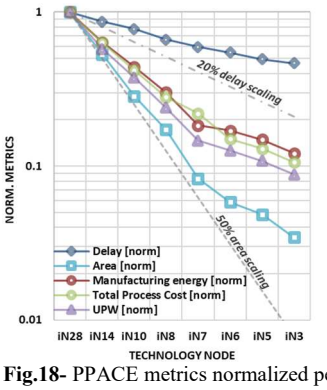

Fig.18- PPACE metrics normalized per standard cell area (inverter cell) and to iN28 values to obtain the scaling trend. Area scaling brings a reduction per transistor of energy of manufacturing and UPW consumption that is slowing down at scaled nodes.

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