Mitigating the Length of Diffusion Effect by Back-End Design-Technology Cooptimization

Jiwei Zhang, Hao Zhu, *Member, IEEE*, Lin Chen, Qingqing Sun, and David Wei Zhang

***Abstract*— The length of diffusion (LOD) effect in low-V_t (LVT) and standard-V_t (SVT) logic is investigated and the yield and dynamic power consumption (DPC) have been optimized by using back-end of line (BEOL) design-technology cooptimization (DTCO). The resistor–capacitor (*RC*) characteristics of the Via in the back-end structure at 28 nm node is engineered to improve the *RC* properties which further alleviates the yield and DPC issues originated from the LOD effect. With the *RC* as the mechanism affecting the frequency and power level, it is found that the yield loss and DPC loss can be significantly lowered with *RC* balance optimization of the Via. These results demonstrate that the BEOL optimization can be more efficient in solving such front-end of line (FEOL) issues as compared to the conventional FEOL engineering. In addition to the circuit design improvement, such optimization also provides a promising approach to suppress the layout-dependent LOD effect through process engineering.**

***Index Terms*— Design-technology cooptimization (DTCO), dynamic power consumption (DPC), length of diffusion (LOD), yield loss.**

I. Introduction

THE tradeoff between the speed and leakage power in CMOS logic has urged circuit designers to employ cells with different threshold voltage (V_t) in different blocks. For example, high-V_t (HVT) or ultra-HVT (uHVT) cells are mostly used in low power circuit designs while low-V_t (LVT) [sometimes standard-V_t (SVT)] cells are implemented high-frequency applications like clock path [1], [2]. At advanced technology nodes with scaled devices and boosted integration density, parasitic components can severely degrade the switching characteristics, and process variation can cause leakage increasing the power consumption. In addition, modern logic circuits suffer from severe frequency mismatch issues and thus yield loss, which requires delicate optimization of circuits incorporating devices with various V_t in the design of high-performance and low-power integrated circuits [3], [4]. Fig. 1(a) shows a simple logic device module with SVT and LVT output and input to the frequency measurement module. The output of the circuit is strongly dependent on the frequency mismatch between the SVT and LVT devices. The unit can function correctly with proper yield only when the LVT frequency is higher than SVT. Fig. 1(b) demonstrates the circuit of a D flip-flop (DFF) implemented with SVT and LVT as illustrated in Fig. 1(a). We have simulated the timing diagram of such circuit with different CLK and Data signals. As shown in the simulated input and output waveforms (Fig. 2), if the

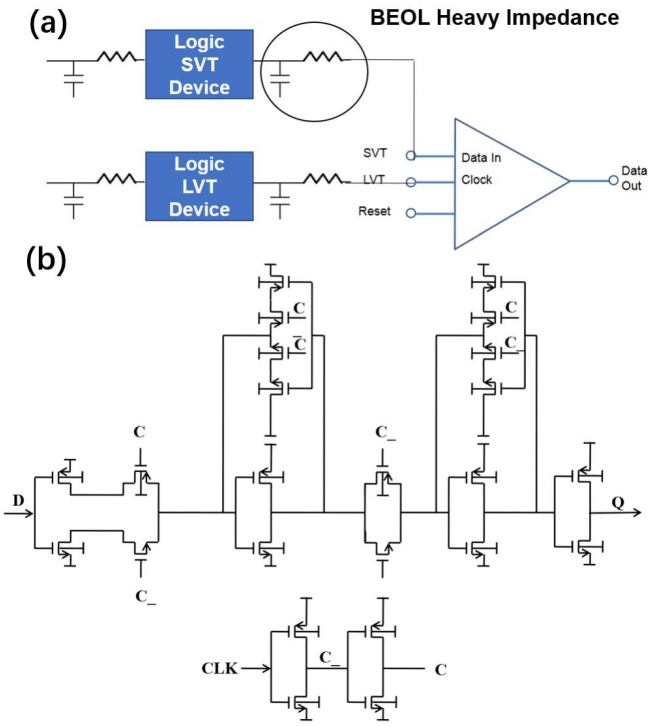

Fig. 1. (a) Logic circuit incorporating SVT and LVT devices. The output of SVT and LVT are input to a frequency measurement module. (b) Circuit schematic of a DFF employing SVT and LVT devices. SVT devices are employed in building data in while LVT devices are used in clock.

Manuscript received September 8, 2021; revised November 25, 2021; accepted January 19, 2022. Date of publication February 4, 2022; date of current version February 24, 2022. This work was supported in part by the NSFC under Grant 61904033, and in part by the Science and Technology Commission of Shanghai Municipality under Grant 20501130202 and Grant 21DZ1100700. The review of this article was arranged by Editor T.-H. Kim. *(Corresponding author: Hao Zhu.)*

Jiwei Zhang is with the State Key Laboratory of ASIC and System, School of Microelectronics, Fudan University, Shanghai 200433, China, and also with Semiconductor Manufacturing International Corporation, Shanghai 201203, China.

Hao Zhu, Lin Chen, Qingqing Sun, and David Wei Zhang are with the State Key Laboratory of ASIC and System, School of Microelectronics, Fudan University, Shanghai 200433, China, and also with the National Integrated Circuit Innovation Center, Shanghai 200234, China (e-mail: hao_zhu@fudan.edu.cn).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TED.2022.3145760.

Digital Object Identifier 10.1109/TED.2022.3145760

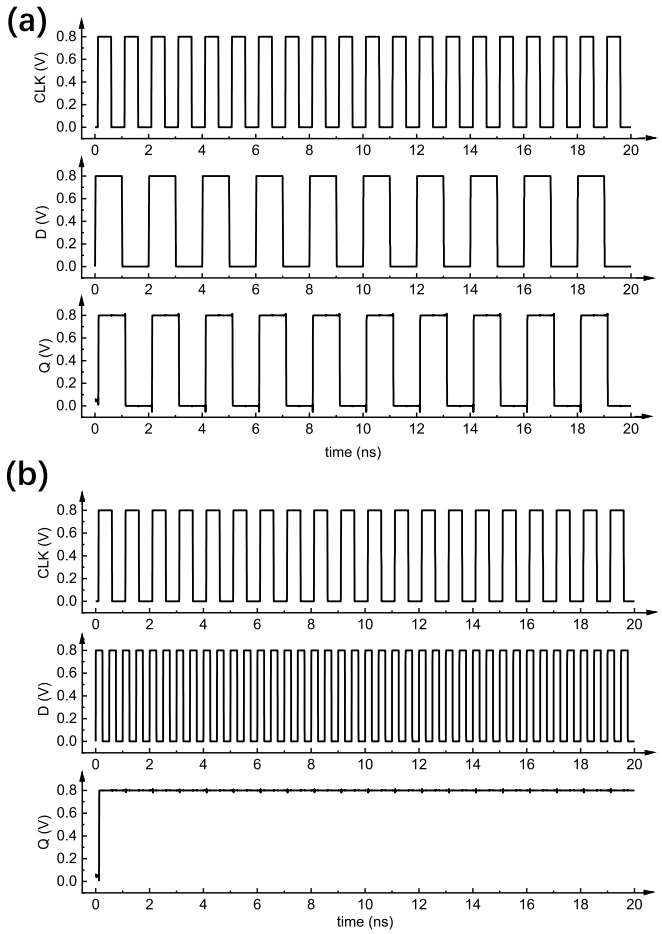

Fig. 2. Input and output waveforms of the DFF circuit shown in Fig. 1(b). (a) LVT frequency is higher than SVT (CLK period 1 ns, data period 2 ns). (b) LVT frequency is lower than SVT (CLK period 1 ns, data period 0.5 ns).

LVT frequency is lower than SVT, function failure occurs leading to yield loss.

The device mismatch in a circuit design is critical to the yield and the performance variation can also lead to higher power consumption. This has necessitated optimization of the layout-dependent effects, especially at advanced technology nodes. For example, the well proximity effect (WPE) describes the influence of distance between active area and the well edge on the uniformity of well implantation concentration profile. Other layout-dependent effects like poly spacing effect (PSE) and oxide spacing effect (OSE) describe the poly spacing and oxide spacing, and the stress induced by the shallow trench isolation (STI) on poly and active area. Nevertheless, the WPE, PSE, and OSE are all edge effects leading to device performance mismatch which are dominated by design factors. In contrast, length of diffusion (LOD) effect, another layout-dependent effect, has a greater impact on the characteristics of individual transistors like the mobility [5]–[7]. LOD is described by the SA and SB parameters measured from poly finger to the oxide boundary on active area, and the saturation current (I_{dsat}) and the device V_t can be significantly influenced by the stress originated from the STI process. In general, LOD

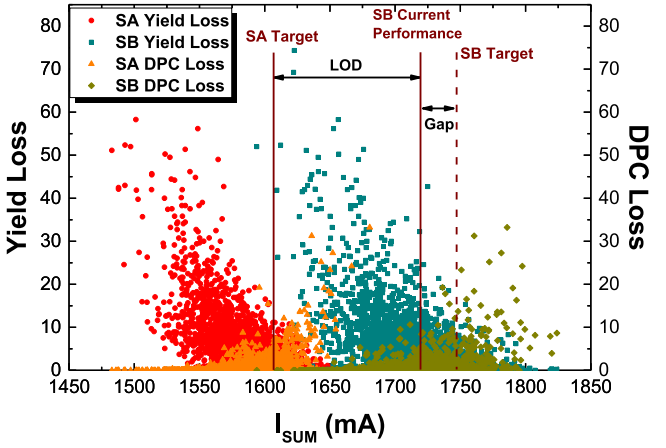

Fig. 3. Yield loss and DPC loss as a function of I_{sum} for SA and SB devices, respectively. The LOD is defined as the difference between the SA and SB current levels.

is proportional to the distance to the oxide boundary [8], [9]. Adjustment of layout can impact the frequency behaviors, especially in LVT as compared to SVT, leading to uncontrollable yield and dynamic power consumption (DPC) loss. More importantly, LOD can be mitigated from process optimization approaches even with a fixed layout design enabling improved device mismatch properties and circuit performance.

In this work, for the first time, we address the above issues by back-end of line (BEOL) design-technology cooptimization (DTCO) at 28 nm technology node. The measured yield loss and DPC loss as well as their dependency on the operation current are studied. The different behaviors of current on LOD between SVT and LVT are compared and analyzed. Since the frequency behaviors are largely affected by the capacitive properties of the circuit, it is efficient to implement DTCO technologies in BEOL process with a large portion of capacitive and resistive components for performance improvement. By optimizing the *RC* properties of the Via structure, a sufficiently large current window with much-improved yield and DPC loss has been achieved.

II. LOD and Yield/DPC Loss

In order to better study the influence of LOD on the yield and DPC performance, we separately assign two devices with different distance to the STI stress region for SVT and LVT, respectively: SA with long distance and SB with short distance. There are nMOS and pMOS for both SA and SB, and I_{sum} is defined as the total saturation current of nMOS and pMOS devices. Typically, to achieve a functional circuit with proper yield and power consumption, I_{sum} is usually limited to an operational window to keep the yield and DPC loss under a certain level. Therefore, the LOD effect can be manifested by the change in the difference of the current level between SA and SB. Fig. 3 shows the yield and DPC loss as a function of I_{sum} for SA and SB, respectively. The circuit shown in Fig. 1 is used for the yield testing. The frequency will increase with larger current level which enables an improved yield. For the DPC testing, the frequency can be obtained by measuring the

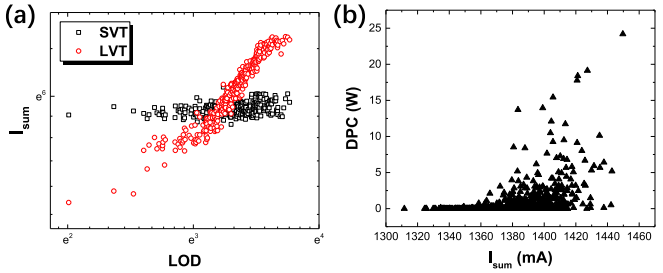

Fig. 4. (a) I_{sum} as a function of LOD strength for SVT and LVT logics, respectively. The SVT demonstrates a nonsensitive behavior to LOD effect, while LVT exhibits increasing trend in I_{sum} with LOD. (b) DPC performance as a function of I_{sum} for a nonoptimized circuit.

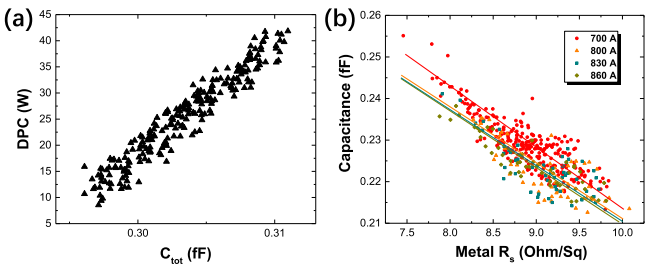

Fig. 5. (a) DPC performance as a function of C_{tot} for a nonoptimized circuit. (b) BEOL *RC* curves for the four via height splits. As compared with the 700-Å circuit, the circuits with increased via height have demonstrated improved *RC* behaviors.

current, since other circuit parameters are fixed. The DPC can be calculated by

$$P_D = afCV_{dd}{}^2 \tag{1}$$

where a represents the switching activity, f is the operation frequency, C is the total capacitance, and V_{dd} is the supply voltage. DPC will decrease with smaller capacitance when V_{dd} and frequency are unchanged.

From Fig. 3, the SA and SB target values are I_{sum} with minimum yield and DPC losses, which are 1600 and 1750 mA, respectively. But the actual current of SB is only as high as 1700 mA due to the LOD effect. As a result, the LOD decreases which further leads to the frequency mismatch. In general, the SA devices can achieve the target I_{sum} easier as compared to the SB devices due to shorter distance to the active area edge and thus less target deviation. On the other hand, SB devices suffers from much severer performance-target discrepancy and the current performance is always lower than the target, leading to smaller LOD.

In the circuit shown in Fig. 1(a), the data out of the frequency measurement module can be affected by the LOD shift which has been tested on both the SVT and LVT logic. Due to the low voltage level of LVT, SA voltage can hardly be decreased to lower I_{sum}. As a result, the variation in LOD is largely determined by the change (increase) of SB voltage, and I_{sum} of LVT will increase with increasing LOD. In comparison, for SVT, there is a much larger margin to decrease SA voltage level. Therefore, when LOD increases, the SA I_{sum} will decrease while SB I_{sum} will increase, leading to an unchanged average value. As shown in Fig. 4(a), the SVT is nonsensitive to the LOD with negligible I_{sum} fluctuation in the tested LOD range, while the LVT demonstrated a clear increasing trend in I_{sum} with increasing LOD. Such increase in I_{sum} with larger LOD can be beneficial to the enhancement of device performance with boosted speed. However, as depicted in Fig. 4(b), this will lead to higher DPC loss which will further lower the frequency degrading the LVT and SVT frequency mismatch property. If the LVT frequency is much lower than the SVT frequency, the circuit shown in Fig. 1(a) will not work resulting in higher yield loss (Fig. 2). Therefore, there is a tradeoff between the LOD and the DPC loss, and thus a limited current window.

III. BEOL Optimization

A. Role of Circuit Impedance and Capacitance

DPC is the dynamic power consumption when driving the device and circuit with switching activities. It is determined by the circuit impedance and capacitance and is dependent on the frequency. With constant LOD, the frequency is also related to the circuit impedance and capacitance: lower *RC* enables higher frequency. Therefore, the circuit capacitance not only impacts the frequency but also the power consumption, which means that lowering the capacitance can reduce the yield loss and DPC loss. Therefore, the optimization of the capacitance can compensate the LOD shift in the circuit and improve the yield ratio and DPC issue.

B. RC Properties Optimization

Although the capacitance of the entire circuit and system consists of the front-end of line (FEOL) and BEOL capacitance, the gate oxide capacitance in FEOL is usually fixed with certain device process design kit (PDK), and the overlap capacitance in FEOL can hardly be lowered without extra processing which can lead to further power loss. Considering the fact that a large number of capacitive elements exist in BEOL structures, it is provident to engineer the capacitance structures for optimization. Fig. 5(a) shows the relation between DPC and BEOL total capacitance (C_{tot}). In BEOL, C_{tot} consists of C_{intra} (capacitance between metal lines in same layer) and C_{inter} (capacitance between metal lines in different layers) [10]. C_{intra} is constrained by the design rule of definite line and space. With lower C_{intra}, metal width will decrease leading to higher metal line resistance (R_s). Generally, metal line resistance is constant to avoid high power loss, and it is more effective and efficient to decrease C_{inter} by enlarging the Via height for a lower total capacitance.

In our *RC* optimization design and experiments, we keep the LOD constant and vary the Via height to examine and compare the performance. It is noted that although increasing the Via height can lower the C_{inter} to a certain extent, larger Via height can lead to increased parasitic metal line resistance. On the other hand, an optimal capacitance exists for the Via height optimization, and additional parasitic capacitive components between Vias when increasing Via height beyond a certain

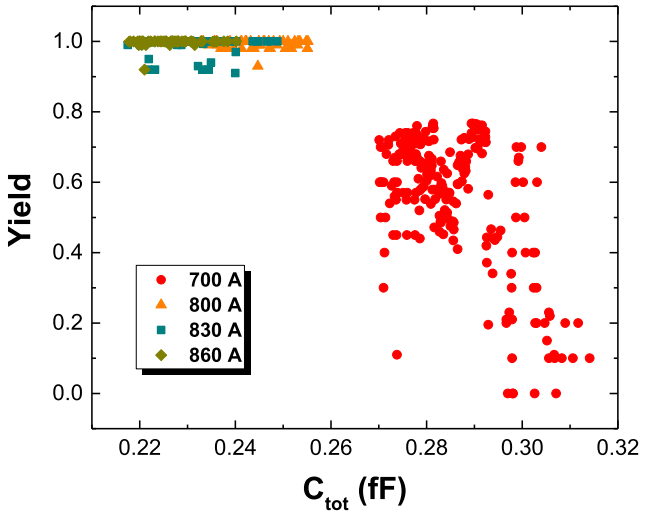

Fig. 6. Yield ratio as a function of the total capacitance for the four via height splits. A very clear improvement in the yield ratio has been observed with increased via height, with the yield ratio approaching 100% for the three increased height splits.

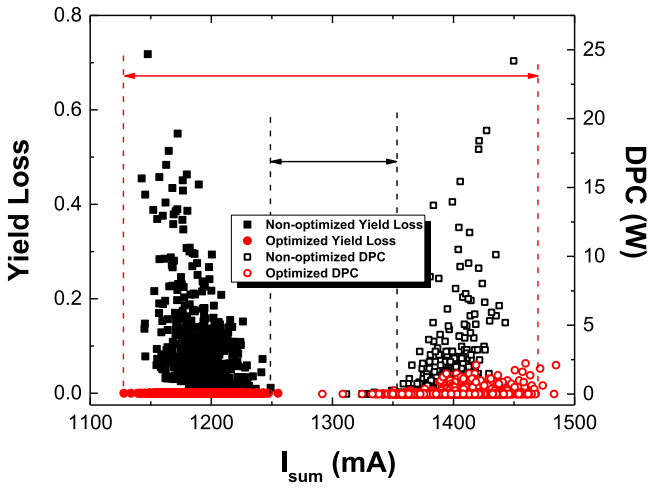

Fig. 7. Yield loss and DPC loss results as a function of I_{sum} to extract the current window of the circuit.

point will inevitably degrade the frequency characteristics as well as the power-performance properties. In our work, four Via height splits have been tested: 700, 800, 830, and 860 Å. Fig. 5(b) shows capacitance versus metal R_s curves of the four splits. It is clear that the *RC* curves are improved with increasing Via height: as compared to the 700-Å sample, the 800, 830, and 860 Å splits are improved by 2%, 2.5%, and 4%, respectively. Since the frequency is inversely proportional to the capacitance, the frequency will be increased with lowered capacitance. As shown in Fig. 5(a), when the total capacitance is decreased, the DPC is also lowered.

Fig. 6 shows the experimental results of the improvement in yield ratio through Via height optimization. Each data point represents the yield ratio of one wafer associated with the total capacitance. As compared to the 700-Å split, the other three splits using increased Via height of 800, 830, and 860 Å have shown much smaller C_{tot} values, and larger Via height enables higher yield ratio reaching up to 100% as shown in Fig. 6. When total capacitance is reduced, for typical circuit, the time to charge the capacitance is reduced and the frequency increases correspondingly. Although the frequency of SVT and LVT increases at the same time, LVT exhibits a larger frequency increase than that of SVT, and the frequency of LVT is always higher than SVT regardless of the device speed. Therefore, although the LOD is constant, the total frequency and LVT frequency become higher, which satisfies the working condition of the module shown in Fig. 1(a), and the yield ratio is greatly improved.

The left panel of Fig. 7 (solid dots) shows the yield as a function of I_{sum}. The yield ratio is significantly improved by lowering the total capacitance and is ~100% for the full-range tested current window, even in the slow devices (with low I_{sum}) in Fig. 6. On the other hand, the dynamic power in the device is consumed in the threshold power, leakage power, loading power, and so forth. Higher DPC means higher leakage and higher loading power which can significantly degrade the device performance increasing the total power consumption and thermal budget. The device reliability and lifetime will thus be deteriorated. The DPC target is commonly defined by yield testing with detailed specifications, and it will lead to DPC loss once exceeded. From (1), DPC power is directly proportional to the capacitance, and it can be improved by lowering the capacitance which has been confirmed by the results shown in the right panel of Fig. 7 (hollow dots). Combined with the results shown in Fig. 4(b), fast devices with higher I_{sum} current level can have better yield ratio, but with higher DPC. By lowering the total capacitance, the DPC level can be maintained in a much lower level even in the fast devices, as demonstrated in Fig. 7 comparing the current window between the circuit with and without *RC* optimization. As illustrated in the figure, the I_{sum} window has been significantly enlarged after the optimization with both improved yield loss and DPC loss.

IV. Conclusion

LOD shift degrades the frequency mismatch leading to a lower yield ratio and circuit performance. On the other hand, with higher DPC, the LVT frequency is also lower than SVT in the circuit. The two issues can result in a much higher yield loss. Although the LOD-based yield loss can be recovered by incorporating fast devices, it conflicts with the scenario of DPC performance improvement. Such problem and challenge have been effectively addressed by using BEOL DTCO technologies by engineering the *RC* properties with smaller total capacitance which can boost the device speed as well as lower the DPC level. The experimental results shown here have demonstrated a significant improvement in both yield loss and DPC loss, which can be instructive in solving conventional FEOL device-level difficulties through BEOL optimizations. It also provides a promising pathway for both device and circuit design engineers toward high-performance and low-power applications in advanced technology node circuits and systems.

REFERENCES

[1] C. Fenouillet-Beranger *et al.*, "Efficient multi-VT FDSOI technology with UTBOX for low power circuit design," in *Proc. Symp. VLSI Technol.*, Jun. 2010, pp. 65–66, doi: 10.1109/VLSIT.2010.5556118.

[2] D. Bol *et al.*, "SleepWalker: A 25-MHz 0.4-V sub-mm^2 7-μW/MHz microcontroller in 65-nm LP/GP CMOS for low-carbon wireless sensor nodes," *IEEE J. Solid-State Circuits*, vol. 48, no. 1, pp. 20–32, Jan. 2013, doi: 10.1109/JSSC.2012.2218067.

[3] F. Klass, A. Jain, G. Hess, and B. Park, "An all-digital on-chip process-control monitor for process-variability measurements," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2008, pp. 408–623, doi: 10.1109/ISSCC.2008.4523230.

[4] A. K. Gundu and V. Kursun, "Energy efficient clock distribution with low-leakage multi-V_t buffers," in *Proc. 29th Int. Symp. Power Timing Model., Optim. Simul. (PATMOS)*, Jul. 2019, pp. 113–118, doi: 10.1109/PATMOS.2019.8862097.

[5] P. Ren *et al.*, "Adding the missing time-dependent layout dependency into device-circuit-layout co-optimization—New findings on the layout dependent aging effects," in *IEDM Tech. Dig.*, Dec. 2015, pp. 11.7.1–11.7.4, doi: 10.1109/IEDM.2015.7409679.

[6] C.-Y. Cheng, Y.-K. Fang, J.-C. Hsieh, S.-J. Yang, Y.-M. Sheu, and H. Hsia, "New observations in LOD effect of 45-nm P-MOSFETs with strained SiGe source/drain and dummy gate," *IEEE Trans. Electron Devices*, vol. 56, no. 8, pp. 1618–1623, Aug. 2009, doi: 10.1109/TED.2009.2022690.

[7] C. Ndiaye, V. Huard, R. Bertholon, M. Rafik, X. Federspiel, and A. Bravaix, "Layout dependent effect: Impact on device performance and reliability in recent CMOS nodes," in *Proc. IEEE Int. Integr. Rel. Workshop (IIRW)*, South Lake Tahoe, CA, USA, 2016, pp. 24–28, doi: 10.1109/IIRW.2016.7904894.

[8] C. Ndiaye *et al.*, "Reliability compact modeling approach for layout dependent effects in advanced CMOS nodes," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Apr. 2017, pp. 4C-4.1–4C-4.7, doi: 10.1109/IRPS.2017.7936315.

[9] J. V. Faricelli, "Layout-dependent proximity effects in deep nanoscale CMOS," in *Proc. IEEE Custom Integr. Circuits Conf.*, Sep. 2010, pp. 1–8, doi: 10.1109/CICC.2010.5617407.

[10] K. You, B. Tang, and F. Ding, "Near-optimal virtual machine placement with product traffic pattern in data centers," in *Proc. IEEE Int. Conf. Commun. (ICC)*, Budapest, Hungary, Jun. 2013, pp. 3705–3709, doi: 10.1109/ICC.2013.6655130.