Cell Designer – a Comprehensive TCAD-Based Framework for DTCO of Standard Logic Cells

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***Abstract*—We present the first practical TCAD-based work flow for design-technology co-optimization (DTCO) of standard cells. The flow consists of parametric cell layout templates, layout-based structure generation, mixed-mode transient electrical device simulation, and data collection and analysis. Based on electrical and structural characterizations of the iN14, iN10, and iN7 nodes, the models presented in this work feature a projection for 5 nm technology nodes based on FinFET, nanowire, and nanosheet. Transient five-stage ring-oscillator simulations show a clear advantage for the FinFET in terms of switching frequency and power consumption.**

I. Introduction

There is great need for effective design-technology co-optimization (DTCO) methods in chip design. So far, compact transistor models along with extracted R/C-networks have been the backbone of DTCO efforts in the context of circuits, functions, blocks, and even entire SoCs [1, 2]. TCAD simulations haven't played a major role in DTCO yet, apart from steady-state single-transistor simulations for calibrating compact models. Full transient TCAD device simulations of cells are still uncommon, especially in design. The reasons for this are the following:

a) Structure generation: Traditionally, TCAD software packages offer process simulation or emulation as means of generating a cell geometry from a GDSII layout. This is not only time-consuming, but also produces overly complex geometries with too many mesh elements. Furthermore, running such tools requires a detailed process flow, which prohibits their use in design, as those flows are not disclosed by the foundry.

b) Model validity: In order to obtain meaningful results from TCAD device simulation, the models therein, especially mobility, must be calibrated. TCAD model calibration is a routine task for foundries but not so much for design, which relies mainly on compact models provided by the foundry.

c) Simulation time: 3D TCAD simulations of cells are vastly more computationally heavy that compact model simulations but capture transistor physics, geometry effects, and parasitic couplings more accurately.

II. Power-Performance-Area Work Flow

The Cell Designer tool flow proposed in this paper addresses all three of these issues, providing a clear path to DTCO of standard cells. The flow consists of five components, (i) layout templates, (ii) layout-based structure generation (LSG), (iii) mixed-mode device simulation, (iv) data collection, and (v) scripting.

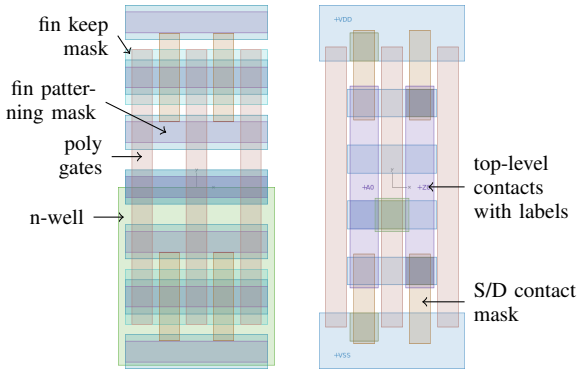

Fig. 1. Left: FEOL & MEOL-parts of layout (fin patterning, well doping, poly gates, contacts), right: BEOL-part of layout (contacts & interconnects); all dimensions in the cell are parametrized: poly pitch, gate lenghts, metal pitches, metal widths, fin pitches and intervals; note that by default the fins are intended to be generated using self-aligned double patterning; labels on the metals layers can be used to reference the device terminals in the mixed-mode simulation.

A. Layout Templates

The layout tool processes layout templates, which are text-based script files defining the geometry of each layer in a procedural fashion. Geometrical parameters, such as pitches, and widths, as well as more fundamental properties of the cell, such as fin, track, and stage counts are conveniently exposed to the user via a graphical interface. A simple inverter template is shown in Figs. 1 and 2. The generated layouts are stored in the industry standard GDSII format.

B. Layout-Based Structure Generation

The layout-based structure generation (LSG) tool translates a two-dimensional layout into a three-dimensional cell geometry by applying chains of constructive solid geometry (CSG) operations [3]. The LSG result of our inverter from Fig. 1 is shown in Fig. 3; a realistic geometry is obtained including layered BEOL structures, as well as tapered trenches, vias, and fins. The CSG recipe itself is presented as text-based script file, which makes the geometrical parameters such as film thicknesses and sidewall inclinations accessible to the user via a graphical interface.

LSG is not a process emulator and as such **does not require detailed process flow information** – knowledge of

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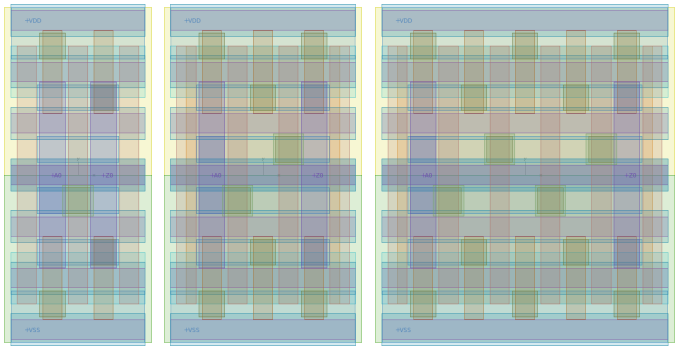

Fig. 2. Three different inverters (1×, 2×, 4×) generated from the same layout template; the layout templates not allow to adjust layer parameters such as pitches and widths, but also to change more fundamental circuit parameters such as, the number of tracks, fins per transistor, and inverter stages.

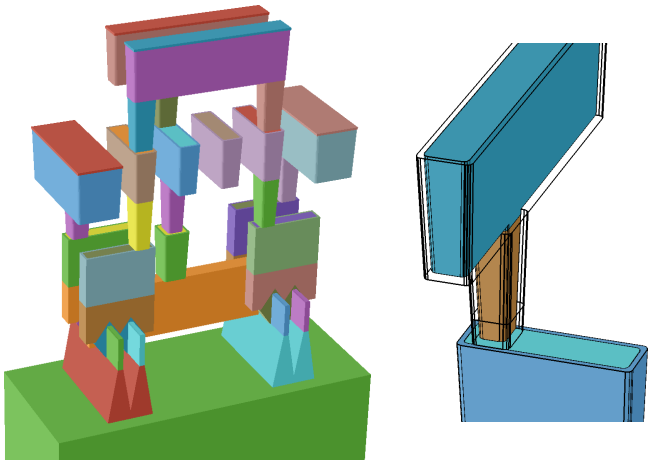

Fig. 3. Left: Inverter cell geometry generated from layout in Fig. 1, right: a close-up shows a realistic interconnect structure with copper material surrounded by a barrier metal layer; the layout-based structure generation (LSG) is parametrized in such way, that fin geometry, various film thicknesses, and metal/via layer heights and taperings can be varied easily.

the final process outcome from SEM/TEM images is sufficient. However, the LSG script is aware of fundamental process features like self-aligned processes for fins and spacers. LSG is quick and accessible to design while providing essentially the same function as a process emulator: generating 3D models from layout. While realistic, the geometry generated by LSG has **simpler surfaces and less mesh points** than one generated by a process emulator, drastically **reducing device simulation time**.

C. Device Simulation Setup

TCAD device simulation of the generated cell is performed by the simulator Minimos-NT [4]. Minimos-NT is based on the drift-diffusion/density-gradient (DD/DG) equations coupled to the Poisson equation and current relations in the interconnects. DD/DG equations make use of empirical models for mobility and quantum correction potentials. The mobility model used here combines the Lombardi [5], Philips [6], and ballistic mobility models [7].

Empirical mobility models are not predictive, and thus need multiple sets of parameters, each calibrated to precisely one technology node. Data for calibration is provided by GTS Nano-Device Simulator (NDS) [8–10], a **subband Boltzmann transport equation** (SBTE) solver that has been shown to be **predictive for advanced technology nodes** [11]. Such a predictive setup produces **meaningful simulation results** even in the absence of complete electrical characterization data.

In the case of this work, the NDS result is fitted to characterization data of the IMEC iN14 node as well as preliminary characterizations of stacked nanowire transistors (NWFETs) [12], using one common, transferable set of a few parameters. From these projections are made for single-transistor curves of iN10, iN7, and iN5, to which the empirical mobility models are fitted.

The generated cell is placed as circuit element in the **mixed-mode** of Minimos-NT (c.f. Fig. 7), where input/supply voltage sources and loads can be added to the device's terminals. If the cell's terminals are named in the layout using labels (Fig. 1), these names are automatically be propagated to the Minimos-NT setup and help identify each terminal in mixed mode. A transient simulation is run to reveal the timing behavior of the cell and its dynamic power consumption.

D. Data Collection and Scripting

Automated curve processing tools extract the timing delays and switching frequency, as well as average dynamic and peak power, and switching energy from the device simulation results. The scripting tool schedules, layout generation, LSG, device simulation, and data processing, and distributes the individual tasks as jobs to a batch queuing system or a cloud computing environment [13].

III. Power-Performance-Analysis for Five-Stage Ring-Oscillator

We now demonstrate the combined features of the presented Cell Designer tool flow to assess the power-performance characteristic of a five-stage ring-oscillator (RO). The layout of the RO is generated from a layout template as shown in Fig. 4. From the layout a 3D model of the RO-cell is generated using LSG, shown in Fig. 5, based on FinFETs. The cell comprises 5 inverters, each consisting of 4 NMOS and 4 PMOS fins, giving a total of 40 active fins. The same layout is used to generate RO-cells based on two alternative technologies, the nanowire FET (NWFET) and the nanosheet FET (NSFET), both shown in Fig. 6, featuring 80 active nanowires and 40 active nanosheets respectively.

Each of the cells is placed in a mixed-mode simulation setup, as shown in Fig. 7, with load resistances of 1 GΩ attached to each terminal to prevent accidental floating. The last output (Z4) is connected to the cell input (A0). Initially, the cell is **upset** by setting the voltage values of Z0, Z1, Z2, Z3, and Z4 to 0 V, VDD, 0 V, VDD, and VDD/2 respectively; a single quasi-stationary simulation step is run in the upset state, which is then used as starting point for the subsequent transient simulation. As seen in Fig. 8, the cell transitions from

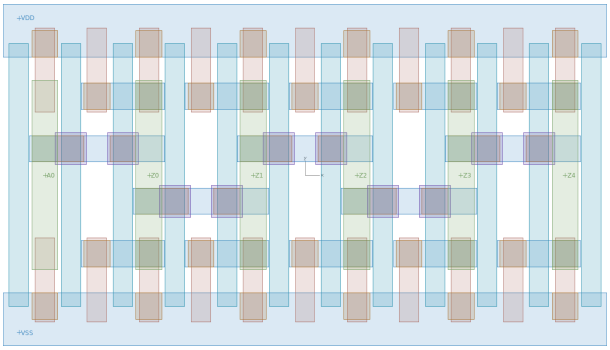

Fig. 4. Five-stage ring-oscillator layout; only poly, contact, and interconnect layers are shown for clarity; the layout is generated from a layout template that allows to specify an arbitrary number of inverter stages, similar to what was shown in Fig. 2.

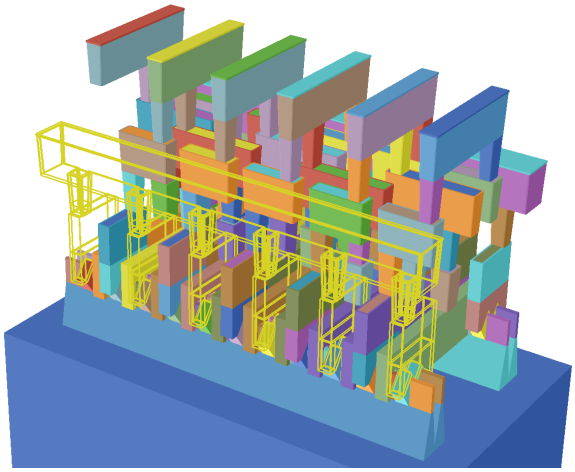

Fig. 5. Five-stage ring-oscillator geometry generated from the layout shown in Fig. 4 using the FinFET technology option; the VSS-part of the power supply was made transparent for better visibility; the oscillator output terminals are visible on top of the cell.

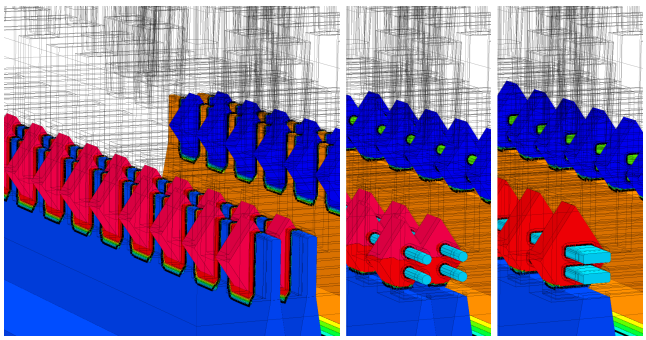

Fig. 6. Three technology options were investigated for the PPA analysis: FinFET, NWFET, and NSFET; the geometry of all three options is shown along with the doping profile; all three geometries were generated from the same layout shown in Fig. 4; FinFET and NWFET were constructed using SADP, while the NSFET was constructed using the fin-patterning mask directly.

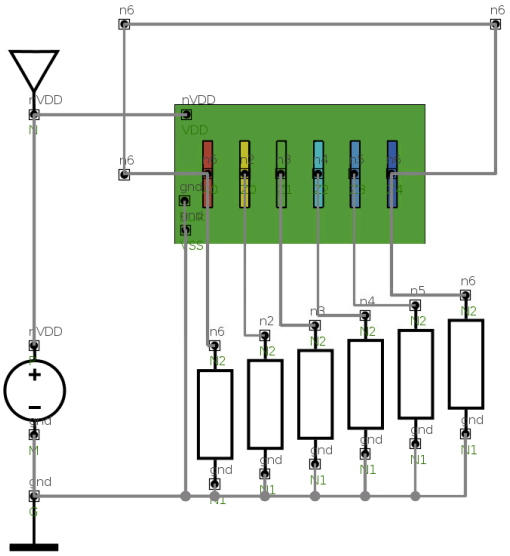

Fig. 7. Five-stage ring-oscillator placed in the mixed-mode of TCAD device simulator Minimos-NT; the ring-oscillator terminals are conveniently displayed in the circuit diagram; mixed-mode also allows to add external loads to the device terminals, mimicking routing resistances and capacitances.

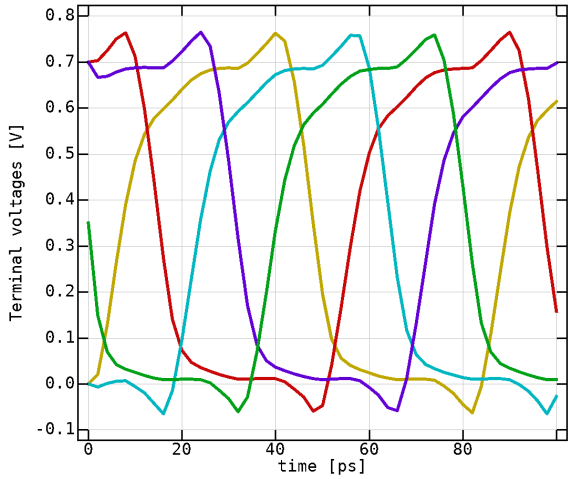

Fig. 8. Output of all ring-oscillator terminals at VDD = 0.7 V; it takes the simulation only a few pico-seconds to assume a stable oscillation pattern.

the initial upset state to a stable oscillation almost immediately. The terminal voltages and dynamic power of the cell are recorded in an output file.

One complete RO-cycle generates enough data to extract the RO-frequency and average power. Since the entire cell (FEOL & BEOL) is simulated as one TCAD model (shown in Fig. 9), all parasitics contained in the simulation domain are automatically being taken into account in the transient simulation.

Varying the supply voltage causes power and RO-frequency to change (Fig. 10). The trade-off between power and frequency is defines by the power-performance characteristic. Figure 11 shows the power-performance characteristics for

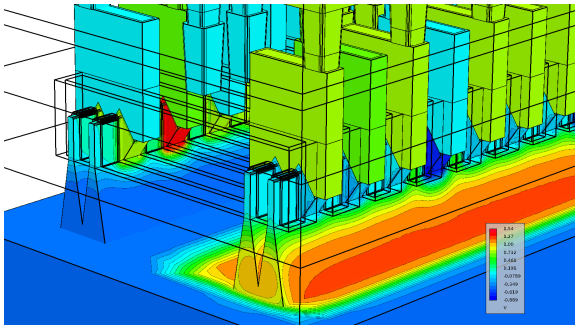

Fig. 9. Electrostatic potential snapshot in FinFET-based ring-oscillator; potential is solved in both the FEOL (transistors, contacts) and the BEOL (interconnects) simultaneously.

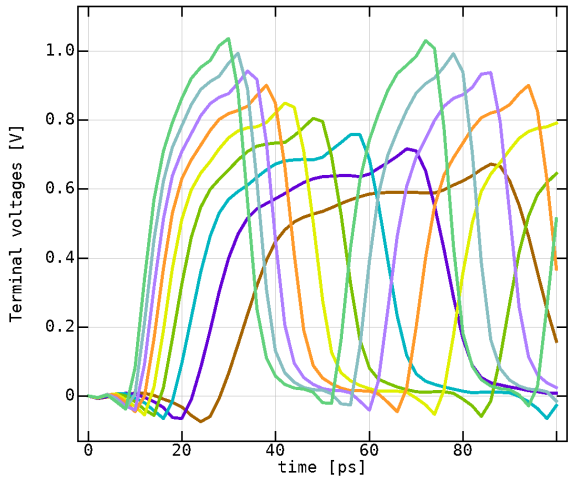

Fig. 10. Output of a single ring-oscillator terminal for VDD swept from 0.6 V to 1 V; the oscillation becomes slower as the supply voltage is reduced.

all three technology options: FinFET, NWFET, and NSFET. All three have the same cell footprint, however the low drive current of the NWFET sets it far apart from the FinFET and NSFET. While the FinFET clearly has the upper hand in the high-performance regime, the NSFET catches up in the low power-regime.

IV. Conclusion

We have presented the TCAD-based Cell Designer tool flow for DTCO of standard cells. The tool flow addresses major issues TCAD-based DTCO faces in design by providing (i) realistic cell geometry generation without detailed process information, (ii) improved turn-around times, (iii) a sound physical basis for transport model calibration with NDS. The capabilities of Cell Designer were demonstrated in a power-performance analysis of ring-oscillators based on FinFET, NWFET, and NSFET technologies.

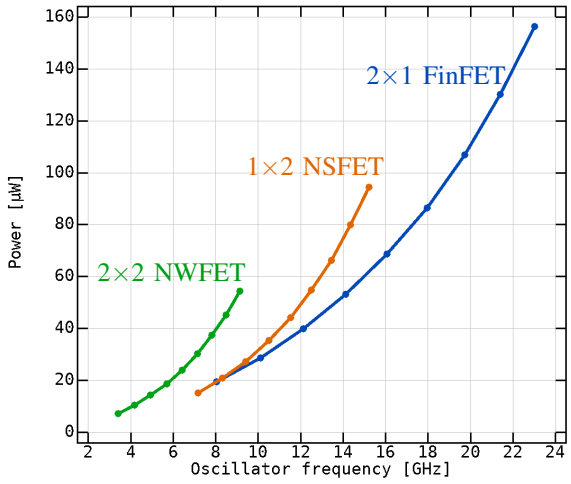

Fig. 11. Power-performance curves for the FinFET, NWFET, and NSFET technology options; in the high-performance regime FinFETs show the least consumed power by comparison, while the low-power regime is contested between FinFET and NSFET

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