Improved MEOL and BEOL Parasitic-Aware Design Technology Co-Optimization for 3 nm Gate-All-Around Nanosheet Transistor

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***Abstract*— In this article, an improved parasitic-aware design technology co-optimization (DTCO) for gate-all-around nanosheet field effect transistor (GAA-NSFET) at 3 nm node is proposed. The presented DTCO flow owns two distinct features. First, a novel de-embedding strategy is designed to avoid the repeated calculation of gate–source/drain contact capacitance. Second, the parasitic resistance of the middle-end-of-line (MEOL) and back-end-of-line (BEOL) is accurately extracted, combing the front-end-of-line (FEOL) simulation and the calculation of MEOL/BEOL equivalent interconnect length. The power, performance, and area (PPA) of the benchmark circuit [15-stage ring oscillator (RO)] are collaboratively optimized. Considering the limitation of contacted gate pitch (CGP) and the process effects, the compromise of structure parameters is studied. GAA-NSFET architecture with 48% reduction in power consumption, 26% increase in speed, and 46% reduction in area is achieved, satisfying the scaling requirement from 5 to 3 nm node. All data here provide an optimization and design foundation for GAA-NSFET in future 3 nm technology node.**

***Index Terms*— Back-end-of-line (BEOL), compact model (CM), design technology co-optimization (DTCO), gate-all-around nanosheet field effect transistor (GAA-NSFET), middle-end-of-line (MEOL), parasitic extraction.**

I. Introduction

With the feature size continuously scaling, novel transistors based on new architecture, material, and mechanism emerge to meet the different performance constrains [1]–[3]. Gate-all-around (GAA) nanowire or nanosheet transistors are considered promising candidates beyond 3–5 nm technology node, because of the ideal gate electrostatics and better power/performance tradeoff compared to FinFET technology [4], [5]. For the logic designs based on GAA field effect transistor (GAAFET), the size of standard cells is determined by contacted gate pitch (CGP) and fin pitch (FP). To reduce the size of standard cell and simultaneously satisfy the requirement of, power, performance, and area (PPA) in microchips, design-technology co-optimization (DTCO) based on TCAD simulation has been developed and has become mandatory in advanced technology nodes [6]–[11]. The technology, transistor, and target circuit design are evaluated together, and the PPA of the target circuit is calculated and fed back during DTCO optimization [10]. Thus, technology parameters can be iteratively adjusted to achieve the best circuit performance.

The current TCAD-based DTCO flow includes front- end-of-line (FEOL) TCAD simulation, compact model (CM) extraction, interconnect *RC* extraction for middle-end-of-line/back-end-of-line (MEOL and BEOL), and benchmarking circuit simulation [12]–[15]. When evaluating the FEOL transistor, FinFET or GAAFET with metal M0 are generally structured and the standard BSIM-CMG model is adopted [16]. As for the case of MEOL and BEOL, the interconnect line with constant length are used to assess the parasitic *RC* load, such as 25 × (CGP + MP), 25 × (CGP + MP)/7.5, and 100 × CGP [17]–[20]; here MP presents metal pitch. However, two distinct limitations exist in the above-mentioned estimation method. First, the assumed equivalent length is not always held for arbitrary technology node, especially for BEOL, whose metal resistivity is sensitive to different process conditions [21]. Second, the assumed equivalent BEOL length may not match with the extracted capacitance from the FEOL SPX simulation. More severely, when extracting the FEOL CM, gate–source/drain contact capacitance C_{co}, gate fringe capacitance C_{if}, and C_{ov} are included in FEOL TCAD simulation. However, during MEOL and BEOL capacitance extraction, the gate–source/drain contact capacitance C_{co} is also contained in SPX 3-D simulation. Therefore, the gate–source/drain contact capacitance C_{co} is repeatedly extracted in the aforementioned DTCO flow, which will inevitably affect the final accuracy and credibility.

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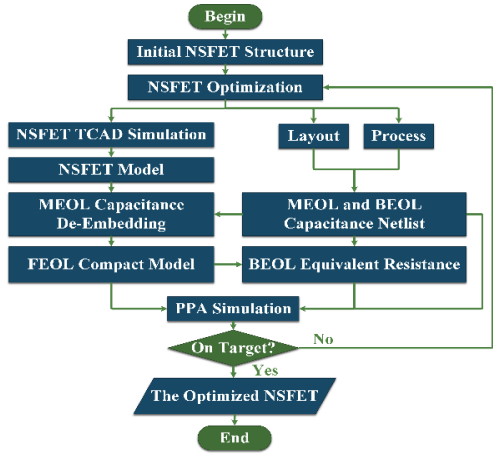

Fig. 1. Proposed DTCO flow for 3 nm GAA-NSFET.

TABLE I
DEVICE PHYSICS PARAMETERS OF STANDARD GAA-NSFET

Design rules of standard NSFET	Value (nm)
Contact Gate Pitch, CGP	45
Fin Pitch, FP	21
Metal Pitch, MP	21
Gate length L_g	15
Length of high-k spacer, LspHK	1.5
Length of high-k spacer, LspLK	4
Source/Drain length, LSD	9.5
Nanosheet thickness, TNS	5
Nanosheet spacer, NSS	9
Nanosheet width, WNS	10

In this work, an improved DTCO flow is proposed to overcome the aforementioned two issues. A novel de-embedding method is designed to avoid the repeated calculation of gate–source/drain contact capacitance, and a modified assessment method for BEOL and MEOL resistance is given. Results demonstrate that the proposed flow has an excellent design exploration co-optimized with patterning for future 3 nm technology node. This work is arranged as followed: Section II illustrates the proposed DTCO flow, including FEOL process simulation, CM extraction, MEOL/BEOL parasitic extraction, and the de-embedding for MEOL contact capacitance. Section III demonstrates the validity of the proposed flow, taking the CGP optimization as an example. The conclusion is drawn in Section IV.

II. IMPROVED DTCO FLOW DESIGN

Fig. 1 depicts the proposed improved DTCO flow for 3 nm GAA nanosheet field effect transistor (GAA-NSFET), including FEOL process and device simulation, CM extraction, resistance extraction of MEOL/BEOL, and benchmark circuit simulation. The innovation of the proposed DTCO flow exists in the avoidance of repeated calculation of gate–source/drain contact capacitance, as well as the accurate extraction of equivalent resistance for MEOL and BEOL. Each step is illustrated as follows.

A. Standard Device Simulation and FEOL CM

Fig. 2 depicts the 3-D structure and 2-D cross-section of GAA-NSFET at 3 nm technology node, where three

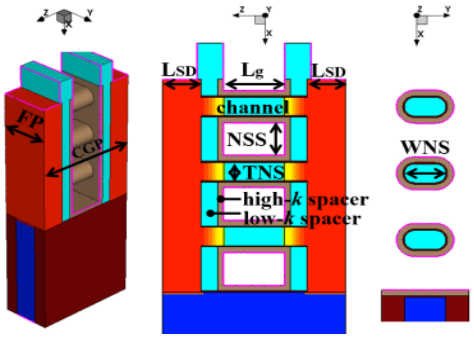

Fig. 2. 3-D structure and 2-D cross-section of 3 nm GAA-NSFET under investigation.

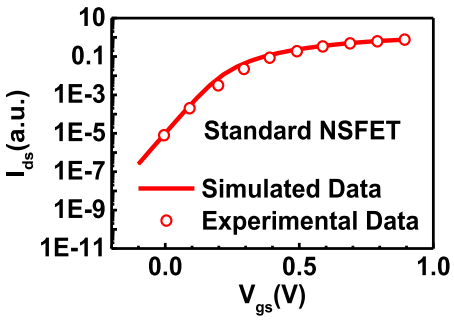

Fig. 3. Comparison of transfer curves between the simulated (line) and experimental measured (symbols) data [23].

TABLE II
ELECTRONIC CHARACTERISTICS OF THE STANDARD NSFET

	V_{th} (V)	SS (mV/dec)	I_{dsat} (μA)	DIBL (mV/V)
NMOS	0.124	65.5	90.49	18
PMOS	-0.137	73.7	88.07	23

nanosheets are vertically stacked. The critical design parameters are presented in Table I. Simulations are performed with 3-D Sentaurus TCAD [22]. The critical physical model includes the stress model, ballistic model, and quantum confinement model. The simulation setup is first calibrated with the reported experimental data [23], as shown in Fig. 3. The excellent agreement between the simulated and experimental data proves the validity of the simulation environment. The electronic characteristics of the standard n-type and p-type NSFET are summarized in Table II, where benchmarking is fixed at $I_{off} = 2.5$ nA under $V_{DD} = 0.65$ V.

Then the CM of FEOL GAA-NSFET is built based on BSIM-CMG. Taking the n-type GAA-NSFET as an example, the comparison between TCAD simulation and BSIM-CMG modeled data is shown in Fig. 4. An accurate agreement is obtained for dc and ac characteristics, and the largest root mean square (rms) error is lower than 2%.

B. MEOL and BEOL Capacitance Extraction

To accurately simulate PPA characteristics of ring oscillator (RO), the interconnection parasitic capacitance/resistance of MEOL and BEOL should be included in the prosed DTCO flow. As a basic unit of RO, the MEOL and BEOL parasitic

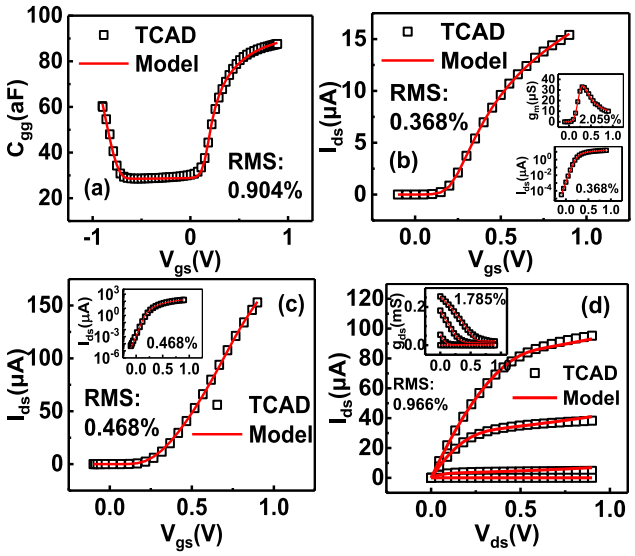

Fig. 4. Comparison between TCAD simulated (symbols) and BSIM-CMG modeled curves (lines) of the standard n-type NSFET. (a) C_{gg}–V_{gs}; I_{ds}–V_{gs} under (b) linear region and (c) saturation region, and (d) I_{ds}–V_{ds}.

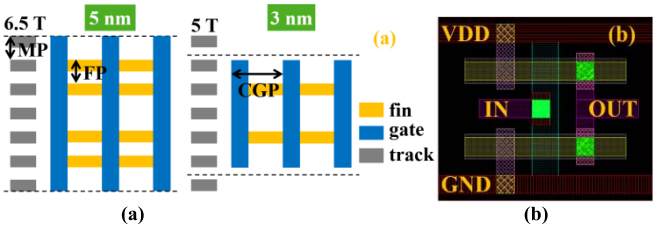

Fig. 5. (a) Standard cell layout template from 5 to 3 nm node. (b) Layout of single-stage inverter in RO.

capacitances ($C_{MEOL\&BEOL}$) of an inverter are first extracted. The standard cell and invert layout under 5 and 3 nm technology nodes are separately depicted in Fig. 5. The area of the standard cell at 3 nm node decreases about 46% compared to that under 5 nm node, satisfying the area scaling (>40%) from 5 to 3 nm. Besides, M1 connection between two-stage inverters is included in the layout to consider the parasitic capacitance in RO. Fig. 6 shows the 3-D structure of an invert built in SPX, and six parasitic capacitances among four terminals (IN, OUT, VDD, and GND) are depicted. The extracted total MEOL and BEOL parasitic capacitance $C_{MEOL\&BEOL}$ based on the above-mentioned standard GAA-NSFET is depicted in Table III. The capacitance related to the "IN" terminal such as C_{GND_IN}, C_{VDD_IN}, and C_{OUT_IN} is significantly higher than other capacitance, due to the complex and huge structure and the central position of the four electrodes. Besides, the total MEOL and BEOL parasitic capacitance (140 aF) approaches the FEOL gate capacitance C_{gg} (84.5 aF for nMOS and 84.1 aF for pMOS), therefore, it cannot be ignored in NSFET at 3 nm technology node.

C. De-Embedding MEOL Contact Capacitance

In FEOL CM extraction, the gate–source/drain contact capacitance C_{co}, gate fringe capacitance C_{if} and C_{ov} are included, as shown in Fig. 7(a). However, during MEOL and

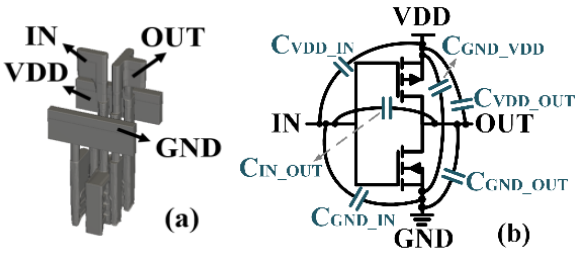

Fig. 6. (a) Metal interconnection structure of inverter. (b) Interconnection parasitic capacitance division of inverter.

TABLE III
$C_{MEOL\ \&\ BEOL}$ EXTRACTION RESULTS FOR INVERTER (UNIT: aF)

C_{GND_VDD}	C_{GND_IN}	C_{GND_OUT}	C_{VDD_IN}	C_{VDD_OUT}	C_{IN_OUT}
4.169	31.348	7.851	33.478	7.869	55.212
C_{total} = 140 aF					

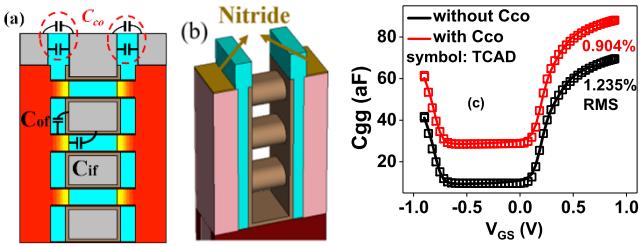

Fig. 7. (a) Schematic of NSFET C_{gg}. (b) Simulation structure of C_{co}. (c) Comparison between $C_{gg\text{-}co}$ (symbols) and BSIM-CMG modeled curve (line).

BEOL capacitance extraction, the gate–source/drain contact capacitance C_{co} is also contained in the SPX 3-D inverter, since the gate–source and drain contacts are constructed in SPX. Thus, the gate–source/drain contact capacitance C_{co} are repeatedly extracted, and it should be removed from FEOL CM or MEOL/BEOL parasitic capacitance. C_{co} contributes to the six parasitic capacitances in Table III, and it is difficult to be eliminated from MEOL/BEOL parasitic extraction. Here, we remove the repeated C_{co} from FEOL CM, to ensure that it is calculated only once during the whole DTCO design. The de-embedding structure is designed as shown in Fig. 7(b), where a very thin (0.5 nm) nitride layer is separately added under the source and drain contact. Thus, the voltage cannot be applied to the bulk–source/drain region, and only the contact capacitance C_{co} exists in the proposed de-embedding structure, while C_{if} and C_{ov} do not exist. Once obtaining C_{co}, remove it from the previous FEOL C_{gg}. After de-embedding C_{co}, the gate capacitance curve in Fig. 4(a) should be refitted to refresh the FEOL CM, by only adjusting the model parameters related to gate capacitance, while other parameters are no longer modified. Fig. 7(c) shows the comparison of the gate capacitance curve before and after de-embedding C_{co}, where C_{gg-co} represents the gate capacitance removing C_{co}.

D. BEOL Equivalent Resistance Extraction

The equivalent resistance of MEOL can be directly simulated by setting the resistivity in TCAD simulation. However,

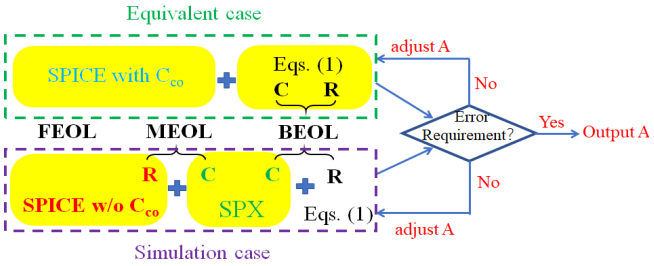

Fig. 8. Method to determine the undetermined coefficient "*A*" related with equivalent MEOL length.

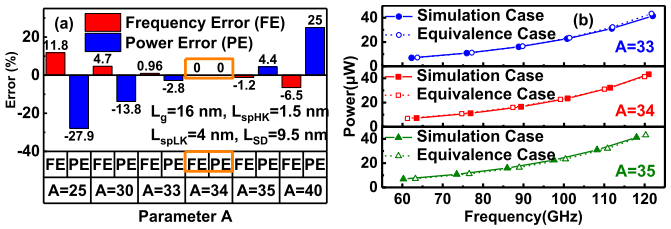

Fig. 9. For 15-stage RO with three-fan-out. (a) Error distribution between simulation and equivalence case for different coefficient *A* at V_{DD} = 0.65 V. (b) Power-frequency characteristics of under different BEOL interconnect lengths.

the resistance of BEOL cannot be directly extracted by setting the metal resistivity in SPX simulation, because of the high sensitivity to process variations [21]. To accurately extract the equivalent resistance of BEOL, an improved estimation method is proposed here. The equivalent BEOL length $L_{\mathrm{BEOL,equ}}$ is not a fixed value, while a value to be calculated as

$$L_{\mathrm{BEOL,equ}} = A(\mathrm{CGP} + \mathrm{MP}) \tag{1}$$

where "*A*" is an undetermined coefficient. To reduce *RC* delay, *Ru* has been adopted as BEOL interconnect metal at 3 nm technology node [20], and the unit resistance and capacitance are separately 995 Ω/μm and 225 aF/μm [24]. Fig. 8 depicts the method to determine the coefficient "*A*" related to equivalent BEOL length, by comparing the equivalent case with the simulation case. In the simulation case, the parasitic capacitance of MEOL/BEOL is based on the extraction from SPX simulation. FEOL *RC* and MEOL resistance come from the SPICE model without C_{co}, and BEOL resistance is estimated by (1). While in the equivalent case, the *RC* load of FEOL and MEOL both come from the SPICE model with C_{co}, and the *RC* load of BEOL is calculated from (1). On the circuit level, if the PPA characteristics obtained from the simulation case is the same as that from the equivalent case, i.e., the capacitance of BEOL in the actual SPX tool is the same as the calculated value from (1), it means that the actual BEOL interconnect length is indeed *A* (CGP + MP).

Taking 15-stage RO with three-fan-out based on above-mentioned standard GAA-NSFET as an example, when the coefficient "*A*" increases from 25 to 40, the calculated deviation between the simulation and equivalent case gradually decreases and then increases, as shown in Fig. 9(a). The minimum error appears at $A = 34$, and the comparison of

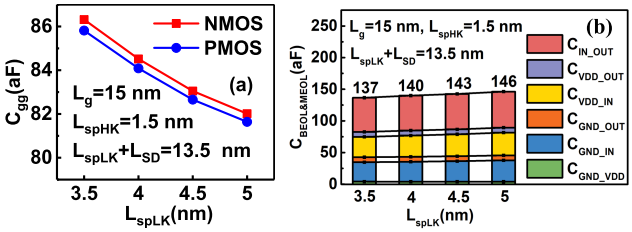

Fig. 10. Variation of parasitic capacitance under the tradeoff between L_{spLK} and L_{SD}. (a) FEOL gate capacitance C_{gg}. (b) MEOL/BEOL capacitance $C_{\mathrm{MEOL\&BEOL}}$ of an inverter.

power-frequency characteristics between simulation and equivalent case with $A = 33$, 34, and 35 are separately depicted in Fig. 9(b). The fitting situations for $A = 33$ and $A = 35$ both have certain deviations, so the accuracy of $A \pm 1$ could obtain an accurate fitting result. On the other hand, it can be seen that the interconnect length of BEOL cannot always be assumed as 25 (CGP + MP) for arbitrary processes and circuits, and it should vary for different processes and circuits. So far, the equivalent resistance of BEOL has been accurately determined, and the obtained equivalent BEOL length is obviously different from the conventional fixed value.

III. Structure Optimization Under CGP Limitation

The critical dimension of GAA-NSFET along channel direction is limited by CGP, including gate length L_{g}, high-*k* spacer length $L_{\mathrm{spH}K}$, low-*k* spacer length $L_{\mathrm{spL}K}$, and source/drain length L_{SD}, as shown in Fig. 2, and calculated as

$$\mathrm{CGP} = L_{\mathrm{g}} + 2(L_{\mathrm{spH}K} + L_{\mathrm{spL}K} + L_{\mathrm{SD}}). \tag{2}$$

Therefore, under a fixed CGP restriction, the compromise of the structural dimension can be optimized, in terms of the performance on the device level and RO circuit level. CGP is fixed as 45 nm at 3 nm technology node, and the tradeoff exists between every two variables. In this section, the effects of such physical parameters on RO performance are evaluated based on the above-proposed optimized DTCO flow. The optimization aims at obtaining 40% area shrink, 20% frequency faster and 40% power reduction, compared to the reported 5 nm technology node [19]. In the following DTCO optimization, the maximum error of parameter "*A*" is lower than 5.6% when determining BEOL equivalent resistance.

In the GAA-NSFET fabrication process, the source and drain are formed through the epitaxy process under the mask of the low-*k* spacer. In the subsequent high-*k*-metal-gate (HKMG) process, after the nanosheets are released, the first dielectric SiO_2 is generated by thermal oxidation, and then the second dielectric HfO_2 is deposited by atom layer deposition (ALD). Thus, HfO_2 with the same thickness will be deposited on the sidewall of the low-*k* spacer, i.e., the high-*k* spacer. Consistent with the previous report [25], [26], the saturation driving current I_{dsat} increases with $L_{\mathrm{spL}K}$ decreasing (i.e., L_{SD} decreasing), while the low-*k* spacer effectively reduces the parasitic capacitance to enhance the switching performance.

The competition between $L_{\mathrm{spL}K}$ and L_{SD} is first discussed. Fig. 10 depicts the variation of FEOL gate capacitance C_{gg} of a

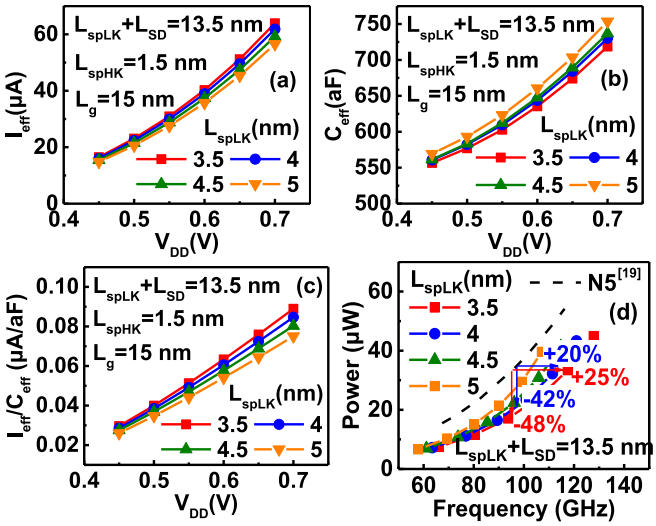

Fig. 11. Key characteristics of 15-stages RO. (a) I_{eff}, (b) C_{eff}, (c) I_{eff}/C_{eff}, and (d) power-frequency characteristics.

single transistor, and MEOL/BEOL capacitance of an inverter for varied L_{spLK}. The gate capacitance C_{gg} in transistor level is expected to decrease with L_{spLK} increasing. The decreased C_{gg} in turn weakens the gate coupling and degrades I_{dsat}. However, contrary to FEOL gate capacitance C_{gg}, MEOL/BEOL capacitance of a single inverter increases with L_{spLK} increasing, due to the area enlargement of the capacitors with the low-k spacer as the dielectric. Therefore, a tradeoff exists between FEOL gate capacitance C_{gg} and MEOL/ BEOL capacitance. Furthermore, MEOL/BEOL capacitance has approached or even exceeded the FEOL transistor-level capacitance C_{gg}. When L_{spLK} increases from 3.5 to 5 nm, FEOL capacitance C_{gg} decreases about 4.3 aF, while MEOL/BEOL capacitance $C_{MEOL\&BEOL}$ increases about 9 aF. The variation of parasitic resistance R_{eq} has the same trend as $C_{MEOL\&BEOL}$, which will further degrade the effective current at the circuit level. Therefore, a careful co-optimization design should be performed from the point of circuit level.

Fig. 11 depicts the variation of key performance of 15-stage RO under the tradeoff between L_{spLK} and L_{SD}. Here I_{eff} and C_{eff} separately present the effective current and load capacitance of 15-stage RO, and are calculated as

$$I_{eff} = P/V_{DD} \tag{3}$$

$$C_{eff} = I_{eff}/(f \cdot V_{DD}) \tag{4}$$

where P and f are separately the total power consumption and the oscillation frequency of 15-stage RO. Consistent with the variation of transistor saturated current I_{dsat}, I_{eff} here decreases with L_{spLK} increasing, as shown in Fig. 11(a). Furthermore, I_{eff} is proportional to the total power consumption of the circuit, thus RO based on NSFETs with larger L_{spLK} has lower consumption at the same V_{DD}. As discussed earlier, the increased $C_{MEOL\&BEOL}$ dominates the total parasitic capacitance, as a result, C_{eff} of15-stage RO increases with L_{spLK} increasing, as shown in Fig. 11(b). The frequency is proportional to the ratio of I_{eff}/C_{eff}, and also decreases with L_{spLK} increasing, as shown in Fig. 11(c).

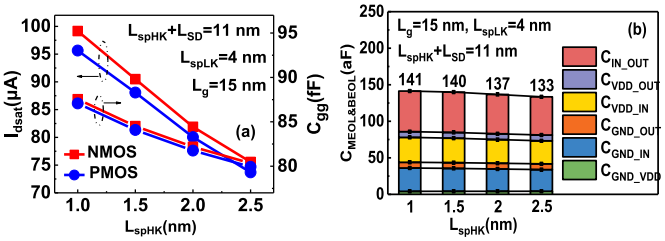

Fig. 12. Variation of (a) I_{dsat} and C_{gg} of NSFET and (b) $C_{MEOL\&BEOL}$ of single inverter in L_{spHK}–L_{SD} case.

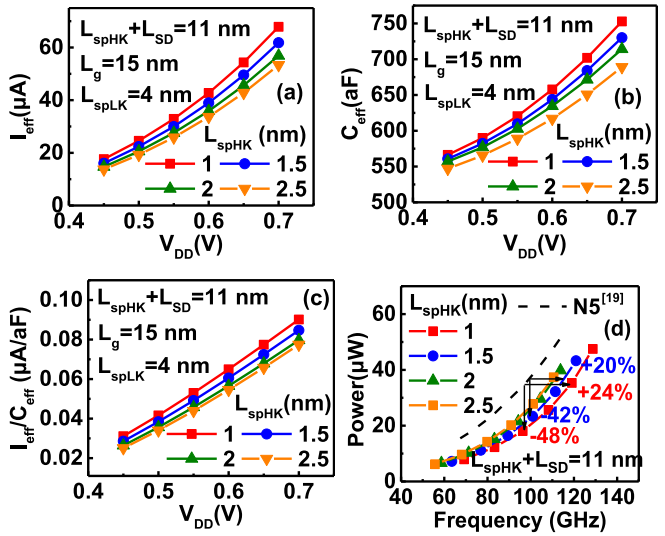

Fig. 13. (a) I_{eff}, (b) C_{eff}, (c) I_{eff}/C_{eff}, and (d) power-frequency characteristics of the RO in L_{spHK}–L_{SD} case.

In conclusion, both the power consumption and frequency of 15-stage RO decrease with L_{spLK} increasing, therefore, RO performance can be explored by the power-frequency characteristics. As shown in Fig. 11(d), the power-frequency curves shift to the left with L_{spLK} increasing, indicating degraded PPA characteristics. Compared to the power-frequency curve at the 5 nm technology node in [19], two cases satisfy the scaling requirements down to the 3 nm node. One is the standard NSFET, and the other is the structure with L_{spLK} of 3.5 nm and L_{SD} of 10 nm, which reduces power consumption by 48% and increases speed by 25%.

In the tradeoff case between L_{SD} and L_{spHK}, as shown in Fig. 12(a), FEOL gate capacitance C_{gg} decreases with L_{spHK} increasing, because the high-k spacer and gate oxide HfO_2 are deposited simultaneously, and the increased gate oxide reduces C_{gg}. Besides, the driven current I_{dsat} on transistor level inevitably degrades with L_{spHK} (i.e., t_{HfO2}) increasing. Here $C_{MEOL\&BEOL}$ of a single inverter is shown in Fig. 12(b), and it also decreases with L_{spHK} increasing. Because the high-k spacer is completely surrounded by the gate electrode, C_{IN-OUT}, C_{VDD-IN}, and C_{GND-IN} decrease significantly compared to other capacitances. The equivalent resistance also decreases with L_{spHK} increasing, which is beneficial to improve the circuit drive current.

As a result, both I_{eff} and C_{eff} decrease with L_{spHK} increasing in the tradeoff between L_{spHK} and L_{SD}, as shown in

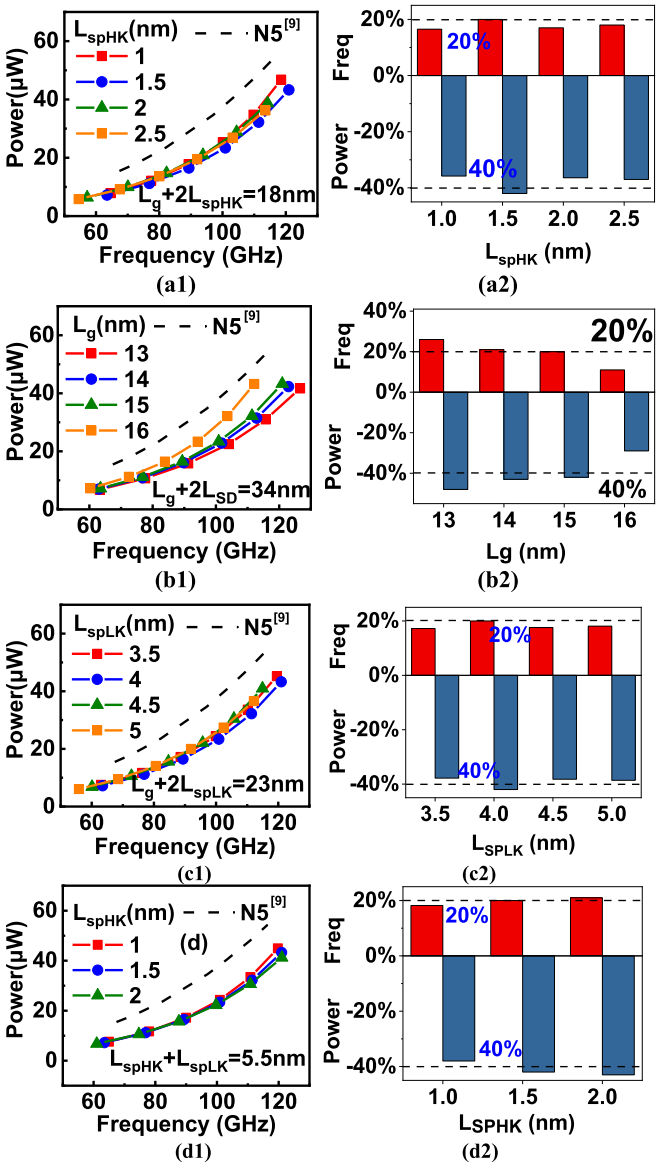

Fig. 14. Power-frequency characteristics of the 15-stage RO in the tradeoff case. (a) L_{spHK}–L_g. (b) L_g–L_{SD}. (c) L_g–L_{spLK}. (d) L_{spHK}–L_{spLK}.

Fig. 13(a)–(c). Furthermore, I_{eff}/C_{eff} also decreases as L_{spHK} increases. As depicted in (3) and (4), the power consumption and operation frequency of 15-stage RO are separately proportional to I_{eff} and I_{eff}/C_{eff} under the same V_{DD}. Fig. 13(d) shows that although the improvement of operation speed requires the loss of power consumption, the increment of operating frequency is higher than the degradation of power consumption. Thus, the structure with smaller L_{spHK} can obtain better performance at the circuit level. The solution with L_{spHK} = 1 nm and L_{SD} = 10 nm is proved to own the best performance, although the interconnection capacitance is slightly increased. Compared to the 5 nm node, the power consumption of RO reduces by 48% and the speed improves by 24%.

For the remaining four cases, the optimized PPA characteristics are also investigated, as shown in Fig. 14. Each case has an optimized combination that satisfies the scaling requirement from 5 to 3 nm technology node. For example, the case with

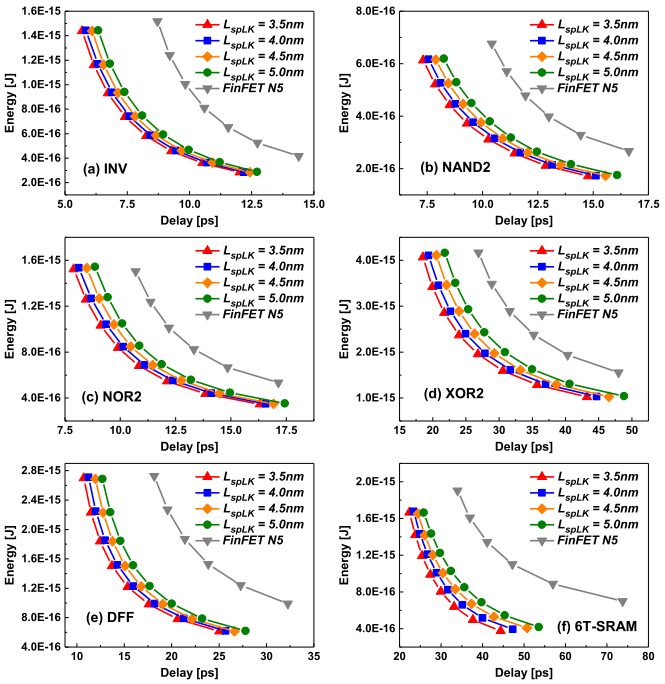

Fig. 15. Power-frequency characteristics comparison of other logic gate circuits between 5 and 3 nm in L_{spLK}–L_{SD} tradeoff case. (a) Inverter. (b) NAND2. (c) NOR2. (d) XOR2. (e) DFF. (f) 6T-SRAM. Here the sum of L_{spLK} and L_{SD} is fixed as 13.5 nm.

L_g = 13 nm and L_{SD} = 10.5 nm owns a 26% improvement of operation speed and 48% decrement of power. To make the proposed method trustworthy, taking the tradeoff between L_{spLK} and L_{SD} as an example, the evaluations of other logic gate circuits are also carried out from 5 to 3 nm technology nodes including INV, NAND2, NOR2, XOR2, D flip-flop (DFF), and 6T-static random access memory (SRAM). As shown in Fig. 15, it can be found that a tradeoff between frequency (delay) and power exists, and a smaller L_{spLK} represents a better performance, i.e., a lower power at a fixed delay. Compared to the 5 nm technology node, the cases with L_{spLK} = 3.5 and 4 nm at 3 nm node satisfy the scaling requirement, i.e., the power decreases over 40% at a fixed delay, and the delay decrease over 20% and at fixed power.

IV. Conclusion

In this article, we proposed the improved DTCO flow that combined the FEOL CM and parasitic *RC* of MEOL and BEOL for 3 nm GAA-NSFET. The electronic characteristics of the FEOL were described based on the BSIM-CMG. The netlist of the interconnection parasitic capacitance was extracted toward the layout and process flow. The repetitive contact capacitance in FEOL CM and capacitance netlist was extracted and de-embedded. The equivalent parasitic resistance of BEOL was extracted by the proposed equivalent simulation method. Subsequently, considering the limitation of CGP and the influence of the structural dimensions on the process, the tradeoff optimization of the NSFET structural dimensions was explored by the proposed DTCO flow. Taking RO as the benchmarking circuit, the best NSFET structure has achieved a 46% reduction in area, a 48% reduction in power consumption, and a 26% increase in frequency.

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