Materials to Systems Co-Optimization Platform for Rapid Technology Development Targeting Future Generation CMOS Nodes

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(Invited Paper)

***Abstract*— Design technology co-optimization (DTCO) has been a workhorse in optimizing logic technology innovations for a few generations now. With increased complexity associated with each new node and the growing number of technological innovations, it is time to expand the conventional DTCO flows. In this article, we present a novel materials to systems co-optimization (MSCO) platform, expanding the boundaries of traditional DTCO to encompass materials modeling to all the way to system design. To demonstrate the application of our MSCO platform, we discuss various front-end-of-line (FEOL) and middle-of-line (MOL)/back-end-of-line (BEOL) technologies and show their impact on device and circuit performance.**

***Index Terms*— Back end of line (BEOL), complementary FET (CFET), FinFET, front end of line (FEOL), gate-all-around (GAA), materials to systems co-optimization (MSCO), middle of line (MOL), parasitic capacitance, parasitic resistance.**

I. Introduction

THE transistor density has doubled every technology node following Moore's law [1], whose pace was a result of compromise between enhanced chip performance and the cost of shrinking the technology [2]. This rapid scaling has continued with: 1) innovative transistor knobs such as strain engineering, high-K metal gate, and FinFET technology [2] and 2) area scaling by the co-optimization of the design and process technologies (DTCO) [3]. The importance of DTCO was well demonstrated with the long path of maturing extreme ultraviolet lithography (EUV) to succeed in 193-nm immersion technology. The solutions in design side, such as unidirectional metal layers and contact-over-active-gate (COAG) technology, served the purpose of cell height scaling [4], [5]. DTCO now has become an essential flow for performance targeting in advanced nodes. It was reported that over 40% of the total performance gain would be attributed to DTCO in a 5-nm node [6].

Beyond performance optimization, DTCO is now an indispensable flow for the development of advanced nodes [7]. For pathfinding of the future nodes, traditional TCAD simulation was adopted to reduce the development cost and time-to-market [8]. In the traditional TCAD-based DTCO, the front-end-of-line (FEOL) technology options are realized in the TCAD process and device simulation ahead of fabrication devices. The traditional TCAD-based DTCO has evolved into advanced modeling-based DTCO (see Fig. 1) where a compact model calibrated to the electrical characteristics from the traditional TCAD simulations is added to the flow, along with the parasitic resistance and capacitance extraction from middle-of-line (MOL) and back-end-of-line (BEOL) process modeling to optimize the power, performance, and area (PPA) at small circuit level, such as ring oscillator. The calibration of compact model was automated to enable a variability-aware DTCO, which generally demands a huge number of sample data [9]. Recently, system-technology co-optimization (STCO) has been proposed, which is an advanced version of DTCO for optimization of the 2.5-D and 3-D IC integration [10]. Thus, over the years, the scope of DTCO has been extended from modeling for individual devices to versatile multiscale/multidomain modeling framework in response to the growing challenges for node scaling. It is expected that the coverage of DTCO would grow with technology node.

Recognizing these challenges and the shortcomings of existing DTCO or STCO frameworks, at Applied Materials [11], we developed a "materials to systems co-optimization" (MSCO) platform, which extends the conventional DTCO by considerations of various knobs, such as device-level choices

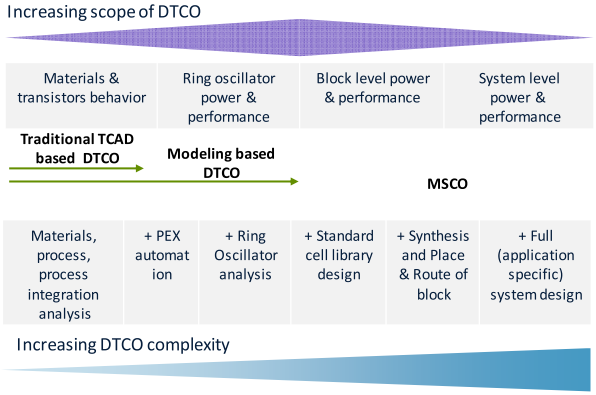

Fig. 1. Different types of DTCO and comparison of their scopes and complexity.

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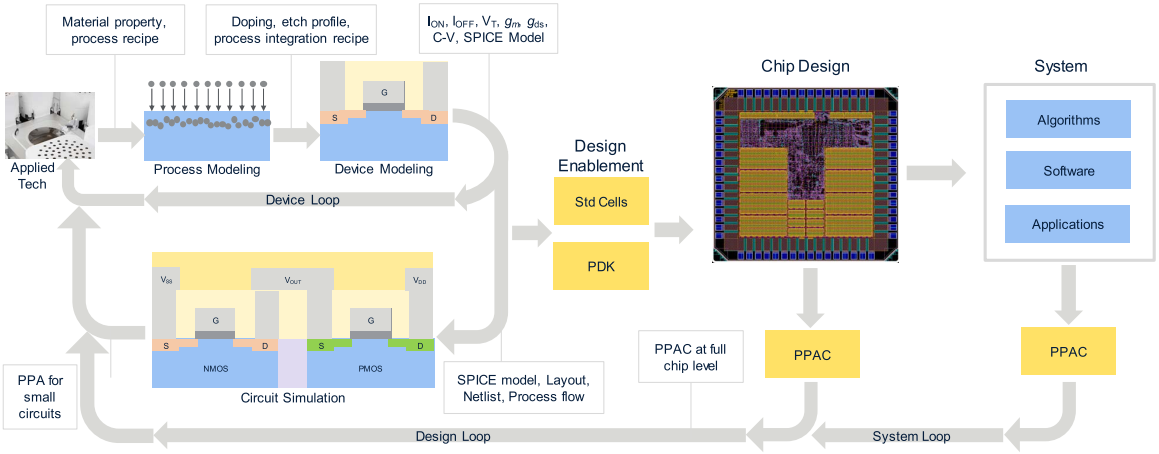


Fig. 2. Detailed block diagram of the MSCO platform.

including complex materials, process steps, device architecture, as well as design-level choices such as design rules, number of metal tracks in a standard cell, power distribution, and others [12]. This MSCO platform not only extends the coverage of technology co-optimization from the atomistic simulations to the system level but also enables rapid assessment of several newer technological knobs for quick evaluation of the impact at a system level. Section II describes the basic building blocks of this MSCO platform. In the subsequent sections, we describe various FEOL and MOL/BEOL technologies and their evaluation using this MSCO platform.

II. Description of MSCO Platform

Fig. 2 shows a detailed view of the MSCO platform, starting from material and process modeling of Applied Materials' technologies and finally evaluating PPA and reliability at chip level for the intended material, process, or structural modification. To evaluate the impact of material modification using MSCO, first atomistic modeling is deployed to calculate properties of different materials. Material resistivity, grain boundary scattering, and surface scattering-related parameters are typical examples of outputs from atomistic modeling. For structural and process flow modifications, process modeling is performed using TCAD process simulation tools, generating a 3-D device structure, such as for logic FinFET or gate-all-around (GAA) device, FEOL, or MOL/BEOL segments. Next, this 3-D structure, along with the modifications in material properties is used for electrical modeling of device characteristics. The typical output of the FinFET or GAA modeling is its current–voltage and capacitance–voltage characteristics. The typical output of MOL/BEOL modeling is parasitic resistances and capacitances. The device performance can be optimized at this level by looking at its performance metrics, such as subthreshold swing, DIBL, and I_{ON}–I_{OFF}. This can help in narrowing down the range of optimization parameters in any given technology. Next, a SPICE model is formed by combining the FEOL transistor I–V/C–V characteristics and MOL/BEOL parasitic resistance and capacitances. Using this transistor model, PPA analysis can be performed for small circuits, such as ring oscillator (RO). Next, using Standard Cell Library Compiler (SLiC) [13], layouts of standard cells are created based on the typical design rules and appropriate assumptions for a given node. Combining these layouts and individual transistor characteristics, the standard cells are characterized and a process design kit (PDK) is generated. The standard cells and PDK are then used to synthesize and for place-and-route for a chip design. The PPA metric is revaluated at this chip level for the technology knobs under assessment. Next, this chip is integrated in a system with typical algorithms, software and applications, which enables us to do a further PPA analysis at the system level, specific to the system application.

In the next sections, we will evaluate different technologies and their impact on circuit performance using our MSCO platform. We will look at different FEOL and MOL/BEOL-related technologies. For conciseness, we will focus on PPA evaluations of small circuits. We will use a 31-stage ring-oscillator (RO) circuit as a small circuit representative; however, any other circuit, such as a standard cell or an static random access memory (SRAM) bit-cell or array, can also be used for this purpose as described in our previous work [14].

III. FEOL Technology Development Using MSCO Platform

In this section, we focus on FEOL technology development using the MSCO platform. For current FinFET technologies, single diffusion break (SDB) [5], [15], [16] has been used as a key area-scaling enabler; however, it demands stringent mask-placement alignment, lack of which leads to epi-volume and drive-current variations. Self-aligned SDB (SA-SDB) [16] has been proposed to relieve some of these issues [see Fig. 3(a)], but it relaxes the channel stress of the pMOS device, similar to the dual diffusion break (DDB) technology. Recent studies have shown up to ∼90% stress relaxation for a pMOS FinFET device next to fin-cuts, leading to a severe drive-current and performance loss for pMOS [17]. To recover the channel stress in pMOS, a stressed dielectric deposition is proposed [18] for SA-SDB fill. The MSCO is deployed to study the impact of stress-type (whether tensile or compressive) and its magnitude on nMOS and pMOS devices and RO performance. About 2-GPa compressive stress in the SDB-fill dielectric was shown to be necessary to recover the pMOS channel stress. However, the same 2-GPa compressive stress can lead to 40% performance degradation in the nMOS device. If the same

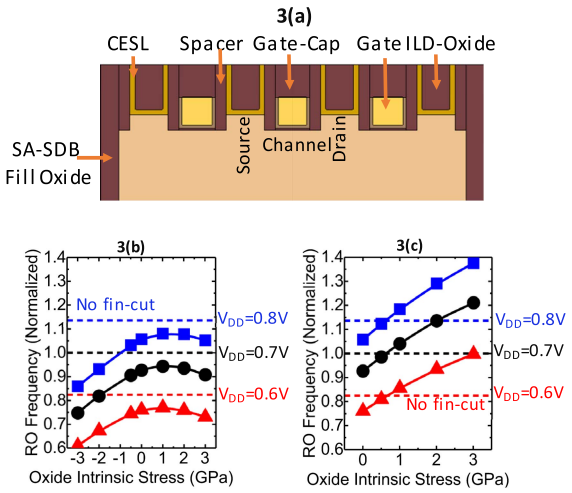


Fig. 3. (a) FinFET cross section through fin showing SA-SDB fin-cut, with a number of devices (NODs) being three between two fin-cuts. (b) RO performance for NOD = 1 when the same stress-type (either compressive or tensile) is used for SA-SDB dielectric fill for both nMOS and pMOS. (c) Ring-oscillator performance when tensile stress is used for nMOS and compressive stress is used for pMOS in SA-SDB dielectric fill.

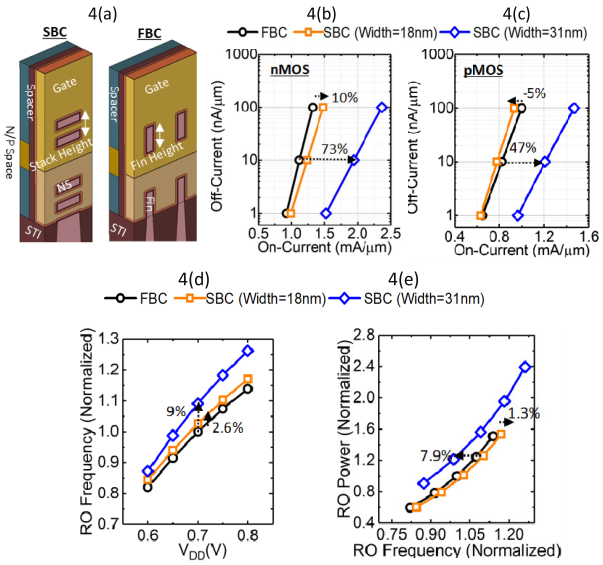


Fig. 4. (a) Structures of different CFET configurations—sheet-based (SBC) and fin-based (FBC). I_{ON}–I_{OFF} characteristics comparison between FBC and SBC (for 18 and 31 nm sheet width) for (b) nMOS and (c) pMOS. Ring-oscillator performance comparison for SBC and FBC CFETs—(d) at constant V_{DD} and (e) at constant power.

stressed dielectric fill is used for both nMOS and pMOS FinFETs, then it was shown that about 1-GPa tensile stress gives the best RO performance for device with SA-SDB fin-cuts [Fig. 3(b)] and the same leakage (achieved by gate work-function tuning), the best being 5% worse than the baseline RO with devices without fin-cuts. On the other hand, if the opposite type of stressed fill is used for nMOS and pMOS, then the RO performance can be completely recovered for ~1 GPa [Fig. 3(c)], stressed dielectric fill, with an opportunity of improving the RO performance beyond the baseline using higher stress values.

This was an example of transistor performance optimization for an FEOL knob—SA-SDB fill oxide stress. First, we studied the impact of this FEOL knob on nMOS and pMOS performance using traditional TCAD, and then using MSCO, we optimized this knob for maximum ring-oscillator performance. Beyond optimizations, MSCO can also be used for technology pathfinding, such as to choose the right transistor architecture. For 2-nm node and beyond, complementary FET (CFET) is a major transistor architecture candidate for logic area scaling continuation. In CFET, the nMOS (or pMOS) device is built on top of pMOS (or nMOS), thus saving the footprint equivalent to one of the devices [19], [20]. The individual nMOS and pMOS devices can be either fin-based or nanosheet-based, thus giving rise to two architectures of CFET—fin-based CFET (FBC) and sheet-based CFET (SBC) [21] [see Fig. 4(a)]. MSCO platform is used for rapid assessment of these CFET architectures by comparing their performances. The SBC device is dominated by (100) surface with higher electron mobility, thereby showing 10% better performance of nMOS for the same effective channel width [see Fig. 4(b)]. On the other hand, the FBC device is dominated by (110) surface with higher hole mobility, thereby showing 5% better pMOS performance for the same effective channel width [see Fig. 4(c)]. However, when compared with the same footprint, the SBC-one shows much better performance for both nMOS and pMOS, indicating its superiority. The SBC CFET also shows higher RO performance at the same V_{DD} [see Fig. 4(d)]. However, at iso-power, the FBC-CFET or SBC-CFET with lower sheet width seems to be better options [see Fig. 4(e)].

Speaking of CFET, it is good to compare it with FinFET to understand its application space. The SBC-CFET configuration is used for this study. Typically, to accommodate both nMOS and pMOS sheets within a reasonable stack height, two sheets per nMOS and pMOS devices are chosen for CFET [see Fig. 5(a)]. CFET sheet width is chosen to be 31 nm, which is similar to the footprint of two fins. With this configuration, the effective channel width of CFET becomes only 144 nm, compared to 230 nm in FinFET with a two-fin device. This leads to a worse I_{ON}–I_{OFF} performance for CFET than FinFET [see Fig. 5(b)] [22]. The other source of circuit performance degradation in CFET is MOL/BEOL parasitics, arising from super-via resistance [see Fig. 5(c)], scaled layouts, and device stacking [see Fig. 5(d)]. All these factors lead to 20% iso-power performance reduction in CFET, CFET drive-strength, and super-via parasitics contributing to 5% each.

IV. MOL/BEOL Technology Optimization Using MSCO Platform

In this section, we will focus on MOL- and BEOL-related technology optimizations and their impact on circuit performance. One of the important structural elements of RO is via-0 and its associated parasitic resistance and capacitances [23]. Fig. 6 shows the via-0 resistance and capacitance trends with its size. Larger via results in lower via-0 resistance but higher via-0 capacitance, whereas there is also a strong dependence on via-0 conductor material and surrounding dielectric material properties. RO simulation shows that there is an optimum via-size, the optimum size being dependent on via-0 material resistivity properties.

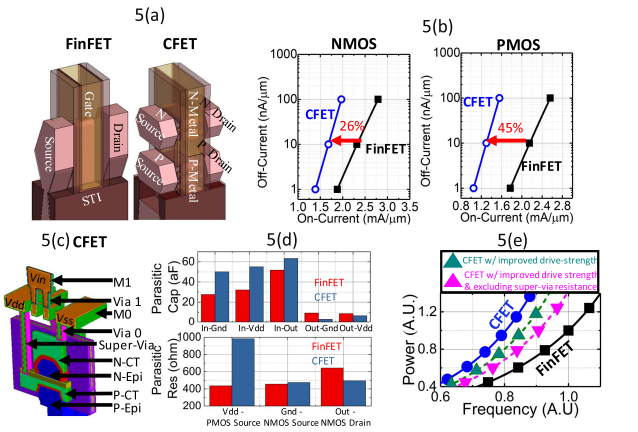


Fig. 5. (a) 3-D structures of FinFET and CFET used in simulation. (b) I_{ON}–I_{OFF} characteristics comparison between FinFET and CFET for nMOS and pMOS. (c) MOL/BEOL 3-D structures of CFET inverter showing the super-via in CFET. (d) MOL/BEOL parasitic resistance and capacitance comparison for CFET and FinFET. (e) RO performance comparison between FinFET and CFET, indicating the performance degradation due to CFET drive-strength and super-via parasitics.

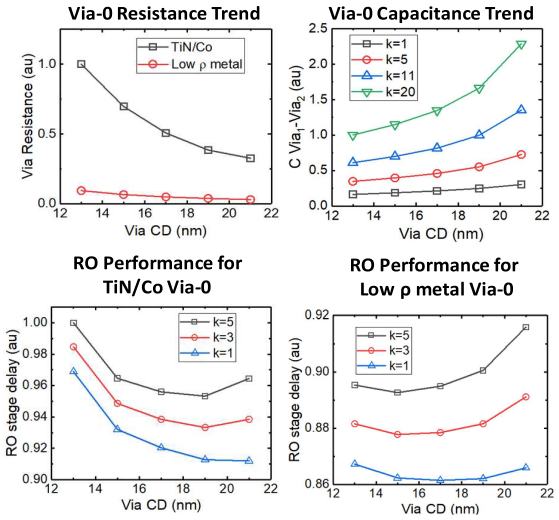
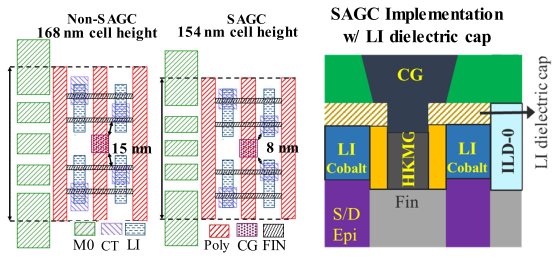


Fig. 6. Impact of via-0 size in a ring oscillator on its resistance, capacitance, and ring-oscillator performance.

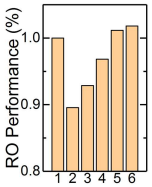
Amongst different MOL/BEOL area scaling technology [24], [25], self-aligned gate contact (SAGC) [26], also known as COAG [5], [27] is of special importance. SAGC helps to bring gate–drain and source–drain contacts closer together, gate contact inside the active region being the extreme case. This allows the M0 pitch scaling and subsequently standard cell area scaling (see Fig. 7). To alleviate the time dependent dielectric breakdown (TDDB) and other reliability issues, a dielectric cap is inserted on top of source/drain metal contact (local interconnect LI) in the SAGC technology, which can be realized with Centura Ultima HDP-CVD, and ALD Olympia deposition technologies developed by Applied Materials. Depending on the material systems used, an LI metal cap might also need to be inserted in between local interconnect and LI dielectric cap using Applied Materials' Endura PVD deposition technology. Furthermore, selective etch processes are required to etch the S/D dielectric cap, gate-cap, and interlayer dielectric (ILD)-0 materials to form the upper level interconnects. For this purpose, Applied Materials' has developed Centris Sym3 equipment with proper optimization of different



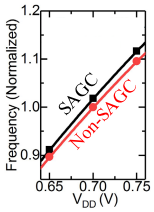
Standard Cell Library Scaling

Parameter	# of inputs			Total cell Area	non-SAGC	208
	1	2	3		SAGC	159
Cell count (%)	27	38	35	Area Benefit	SAGC: 24 %	
Cell area: non-SAGC	1	2	3			
Cell area: SAGC	0.92	1.84	1.83			

Fig. 7. Inverter area scaling using SAGC, achieving 8% area benefit for inverter. To relieve the reliability issues, SAGC uses a dielectric cap on top of S/D local interconnects. Using SAGC, up to 24% of area scaling in standard cell library is possible.



Process options
1. Non-SAGC
2. Un-optimized SAGC
3. SAGC w/ sel-W at MOL
4. (3) + Co at BEOL
5. (4) + AlO_x as LI dielectric cap
6. (5) + sel-W as LI metal cap



SAGC PPA Metric

Metric	Non-SAGC	SAGC Iso-Power	SAGC Iso-Performance
Power	1	1	0.98
Performance	1	1.01	1
Area	1	0.92	0.92

Fig. 8. Use of different advanced MOL and BEOL technologies to recover the circuit performance degradation due to SAGC and area-scaling parasitics. With these additional performance boosters, it is possible to achieve similar power and performance with 8% inverter area scaling.

etch chemistries. This LI dielectric cap and metal cap along with M0 pitch scaling add additional MOL/BEOL parasitic resistance and capacitances to the circuit, which can degrade the circuit performance. The circuit performance degradation depends strongly on S/D contact recess, LI dielectric cap thickness and its dielectric constant, and LI metal cap thickness and its resistivity. Our MSCO platform is deployed to quantify this circuit performance degradation and optimize the different SAGC process parameters to limit this performance degradation [28].

To recover the circuit performance, novel MOL and BEOL technologies, such as selective tungsten and Cobalt M1-V1, are added (see Fig. 8). Thus, with SAGC, along with other novel MOL/BEOL technologies, can enable area scaling while maintaining performance at the desired level.

In addition to MOL/BEOL resistances investigation, the MSCO platform can also be used to evaluate MOL/BEOL parasitic capacitance reduction techniques. One such parasitic capacitance reduction technique is air spacer at MOL/BEOL level. Air spacer has been studied in detail for FEOL application as a replacement of gate sidewall spacer [29]. However, due to involvement of numerous materials and stringent selective etch requirements, incorporation of air spacer at FEOL is quite challenging. On the other hand, logic industry has already incorporated air spacer at M4 and M6 levels for 14-nm

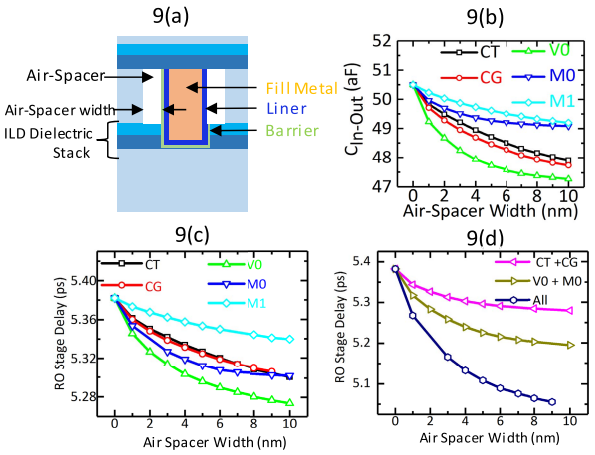


Fig. 9. MSCO modeling of MOL/BEOL air-spacer impact on parasitic capacitance and circuit performance. (a) Simplified air-spacer implementation for modeling study. (b) Capacitance reduction when air spacer is implemented in different MOL/BEOL modules. (c) Ring-oscillator performance improvement with air-spacer implemented separately in MOL/BEOL modules. (d) Ring-oscillator performance improvement when air spacer is implemented in multiple MOL/BEOL modules.

technology node [4]. To further reduce MOL and BEOL parasitics, air spacer can be incorporated at contact-trench (CT), contact-gate (CG), via-0, M0, M1, and different other levels. Using our MSCO flow, we evaluated the impact of introducing air spacer at each location separately [see Fig. 9(a)] [30]. Our modeling results suggest that incorporating air spacer at via-0 can give the maximum capacitance reduction (6%) [see Fig. 9(b)]. If air spacer is incorporated at all MOL/BEOL modules, then this can lead to 18% capacitance reduction. Along the same line, insertion of air spacer at via-0 can lead to a performance increase of 1.9% [see Fig. 9(c)]. Similarly, if air spacer is inserted at all MOL/BEOL modules, then about 6% performance benefit is expected [see Fig. 9(d)].

Speaking of very recent innovations targeting the MOL/BEOL parasitics reduction, selective tungsten deposition technology is worth mentioning. Conventional CVD tungsten (W) fill process needs titanium nitride (TiN) liners, at least 2 nm thick and highly resistive. On top of that, CVD W deposition also needs an ALD-W nucleation seed, which is also generally of higher resistivity. With the via-0 critical dimension (CD) getting scaled in current technologies, the TiN liner and nucleation W occupy a major portion of the via-0, thus increasing its resistance, ultimately leading to degradation of circuit performance. To tackle this issue, a new liner-less W deposition technology has been developed in Applied Materials' Endura Volta deposition equipment. The selective-W deposition process is also a bottom-up fill approach [31] (see Fig. 10), and thus, it also relieves the problem of void or seam at the middle of via-CD for CVD-W deposition. Using the MSCO flow, we demonstrated that the liner-less selective tungsten deposition process enables 75% via-0 resistance reduction and 5% a circuit performance improvement at typical 3-nm technology node dimensions (see Fig. 11).

MSCO enables assessment of material, process, and device innovations at a design or system level. To further evaluate the impact of selective tungsten at a chip level, a popular processor core was used for benchmarking the PPA results against the

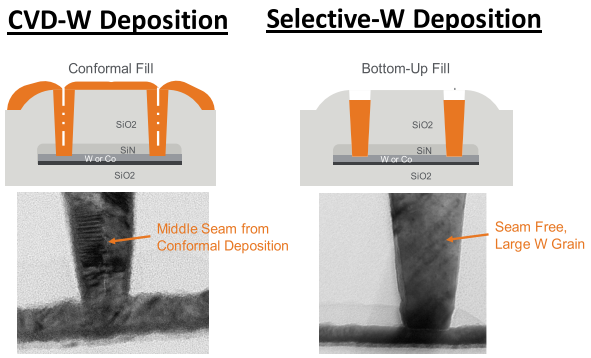


Fig. 10. Comparison of conventional CVD tungsten deposition with seam and bottom-up selective tungsten deposition.

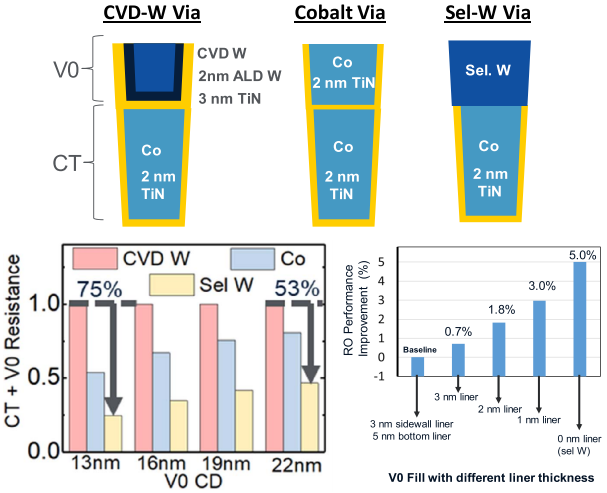


Fig. 11. Via resistance and ring-oscillator performance improvement with liner-less selective-W via-0 deposition.

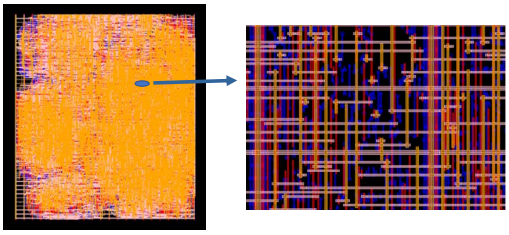


Fig. 12. Design of digital processor using the developed standard cell library and the PDK. A zoomed-in image shows different interconnect layers in the design.

baseline CVD tungsten (see Fig. 12). Typical 7-nm foundry design rules and a standard cell library generated with SLiC consisting of logic transistors and interconnect layers were used [13]. A PDK with a set of design rules required for the experiment was also developed. The table in Fig. 13 shows the comparison of PPA metric at different levels between the baseline (CVD tungsten) and selective tungsten. The iso-V_{DD} performance improvement with selective tungsten at different levels is found out to be very similar (~4%). However, at RO and standard cell library level, the performance benefit comes at a cost of increasing power, which is typically expected. The design constraints and other parameters for synthesis and place and route were constant between the baseline reference and selective tungsten runs. At the design level, the implementation with selective tungsten via-0 is optimized by the electronic design automation (EDA) tools to reduce the overall power consumption by using fewer transistors, standard

PPA Extraction Level	Performance	Power
Ring Oscillator	4.2%	+ 4.2%
Standard Cells	4.4%	+ 1.2%
Digital Processor	4.0%	- 4.6%

Fig. 13. Comparison of PPA metric improvement with selective tungsten via-0 in comparison to conventional CVD tungsten via-0 at different levels of design—ring-oscillator, standard cells, and digital processor design.

cells, and nets (sacrificing some performance along the way) than the implementation with CVD tungsten via-0. With a lower number of transistors, the dynamic power consumption reduces the design with selective tungsten via-0, as there are now fewer transistors charging and discharging in the design. Further investigations to analyze the impact of the selective tungsten at processor design level are currently on the way.

V. Conclusion

In this article, we described the basic building blocks of the MSCO platform for evaluation and co-optimization of various technology knobs. This MSCO platform was deployed on various examples, such as SA-SDB and CFET as FEOL technology and via-size optimization, SAGC, selective tungsten, and air spacer as MOL/BEOL technology. MSCO flow is used extensively to evaluate the impact of these technologies and also to optimize the process parameters for maximum PPAC benefits (power, performance, area, and cost) with considerations to end application. MSCO is critical for co-optimization and acceleration of innovations with the scope of materials to systems.

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