# Design Technology Co-optimization (DTCO) Study on Self-Aligned-Via (SAV) with Lamella DSA for sub-7 nm Technology

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## ABSTRACT

In this paper, we present a design technology co-optimization (DTCO) flow to pattern self-aligned via (SAV) using two masks with grapho-epitaxy of lamella BCP and 193i for sub-7nm design. We show that it is necessary to consider both metal and via layers at the same time in creating design rules with process variations. Due to lamella DSA's own characteristics, it can be easily applied in dense memory or SRAM applications for SAV patterning using traditional single-material metal hard mask. However, to achieve two-mask SAV solution for logic applications, we need to apply alternating hard mask in metal to cut lamella DSA patterns without compromising the technology scaling.

**Keywords:** directed self-assembly (DSA), grapho-epitaxy, lamella BCP, guiding pattern, DSA grouping and decomposition, self-aligned via (SAV), DTCO

## 1. INTRODUCTION

As an alternative technology to extend optical lithography to sub-7nm node, directed self-assembly (DSA) of block copolymers (BCPs) has the potential to reduce mask numbers by grouping the neighboring sub-resolution features together and putting them on the same mask using single material system with 193i. For that reason, there has been substantial progress made in simulating and printing Fin and contact/via layers with DSA grapho-epitaxy for sub-7nm node[1-7].

During the past few years, our research has been focusing on the grapho-epitaxy DSA using *cylinder* BCP with 193i[7-9]. Our data shows that it is critical to pattern optimum guiding patterns faithfully, which usually are in peanut shapes as shown in Figure 1, to avoid phase transitions, and eventually achieve none-$L_0$ pitches patterning.

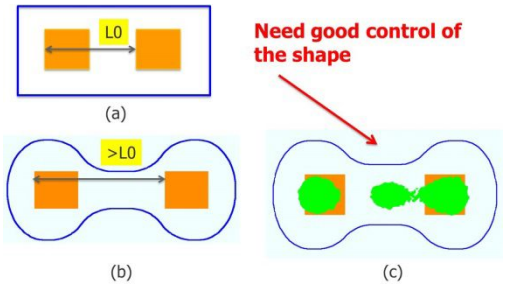


Figure 1 Grapho-epitaxy DSA using *cylinder* BCP (a) guiding patterns for via pitch in $L_0$ (b) guiding pattern for via pitch > $L_0$ (c) bad guiding pattern yields phase transition for in none-$L_0$ via pitch.

In this paper, we will focus on the self-aligned contact/via (SAV) patterning with grapho-epitaxy DSA using *Lamella* BCP. Lamella shows better process window than cylinder BCP according to IBM's experimental results as shown in

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CCC code: 0277-786X/17/$18 · doi: 10.1117/12.2258056

Figure 2. In addition, the guiding pattern shape for lamella DSA theoretically is simple, mostly rectangles with optimum width being integer times $L_0$. Figure 3 shows the Monte Carlo (MC) simulation results on various guiding patterns by changing guiding pattern width (vertically) and length (horizontally). Different numbers of rows of DSA line patterns are formed with different guiding pattern sizes. Phase transitions/defects can happen with none-optimized guiding pattern.

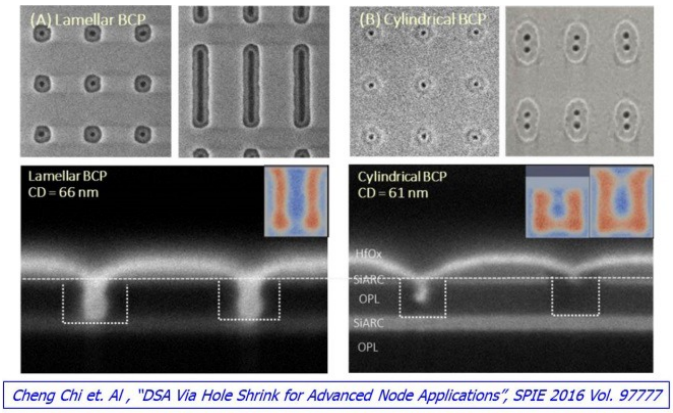



Figure 2 IBM's experimental results from Cheng Chi et. Al[4].

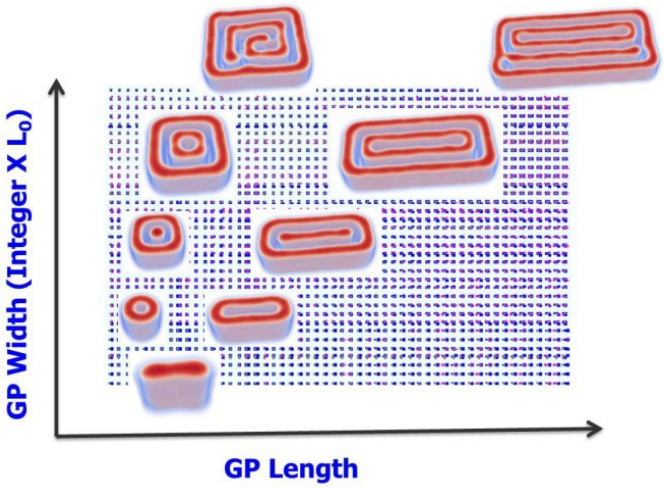



Figure 3 Monte Carlo (MC) simulation results on various guiding patterns in different widths and lengths.

Vias connect two metal layers e.g. via1 connects M1 in bottom and M2 in upper layers. The traditional single-material-hard-mask SAV process is realized by taking advantage of the trench first metal hard mask scheme for dual-damascene structures, and it has been widely established and adopted in Fabs to overcome the tight process control on overlay and CDU at smaller nodes. In general, SAV aligns to the upper metal layer. Figure 4 demonstrates the four major steps to realize the traditional single-material-hard-mask SAV: start with the metal patterning on hard mask, followed by via patterning, then self-aligned via (to metal) etches, and finally metal etch.

As shown in Figure 5 (a), the SAV process allows an enlarged via target for lithography in that the to-be-aligned via edges can be pushed outward on target without being concerned of electrically touching neighboring metals. This actually enables better process window for lithography, and results in lower resistance thus better electrical performance due to bigger vias than the none-SAV process. However, since the space between the metal-top of the none-related metal (M1) to via-bottom can be small as shown in Figure 5 (c), we need to optimize the CDU along the none-aligned orientation in Figure 5 (b) to mitigate the time dependent dielectric breakdown (TDDB) issues.

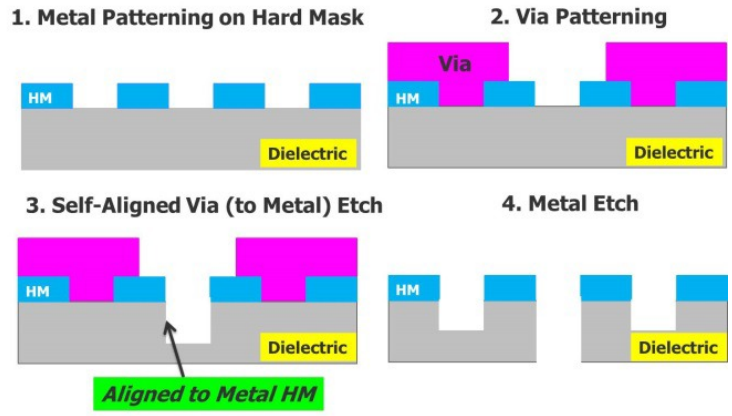



Figure 4 The four major steps to realize traditional single-material-hard-mask SAV.

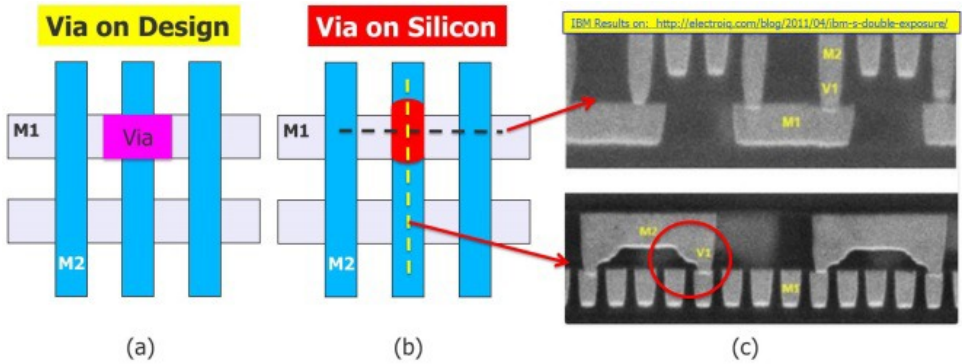



Figure 5 (a) The top-down view of via in rectangle shape for lithography; the aligned-to-metal layer (M2) is in vertical (blue) (b) the SAV on silicon with left/right edges aligned to M2 edges after etching (c) the IBM cross-section SEM images of SAV with metals (M1&M2) along the none-aligned orientation (http://electroiq.com/blog/2011/04/ibm-s-double-exposure). The M1-top can be very close to V1-bottom and cause TDDB issues.

In this paper, we provide a detailed design technology co-optimization (DTCO) study on realizing SAV with lamella DSA. In Section 2, we investigate the design and grouping constructs i.e. 1D and 2D with the gridded-design architecture. Since this technology involves via and metal layers simultaneously, in Section 3, we create design rules for metal layer and DSA templates by considering process variations. We use Template Error Enhancement Factor (TEEF) analysis to show that lamella DSA can reduce half of the CDU from the guiding pattern at proper aspect ratios. In Section 4, we demonstrate a 2-mask solution with DSA for via-design in SRAM applications at 5nm. We will show that to enable logic with two masks it needs help from alternating hard mask on the metal layer.

## 2. DESIGN AND GROUPING CONSTRUCTS FOR SAV USING LAMELLA DSA

As we know, DSA with cylinder BCP has strict requirements on the shape control to achieve none-$L_0$-pitch via patterning, about which SAV cannot help either because DSA with cylinder BCP generates discrete cylinders. However, lamella DSA can leverage the SAV capability to realize multiple-pitch patterning easily using bar-shape templates as long as the aligned-to-metal (upper metal e.g. M2) layer allows.

In the SAV process, the metal layer serves as the natural cut layer for lamella DSA patterns in forming vias. The metal layer is mostly unidirectional for sub-10nm designs because bi-directional metal is not compatible with higher-order frequency multiplication e.g. self-align quadruple patterning (SAQP)[10]. Lamella DSA usually generates uniform lines/spaces in pitch of $L_0$, which usually match to the underlying metal pitch e.g. M1 pitch for V1. To realize design targets, it requires concurrent considerations on designs of at least two layers together i.e. aligned-to-metal (M2) and via (V1) layers by feeding information on via-grouping. Figure 6 shows a design technology co-optimization (DTCO) flow for both via and aligned-to-metal design using lamella DSA. We need to make sure that the final design is SAV lamella-

grouping friendly, and is optimized in such a way that maximum number of vias can be grouped with the aligned-to-metal design, which is an intrinsic cut mask layer.

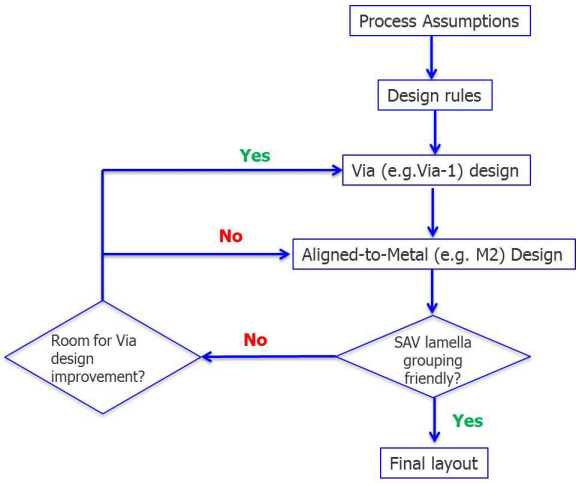



Figure 6 The DTCO flow for SAV with lamella DSA

In the following, we demonstrate some metal-via-design constructs with different grouping using lamella DSA for SAV.

### 2.1 One-Dimension Grouping

Figure 7 assumes one-dimension grouping. The left two columns are examples for grouping vias in a single row, and the right two columns for grouping vias in two rows. Theoretically, we can group vias in more than two rows, and realize via designs on multiple rows when combined with proper aligned-to-metal layer.

When the guiding pattern width is about $L_0$, we expect one bar formation (in solid pink) with lamella DSA. Depending on aligned-to-metal designs (in blue), e.g. M2 design for via1 layer, dense or multiple-pitch SAV (in red) can be realized. The pitch tuning comes from the align-to-metal layer, and it behaves as the AND Boolean operation between via and aligned-to-metal layers, which is that anything from DSA formation landing on the aligned-to-metal layer will be kept, and the rest will be cut.

Similarly, when the guiding pattern width is about $2L_0$, a DSA ring is formed as shown in Figure 6, and the pitch between two lines along the width orientation (here it is vertical) is $L_0$. We rely on the aligned-to-metal layer to cut the ringside. With different aligned-to-metal designs, it can form dense SAV in two rows as needed in many memory applications, or staggered SAVs that appear in many logic applications.

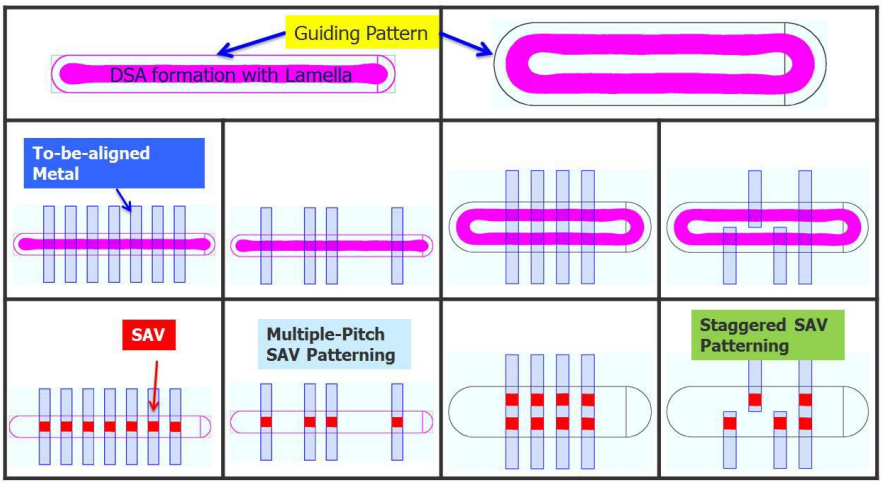



Figure 7 One-dimension grouping with lamella DSA for SAV. Left two columns are for vias grouping in single row; right two columns are for vias grouping in two rows.

### 2.2 Two-Dimension Grouping

In general, lamella DSA favors one-dimension grouping and thus one-dimension guiding pattern. If there was no corner rounding on the 2D guiding patterns, the lamella DSA formation i.e. in solid pink could be organized, and follow the template's guidance as shown in the left column of Figure 7. After metal cut for SAV, it may realize the design intentions – target in green, and SAV in red as shown on the bottom of left column.

However, it is inevitable to have corner rounding in patterning 2D guiding patterns such as T-shape or L-shape. The right columns of Figure 8 clearly demonstrates that it would cause random phase transitions, and ruin the design targets completely with vias being missing in those corner-rounding locations. Therefore, 2D grouping is forbidden with lamella DSA.

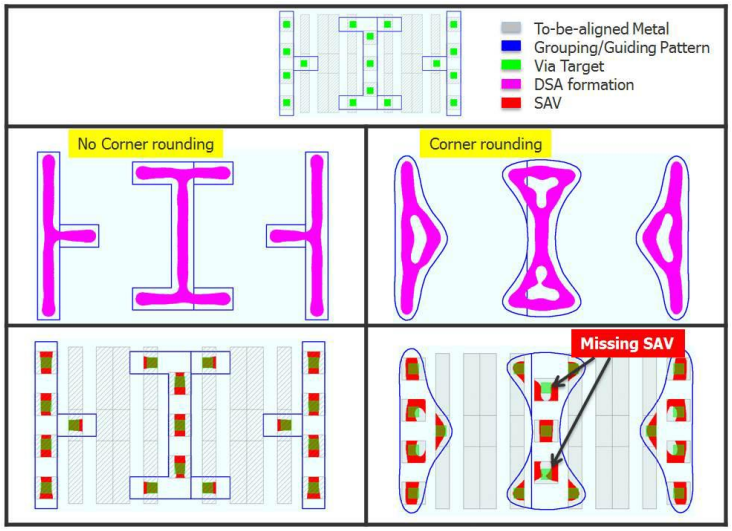



Figure 8 Two-dimension grouping for SAV is forbidden.

## 3. DESIGN RULES STUDY

### 3.1 Design Rule Analysis

Since the SAV process involves two layers simultaneously: the aligned-to-metal layer and the via layer, it is necessary to consider the process interactions between these two layers in setting up design rules and lamella DSA template dimensions, for which Figure 9 is an example. Assume that due to process variations such as overlay $\sigma_{OVL}$ and templates' CDU, the real guiding pattern (in red) not only has the center moved away from the target (in blue) but also has the CD increased. After the lamella DSA formation – the bar (in red) formed in Figure 9 (b), the cut layer i.e. the aligned-to-metal layer (in blue) will give the SAV (in red hash) shown in Figure 9 (c). We can see that, in addition to the changes from the target in terms of via CD and center, the process variations result in SAV formed in unwanted locations, and violate the design intention. Therefore, we need to set up the corresponding design rules to avoid this from happening in the first place.

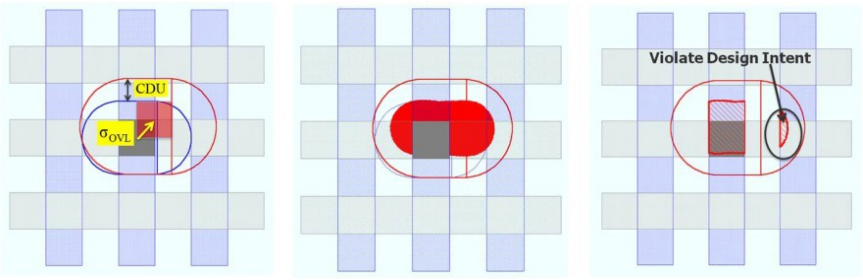
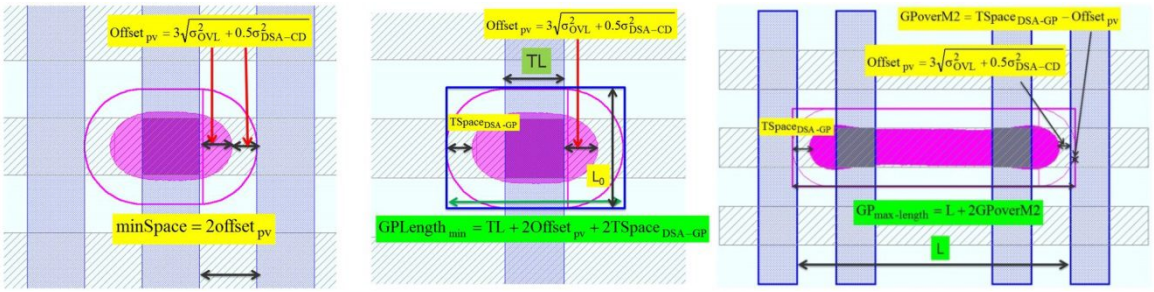



Figure 9 Process variations on templates patterning e.g. overlay and CDU could cause SAV formed on unwanted locations and violate design intentions.

Figure 10 shows an example on the design rule set-up when the grouping is on single via or vias from one single row. As shown in Figure 10 (a), in order to enable lamella DSA for the SAV process, given the process overlay $\sigma_{OVL}$ and the DSA pattern's CDU of $\sigma_{DSA\_CD}$, the min. space of the aligned-to-metal should be $2\text{offset}_{pv}$ with single-row-via grouping, where $\text{offset}_{pv}$ is the space needed to accommodate the process variations, and is defined as $\text{offset}_{pv} = 3\sqrt{\sigma_{OVL}^2 + 0.5\sigma_{DSA-CD}^2}$. Usually for a specific lamella BCP material with natural pitch $L_0$, the tip-to-tip space between the guiding pattern and the formed DSA pattern, $\text{TSpace}_{DSA\text{-}GP}$, is about $L_0/4$. For a horizontal guiding pattern with no neighboring aligned-to-metal features, assume the distance between the left-most edge to the right-most edge on the via layer is TL, then the minimum guiding pattern length is $\text{GPLength}_{min} = \text{TL} + 2\text{Offset}_{pv} + 2\text{TSpace}_{DSA-GP}$ as shown in Figure 10(b). However, if there are neighboring aligned-to-metal features where there are no vias landing on them, then the maximum guiding pattern length is the following: $\text{GPLength}_{max} = \text{L} + 2\text{GPOverM2}$, where L is the space between the two metal features having no vias, and GPoverM2 is the maximum length that the guiding pattern can run over the metal without causing unwanted SAV formed. As shown in Figure 10 (c), $\text{GPOverM2} = \text{TSpace}_{DSA\text{-}GP} - \text{offset}_{pv}$ which can be positive or negative. When it is negative, the template edge should fall into the metal space region; but if it is positive, the template edge can land on the neighboring metal feature.




(a) (b) (c)

Figure 10 Design rule analysis when the grouping is on single via or vias from single row (a) min. space of the aligned-to-metal layer (e.g. M2) (b) the min. guiding pattern length (c) the maximum guiding pattern length when there are neighboring aligned-to-metal features having no vias.

Similarly, we can do the design rule analysis for groupings of vias in two or more rows. The template width for 2-row-via grouping should be about $2L_0$, but the length should be set in a way to avoid the situation demonstrated in Figure 11, where the vias on the top row could connect to the vias below – causing electrical shorts if it were not the design intention.

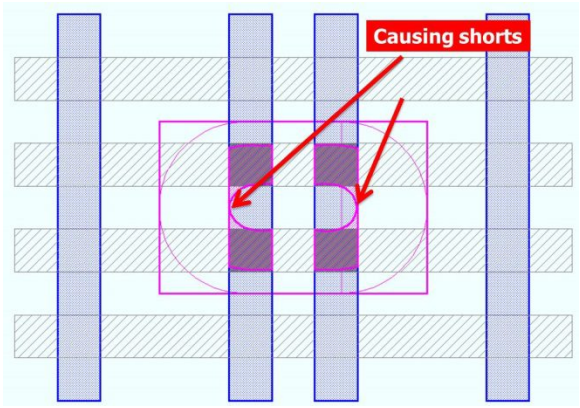
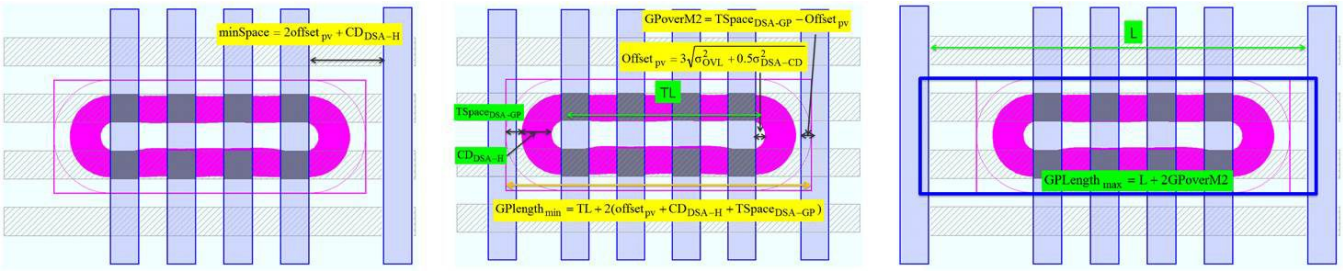



Figure 11 The template size should be designed properly for multiple-row-via grouping to avoid unwanted SAV merging.

As implemented for single-row-via grouping, Figure 12 (a) shows that the minimum metal space should be $2\text{offset}_{pv} + \text{CD}_{DSA-H}$ for grouping of 2-row vias, where $\text{CD}_{DSA\text{-}H}$ is the end width of the DSA ring-pattern. Figure 12 (b) and (c) demonstrates the minimum and maximum guiding pattern length with or without neighboring metal features.




(a) (b) (c)

Figure 12 Design rule analysis when the grouping is on vias in two rows (a) min. space of the aligned-to-metal layer (e.g. M2) (b) the min. guiding pattern length (c) the maximum guiding pattern length with neighboring aligned-to-metal features having no vias.

After implementing the analysis for various groupings, Figure 13 summarizes the basic design rules for grouping of vias from single row up to four rows in terms of the minimum metal space and guiding pattern length.

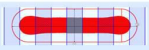
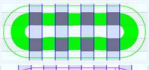
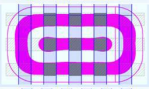
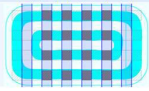
| Guiding Pattern with DSA Formation | Min. Space for Metal Layer | Min. SAV Guiding Pattern Length |
|---|---|---|
|  | $2\text{offset}_{pv}$ | $TL + 2(\text{offset}_{pv} + \text{TSpace}_{DSA-GP})$ |
|  | $2\text{offset}_{pv} + CD_{DSA-H}$ | $TL + 2(\text{offset}_{pv} + CD_{DSA-H} + \text{TSpace}_{DSA-GP})$ |
|  | $2\text{offset}_{pv} + L_0$ | $TL + 2(\text{offset}_{pv} + L_0 + \text{TSpace}_{DSA-GP})$ |
|  | $2\text{offset}_{pv} + L_0 + CD_{DSA-H}$ | $TL + 2(\text{offset}_{pv} + L_0 + CD_{DSA-H} + \text{TSpace}_{DSA-GP})$ |

Figure 13 Design rules' formulas for grouping of vias from single row to four rows.

To put things into perspective, if we use lamella BCP with $L_0$ of 32nm, and assume the process assumptions listed in Table I, then for Nx1 via arrays (where N means number of rows, and "1" means one via in each row), the min. metal space and guiding pattern length are summarized in Figure 14. For example, the min. metal space needs to be at least 30 nm if we group vias in two rows; and the minimum guiding pattern length has to be 84 nm for 2x1 grouping. Obviously, for sub-7nm node where the metal pitch is below 50nm, we can only allow single row grouping with the single-material hard mask on metal for SAV.

Table I: Process Assumptions

| L0 | $CD_{DSA-H}$ | $TSpace_{DSA-GP}$ | $Offset_{pv}$ |
|---|---|---|---|
| 32 nm | 16 nm | 8 nm | 7nm |

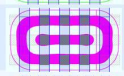
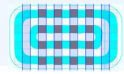
| Guiding Pattern with DSA Formation | Via Array | Min. Space for Metal Layer | Min. SAV GPLength |
|---|---|---|---|
|  | 1X1 | 14 nm | 52 nm |
|   | 2X1 | 30 nm | 84 nm |
|  | 3X1 | 46 nm | 116 nm |
|  | 4X1 | 62nm | 134 nm |

Figure 14 The design rules correspond to the process assumptions in Table I.

### 3.2 Template Error Enhancement Factor (TEEF) Analysis

In the previous papers[8-9], we introduced the TEEF notation to describe the sensitivity of DSA printing infidelity to the template printing infidelity under no phase transitions. Here, we use a simplified TEEF definition for lamella DSA guiding pattern selection. we do a constant size-up or size-down around the nominal template contour, and then evaluate how the DSA CD change with respect to the constant sizing s. For those templates yielding no phase transitions, we formulate $\text{TEEF} = \frac{\Delta \text{CD}_{\text{DSA}}}{\text{s}}$. Figure 15 shows that both the lamella-DSA pattern edge displacements from target (in solid red; left y-axis) and TEEF (in dashed blue; right y-axis) vary with the guiding pattern aspect ratio for templates of 1-row-via grouping. The aspect ratio is better to be above two and half for multi-via grouping to achieve small edge displacement (< 0.5 nm) and TEEF (~0.5). In general, the lamella-DSA-formed pattern will have half of the CDU on the templates – the powerful rectification capability of DSA.

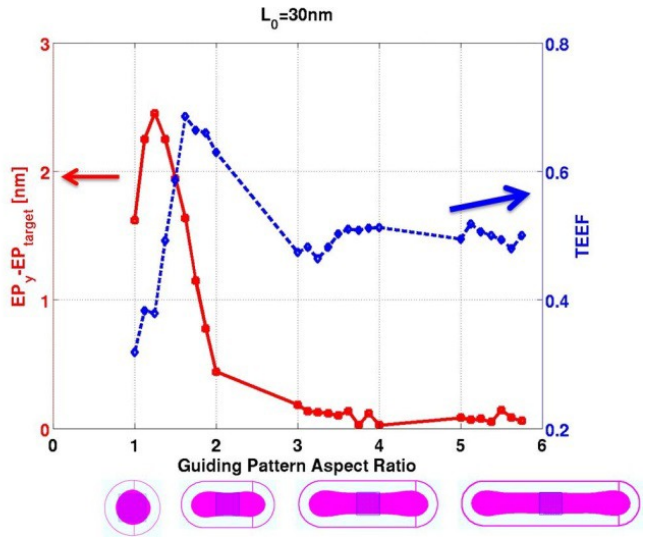



Figure 15 single-row-via grouping: the edge displacement form the target (left y-axis) and TEEF (right y-axis) Vs. guiding pattern aspect ratio

## 4. LAMELLA DSA APPLICATIONS FOR 5NM VIA DESIGN

In this section, we will show lamella DSA applications in both memory and logic designs at 5nm node.

### 4.1 SRAM

Lamella DSA for SAV is very friendly to memory applications where via-design is generally dense but regular, easy to use 1D grouping. Figure 16 shows the grouping and 2-mask decomposition for a 5nm SRAM design. The left column demonstrates the 1D grouping results (in green) for an A2X2 cell. When it is extended to a bigger cell e.g. A16X16, the grouping results have some crossings as shown in the middle column. However, we can split these crossings onto two masks according to their orientations i.e. vertical or horizontal alternatively as shown in the right column in Figure 16, which results in no 2D guiding patterns. These two masks (in pink and sky blue) actually have the same guiding pattern layout.

After implementing proper OPC, we obtain the imaging contours at various process conditions shown in Figure 17 (a), and then feed them into MC simulations to check the lamella DSA formation. Figure 17 (b) shows the lamella DSA bars corresponding to inner and outer imaging contours: pink for outer, and blue for inner.

Combined with the aligned-to-metal layer, Figure 18 shows the generated SAV (pink or blue) against target (in solid black) when guiding patterns are inner (blue) or outer (pink) imaging contours. It can be seen that all the centers of SAVs are aligned to the targets' with edges defined either by the aligned-to-metal layer or by the formed lamella DSA patterns.

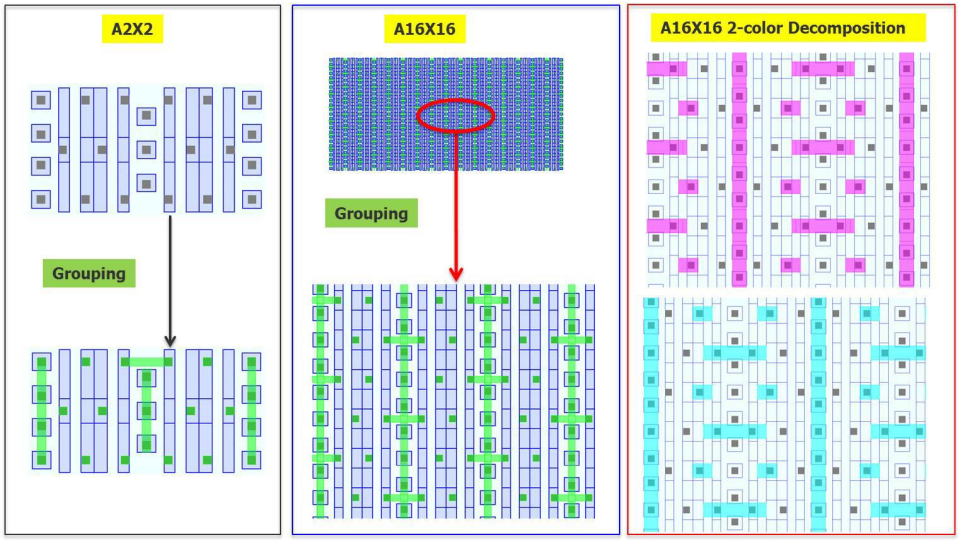
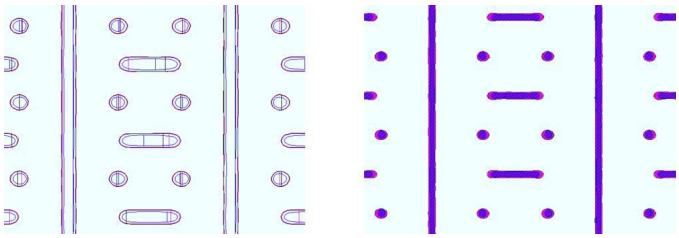
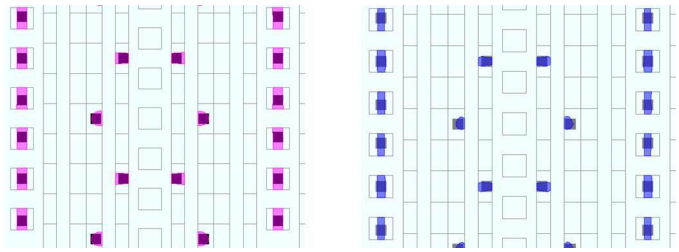



Figure 16. SRAM: Lamella DSA grouping and decomposition.



(a) (b)

Figure 17 (a) Imaging contours for one of the decomposed mask (sky blue) (b) MC simulation results corresponding to the inner (blue) and outer (pink) imaging contours as the guiding patterns.



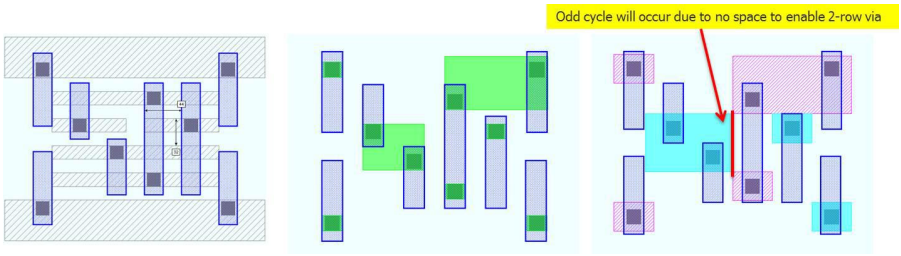
(a) (b)

Figure 18 SAV formations with the aligned-to-metal (in empty dark) against target (in sold dark) (a) use outer imaging contour as the guiding pattern (b) use inner imaging contour as the guiding pattern

### 4.2 Logic

The via-design in logic applications is typically random, and splitting them into two masks could be very challenging for sub-7nm node, even with the grouping capability from lamella DSA. Figure 19 (a) shows a NAND standard cell with min. pitch in the aligned-to-metal (in vertical direction and in blue color) layer being 44nm and the min. pitch of the metal in bottom being 32nm. As shown in Figure 19 (b), we need to group vias from at least two rows (in green) to reduce the mask number from four to two, which is corresponding to patterns in pink and sky blue shown in Figure 19 (c). However, as the design rules listed in Figure 14, we need at least 30nm space in the align-to-metal layer to enable the 2-row via lamella DSA patterning given the BCP material with $L_0$ of 32nm (matched to the metal pitch in bottom), while the space here is only 22nm. In addition, we cannot move the right edge (in red) of the blue-color guiding pattern

in Figure 19 (c) further right to form a 2D L-shape pattern with its neighbor because the corner rounding in imaging would ruin the lamella DSA as discussed in section II.




(a) (b) (c)

Figure 19 (a) NAND standard cell design: aligned-to-metal layer is in vertical orientation with pitch of 44 nm; the metal pitch in bottom is 32nm (b) attempted via grouping (c) guiding pattern decomposition: not enough space for grouping of two-row-via

To enable the 2-mask solution for logic, we need the alternating material self-aligned patterning process proposed by Han et al[11]. It takes the advantage of the spacer deposition in self-aligned multiple patterning such as quadruple/octuplet (SAQP/SAOP) or triple/sextuple (SATP/SASP) for the metal layer, and generate hard mask layers with alternating etching selectivity. As shown in Figure 20, the etching selectivity is alternating as A-B-A-B… or A-B-B-A-B-B… For example, A-type line will not be etched when etch on B-type, and vice versa.

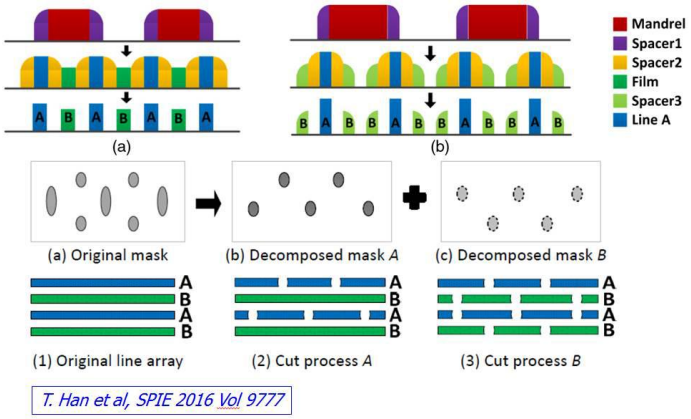
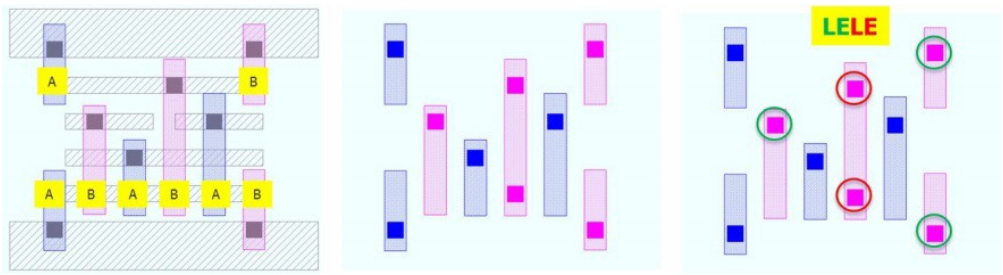



Figure 20 Alternating material self-aligned patterning process by Han et. al.[11].

Applying this technology to the aligned-to-metal layer and implementing the SAV process, we see that the aligned-to-metal layer generated with alternating A-B-A-B type of etching selectivity automatically gives two colors to the via-layer as shown in Figure 21 (a) and (b) – any vias landing on A-type metal will be in a separate etching step from vias on B-type metal. However, we also see from Figure 21 (c) that, with the traditional multiple patterning technique e.g. LELE, it still needs 2-color to decompose the B-type via (pink) in addition to A-type via (blue) single patterning, so it needs at least 3 masks.




(a) (b) (c)

Figure 21 (a) Applying alternating material self-aligned patterning process to the aligned-to-metal layer to generate A-B-A-B type of hard masks with alternating etching selectivity (b) vias are pre-assigned to two colors: type A (blue) and type B (pink) (c) need two masks to pattern vias assigned to type B

Lamella DSA can help to reduce the mask number further for this situation. As we mentioned earlier, due to different etching selectivity for A and B type of metal, now the edges of the guiding pattern for B-type via (in pink) can run cross the A-type metal (vice versa) without causing any electrical concerns,. Therefore, there is more space to enable multiple-row via grouping and use longer guiding pattern. Figure 22 demonstrates a possible 2-mask solution for the design in Figure 19.

In logic applications, there are often two vias on the same I/O net, which will always be pre-assigned to the same color. We need to make sure them to be in the single exposure pitch as labeled in Figure 22 (a). Considering the characteristics associated with this specific process, we can change the design architectures correspondingly. For example, for the design node associated with the design of Figure 19, we can set up the design rules that the top metal pitch to be 40 nm instead of 44nm, and the bottom-metal pitch 36nm instead of 32nm. Thus, we may meet the decomposition requirements without degrading the area scaling.

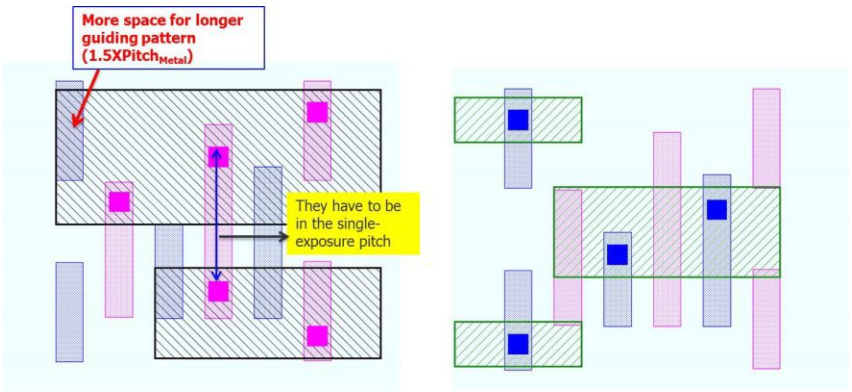



Figure 22 A two-mask solution for design in Figure 19 using alternating material self-aligned patterning process for the aligned-to-metal layer

## 5. CONCLUSION

Based on the fact that the metal hard mask layer acts as an intrinsic cut layer for the patterns generated from grapho-epitaxy with lamella BCP in the self-aligned via (SAV) process, we present a design technology co-optimization (DTCO) flow to pattern vias using two masks for sub-7nm design with 193i.

As seen from the MC simulation results, the lamella DSA for SAV does not support 2D grouping. However, it is friendly to long range grouping, and can realize multiple-pitch via patterning in one direction given proper aligned-to-metal designs. In addition, it supports via designs with different pitches in x and y directions. We see that, due to lamella DSA's own characteristics, it can be easily applied in dense memory or SRAM applications.

Since the SAV process involves two layers simultaneously: the aligned-to-metal layer and the via layer, we take into account of the process interactions between these two layers, and consider the process variations to set up design rules of the metal/via layers including the lamella DSA template dimensions. To meet the sub-7nm design rules, we can only allow one-row-via grouping for lamella DSA with the traditional SAV process assuming single-material metal hard mask.

Finally, we showed promises to achieve two-mask SAV solution for logic application by using alternating hard mask in metal to cut the lamella DSA patterns without compromising the technology scaling.

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## REFERENCES


[1] Y. Seino, H. Kato, H. Yonemitsu, H. Sato, M. Kanno, K. Kobayashi, et al., "Application of Directed Self‐Assembly Lithography to Semiconductor Device Manufacturing Process," Electronics and Communications in Japan, 98, 59-64 (2015).

[2] C.-C. Liu, F. L. Lie, V. Rastogi, E. Franke, N. Mohanty, R. Farrell, et al., "Fin formation using graphoepitaxy DSA for FinFET device fabrication," Proc. SPIE, 9423,94230S-1 (2015)

[3] C. Bencher, H. Yi, J. Zhou, M. Cai, J. Smith, L. Miao, et al., "Directed self-assembly defectivity assessment. Part II," Proc. SPIE, p. 8323, 83230N (2012)

[4] Cheng Chi, Chi-Chun Liu, Luciana Meli, Kristin Schmidt, Yongan Xu, Anuja DeSilva, Martha Sanchez, Richard Farrell, Hongyun Cottle, Daiji Kawamura, Lovejeet Singh, Tsuyoshi Furukaw, Kafai Lai, Jed W. Pitera, Daniel Sanders, David Hetzer, Andrew Metz, Nelson Felix, John Arnold, Matthew Colburn, "DSA Via Hole Shrink for Advanced Node Applications," Proc. SPIE, 9777,97770L (2016)

[5] R. Gronheid, P. A. R. Delgadillo, T. R. Younkin, I. Pollentier, M. Somervell, J. S. Hooge, et al., "Frequency multiplication of lamellar phase block copolymers with grapho-epitaxy directed self-assembly sensitivity to prepattern," Journal of Micro-Nanolithography Mems and Moems, 11, 031303 (2012)

[6] Kafai Lai, Chi-Chun Liu, Hsinyu Tsai, Yongan Xu, Cheng Chi, Ananthan Raghunathan, Parul Dhagat, Lin Hu, Oseo Park, Sunggon Jung, Wooyong Cho, Jaime Morillo, Jed Pitera, Kristin Schmidt, Mike Guillorn, Markus Brink, Daniel Sanders, Nelson Felix, Todd Bailey, and Matthew Colburna, " Design technology co-optimization assessment for directed self-assembly-based lithography: design for directed self-assembly or directed self-assembly for design," Journal of Micro-Nanolithography Mems and Moems 16(1), 013502 (2017)

[7] Y. Ma, J. A. Torres, G. Fenger, Y Granik, J. Ryckaert, G. Vanderberghe, J. Bekaert, James Word, "Challenges and opportunities in applying grapho-epitaxy DSA lithography to metal cut and contact/via applications," proc. SPIE 9231, 92310T (2014)

[8] Y. Ma; J. Lei, J. Andres Torres, L. Hong, J. Word, G. Fenger, A. Tritchkov, G. Lippincott; R. Gupta, N. Lafferty, Y. He, J. Bekaert, G. Vanderberghe, "Directed self-assembly graphoepitaxy template generation with immersion lithography," Journal of Micro-Nanolithography Mems and Moems, 14, 031216 (2015)

[9] Yuansheng Ma, Yan Wang, James Word, Junjiang Lei, Joydeep Mitra, Juan Andres Torres, Le Hong, Germain Fenger, Daman Khaira, Moshe Preil, Jongwook Kye, and Harry J. Levinson, " Directed self-assembly compliant flow with immersion lithography: from material to design and patterning," Journal of Micro-Nanolithography Mems and Moems, 15, 031610 (2016)

[10] L. Liebmann, A. Chu, and P. Gutwin, "The daunting complexity of scaling to 7nm without EUV: Pushing DTCO to the extreme," Proc. SPIE, 9427, 942702 (2015)

[11] Ting Han, Hongyi Liu and Yijian Chen, "A Paradigm Shift in Patterning Foundation from Frequency Multiplication to Edge-Placement Accuracy – A Novel Processing Solution by Selective Etching and Alternating-Material Self Aligned Multiple Patterning", Proc. SPIE, 9777, 977718 (2016)