A DTCO approach on DRAM bit line capacitance and sensing margin improvement

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Abstract

A Design Technology Co-Optimization (DTCO) study was performed on DRAM array bit line capacitance (C_BL) for optimum array sensing margin. C_BL related structural parameters involving bit line width, bit line spacer width, spacer film stacks, and cell contact width were explored. C_BL, bit line resistance (R_BL) and cell contact resistance (R_CC) were calculated correspondingly, and reflects onto the relative changes of sensing margin (ΔV_{sm}) and writing recovery time (Δt_{WR}). The tradeoff between ΔV_{sm} and Δt_{WR} were revealed. Considering the process feasibility, optimum C_BL are proposed, sensing margin gain and t_{WR} loss are evaluated.

1. Introduction

DRAM keeps shrinking for higher memory density and speed. C_BL plays a key role of achieving sensing margin in the scaling. However, the improvement of C_BL is limited by the increase of CC, BL resistance due to the very limited space constrained by BL pitch size. The resistance increase will further cause the degradation of t_{WR}. Thus the optimization of C_BL requires us to consider both process feasibility and timing impact. The method of DTCO gains popularity since technology scaling forces a structured development with design for higher yield and performance [1]. DRAM core, as an analogue system, can better take the advantage of the method. The maturity of process simulation tools also allows us to accurately correlate process parameters to electrical parameters. In this work, a DTCO study on BL capacitance was done for the first time.

2. Method

DRAM array structure model was built based on real process flow and layout using Coventor Semmulator. Within the same software, Capacitances were calculated giving the dielectric constants, while resistances calculated giving the conductor resistivity. BL, made of tungsten and poly silicon stack, resistance is dominated by tungsten. However, tungsten resistivity increases exponentially when getting less than the critical size ~20 nm. A tungsten film resistivity to thickness relationship was fed into Semmulator for an accurate calibration. Locating within the complicated array 3D structures BL capacitance consists of the capacitance of BL to word line, substrate, BL, cell contact (CC), among which BL to CC (C_BLCC) capacitance dominates. Either increasing BL spacer thickness or reducing dielectric constant can reduce C_BLCC (Figure 1). With fixed BL pitch, BL spacer expansion will make smaller CC area or BL width, resulting in the resistance increase of cell writing path. ΔV_{sm} and Δt_{WR} were calculated for DTCO comparison. Sensing margin relates to charge sharing of cell and BL, SA mismatch, circuit noise etc. Disregarding the circuit part, we only consider the charge sharing. ΔV_{sm} can be simply expressed as

$$\Delta V_{SM} = (V_{ary} - V_{BLP}) * C_s / (C_{BL} + C_s) \quad (1)$$

, where V_{ary} is cell fully charged voltage, V_{BLP} the BL pre-charge voltage, and Cs the cell capacitance. t_{WR} is the time needed to charge the cell up to 90% of V_{ary}. Considering charging high, the cell transistor always works in linear region, the cell transistor can be approximated with a simple resistor. t_{WR} can be expressed as

$$t_{WR} = C_s R * \ln 10 \quad (2)$$

, where R is the sum of cell transistor channel resistance (R_{on}), cell contact resistance (R_CC), BL contact resistance (R_BLC), and BL resistance (R_BL). In this work R_{on} and R_BLC are kept to reference value, R_CC is assumed to change linearly with CC area, R_BL change exponentially with BL width as discussed above.

Different BL spacer constitutes were explored, including pure silicon nitride, nitride/oxide/nitride (NON) and nitride/airgap/nitride (NAN), each with lower dielectric constant. While BL width was fixed the tradeoff between BL spacer width and CC area was investigated, the corresponding ΔV_{sm} and Δt_{WR} were compared. Similarly, while CC is fixed tradeoff between BL spacer width and BL width was investigated. As BL vertical etching is normally tapered, the etching angle also influence the BL spacer width. Different BL etching angles were investigated.

3. Results

The cross section of BL spacer region in DRAM 3D

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model is shown in Figure 1. A large overlap exists between BL and CC. BL spacer showing in Figure 1 consists of NON multiple layers. Cell landing onto active area forms a poly to silicon interface. BL contact (BLC) also forms a poly to silicon interface. Both interface show high contact resistance. BL etching angle is also shown in the figure.

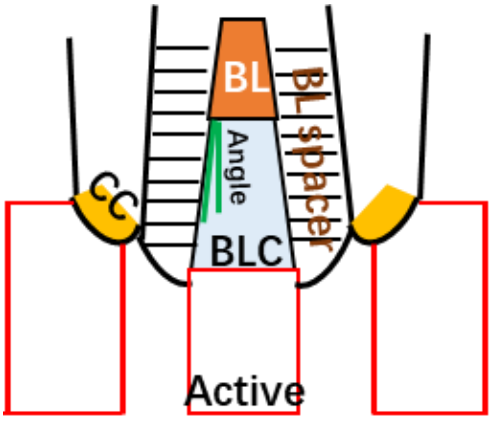

Figure 1. Cross section of BL in DRAM array schematical view.

3.1 C_BL simulation and silicon validation

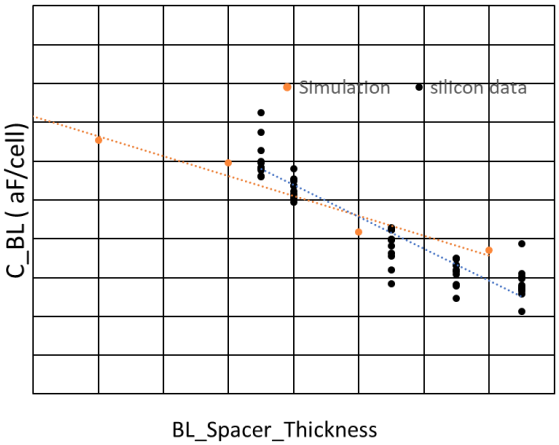

Figure 2. C_BL simulation (orange dots) and silicon (black dots) values with different BL spacer thickness and pure nitride.

C_BL simulation was compared with silicon data for validation (Figure 2). In the comparison, BL width keeps fixed, while the BL spacer thickness and CC area varies. BL spacer consists of pure nitride. The simulation matches the silicon data with a gap < 2 aF/cell, which proves our simulation method reliable.

3.2 R_CC and C_BL

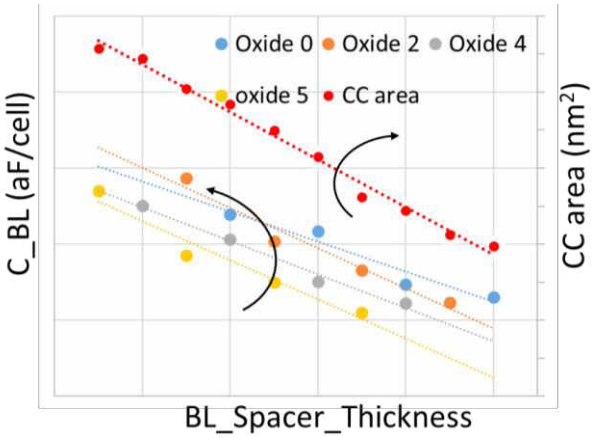

Figure 3. Correlation between C_BL and CC area for fixed BL. Different sandwiched oxide thickness of 0, 2, 4, 5 nm are compared.

The correlation between C_BL and CC area is shown in Figure 3. BL width and etching angle are fixed. BL spacer thickness sweeps with different sandwiched oxide thickness of 0, 2x, 4x, 5x nm. C_BL decreases at a rate of 1.5x~2x aF/cell/nm as BL spacer thickness increase. With thicker sandwiched oxide C_BL gets smaller.

Using typical values for CC resistance, C_s, V_{ary}, V_{BLP}, assuming WL number in one MAT is 800, the correlation between ΔV_{sm} and Δt_{WR} can be calculated using the method described in section 2. Figure 4 shows the result. Sensing margin increases with the rate of 3.9x~5.1x mV/nm, while t_{WR} with the rate of 0.038x ns/nm.

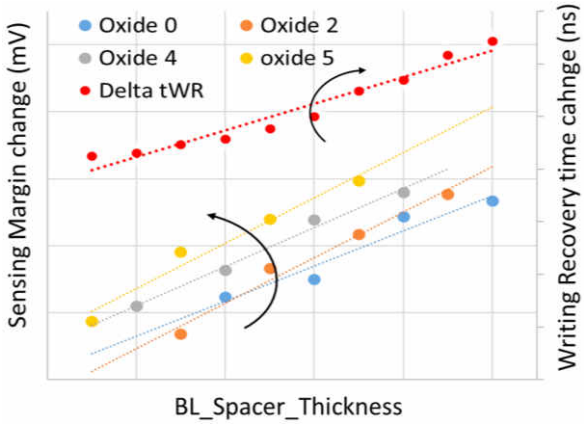

Figure 4. Correlation between sensing margin and t_{WR}. Different sandwiched oxide thickness of 0, 2, 4, 5 nm are compared.

3.3 R_BL and C_BL

Fixing CC, and BL etching angle, varying BL spacer thickness and BL width, the correlation between C_BL and R_BL were explored. The BL spacer thickness varies by changing sandwiched oxide thickness. Figure 5 shows R_BL increases significantly when BL width

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decrease (BL spacer thickness increase). C_BL decrease at the rate of 5.25x aF/cell/nm. ΔV_{sm} and Δt_{WR} trends are shown in Figure 6. In the calculation of $\Delta t_{WR,}$ the extreme case of furthest cell (the 800th) writing is considered. Sensing margin changes with a rate of 15.8x mV/nm. t_{WR} changes with the rate of 0.3x ns/nm. Comparing to that of fixing BL width, sensing margin improvement in fixing CC has a higher efficiency. However, the t_{WR} loss is also large.

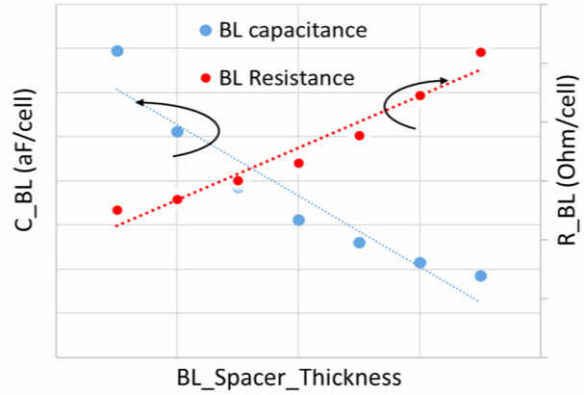

Figure 5. Correlation between C_BL and R_BL for fixed CC.

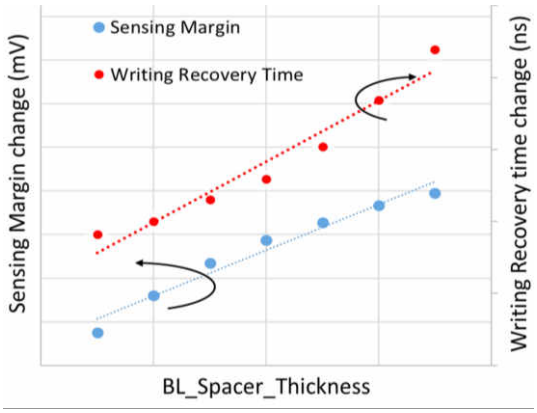

Figure 6. Correlation between sensing margin and t_{WR} for fixed CC.

3.4 BL etching angle

Tapered BL etching profile will cause the bottom BL spacer narrower than the top, thus degrade C_BL. Comparing C_BL with different tapered angles of 8x and 14x degrees, that of 8x degrees shows 1.5x aF/cell smaller (Figure 7).

3.5 Air gap

The state of art BL spacer material uses Nitride/Air gap/Nitride (NAN). We simulated C_BL of NAN with intermediate air gap width 5x nm. C_BL is 40.5x aF/cell, which is 13.5x aF/cell smaller than that with 8x nm intermediate oxide, proving the strong capability of air gap in reducing C_BL

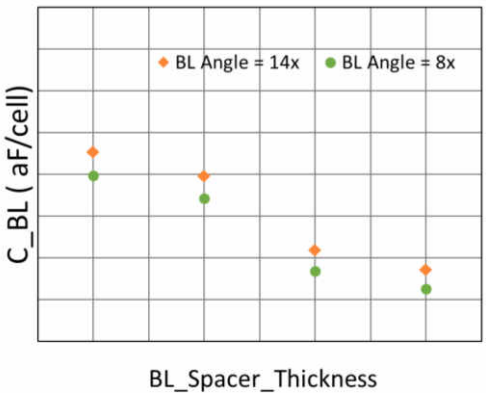

Figure 7. C_BL with different BL etching anlges of 14x degrees (orange dots) and 8x degrees (green dots)

4 Discussion

By using the DTCO methodology, we can see clear tradeoff between sensing margin and writing recovery time, which succeeded from the tradeoff between C_BL and R_BL/R_CC, and in the end attributes to the fixed pitch size. BL spacer thickness and dielectric constant determines C_BL. Inserting oxides or air reduced dielectric constants. It's demonstrated even 1 nm oxide can effectively reduce C_BL. Using air gap, we can even push C_BL down to 40.5x aF/cell without impacting $t_{WR.}$ However, air gap technology is much more difficult. Regarding BL spacer thickness we have two strategies to improve C_BL. One way is to fix BL width, expand BL spacer, and use as thick as sandwiched oxide, by which t_{WR} lose is relatively small. Considering process feasibility, optimum C_BL is 46.5x aF/cell, with the t_{WR} loss of 0.21x ns comparing to our POR. The second way is to fix CC. The optimum C_BL is 43.5x aF/cell, but with a big t_{WR} loss of 1.8x ns. The bigger t_{WR} loss is due to exponential BL resistance increase and long BL length in worse case. The smaller C_BL than the fixed BL may be due to more BL spacer filled in when BL width reduces because one side of BL spacer is deeper (Figure 1).

5 Conclusion

DTCO study of C_BL shows that tradeoff exists between sensing margin and t_{WR}. The contradictory originates from the intrinsic DRAM BL structure. It's revealed that fixing CC leads to larger C_BL reduction, but also bigger t_{WR} loss comparing to fixing BL. Air gap can significantly reduce C_BL. With feasible process parameters, optimum C_BL gain and t_{WR} loss are 46.5x/0.21x, 43.5x/1.8x, 40.5x/0 for fixed BL, fixed CC, air gap respectively. Fixed CC method is more suitable for overall performance.

References

[1] K. Wilcox and L. Gentile, IEEE Solid-State Circuits Magazine, 3, p.58 (2019)

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