Response Surface Methodology for Statistical Characterization of Nano CMOS Devices and Circuits

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***Abstract*— The accurate prediction of the impact of process variations on circuit performance is very crucial in deciding the parametric yield of integrated circuits. This paper presents the simulation methodology for studying the impact of process variations on device and circuit performance in nanometer regime. In this paper, an empirical model for power and delay of 45nm node CMOS inverter is build using the well-known Response Surface Methodology. This work also compares the suitability of different response design in terms of model accuracy.**

***Index Terms*— Response Surface, Process variability, Response Designs.**

I. Introduction

CMOS scaling into nanometer regime is associated with many short channel effects. The various approaches such as channel engineering, work function engineering, and high-K gate materials are used for better short channel performance. However, in addition to short channel effects, impact of process variation on such smaller devices is emerging as the major problem for CMOS scaling beyond 65nm technology node. Process variation results into random variations in performance of identical circuits fabricated on the same wafer. For the estimation of the amount of the variation in circuit performance, conventional circuit design methods are shifted to statistical methods [1]. In this paper, we have presented statistical design flow to quantify the impact of process variations on device and circuit performance.

This paper is organized as follows. Section II describes the CMOS device design methodology. Section III explains implementation of Plackett-Burman Design of Experiment (PB-DOE) to identify the sources of variation causing variability in device and circuit performance. Section IV describes Response Surface Methodology to build empirical models for given response. Implementation of this method is explained in section V. Finally, conclusion and future scope is given in section VI.

II. Device Design

The process flow to design NMOS and PMOS devices to meet ITRS specifications at a specific technology node is shown in Fig 1. The process flow starts with assuming an oxide thickness (T_{ox}) and gate length (L_G) with their values specified in ITRS corresponding to specified technology node, as inputs to the process simulator. The other process parameters such as the various implant doses, etc are tuned to match I_{off} and I_{on} values of the resulting device as per ITRS specifications.

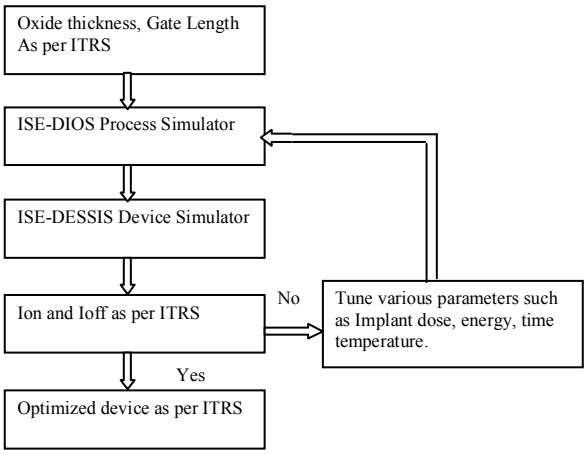

Fig. 1. Device Design Flow using Dios and Dessis

For this work, 45nm technology node CMOS devices are designed using process simulator (DIOS) and device simulator (DESSIS) as shown in Fig. 1. The device simulations are performed by assuming metal gate with suitable work function and high-K gate material. The specifications of these TCAD devices are matched as per the ITRS guidelines [2] by tuning various process parameters as shown in Fig. 1. These tuned process parameters are considered as nominal process parameters. In this work, the impact of process variations on device and circuit performance is studied with respect to these nominal process parameters. The IdVg characteristics of 45nm node NMOS and PMOS devices are shown in Fig. 2a and Fig. 2b respectively.

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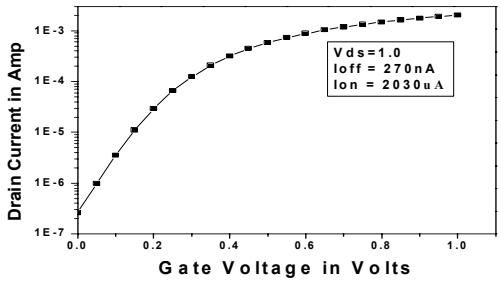

Fig. 2a. IdVg characteristics of 45nm node NMOS device

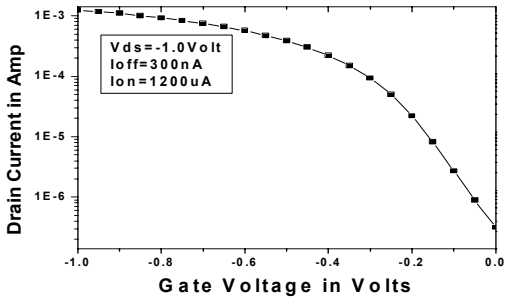

Fig. 2b. IdVg characteristics of 45nm node PMOS device

III. SOURCES OF PROCESS VARIATIONS

In order to study process variation impact on devices and circuit performance, it is important to identify sources of variations causing variability in device and circuit performance. Plackett-Burman Design of Experiment (PB-DOE) [3] is identified as one of the method to obtain contribution of each process parameter on given response in minimum number of experimental runs. PB-DOE is two level fractional factorial experiments in which each process parameter is having two levels i.e high level and low level. In this study, low and high levels are considered as -10% and +10% of nominal values respectively. In this work, we have implemented PB-DOE on 45nm node NMOS and PMOS devices to identify dominant process parameters causing device variability.

A. Process Variation Impact on NMOS Device

The percentage variation in I_{off} and I_{on} of NMOS device due to various process parameters is shown in Fig. 3a and Fig. 3b respectively. These figures show that a variation in gate length causes maximum variability in I_{off} and I_{on} as reported in [4]. This validates the suitability of PB-DOE in identifying sources of variability. These figures also show that process parameters such as oxide thickness, gate length, source/drain implant energy and ldd implant dose contributes to more than 92% variability in I_{off} and I_{on}. Hence, only these parameters are considered to study impact of process variations on circuit performance and remaining are ignored, as their contribution to device variability is negligible.

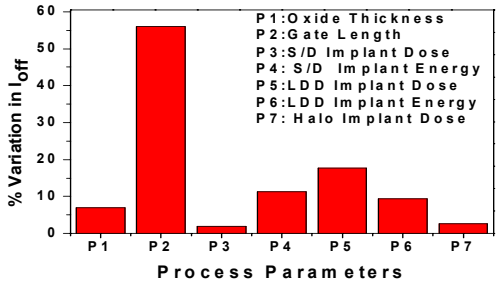

Fig. 3a. Percentage Variation in I_{off} of 45nm node NMOS Device

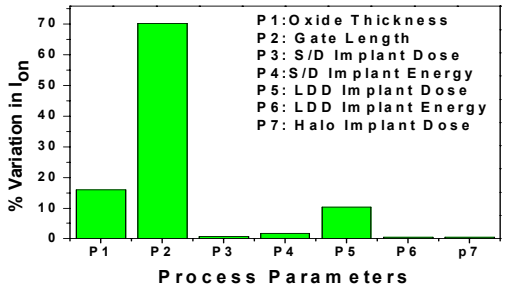

Fig. 3b. Percentage Variations in I_{on} of 45nm NMOS Device

B. Process Variation Impact on PMOS Device

Impact of process variations on I_{off} and I_{on} of 45nm node PMOS device is shown Fig. 4a and Fig. 4b respectively. These figures also show that a variation in gate length causes maximum variability in I_{off} and I_{on} of PMOS device. Similarly, ±10% variation in gate length, source/drain implant dose and halo implant dose contributes to more than 97% variability in I_{off} and I_{on} of PMOS device as illustrated in Fig. 4a and Fig. 4b respectively. These process parameters of PMOS devices are considered for the inverter simulations and remaining parameters are ignored, as their contributions to device variability are less than 5%.

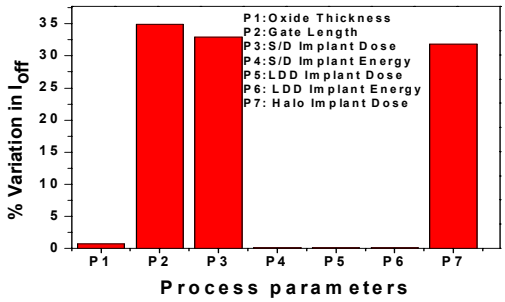

Fig. 4a. Percentage Variation in I_{off} of 45nm node PMOS Device

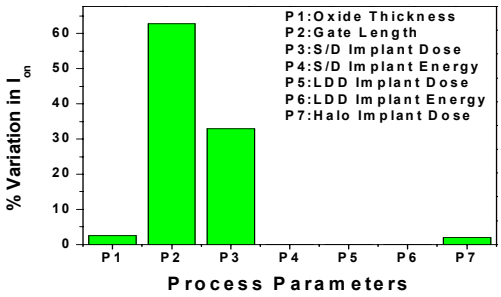

Fig. 4b. Percentage Variation in I_{on} of 45nm node PMOS Device

C. Process Variation Impact on CMOS Inverter

This section explains implementation of PB-DOE to identify the major process parameters causing variability in delay and power of 45nm node CMOS inverter. CMOS inverter is simulated using ISE-Mixed Mode simulator. In PB-DOE, we have considered major process parameters causing variability in NMOS and PMOS device as explained in earlier section. Fig 5a and Fig. 5b shows impact of process variations on delay and power of CMOS inverter respectively.

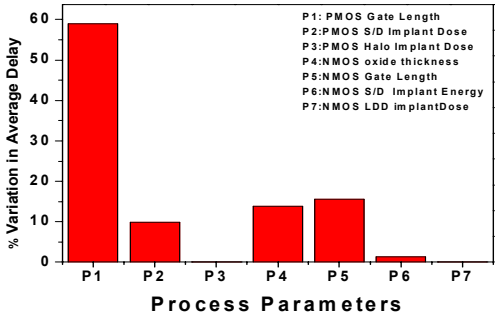

Fig. 5a. Percentage Variation in Average Delay of 45nm node CMOS Inverter

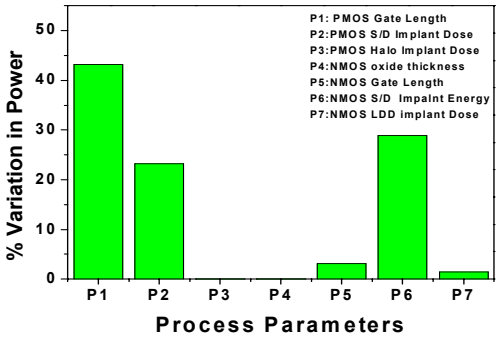

Fig. 5b. Percentage Variations in Total Power of 45nm node CMOS Inverter

Fig. 5a shows that PMOS gate length, NMOS oxide thickness and NMOS gate length contributes to more than 95% variability in average delay. This is obvious as these process parameters contributes to maximum variability in on current (I_{on}) of respective transistors. PMOS gate length, PMOS source/drain implant dose and NMOS source/drain implant energy contributes to more than 90% variability in total power as shown in Fig 5b. These process parameters are considered to build response surface model for average delay and power of CMOS inverter and remaining parameters are ignored

IV. Response Surface Methodology

This section explains the methodology to build the response surface model [RSM] between response and input parameters when relation between input and output is unknown [5]. The PB-DOE explained above is used to screen out the less important process parameters as explained in above sections. In order to build non-linear second order model various three level response designs such as Box-Behnken's design, Composite Design with Face Centered (CCF) [6] are used. Box-Behnken design for three-process parameter is shown in Table 1. The P_1 to P_3 indicates the most sensitive process parameters for given response, which are obtained after the analysis of PB-DOE, which is explained in last section. In matrix '-' and '+' indicates the low level and high level of process parameter while '0' represents nominal value. Then simulations are performed as per this matrix and corresponding responses are measured.

Table 1. Box-Behnken Matrix

	P_1	P_2	P_3	Y
1	-	-	0	Y_1
2	-	+	0	Y_2
3	+	-	0	Y_3
4	+	+	0	Y_4
5	-	0	-	Y_5
6	-	0	+	Y_6
7	+	0	-	Y_7
8	+	0	+	Y_8
9	0	-	-	Y_9
10	0	-	+	Y_{10}
11	0	+	-	Y_{11}
12	0	+	+	Y_{12}
13	0	0	0	Y_{13}
14	0	0	0	Y_{14}
15	0	0	0	Y_{15}

The second order RSM is given by

$$Y = \beta_0 + \beta_1 P_1 + \beta_2 P_2 + \beta_3 P_3 + \beta_{11} P_1^2 + \beta_{22} P_2^2 + \beta_{33} P_3^2 + \beta_{12} P_1 P_2 + \beta_{13} P_1 P_3 + \beta_{23} P_2 P_3 \quad (1)$$

where β's are regression coefficient and P_1, P_2 and P_3 are most sensitive process parameters. Y is the response of interest and it can be either device response or circuit response as mentioned above.

The regression coefficients are obtained using method of Least Square Error (LSE) as given below.

$$\beta = [X^T X]^{-1} X^T Y \quad (2)$$

where β is the coefficient matrix of (10×1) order. The X is Box-Behnken matrix of (15×1) order as shown in Table 1. Y is response matrix of (15×1) order. In this way, RSM is build in terms of the most sensitive process parameters. Once response model is build, one can predict the variability for different combinations of process parameters.

V. Implementation of Response Surface Methodology

This methodology is implemented to build response model for average delay and power of 45nm node CMOS inverter in terms of most sensitive parameter as identified in last section. Central Composite Design with Face Centered (CCF) and Box-Behnken response designs are used to build the model response model for average delay and power. Root mean square (RMS) error and R^2 [6] value which are measure of accuracy of model are in given in Table 2. The CCF design approach shows around 40% improvement in RMS error and 20% improvement in R^2 value as compared to Box-Behnken design.

Table 2.Comparison of CCF and Box-Behnken Design

Parameter	Delay		Power	
	CCF	Box-Behnken	CCF	Box-Behnken
% of RMS error	2.23	3.96	2.95	3.63
% of R^2 Value	91	76	94	77

The RSM is used to obtain statistical distribution for delay and power of CMOS inverter. For this purpose, random samples of process parameters are generated using Gaussian distribution with constant mean and different standard deviations. The results are shown in Table 3. These results show that standard deviation of delay and power is proportional to standard deviation of process parameters.

Table 3. Statistics of Inverter Performance

standard deviation of process parameters	Delay		Power	
	Mean	Standard Deviation	Mean	Standard Deviation
5%	4.68 ps	0.18 ps	855 µW	52 µW
10%	4.68 ps	0.37 ps	855 µW	110 µW
15%	4.68 ps	0.54 ps	858 µW	162 µW

Finally, statistical distribution of delay and power of CMOS inverter for large number of random samples of process parameters are shown in Fig. 7 and Fig. 8 respectively.

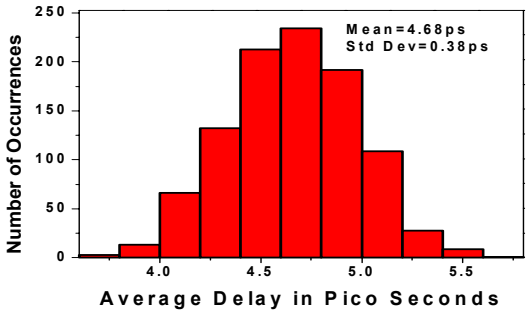

Fig. 6a. Distribution of Average delay of 45nm node CMOS Inverter

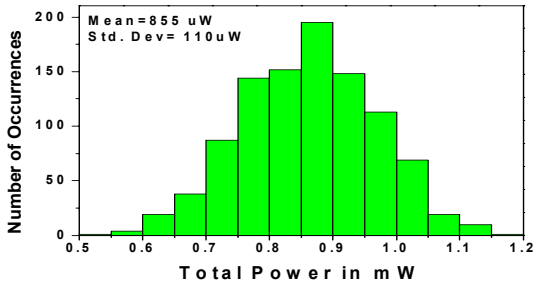

Fig. 6b Distribution of Total Power of 45nm node CMOS Inverter

VI. Conclusion and Future Scope

In this work, we have identified suitability of PB-DOE to identify major sources of variations causing variability in device and circuit performance. We have also developed response surface model for delay and power, which is used to predict performance spread to due sensitive process parameters. In this work, we have also shown that CCF response design results in better accuracy of response model as compared to Box-Behnken response design.

The response surface model developed in this work can be used to predict parametric yield of integrated circuits. This model also provides guidelines for optimization of process parameters to improve parametric yield under process variations.

References

1]S.R. Nassif, "Modeling and analysis of manufacturing variations," Proc. IEEE Conf. on Custom Integrated Circuits, PP.223-228, May 2001.

[2]International Technology Road Map for Semiconductors http://public.itrs.net

[3]Tuna B. Tarim, H. Hakan Kuntman and M.Ismail, " Statistical Design of Low Power Square Law CMOS cells for high yield," Analog Integrated Circuits and Signal processing, Vol.23, Nov. 2000.

[4] Yu Cao and Lawrence T Clark, "Mapping statistical process variations towards circuit performance variability: An Analytical Modeling approach," Annual ACM IEEE Design Automation Conference 2005.

[5] Raymond H Mayers and Douglas C Montgomery, "Response Surface Methodology," Wiley Series in Probability and Statistics

[6]Ayhan A. Mutlu and Mahmud Rahman, "Statistical methods for estimation of process variation effects on circuit operation," IEEE Transaction on Electronics Packaging Manufacturing, Vol, October 2005

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