4M-3

Logic Block Level Design-Technology Co-Optimization is the New Moore's Law (Invited)

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***Abstract*—Over the last several technology generations the slower feature scaling has been increasingly complemented by DTCO. Initially, DTCO was employed at a smaller scale to decide which technology modules to introduce to achieve target PPAC (Power-Performance-Area-Cost) specs. Then it was extended to evaluate and optimize a combination of design rules and logic library cell design. Now, DTCO is being extended to cover logic block PPAC for a variety of specific target applications ranging from high performance computing to low power mobile chips. In this talk, we focus on the latest trends in logic block level PPAC analysis and highlight several key components of such analysis that are necessary to achieve the required accuracy at the early pre-silicon DTCO stages.**

Keywords—DTCO, PPA, Moore's law, digital design, advanced CMOS

I. Introduction

Typical chips contain multiple blocks that are easily visible in chip images (Fig. 1). Most of the blocks are dedicated to performing logic processing and to SRAM (Static Random Access Memory). Considering that logic blocks represent a major part of the chip area and determine its power consumption, performance, and cost, it is critical to improve their PPAC by trying different design and technology scenarios in DTCO.

Due to increasingly restrictive design rules, there is not much PPAC gain can be achieved by optimizing individual logic library cells. However, increasing the scope to ring oscillators provides a bigger room to play [1,2], and taking it to logic block level gets into double digit PPAC gains (Fig. 2). Currently, the main DTCO objectives are to maximize the PPAC gain, to speed up the runtime, and to get higher accuracy, which is what we address in this work.

II. DTCO Scope and Tool Flow

DTCO for advanced CMOS has to span from ab-initio atomistic analysis of sub-transistor scale structures through transistor scale analysis of advanced electron transport to library level analysis of interconnect resistance and capacitance to digital flow that tends to go beyond million transistors (Fig. 3).

It is very important that all DTCO stages are performed with high enough accuracy to provide meaningful results that can guide harmonization of design and technology for a given set of manufacturing possibilities. Let's zoom in into several key parts of the DTCO flow and review the necessary level of detail to achieve high enough PPAC accuracy.

III. Well Proximity Effect

N-well and p-well doping for the CMOS technology is known to produce WPE (Well Proximity Effect) due to the high energy dopant ions scattering out of the photoresist mask, which increases surface doping near the well masks and increases the threshold voltage there by tens of millivolts [3, 4].

The implant ion scattering is similar for planar MOSFETs and FinFETs, with threshold shifts happening within several hundred nanometers of the well mask (Figs. 4 and 5). Due to the physical nature of WPE, predictive WPE modeling is only possible with Monte Carlo binary collision model [5] that gives highly accurate results and exhibits some statistical noise that reflects actual dopant statistics (Figs. 6 and 7).

The shape of the mask is one of the key components of getting the WPE characterization correctly. The corner rounding that is caused by optical lithography effects despite OPC (Optical Proximity Correction) affects the exact location of the WPE (Figs. 8 and 9). For the FinFET technology with tight fin pitches, such WPE shifts translate into a fin getting threshold shift or not, which makes a profound difference in terms of circuit timing and off-state leakage [4].

IV. Real Wire Analysis

The design intent interconnect wires (Fig. 10) are often implemented into the shapes that are quite different due to the litho effects and opportunistic mask retargeting (Fig. 11). As an illustration of typical interconnects with 25 nm minimum wire pitch that corresponds to 3nm node, we take a design intent layout shown on Fig. 12. A single exposure EUV (Extreme Ultra-Violet) lithography rigorous model [6] transfers design intent layout into the "sausages" (Fig. 13).

Cobalt wires with width getting below 13 nm exhibits strong non-linear resistivity behavior that requires a special "Dracula coffin" narrow wire resistance model [7]. Applying such model that is calibrated to Si data to the two versions of interconnect layout shows drastic difference in wire conductivities (Figs. 14 and 15). Interconnect resistance calculation involves building a faithful 3D interconnect geometry (Fig. 16) and applying narrow wire resistance model.

The wire resistance differences between design intent and post-litho layouts range from +14% to -28% (Fig. 17). Such differences make a big PPAC impact and therefore require careful modeling of litho effects and narrow wire resistance.

References

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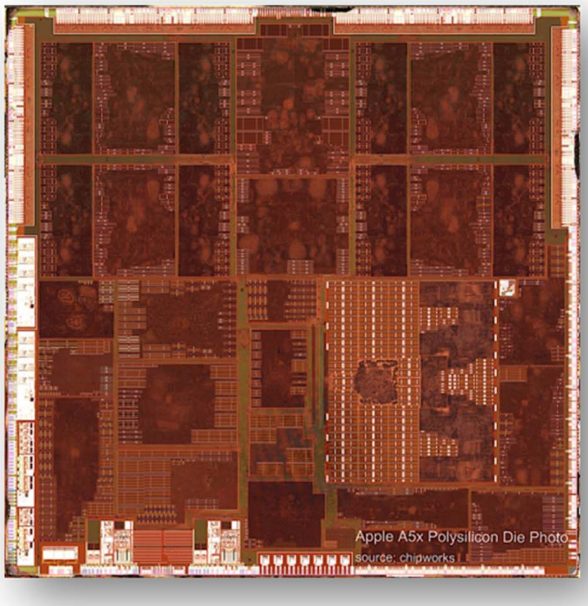

Fig. 1. Typical chip contains multiple blocks that perform different functions. Most of the chip area is occupied by logic blocks and SRAM memory blocks.

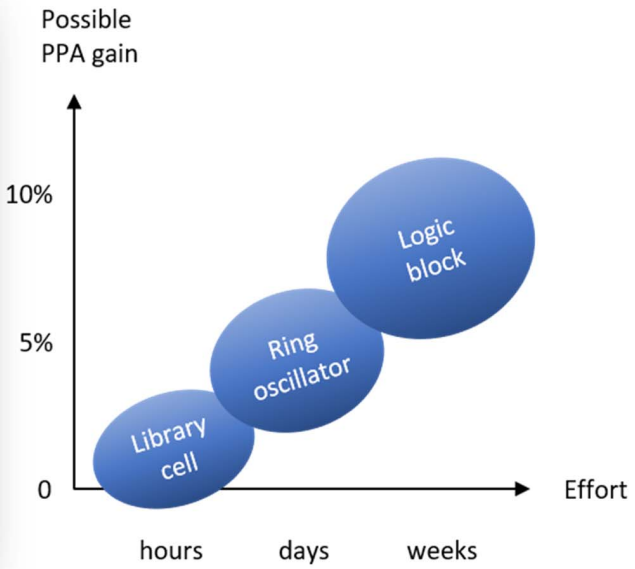

Fig. 2. Potential Power-Performance-Area gain due to optimization of the individual logic library cells is typically within low single digit percentage. For the ring oscillator optimization, it increases to middle single digits, and for logic block optimization it can reach double digits.

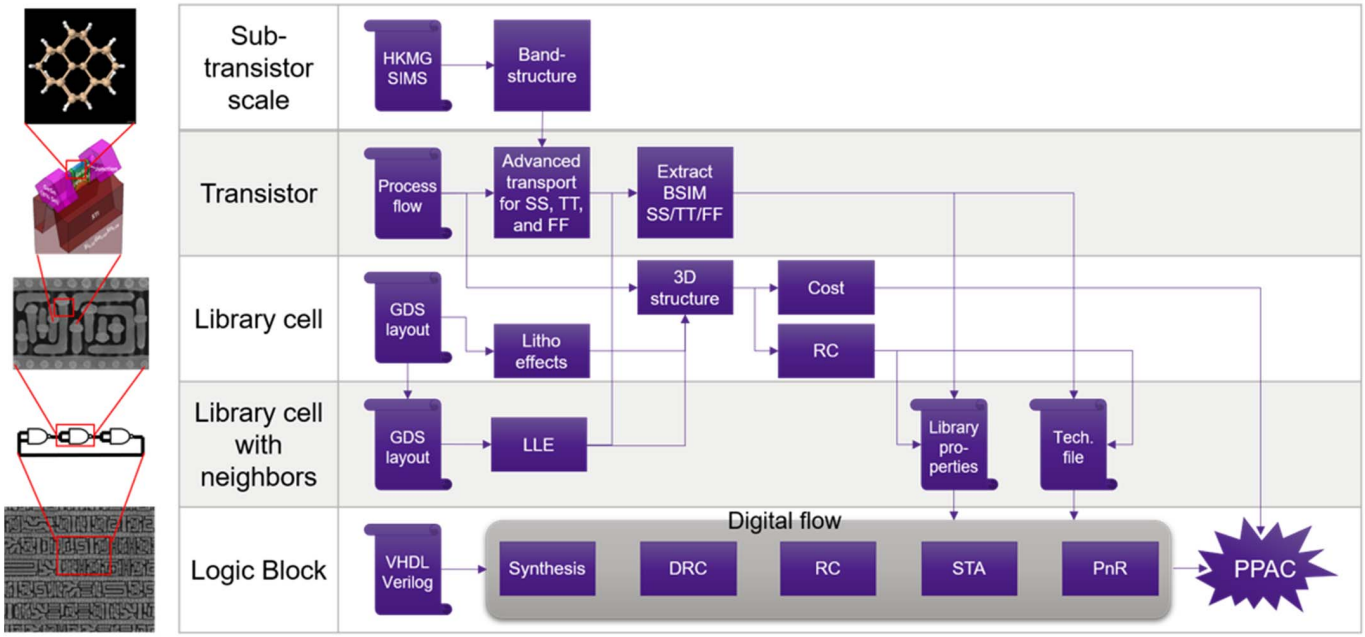

Fig. 3. Design flow for advanced CMOS logic is spanning sub-transistor ab-initio material engineering, transistor level analysis, library cell characterization, then several library cells for estimation of the layout proximity effects, and finally logic block PPAC analysis. Abbreviations: HKMG: High-K Metal Gate, SIMS: Secondary Ion Mass Spectrometry, SS: Slow/Slow process corner, TT: Typical/Typical corner, FF: Fast/Fast corner, GDS: layout format, RC: Parasitic resistance and capacitance, LLE: Local Layout Effects, RTL: Register Transfer Level, DRC: Design Rule Check, PnR: Place and Route, STA: Static Timing Analysis.

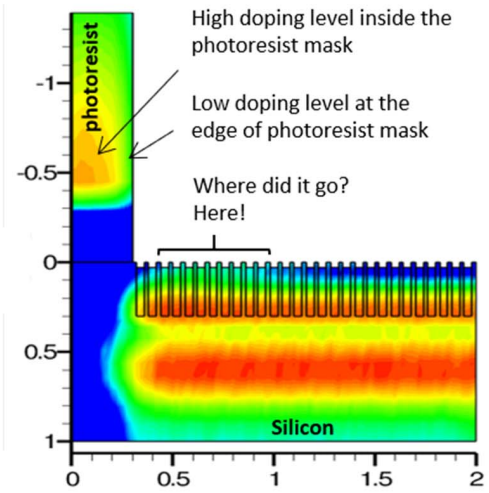

Fig. 4. Illustration of the Well Proximity Effect due to the scattering of implanted ions out of the photoresist edge into adjacent silicon with multiple fins. This is 2D cross-section in the direction across the fins.

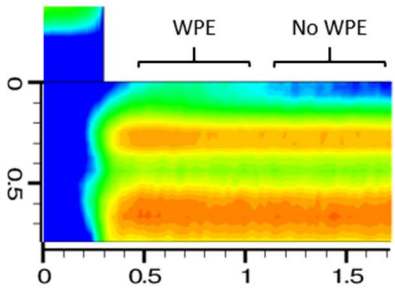

Fig. 5. WPE for the planar MOSFETs. The peak of the well implant here is deeper than for the FinFETs, because here amorphous STI oxide does not contribute to the ion scattering, but the surface WPE effect is similar to FinFETs.

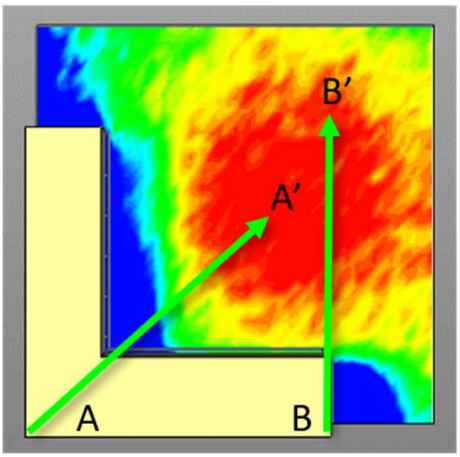

Fig. 6. Top view of the well implant scattering for a photoresist mask with design intent shape.

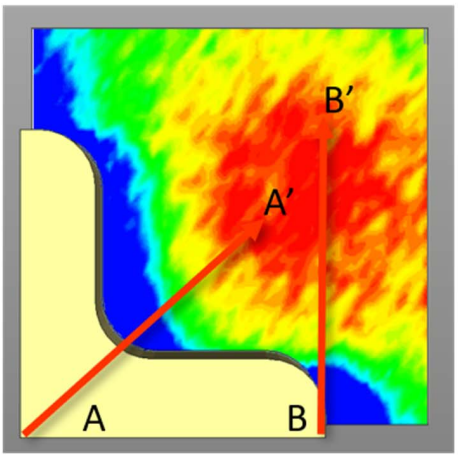

Fig. 7. Top view of the well implant scattering for a photo-resist mask with corner rounding due to litho/OPC effects.

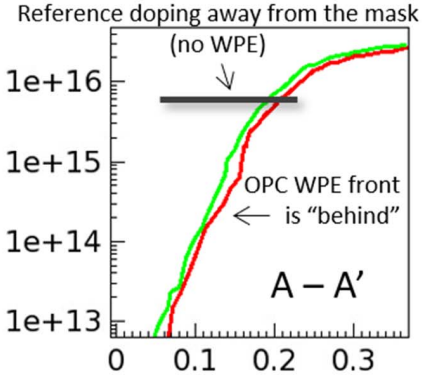

Fig. 8. Doping profile on silicon surface along the A-A' line for the mask with design intent and the mask with OPC-induced corner rounding.

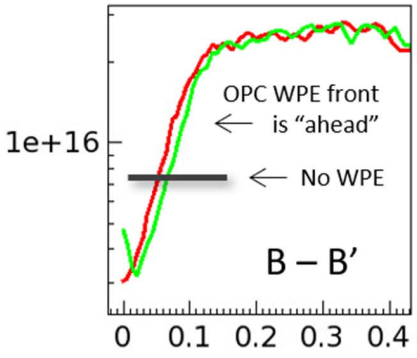

Fig. 9. Doping profile on silicon surface along the B-B' line for the mask with design intent and the mask with OPC-induced corner rounding.

Fig. 10. Top view of interconnect fragment based on design intent.

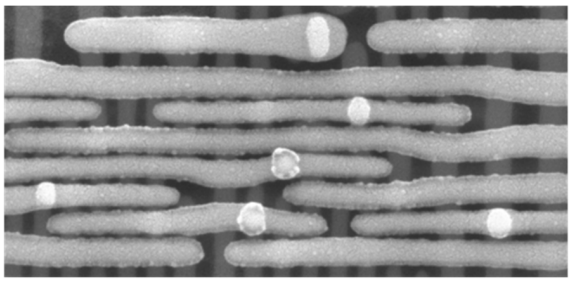

Fig. 11. SEM image of the silicon structure of the same interconnect fragment as on Fig. 10. Source: TechInsights.

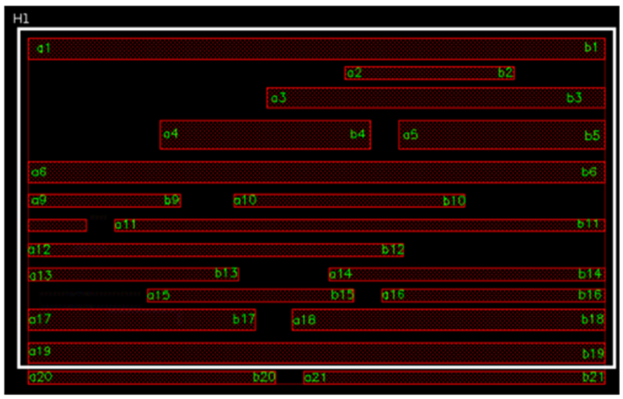

Fig. 12. Design intent layout with wire labels.

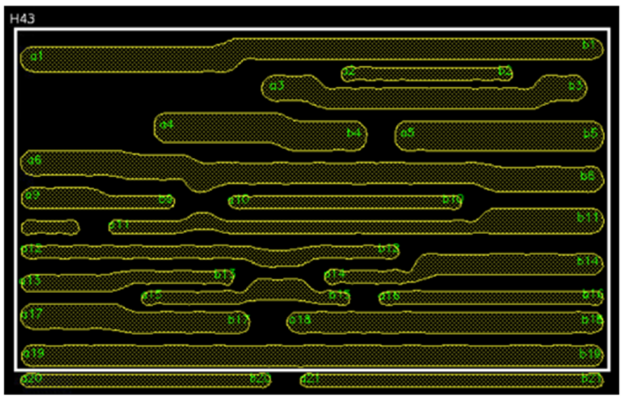

Fig. 13. Post-litho layout with wire labels.

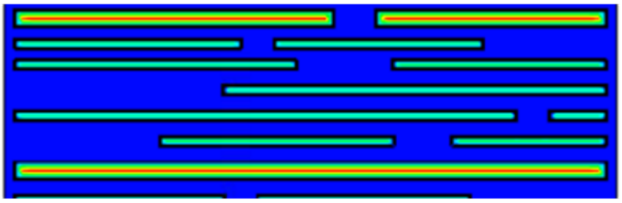

Fig. 14. Top view of cobalt conductivity map for design intent layout.

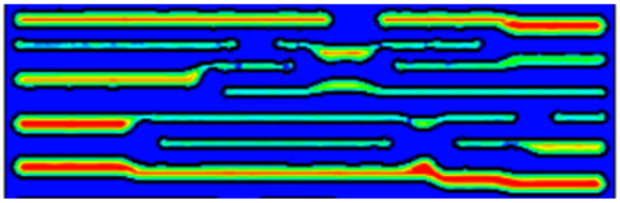

Fig. 15. Top view of cobalt conductivity map for the post-litho layout. Red color means high conductivity, green color – lower conductivity, and blue – the lowest.

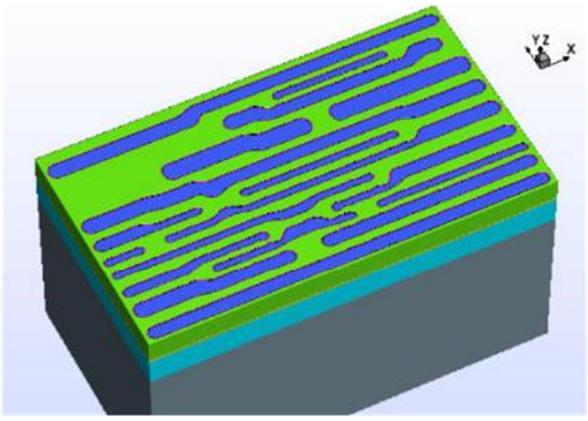

Fig. 16. 3D interconnect structure with the post-layout metal and dielectric shapes. Single EUV exposure with 25 nm minimum wire pitch.

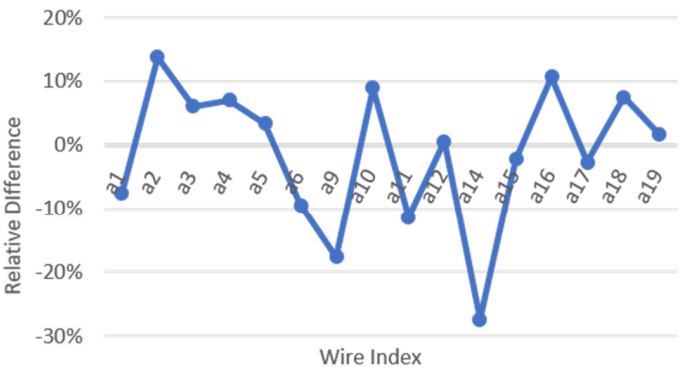

Fig. 17. Resistance difference between design intent and post-litho wires based on the IMEC/SNPS narrow wire resistivity model that is calibrated to Si data.