Design for Manufacturability in Backend Reliability and Packaging of Nanoscale Technologies

Y.K. Lim[1, 2], J.B. Tan[1], K.L. Pey[2], E.C. Chua[1], Y.H. Yeo[1], Thomas Fu[1] and L.C. Hsia[1]
[1]Chartered Semiconductor Manufacturing Ltd., 60 Woodlands Industrial Park D Street 2 Singapore 738406
Phone: 65-6413-7618; Fax: 65-6413-7506, Email: limyk@charteredsemi.com
[2]Microelectronics Center, School of Electrical and Electronic Engineering, Nanyang Technological University, Nanyang Avenue, Singapore 639798

Abstract

Integration of copper (Cu) and low-k dielectrics has posed significant challenges for device reliability and packaging. For faster and successful semiconductor product introduction, early implementation of simulation model for physics and mechanical studies, and the subsequent design for manufacturability (DFM) are important considerations for device reliability and packaging communities. In this paper, several structural designs and finite element analysis (FEA) simulation models were employed to illustrate the importance of DFM in backend reliability and packaging. Also, its extendibility to future nanoscale technologies employing porous ultra low-k Cu interconnects was discussed.

Introduction

As the circuit feature size continues to shrink, the increase of propagation delay due to interconnect, i.e. RC delay, becomes dominant and has limited the advancement of high performance IC. Hence, the industry gradually migrated from aluminum (Al) to material of lower resistivity like Cu, and the replacement of silicon dioxide (SiO_2) with low-k materials to reduce the RC delay. However, low-k dielectrics pose significant challenges to process integration, reliability, and packaging [1-6]. They have low hardness and modulus, poor adhesion with other films and low thermal conductivity, leading to cracking, delamination, and reliability and packaging failures. In this paper, the effects of structural designs on backend reliability and packaging were studied. The effectiveness of the structural designs in improving the reliability and packaging were confirmed via FEA simulation. In view of the increasing challenge for faster and successful semiconductor product introduction, early utilization of simulation model and the subsequent DFM are strongly recommended to provide a comprehensive solution to reliability and packaging of future nanoscale CMOS devices.

Results and Discussion

A. Effect of Via Gouging Depth on Backend Reliability

Via gouging into underlying metal during Cu interconnects fabrication is unavoidable. Over etch during via bottom opening, physical Ar sputtering employed to clean via bottom or diffusion barrier layer first deposition method would result in certain degree of via gouging [7,8]. Figures 1 and 2 show appropriate control of via gouging depth could enhance the electromigration (EM) and stress migration (SM) reliability [6,8] of Cu interconnects respectively.

FEA simulated hydrostatic stress distribution in M1 around gouging holes with depth of 62Å and 400Å was performed to study the corresponding mechanism responsible for the improvements observed (see Figs. 3(a) and (b)) [6]. In Fig. 3(b), the high tensile stress region was shifted downwards into M1, away from the Cu cap/via interface, which was considered to be one of the dominant nucleation sites of voids due to presence of high density of interfacial defects. Also, the reduction in tensile stress was found to be approximately 50MPa thus the driving force for void nucleation was correspondingly reduced, leading to improved EM and SM reliability.

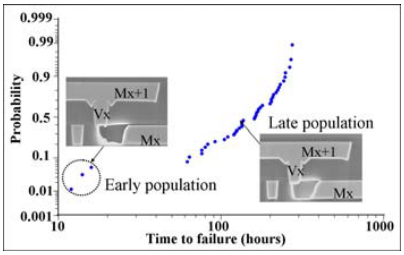

Fig. 1 As supported by physical analysis, EM time-to-failure was enhanced with appropriate control of via gouging depth.

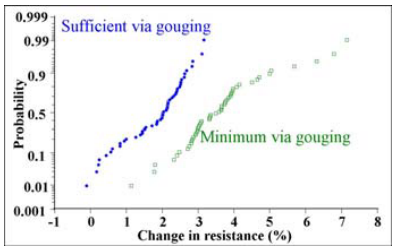

Fig. 2 Similar trend was observed for the SM reliability of Cu interconnects. It improved with sufficient via gouging.

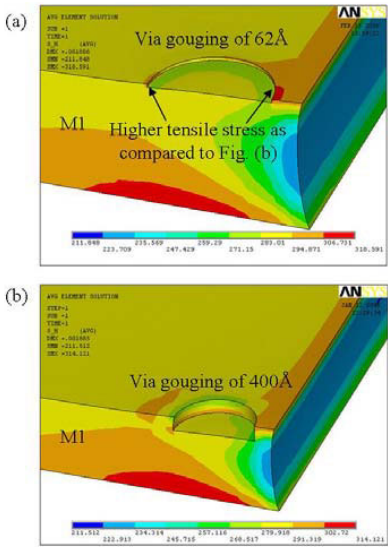

Fig. 3 Hydrostatic stress distribution in M1 around gouging hole with depth of (a) 62Å and (b) 400Å during SM test. The unit of stress distribution is MPa.

B. Effect of Redundant Via(s) on Backend Reliability

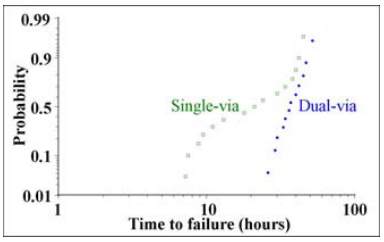

Fig. 4 The EM reliability of Cu interconnects was significantly improved with dual-via structure.

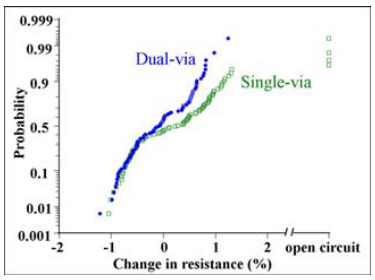

Fig. 5 The SM reliability of Cu interconnects improved with dual-via structure.

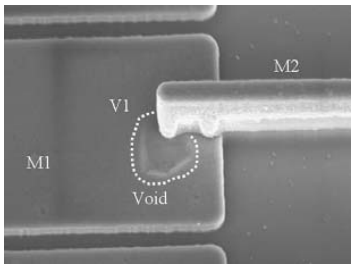

Fig. 6 A dual-via structure after SM test. As shown by the dotted lines, the formation of stress-induced void beneath the inner via was clearly seen.

The inclusion of redundant via(s) was shown to be an effective approach in improving the EM and SM reliability of Cu interconnects. EM time-to-failure lognormal plot of single and dual-via structures are shown in Fig. 4. EM lifetime was improved with dual-via structure. Additional driving force needed for void nucleation and less sensitivity to resistance change associated with redundant via are believed to be the dominant mechanisms resulting in improved EM reliability. Figure 5 shows the percentage change in single and dual-via chain resistance after SM test. Similar trend was observed; SM reliability was drastically improved with dual-via structure [6]. As shown in Fig. 6, physical analysis performed on dual-via Cu interconnects after SM test revealed that stress-induced void was consistently found to form beneath the inner via only [9].

Figure 7 shows the FEA simulated hydrostatic stress distribution in M1 around gouging holes of a redundant via structure during SM test [6]. The inner via of the wide Cu metal lead (i.e. Via A) consistently suffers a higher hydrostatic stress distribution than that of the outer via (i.e. Via B) that is closer to the end of M1. The difference in tensile stress at the Cu cap/via interface of the two vias was found to be approximately 40MPa, indicating a much larger driving force for void nucleation at Via A. Moreover, since Via A was further away from the end of M1, it encountered a higher effective diffusive volume of vacancies than that of Via B. This explained why Via A was a much weaker via that was more prone to stress-induced voiding. The sacrificial role of Via A led to minimal degradation in the SM reliability [1,6].

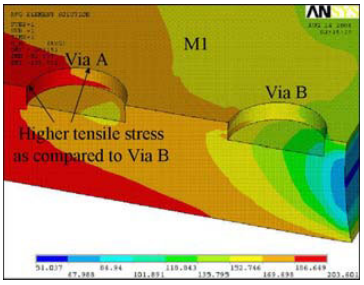

Fig. 7 Hydrostatic stress distribution in M1 around the gouging holes in a redundant via structure during SM test. The unit of stress distribution is MPa.

C. Effect of Inter-layer Structural Design on Heat Propagation

During switching transients, power bus in the circuit may carry large amount of current and cause significant heating to the chip. Steep temperature gradient developed between inter-layers and coefficient of thermal expansion (CTE) mismatch between different materials could lead to delamination. FEA simulation was employed to study the heat propagation of different inter-layer structural designs during continuous high current flow. Figure 8(a) shows the schematic of two different inter-layer structural designs (i.e. designs A and B) used in this study. The corresponding heat propagation plotted along AA' at constant current of 50mA/μm is showed in Fig. 8(b). Comparing to design A, the temperature gradient of design B was gentler. This was attributed to Cu dummies inserted between the underlying power bus of design B that helped in the heat propagation. As such, design B is recommended for chip with high current power bus to prevent the formation of steep temperature gradient between inter-layers, which causes delamination.

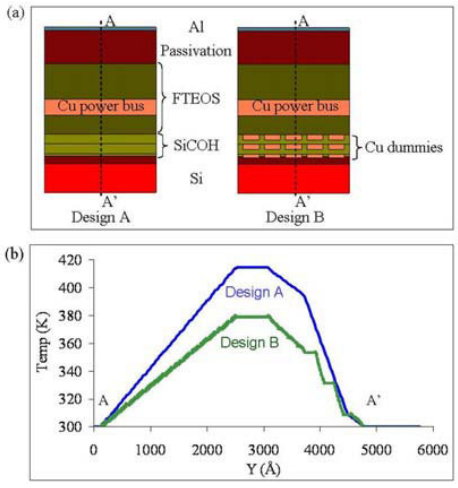

Fig. 8(a) Schematic of inter-layer structural designs A and B. (b) The corresponding heat propagation plotted along AA'shown in (a).

D. Effect of Structural Design under Pad on Wire bond

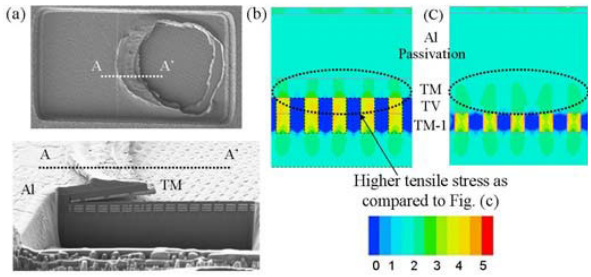

Fig. 9(a) Placement of top metal under pad caused it to tear during wire pull. Stress distribution under pad (b) with and (c) without top metal and vias during wire pull. Top metal and vias show high tensile stress when placed directly under bond pad. The unit of stress distribution is GPa.

The ability to withstand stress during wire bond varies with different structural designs under pad. Figure 9(a) shows placement of top metal (TM) under pad caused it to tear during wire pull. Figures 9(b) and (c) show FEA simulated stress distribution under pad with and without top metal and vias (TV) respectively, during wire pull with a force of 2GPa. High tensile stress found in top metal and vias of Fig. 9(b) favored pad tearing. As such, placement of top metals and vias under pad is prohibited for robust wire bond packaging.

E. Low Volume Bumps

As technology advances, chips of varying sizes, different bump pitches and passviations are employed to fit the wide range of applications. This trend has significantly increased the challenges of bumping process. As illustrated in Fig. 10(a), low volume bumps were formed when oxide/silicon nitride (Si_3N_4) passivation was employed. This was attributed to insufficient spacing between Al lines, thus overhang was formed after oxide/Si_3N_4 deposition (see Fig. 10(b)). During bumping, the overhang resulted in a non-uniform sputtered Ti/Cu layer which affected the subsequent nickel (Ni) and solder plating process, leading to smaller bumps. This was not observed for polyimide passivation because the spin coated layer was thicker and no overhang was formed. Thus, spacing between Al lines is more critical to bumping when oxide/Si_3N_4 passivation is employed.

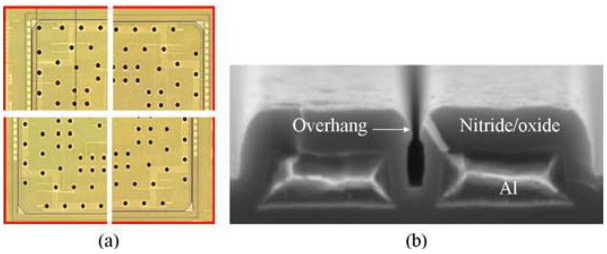

Fig. 10(a) Low volume bumps of size 70um observed versus normal size of 85um. (b) Insufficient spacing between Al lines causes overhang after oxide/Si_3N_4 deposition leading to low volume bumps.

F. Roles of DFM in Backend Reliability and Packaging

DFM, commonly used for process optimization with designs, could play a more significant role in backend reliability and packaging of CMOS devices. As illustrated in the previous sections, DFM could be further developed to make Cu interconnects more resilient to reliability degradation and packaging related failures. However, in order to make DFM more useful and applicable, a thorough understanding of the dominant failure mechanisms relating to reliability and packaging is necessary. FEA simulation is one of the approaches to provide in-depth understanding of various reliability and packaging failures seen in today's state-of-the-art CMOS technologies since it is no longer cost effective to study these failures through the standard design for experiment (DOE) approach. This implies that early implementation of simulation model for physics and mechanical studies and the subsequent DFM shown in the flow chart in Fig. 11 would be important considerations for device reliability and packaging communities in future nanoscale technologies.

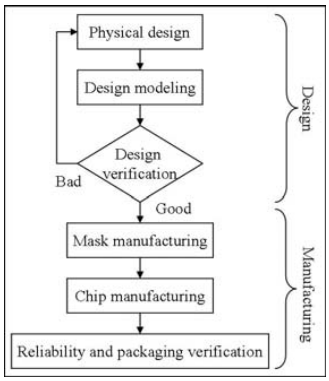

Fig. 11 Early implementation of simulation model for physics and mechanical studies and the subsequent DFM are important considerations for device reliability and packaging communities.

Conclusion

DFM plays an important role in backend reliability and packaging of CMOS devices. In addition, the application of FEA simulation has proven to provide the required insight for effective implementation of DFM to achieve robust backend reliability and packaging. Due to more complex structures and advanced materials such as porous ultra low-k dielectrics, being used for future nanoscale technologies, early utilization of simulation model and the subsequent DFM are strongly recommended to cope with the increasing reliability and packaging challenges.

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References

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