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A 65 nm Standard Cell Library for Ultra Low-power Applications

Marten Vohrmann, Saikat Chatterjee, Sven Lütkemeier*, Thorsten Jungeblut, Mario Porrmann, Ulrich Rückert
Cognitronics and Sensor Systems Group
CITEC, Bielefeld University
33619 Bielefeld, Germany
Email: {mvohrmann,schatterjee}@cit-ec.uni-bielefeld.de
*Former group member, now at Beckhoff Automation GmbH & Co. KG

***Abstract*—This paper describes the development of a 65 nm standard cell library designed for building highly energy-efficient digital circuits. In total 43 logic cells and 19 special cells for clock-tree synthesis and place and route purposes are implemented using a commercial 65 nm bulk technology. As a result full-chip implementation of low-power systems operating at ultra-low voltage is feasible. The benefits of this subthreshold cell design are demonstrated by synthesis and analysis of a sample circuit for supply voltages from 250 mV to 1.2 V. Power analysis at gate-level shows an improvement in energy consumption by a factor of 9.25 with a total energy consumption of 11.7 pJ per clock cycle in the subthreshold domain.**

***Keywords*—ultra low-power, subthreshold library design, 65 nm bulk technology**

I. Introduction

In the current and future era of nanoelectronics power consumption has been the most concerning factor. Subthreshold operation is considered to be a possible solution to meet the low-power requirements [1]. Since the dynamic power consumption varies quadratically and the static power exponentially with the supply voltage, a significant amount of energy can be saved while operating below the threshold voltage. While the latter is the main advantage of subthreshold operation, performance drawbacks are significant. Therefore, this design methodology is primarily used for energy-constrained applications, where performance is not the main concern. Examples are biomedical implants [2], wireless sensor networks [3] or radio frequency identification (RFID) [4]. Standard cells form the building blocks for the design of digital circuits and are composed in so called standard cell libraries. In consequence of the increased sensitivity of the cells towards process variations and changes in temperature and supply voltage during subthreshold operation, the main focus, while designing standard cells for this operation mode, lies on the robustness of the cells. In the following we present a design methodology for a full custom cell library, which contains the approach proposed in [5].

The challenges in subthreshold designs were thoroughly explored in [6], whereas the authors of [7] propose the utilization of the reverse short-channel effect for optimization of transistor dimensioning. In contrast to the proposed subthreshold methodology in this paper, the authors of [8] propose a subthreshold energy model to determine the optimum supply voltage for primarily minimizing the energy consumption.

For the interconnection of the subthreshold parts and above-threshold modules, resource-efficient and highly robust level shifters are required. Attempts have been made in the past to design efficient and robust level shifters, e.g., [9]. In [10], the concept of a high-speed level shifter using zero-threshold MOSFET was introduced. The proposed level shifter in [11] relies on a pull-up transistor stack whereas the stack does not depend on the input voltage. Here, the power consumption is reduced without any compromise on rise and fall delay. To combat with the delay, a short-circuit current limiting approach is proposed in [12]. The suggested level shifter in [13] is included in the proposed subthreshold library and allows for the implementation of multi-supply voltage designs. The concept is further utilized in [14] and [15].

The following Section II depicts the design methodology and gives an overview on the implemented cells. In Section III the characteristics of the subthreshold library are shown by synthesis and analysis of a benchmark circuit. We will come to a conclusion in Section IV.

II. Subthreshold Design Methodology

The proposed library has been designed using a commercial 65 nm low-power technology, which offers six different transistor types for PMOS and NMOS devices. The gate-oxide thickness can be chosen for either low-power (LP) or general purpose applications (GP). Besides two different gate-oxide options, the technology offers three transistor types with distinct threshold voltages (Low V_t (LVT), Standard V_t (SVT), High V_t (HVT)). To find a trade-off between low-power properties and achievable clock frequency, LP transistors with standard threshold voltage (SVT, $V_{th} = 450\,mV$) are chosen for the standard cell designs.

The design of standard cells for subthreshold operation is a challenging task, as the circuits become much more sensitive towards process variations, temperature, and supply voltage changes. Common approaches for dimensioning CMOS logic gates for subthreshold operation mainly focus on the DC transfer characteristics, e.g., the noise margin. Using robustness as a particular target function leads to an optimization towards a single design criteria and may result in over-pessimistic results. Accordingly, configurations with much better timing and power consumption, while diminishing noise margin to a little extent, are possibly omitted. This was taken into account by a multi-objective approach where besides noise margin

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(NM) energy consumption (E_{gate}) and propagation delay (t_{pd}) were additionally considered during optimization:

$$NM = min\{NM_H, NM_L\} \quad (1)$$
$$t_{pd} = max\{t_{pLH}, t_{pHL}\} \quad (2)$$
$$E_{gate} = E_{dyn} + E_{in} \quad (3)$$

During the optimization process the design parameters of PMOS and NMOS transistors are varied to find optimal trade-offs between these objectives. Since it has been proposed in [5], that a fixed gate length of 90 nm for both of the transistors is beneficial for robust cell behavior, the widths of NMOS (W_n) and PMOS (W_p) remain free parameters for the optimization. To account for the logic level degradation the transistor stack is set to a maximum of two which results in the lowest possible supply voltage limit [16].

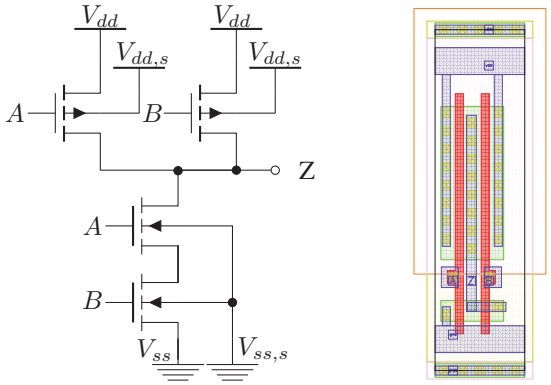
Since standard cell design for subthreshold operation typically results in transistors with a much bigger gate length and width, an area optimized standard cell frame is used and implemented as parametric cell (pcell). This frame allows for larger PMOS ($W_{p,max} = 2.3\,\mu m$, $W_{n,max} = 0.65\,\mu m$) designs without the need of transistor splitting. Using this standard cell frame, substrate- and well-tap cells can be separately connected ($V_{dd,s}$, $V_{ss,s}$) to exploit the benefits of backgate-biasing techniques.

A. Combinational Logic

The entire library is designed with a restriction on gates with a maximum degree of two. A multi-objective optimization approach has been performed for each cell for the minimum drive strength. To enhance the optimization of the synthesis tools, each logic function is implemented with different drive strengths. Gates with larger drive strengths are implemented by connecting the corresponding gates with the smallest drive strength in parallel, while they are fed with the same input. Standard CMOS design rules are used to realize the cells for AOI22, INV, NAND2 NOR2 and OAI22. The buffer (BUF) is implemented using a two stage implementation with each stage consisting of parallel connected inverters. To ease the layout design of the minority-3 gate (MIN3) and the (inverted) 2-to-1 multiplexer (MUXI2), schematic variants consisting of symmetric NMOS- and PMOS-parts are chosen. In case of the MIN3 gate, this variant is also known as mirrored gate implementation. The Table I shows the sizing of each cell with the corresponding Boolean functions.

TABLE I. DIMENSIONS OF COMBINATORIAL GATES

Gate	Boolean Function	W_n [µm]	W_p [µm]
AOI22	$\overline{(A \wedge B) \vee (C \wedge D)}$	0.250	2.050
BUF	A	0.265	2.050
INV	$\overline{A}$	0.265	2.050
MIN3	$\overline{(A \wedge B) \vee (B \wedge C) \vee (C \wedge A)}$	0.250	2.050
MUXI2	$\overline{(A \wedge \overline{S}) \vee (B \wedge S)}$	0.250	2.150
NAND2	$\overline{A \wedge B}$	0.230	1.710
NOR2	$\overline{A \vee B}$	0.240	2.150
OAI22	$\overline{(A \vee B) \wedge (C \vee D)}$	0.245	2.200

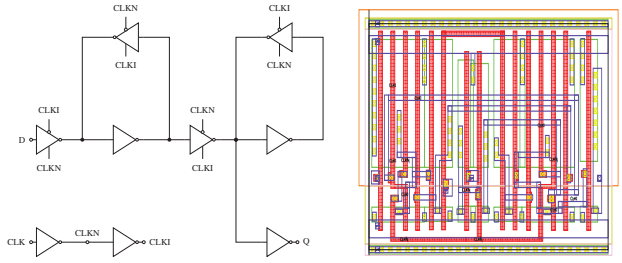


(a) Schematic (b) Layout

Fig. 1. The schematic and the layout of the NAND gate

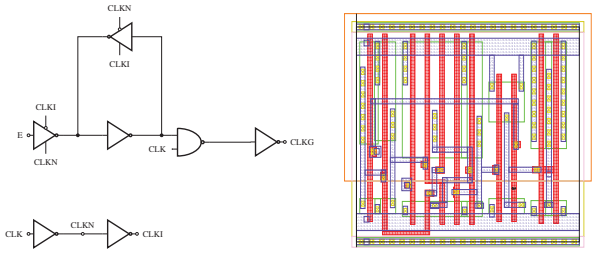
B. Sequential Logic

Sequential circuit elements, i.e., flip flops or memory cells, can be subdivided into static and dynamic elements. Dynamic flip-flops have low power loss over their static counterpart due to the lack of feedback elements and smaller delay times (clock to output delay). However, in subthreshold region because of low supply voltage, the stored dynamic charge is very low, resulting in corruption or loss due to noise effects, coupling with other systems, leakage currents, or radioactive radiation. In the proposed subthreshold library, C2MOS flip-flops are considered because of a very good combination of delay times, energy consumption, lower operating voltage limit and critical load. Again, due to benefits for subthreshold operation, static CMOS technology is used for the flip-flop realization (see Figure 2). Each of the two-part C2MOS gates can be regarded as an inverted 2-to-1 multiplexer. By means of two inverters, inverted and non-inverted clock signals (CLKI, CLKN) are generated locally from the input clock signal (CLK) to minimize the load for the clock tree. Additionally, optimization of the clock delay inside the flip-flop can be achieved easily by this approach. The output (Q) is buffered by a separate inverter. Therefore, the set-up and hold times of the flip-flops are maintained independent of the output load and higher drive strengths can be realized by increasing the inverters only. Overall, the flip-flop requires 26 transistors in this proposed C2MOS implementation.



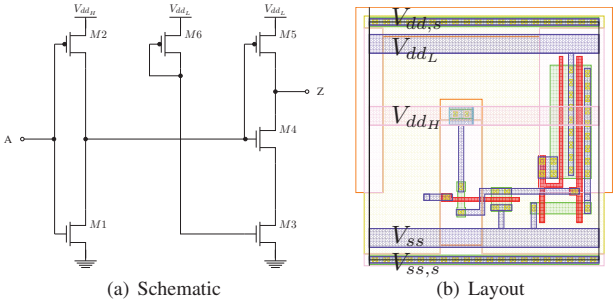
(a) Schematic (b) Layout

Fig. 2. Schematic and layout of the C2MOS flip-flop



(a) Schematic (b) Layout

Fig. 3. Schematic and layout of the clock-gating cell



(a) Schematic (b) Layout

Fig. 4. Schematic and layout of the down level shifter

C. Clock Tree Elements

Distribution of global clock signals to the sequential elements is necessary in synchronous digital circuits to ensure uniform time intervals. Multi-stage clock tree drivers are necessary as the ability of a single clock input is limited to drive a large number of flip-flops present in the circuit. The duty cycle of the clock is maintained at 50%. The clock buffer of this subthreshold library is implemented with a two-stage structure. The output stage of a clock buffer is composed of parallel connected inverters to implement different drive strengths. Likewise, the input stage is composed of parallel connected inverters. The number of inverters is chosen such that the ratio of total transistor width of output to input stage ranges between 2 and 3. The width of the PMOS transistors is optimized to match the delay times for rising and falling edges at a supply voltage of 300 mV. To aid synthesis tools during logic and clock tree optimization, 12 clock driver cells with different drive strengths are implemented. In addition, a special clock gating cell is implemented as depicted in Figure 3. To suppress glitches at the output of the clock gate, latch-based clock gate circuits are implemented. This ensures that the output signal can only be activated during the low phase of the clock, so that no faulty clock edges can occur. The dimensioning of the latch is identical to the latch cells of the logic library. However, the PMOS transistor widths of the output side NAND gates and inverters are optimized so that a symmetrical rising and falling behavior can be achieved with the clock drivers.

D. Level Shifter

Level shifter cells are needed for the logic level translation of signals between subthreshold and above threshold domains. For the 65 nm subthreshold library, the supply voltage is used as low as 250 mV and as high as 1.2 V with the temperature maintained at 25 °C. For this purpose, up- and down-level shifter are needed for up- and down-scaling of the logic level. The up-level shifter circuit and its function has already been discussed in [13] where static current flow is restricted by using a Wilson current mirror. That circuit shows good scaling behaviour of the switching time with the increase of supply voltage. The circuit diagram of the down-level shifter, which is optimized for 65 nm technology as well, is shown in Figure 4. The additional transistor M6 is added to avoid the direct connection between the supply voltage and the gates connected to M3.

E. Place and Route Cells

In addition to functional elements the subthreshold library contains cells that are needed by the place-and-route tools. These are so called decap cells, filler cells and tie-hi, tie-lo cells.

Decap cells provide large decoupling capacitances which are used for stabilization of the supply voltage. Practically, the gate capacitances of large-scale transistors are used as the capacity here. In contrast, filler cells do not contain any transistors. These cells are used to provide a complete structure of the n-well, doping regions, substrate and well contacts and the supply lines (power rail).

Tie-hi and tie-lo cells are used to apply constant logic levels to signal nets without a direct connection to the power and ground nets. Consequently, the use of tie cells increases the robustness of a digital circuit towards voltage spikes (e.g. caused by electrostatic discharge (ESD)) on the power and ground nets. The requirements for dimensioning tie cells are as follows. First, the output signal should quickly reach the stable final value after the startup of the circuit. Secondly, the output impedance should be low even after reaching the final voltage level. Also, the voltage level should be robust against external interference, e.g., due to capacitive coupling of neighboured nets. To meet those requirements maximum transistor widths are chosen for the PMOS and NMOS of the tie cells ($W_{p,max} = 2.3\,\mu m$, $W_{n,max} = 0.65\,\mu m$).

III. AES HARDWARE ACCELERATOR

Our subthreshold library contains 43 cells for logic synthesis. Since all cells are fully characterized from 250 mV to 1.2 V power estimations can be performed at gate-level. For the evaluation of the performance and energy efficiency, a hardware accelerator for the Advanced Encryption Standard (AES) is synthesized and analyzed with this library.

The architecture allows the de- and encryption of 128 bit data blocks with either 128, 192 or 256 bit AES keys and can be integrated into microprocessor designs. A 32 bit bus-interface is utilized for this purpose. Using this interface, the encryption key is split up into 32 bit chunks and transferred to the AES core. Once the AES core is set up with the proper encryption key 32 bit data-block chunks are transferred and encoded by the core. To prove the functionality of the AES core, it has been previously integrated in a chip prototype of the CoreVA processor [17].

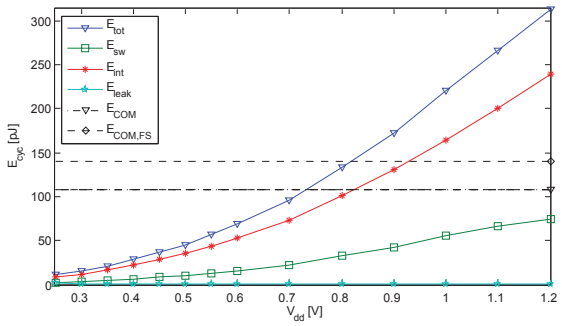


Fig. 5. Energy per cycle measurement of the AES benchmark circuit (simulated)

The AES hardware accelerator has been synthesized for supply voltages from 250 mV to 1.2 V resulting in a maximum clock-frequency between 82.5 kHz (at 250mV) and 478.5 MHz (at 1.2 V). Figure 5 shows an estimation of the energy per clock-cycle for the different voltage levels. In addition to the total energy per clock cycle E_{tot} the dynamic (E_{int}, E_{sw}) and static portions (E_{leak}) are depicted. The minimum point of energy with a total energy consumption of 11.7 pJ per clock cycle can be observed at 250 mV. A comparison of the subthreshold library with a commercial 65 nm bulk library can only be done at nominal voltage (1.2 V), since the commercial cells (LP, SVT transistors) are only characterized for that voltage level. Furthermore, to allow for a fair comparison, the amount of cells can be reduced to the same set of cells that are present in the subthreshold library. Comparing the results for the full set ($E_{STM,FS}$) of cells with the minimum number (E_{STM}) may give an indication of performance gain possible by implementing subthreshold standard cell libraries with thousands of different elements. Synthesis with the reduced set of cells in the commercial library results in a maximum clock frequency of 675.7 MHz and a total energy (E_{COM}) of 108.3 pJ per clock cycle. In contrast, utilization of all available commercial cells leads to a maximum clock frequency of 1.39 GHz and a total energy of 140.1 pJ per cycle. Regarding the subthreshold implementations, energy savings by a factor of 9.25 can be achieved while operating at 250 mV. It has been shown in [17], that a microprocessor built with the same commercial cells was fully operational down to a supply voltage of 200 mV.

IV. Conclusion

In this paper an overview of a robust and energy-efficient standard cell library has been given. In total 62 gates have been designed and fully characterized for voltages between 250 mV and 1.2 V. Besides 43 standard-logic elements, we implemented 19 additional cells, including level shifter cells for multi-supply voltage designs and clock-tree elements as well as place and route cells. Using a multi-objective optimization approach, each cell is tuned for robustness and energy-efficiency. The evaluation of an AES hardware accelerator circuit has shown, that the energy consumption can be reduced by a factor of 9.25 while operating at subthreshold mode. Furthermore, the maturity of the proposed subthreshold library has also been shown in [17], where samples of the implemented processor design were fully operational at 200 mV. Future works towards ultra-low power design will cover 28 nm fully depleted silicon on insulator (FD-SOI) technology and the exploitation of back-gate biasing techniques.

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