Advanced Node DTCO in the EUV Era

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***Abstract*—**EUV lithography has finally made it into high-volume manufacturing and this has reset the approach to leading-edge Design Technology Co-Optimization. ArF immersion lithography multi-pass patterning was on course to push the technology design rules to be so restrictive, that design optimization would become a clear second priority. EUV lithography restores the balance between design optimization for performance, power, and area scale, along with technology optimization for yield and cost. However, due to the late introduction of EUV, this balance may be short-lived, and further rapid improvement in EUV lithography capability is highly anticipated.

I. Introduction

The simple premise of Moore's Law is that the transistor count doubles every time a particular chip manufacturer deemed it worthwhile to shrink the technology [1]. The pace at which this occurred was determined by competition amongst the chip manufacturers and included a consideration of enhanced chip performance and/or functionality, versus the cost of shrinking the technology. As shown in Fig. 1, the pace was incredibly fast in the era where there were no inherent materials or lithography limitations, with a steady 0.7x pitch dimension scale factor in x- and y-directions every 2 years. Cu interconnects, low-k dielectrics, transistor strain engineering, replacement high-k metal gate, and 3-D FinFET overcame materials limitations and allowed 0.7x pitch scale factor to continue [2-4].

Lithography limitations came to the forefront as 13.5nm wavelength EUV technology, the successor to 193nm immersion lithography, continued to be delayed. This forced the industry to heavily co-optimize the technology definition along with the design requirements, in order to squeeze as much design IP block performance/power, area, and cost scaling as possible, with as little pitch and dimensional scaling as possible. This Design-Technology Co-Optimization era of Moore's Law has been very fruitful [5,6] and the methodologies developed in this era will not change significantly with the introduction of EUV lithography. This is partially due to the very late introduction of EUV, i.e. it came too late to revert back to the "simple scaling" era practices. It is also due to the extreme complexity of modern SoCs which are upgraded on a yearly cadence. This favors a high level of pattern predictability and a reduction of EDA complexity.

II. Immersion Multi-Patterning DTCO

The essence of the DTCO process is shown in Fig. 2. To continue on the terminology introduced in Fig. 1, the "simple scaling" era was dominated by process scaling capability. Functional designs at the cell level and block level were simply shrunk, if the design rules were able to scale. In the "materials scaling" era, Cu, low-k, strained silicon, RMG, and FinFET were technology innovations introduced, with little impact on design rule scaling. Design rule scaling was still dominated by lithography capability. Fig. 3 shows Intel's 22FFL technology which features strained silicon, high-k metal gate, and FinFET innovations of the materials scaling era, but with a substantially similar bi-directional design style at M1 that can be traced back through multiple decades of CMOS technologies [7]. It wasn't until lithography hit a wall with 193nm immersion that technology innovations had a large impact on the actual cell-level design style. Fig. 4 shows the decomposition of a bi-directional M1 layer into unidirectional M0 and M1 layers for the first time in Intel 14nm technology. Although this decomposition required an additional metal level to complete the standard cell, when properly optimized, it could provide for extra ordinary cell height scaling. This accelerated cell height scaling so that the cell height would be below the pitch scale factor. This "track-height scaling", where in addition to pitch scale, the number of metal tracks used is simultaneously reduced, became a key element of DTCO to maximize block-level scaling with minimum pitch scale [5,8]. With the addition of contact over active gate technology (COAG) in Intel 10nm, the additional metal level would largely be available for routing and power distribution, as shown in Fig. 5. The COAG could further reduce cell height and cell width for increased overall gate density, and a higher density of available M1 tracks could now be used to improve power distribution and increase routed gate density. As shown in Fig. 6, Intel 10nm leads in overall gate density amongst the 193i-based technologies [9,10].

III. The EUV Era

EUV has been on the lithography roadmap since the clear limits of 193nm immersion lithography were recognized, and the 157nm light source was removed from the roadmap because it required substantial new infrastructure, without enough gain in resolution. EUV also required substantial new infrastructure, but EUV has higher gains in resolution and had a potential to scale further with improved N.A., as shown in Fig. 7. For most manufacturers, the desired intercept for EUV would have been at the 32nm node, where the required poly gate end-to-end could no longer be achieved by a single pass of 193nm

immersion lithography. However, due to constant delays in source power development, materials and infrastructure development, EUV had not been viable and arguably is still not ideal for low-cost high-volume manufacturing as of today.

Despite these ongoing challenges, the EUV era has been ushered in with a fury, and EUV is a welcomed addition to the DTCO toolkit. The strains of multi-pass immersion patterning technologies were at the breaking point in terms of mask count, cycle time, multi-pass metrology complexity, edge placement error compromise, process complexity, and EDA complexity. Essentially, the cost, complexity, and risks of multi-pass patterning caught up to, and exceeded, the high cost of EUV patterning and risks of an immature EUV infrastructure. Intel technology will benefit from a 36% mask count reduction with the introduction of EUV, similar to immersion to EUV mask count reductions reported in [11,12]. Fewer masks per layer translates to much reduced process complexity, tighter process capability, and EDA simplification. Instead of making design compromises due to limits imposed by multi-patterning, EUV patterning is allowing for continued scaling of IP block and SoC performance, power, and area through a robust DTCO process.

IV. EUV Co-Optimization

EUV was introduced about five technology generations too late. This ensures that EUV will not substantially change the way design and technology are co-optimized. There are two reasons for this, the first is track-height scaling, and the second is fundamental EUV capability.

Track-height scaling has been such a large component of the overall DTCO enhancement, it is impossible to go backwards without an overscale of the pitches. Track height scaling was largely enabled by Intel's introduction of unidirectional M0/M1 and COAG. The unidirectional nature places only end-to-end constraints on the design rules, whereas a bi-directional design places both end-to-end and end-to-side constraints, as shown schematically in Fig. 8. It is these end-to-side constraints that tend to limit the track height. So, this would imply that even with superior EUV patterning capability, standard cell designs will not revert to the bi-directional layout style.

This trend is also driven by EUV capability. Being five generations too late, EUV with 0.33 N.A. is being introduced at the tail end of its resolution capability. Cell-level line pitches and via pitches at the time of EUV 0.33 N.A. introduction, are already at or near single pattern limits. This further favors the constraints for the technology optimization to be largely built around uni-directional patterns. To push EUV technology with bi-directional patterns at the limits of resolution would not be a wise decision.

Single pattern EUV, however, does re-introduce the capability to extend patterns, upsize patterns, and jog patterns with much greater ease from a process and EDA standpoint. Examples of these patterns are shown in Fig. 9. These patterns may be used sparingly at the cell level and may be particularly useful at the metal routing levels. Historic trends to limit fine pitch metal layers due to both the process and EDA complexity of heavily multipatterned layers must be re-evaluated as EUV technology matures further. In this sense, EUV is ideally suited to tackle the industry-wide issue of much increased metal and via resistance. EUV patterning allows flexibility of metal and via patterns from the cell level up into the larger signal levels, where well-exercised ArF immersion lithography-based design optimization takes over.

V. Second Generation EUV DTCO

Much of the DTCO work around the second generation of EUV revolved around which layers will use single patterned EUV and which layers are better to double or even multi-pattern. The decisions were complicated by rapid improvements being developed in terms of EUV materials, tooling, and infrastructure, ultimately leading to moving targets for resolution and cost. These decisions directly impact the design, since multi-patterning re-introduces restrictions and EDA complexity. These decisions must holistically encompass both the technology capability, and wise choices of which layers to deploy a particular complexity of EUV, in order to maximize the PPA benefit. Shown in Fig. 10-11 are DTCO studies of first vs. second generation EUV technology. When properly optimized, the flexibility of EUV patterning has a substantial impact on IP block area and performance.

VI. Summary and Conclusions

The EUV scaling era is an exciting time for both designers and technologists. Many of the roadblocks we have collectively hit with multi-patterned technologies can now be lifted, and the design and technology can be co-optimized for maximum PPA benefit. However, because EUV was introduced so late, the next generations of 0.33NA EUV-based technologies will struggle again with the negative multi-patterning tradeoffs until the 0.55NA EUV tools currently in development are available for production. With the benefit of hindsight, a double-patterned EUV layer seems preferable to past multi-patterned immersion layers involving 5-6 masks, but we need to keep the development of 0.55NA tools on track to avoid facing the same many-mask situation with 0.33NA EUV.

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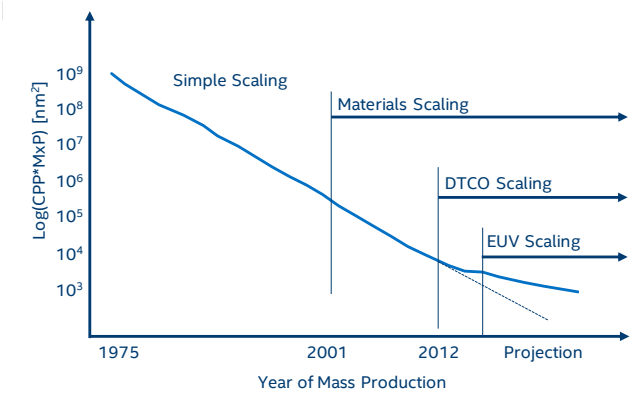


Fig. 1. Technology contacted poly pitch * minimum metal pitch scaling versus year of mass production.

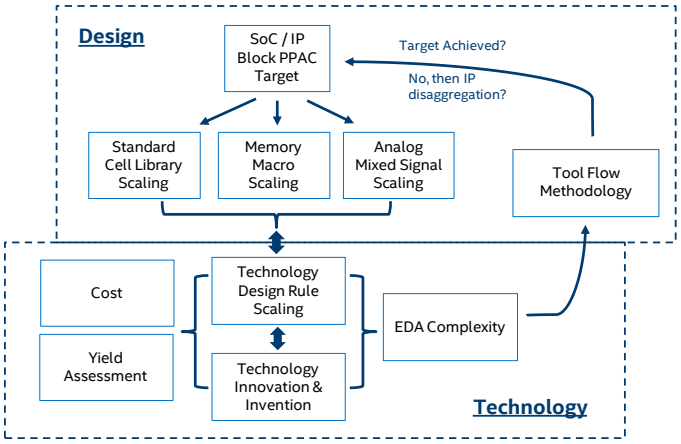
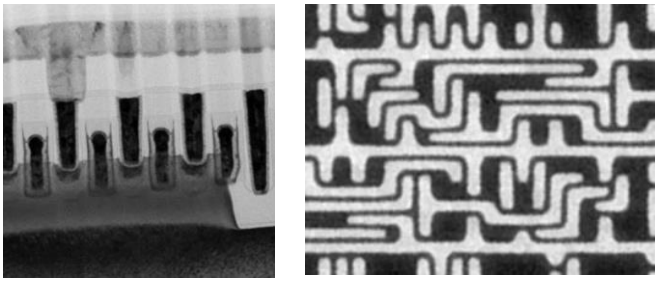
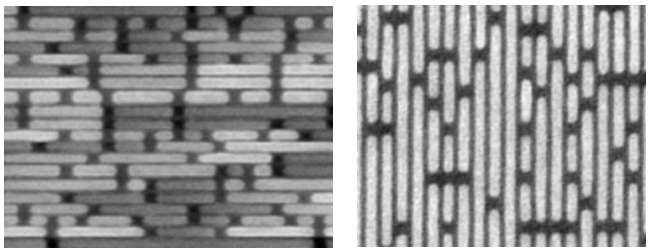


Fig. 2. Design Technology Co-Optimization process.



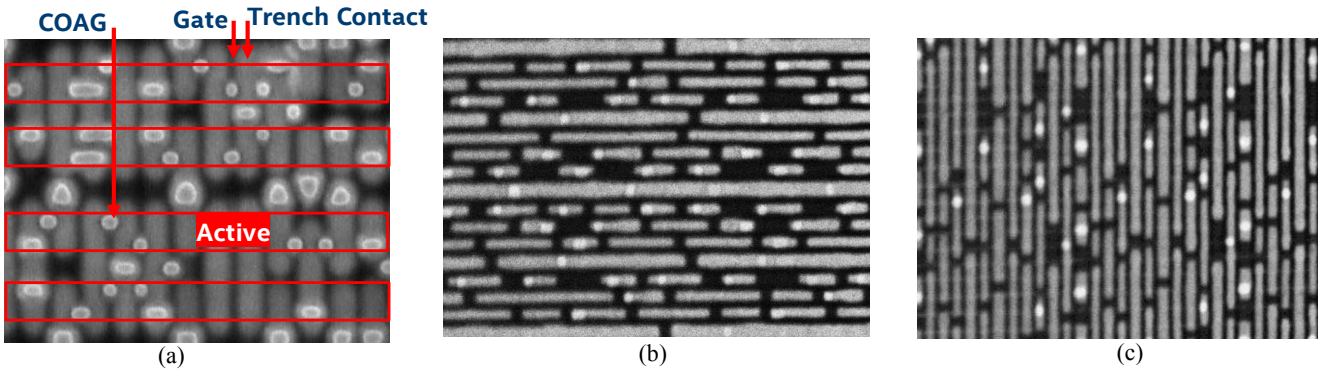
(a) (b)

Fig. 3. Intel 22FFL technology featuring (a) Cu interconnects, eSiGe, HKMG, and FinFET and (b) bi-directional M1.



(a) (b)

Fig. 4. Intel 14nm technology high-density standard cells featuring (a) uni-directional M0 and (b) uni-directional M1.



(a) (b) (c)

Fig. 5. Intel 10nm technology ultra-high-density standard cells featuring (a) contact over active gate (COAG), (b) uni-directional M0 and (c) uni-directional M1, with most tracks available for power and routing.

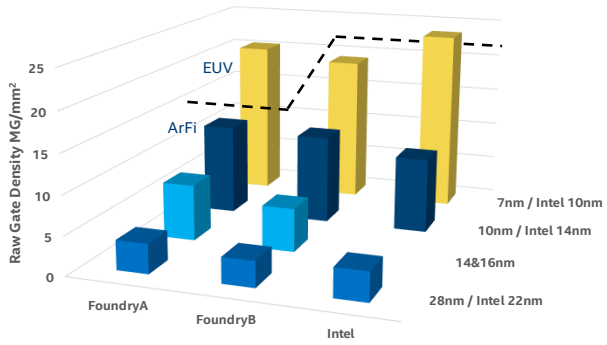


Fig. 6. Weighted simple, complex, and sequential logic gate density vs. technology node name.

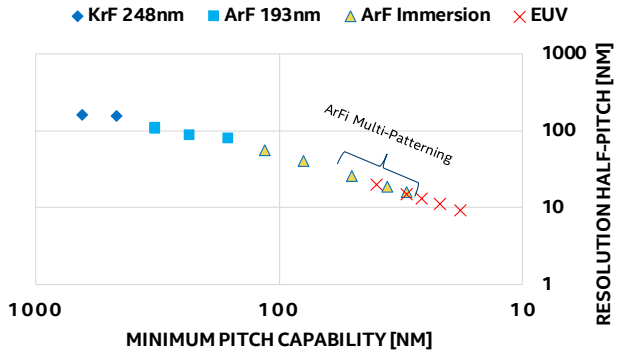


Fig. 7. Lithography technique resolution vs. minimum technology pitch capability, based on Rayleigh's equation. N.A. and k_1 improvement steps are shown within each wavelength.

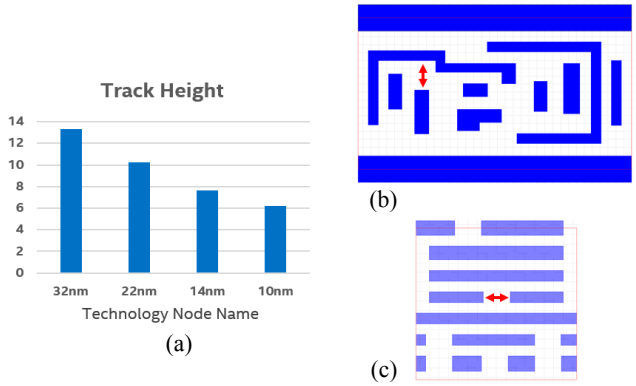


Fig. 8. (a) Intel track height scaling vs. technology node. Schematic showing (b) bi-directional vs. (c) uni-directional layout design rule pinch points.

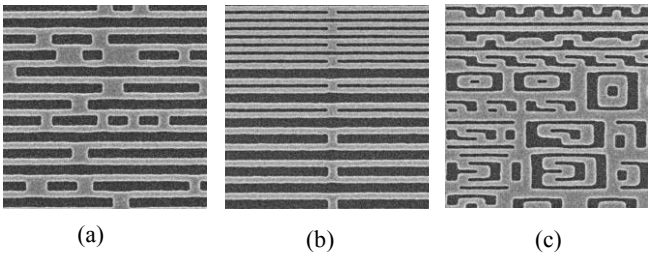


Fig. 9. EUV patterning showing (a) tight 1-D patterning, (b) variable line/space, and (c) 1.5-D patterning capability.

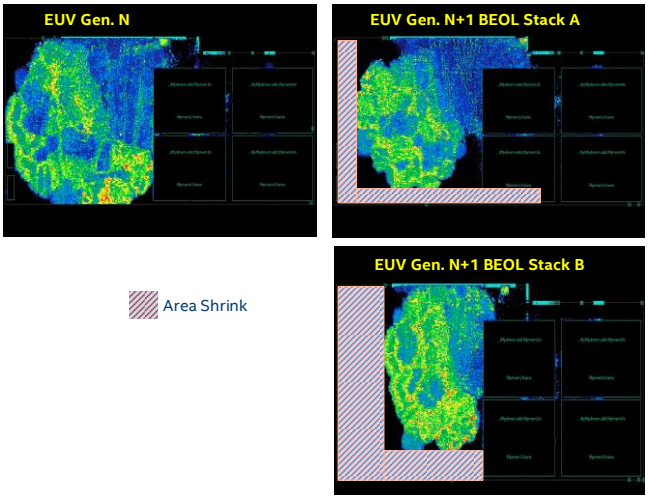
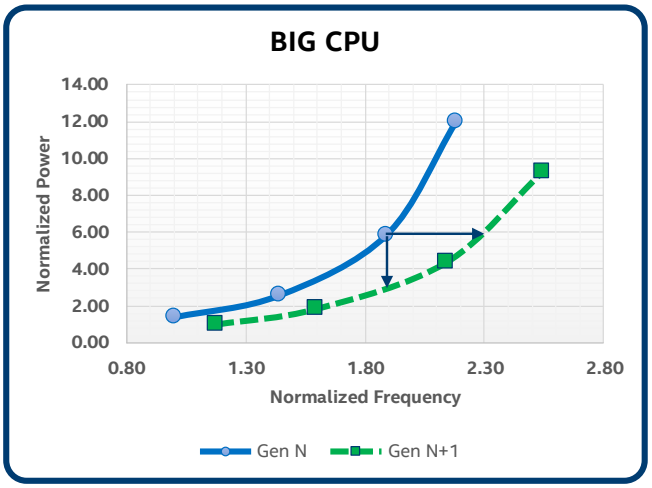


Fig. 10. DTCO study showing area scaling of 2nd generation EUV technology versus different EUV BEOL optimizations.



PPA Metrics	Gen N	Gen N+1
Iso-power frequency	1x	1.25x
Iso-frequency Power	1x	0.55x
Leakage	1x	0.39x
Area	1x	0.69x

Fig. 11. DTCO study showing performance power characteristics of 2nd generation EUV technology.