Benefit Model of Virtual Metrology and Integrating AVM into MES

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Abstract-Frequent monitoring in both tool and process is required to detect the quality issue early so as to improve the process stability of semiconductor manufacturing. However, more tool and process monitoring means more metrology operation cost and longer cycle time. Recently, a promising technology denoted virtual metrology (VM) has bloomed. VM can convert sampling inspection with metrology delay into real-time and online total inspection. Therefore, VM has now been designated by International SEMATECH Manufacturing Initiative and International Technology Road Map for Semiconductors as one of the focus areas for the next generation factory realization road map of the semiconductor industry. The authors have developed the so-called automatic virtual metrology (AVM) system to implement and deploy the VM operations automatically. The purpose of this paper is to develop a business model to measure the profitability of VM based on in-depth manufacturing practices and metrology operations required for semiconductor manufacturing. This paper also proposes a novel manufacturing system that integrates AVM into the manufacturing execution system (MES). The interfaces among AVM, other MES components, and runto-run (R2R) modules in the novel manufacturing system are also defined such that the total quality inspection system can be achieved and the R2R capability can be migrated from lot-to-lot control to wafer-to-wafer control.

Index Terms—Automatic virtual metrology (AVM), manufacturing execution system (MES), run-to-run (R2R) control, wafer-to-wafer (W2W) control.

I. INTRODUCTION

SINCE SHEWHART introduced the statistical process control (SPC) chart in Bell Laboratories' technical memorandum in 1924, SPC has been widely developed and de-

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ployed into industry [1]. SPC is especially important for high-technology industry with a complicated production flow, long process time, and high production cost.

Semiconductor manufacturing also heavily relies on SPC for quality monitoring because it has a very complicated production flow (a 65 nm product has 36+ layers, 500+ operation steps), long process time (a 65 nm product may have 50+ days production cycle time), and high cost (300 mm wafer with 65 nm technology costs U.S. \$3000+, on average) [2], [3]. There are more than 14 000 SPC charts created in production lines to monitor process status through production/test wafers in a most advanced 300 mm semiconductor manufacturing facility.

Current tool monitoring in semiconductor production through SPC is performed during the time when test wafers are processed with the production tools and measured by metrology tools, the inspection items are such as etching rate, stress, and so on. However, the monitoring of semiconductor tools can only be performed periodically due to the high cost of metrology tools and extra cycle time of measurement operation [4]. Therefore, effective sampling strategies to balance the capital investment and quality assurance have been broadly discussed in [2]–[7]. During the past decade, a technology denoted fault detection and classification (FDC) has also been widely applied for fault detection monitoring of semiconductor tools [31].

In addition to using test wafers to monitor process tools' health, on-line monitoring in production wafers is required for improving wafer fabrication quality [5], which is executed by monitoring production wafers under processing through main process tools—lithograph, etch, thin film, chemical mechanical polishing (CMP), and so on. Also, several metrology tools are required to assess the wafer quality, including overlay, critical dimension (CD), and particles.

Effective monitoring metrology could reduce the unnecessary wafer scrap. However, this traditional quality assurance requires millions of investment in a 300 mm fab with advanced process technologies because the routine monitoring requires plenty of metrology tools and utilizes a lot of test wafers. In general, 15–30% of daily production transaction is used by test-wafers operation for off-line tool monitoring, and the consumption of these test wafers increases the operation cost [30]. Besides, on-line process monitoring for the quality assurance of production wafers needs to complete the processes in main process tools and measurements in metrology tools;

and these on-line metrology operations on production wafers will definitely prolong the production cycle time and cause process tool's overall-equipment-effectiveness lost.

Optimizing metrology operation has been discussed to support a cost effective and efficient metrology operation in a 300 mm fab [5]–[9]. Butler and Woods [9] analyzed constraints of tool capacity and quality to obtain the optimal model of best sampling for monitoring. Several researchers proposed new metrology strategies and in-situ metrology to improve overall fab productivity [5], [6]. No matter how efficient a sampling rule or a new metrology hardware technology is developed, metrology operation with test wafers and metrology tools are still required to assure tool performance and quality of production wafers. It seems that there is no better alternative to completely eliminate metrology operation from wafer fabrication.

Recently, a promising technology denoted virtual metrology (VM) has bloomed [15]. VM can provide users with total metrology information of all wafers in a FOUP by merely measuring a single wafer in the same FOUP [27]. Moreover, VM can convert sampling inspection with metrology delay into real-time and on-line total inspection. Therefore, International SEMATECH Manufacturing Initiative (ISMI) added VM into its next generation factory realization Road map of the semi-conductor industry [16]. International Technology Road Map for Semiconductors (ITRS) also designated VM as one of the focus areas on Factory Information and Control Systems and advanced process control (APC) [10], [22].

Moyne [23] listed the key issues that must be addressed in developing an industry-wide VM solution. In fact, those key issues have been addressed by the authors recently. The key issues and their resolutions include the following.

- The VM solution must be adaptive → Resolved by the dual-phase VM scheme [18].
- 2) The VM solution must incorporate VM data quality prediction → Resolved by the reliance index (RI) [19].
- 3) The VM methods need to be improved for determining the fault detection factors that are the best VM predictors → Resolved by the global similarity index (GSI) and individual similarity index (ISI) [19].
- 4) The VM solution must be developed to be re-usable \rightarrow Resolved by the automatic model refreshing [20].

The RI/GSI/ISI and dual-phase VM schemes have been successfully verified in Taiwan Semiconductor Manufacturing Company, Ltd., Hsinchu, Taiwan [19], [26]. All of the resolutions [18]–[20] mentioned above are consolidated and become the automatic virtual metrology (AVM) system that has been successfully deployed in Chi Mei Optoelectronics, Ltd., Tainan, Taiwan [20], [26]. Therefore, the AVM system is mature enough and ready to be integrated into the manufacturing execution system (MES).

The purpose of this paper is to develop a business model to evaluate the profitability of VM based on in-depth manufacturing practices and metrology operations required in semiconductor manufacturing. This paper also proposes a novel manufacturing system by integrating AVM into the MES to convert sampling inspection with metrology delay into real-time and on-line total inspection. The interfaces

among AVM, other MES components, and run-to-run (R2R) controllers are also defined. This integration will provide a new approach of quality assurance in the semiconductor industry with minimum metrology cost and real-time and on-line total quality inspection in all production lines. Also, the feeding of the full set of quality data to R2R controllers will enable more precise wafer-to-wafer (W2W) process control, hence improving the product yield and quality control.

The rest of this paper is organized as follows. Section II summarizes the semiconductor metrology operation domain knowledge and the necessity to apply virtual metrology. Section III provides a business model to quantify the benefit of VM in semiconductor manufacturing. Section IV introduces the AVM system. Section V explains the procedure of integrating AVM into the MES. Section VI elaborates the operating scenarios of applying AVM to support total quality inspection and W2W control. Finally, this paper ends with a summary and conclusions.

II. NECESSITY OF APPLYING VIRTUAL METROLOGY

This section describes the needs for physical metrology operation in semiconductor manufacturing and the necessity of reducing physical metrology with VM for decreasing manufacturing cost. Fig. 1 describes the current physical metrology operating scenarios for supporting quality assurance of semiconductor manufacturing. It includes two monitoring operations—off-line (tool) monitoring and on-line (process) monitoring.

Observing the upper portion of Fig. 1, a continuous process of the normal wafer fabrication is requested to pause for off-line tool quality monitoring; and the fabrication process cannot be resumed until the feedback of metrology data and the quality data of process tool being within the control specification. This off-line tool monitoring design is for the operation steps whose performance could not be measured in production wafers, for example, etching rate. The interruption of production for off-line tool monitoring will cause the productivity loss of the tool. Also, this off-line monitoring requires test wafers (raw materials) and their corresponding preparation that need extra cost. Furthermore, the off-line tool monitoring will prolong the cycle time of wafer fabrication.

The on-line production wafer quality monitoring is depicted in the lower portion of Fig. 1. In daily operation of semi-conductor manufacturing, the sampling plan will define the sampling rule to choose production wafers for metrology operation to do quality inspection; meanwhile, normal production operation will continue in process tools. The metrology data (such as CD) of production wafers will be fed into SPC for quality inspection and the data will be sent to the R2R control system for process tuning. It is noted that the cycle time for production will be increased and some other quality issues in the manufacturing process might be incurred because extra manipulation is needed for this physical metrology operation. In the meantime, on-line fault detection monitoring of tools may also be applied by a FDC system [31].

As mentioned above, metrology operation is essential for quality inspection and control of semiconductor manufacturing. Based on actual transaction volume in a MES of a 300 mm fab, 40–45% of daily manufacturing operation is

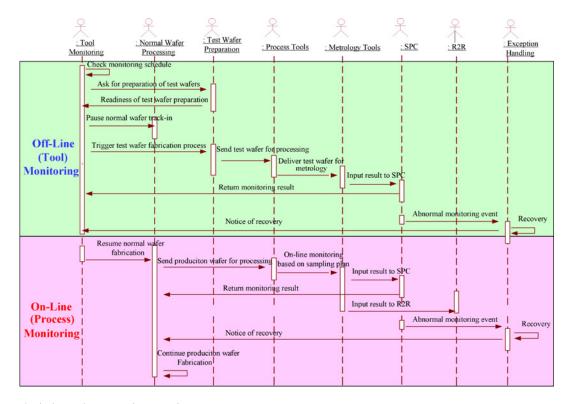


Fig. 1. Current physical metrology operating scenarios.

for metrology operation [30]. Maintaining all the essential metrology operation requires investment of metrology tools, extra operation in process tools and metrology tools, extra test-wafer cost, and so on.

VM is a method to conjecture manufacturing quality of a process tool based on data sensed from the process tool and without physical metrology operation. VM can provide users with total metrology information of all wafers in a FOUP by merely measuring a single wafer in the same FOUP [27]. Moreover, VM can convert sampling inspection with metrology delay into real-time and on-line total inspection [15], [18], [20], [23]. Therefore, the promising approach is to apply VM: to reduce the cost of utilizing real metrology (and its related material handling operation) while achieving the goal of maintaining all the essential metrology operation.

Fig. 2 shows the tool-monitoring and process-monitoring scenarios without and with VM. For the as-is (without VM) portion, the off-line tool monitoring with test wafers and on-line process monitoring with sampling production wafers are performed according to the physical metrology operating scenarios depicted in Fig. 1. For the to-be (with VM) portion, both process monitoring and tool monitoring are executed simultaneously with sampling production wafers by virtue of VM while actual sampling metrology (as shown in the middle of the to-be figure) is only needed for re-training the VM models. The to-be model can also provide total inspection of all wafers owing to VM. The to-be model with VM will improve the overall operation performance in terms of quality assurance, cycle time, and productivity so as to reduce the total manufacturing cost. The benefit for applying VM will be evaluated in Section III.

III. BENEFITS OF VIRTUAL METROLOGY

The driving force for semiconductor-manufacturing improvement is the cost. ISMI set the next generation-fab (NGF) target for 2012 centered at 50% cycle time reduction and 30% cost reduction so as to keep up with Moore's law [16]. ISMI also designated VM as one of the seven next generation realization projects [16], [17]. In [17], a DRAM 12 inch fab model example with capacity of 30 K wafer starts plus 4.5 K non production wafers (i.e., test wafers) per month is utilized. This model is applied with ISMI's 45 nm generic logic process flow that has 658 process steps, 36 litho masks, and 268 metrology steps. The metrology steps are mapped as easy/medium/difficult for VM implementation and optimistic/realistic/pessimistic scenarios are designed respectively for VM penetration. As a result, the VM replacement rates were proposed in [17] as follows.

- [Easy] Film thickness measurements: 50% replacement rate because VM can be easily conjectured from the current tool's process data.
- [Medium] Critical dimension measurements: 20% replacement rate because VM needs the current tool's process data and pre-process metrology data to be accurately predicted.
- 3) [Difficult] Defect inspections and scans: 2% replacement rate because it is difficult to predict the defects induced by the current tool and from the process integration by applying VM technology.

The metrology-tool costs of film thickness, critical dimension, and defect inspection were proposed to be U.S. \$1M, 2M, and 1M, respectively [17]. As for the costs to set up and maintain VM per year were U.S. \$150K for [Easy], \$200K for

[Medium], and \$300K for [Difficult] [17]. It also proposed that each WIP move requires 5 min [17].

Based upon the assumptions listed above and realistic scenario analysis done by Stark [17], this model yields 8.55% cycle time reduction and U.S. \$21M capex reduction, with additional cost of U.S. \$2.7M per year to maintain VM [17].

To evaluate the overall benefit of VM, the VM benefit equation of semiconductor manufacturing operation is proposed in (1)

Benefit =
$$W_O * \left[\frac{1}{1 - (\Delta CT_P + \Delta CT_M)} - 1 \right] * (1 + \Delta Y)$$

 $* (P - C) + \Delta Cost_M + \Delta Cost_T - Cost_V - Cost_O$ (1)

where

W_O number of wafer output per year;

ΔCT_P¹ % cycle time reduction due to VM allowing production wafers to skip metrology sampling steps in the on-line process monitoring flow;

ΔCT_M % cycle time reduction due to VM allowing less test wafers used in the off-line tool monitoring process and more intelligent dynamic metrology and process schemes;

ΔY % enhancement due to improvement on process capability (from VM supporting APC), reduction in scrap, and so forth;

P average selling price per 300 mm production wafer;

C average production cost per 300 mm production wafer;

 $\Delta Cost_M$ cost saving of test wafers per year when applying VM in all production lines;

 $\Delta Cost_T \quad \text{ capex reduction per year when applying } \\ VM \text{ in all production lines;}$

Cost_V additional cost per year to maintain VM;
Cost_Q additional cost per year due to false alarms and missed detections caused by VM.

Observing (1), ΔCT_P for cycle-time reduction, $\Delta Cost_T$ for capex reduction, and $Cost_V$ for VM maintenance can be derived from Stark's results [17]. As for the other factors in (1), they are developed by the authors. Among them, ΔCT_M is due to test-wafers reduction as well as more intelligent dynamic metrology and process schemes; ΔY considers % enhancement due to improvement on process capability (VM supporting APC), reduction in scrap, and so forth; $\Delta Cost_M$ is due to test-wafers reduction; and $Cost_Q$ represents additional cost per year due to false alarms and missed detections, which are resulted from the fact that those VM values are not as accurate as their corresponding actual metrology values.

Utilizing the data of ISMI's fab model [17], we have $W_O = 30K*12 = 360K$ and $\Delta CT_P = 8.55\%$. With five-year apportionment, $\Delta Cost_T = 21M/5 = U.S.$ \$4.2M. And, $Cost_V = U.S.$ \$2.7M. The current average market prices are P = U.S. \$4000 and C = U.S. \$2400.

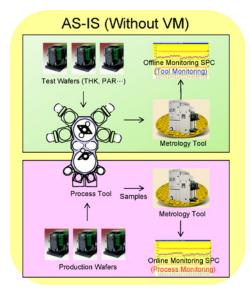
In this fab model, the test wafers to production wafers' ratio is $4.5\,\mathrm{K}/30\,\mathrm{K} = 6.7\%$. Therefore, $\Delta\mathrm{CT_M}$ can have about 1% cycle time reduction. In this 1% reduction, 0.67% is due to VM allowing less test wafers used in the off-line tool monitoring processes and off-line monitoring requires less operating steps than those of on-line monitoring; and the other 0.33% is due to VM enabling more intelligent dynamic metrology and process schemes to further reduce cycle time. As for $\Delta\mathrm{Cost_M}$, the average cost of test wafers is about U.S. \$40 per wafer because test wafers may be recycled; moreover, a half of all the test wafers are assumed to be saved thanks to VM, then $\Delta\mathrm{Cost_M} = 40~*4.5\mathrm{K}~*~12~*~0.5 = \mathrm{U.S.}~$1080\mathrm{K}.$

Moyne pointed out in [23] that the VM solution must incorporate VM data quality prediction when the W2W control consumes the VM data. Khan et al. studied this VM quality issue in [24] and [25]. Cheng et al. [19] also proposed a RI to gauge the reliability level of VM. Furthermore, Cheng et al. presented an APC system and method utilizing VM with RI in [29]. As demonstrated in [29], RI can be utilized to tune the R2R controller gain, α , such that R2R control errors due to VM variability can be compensated. In fact, α is an exponentially weighted moving average (EWMA) coefficient ranged between 0 and 1 [32]. Assume that α 1 represents the EWMA coefficient when actual metrology value is adopted as the feedback of the R2R controller and α 2 stands for the EWMA coefficient if VM value is applied. As stated in [32], α 2 should depend on the quality or reliability of VM and $\alpha 2 < \alpha 1$. Because the value of RI is a good VM reliability evaluation index and 0 < RI < 1, higher RI means better VM reliability [19], we can then naturally set $\alpha 2 = RI \times \alpha 1$ [29]. The details of R2R control utilizing VM with RI will be the subject of future publication.

ΔY percentage enhancement due to improvement on process capability (from VM supporting APC), reduction in scrap, and so forth is estimated below. Assume that the equivalent overall process capability improves from 1.000 to 1.333, its corresponding defect rate can then be reduced from 0.27% to 0.0063% [28]. Therefore, the improvement (ΔY) yields 0.2637%. Note that the improvement (ΔY) mentioned here merely counts for defect-rate reduction. In fact, improvement on process capability can also increase the yield of high-quality product. Therefore, beyond the defectrate reduction, the benefit of process-capability improvement (from VM supporting APC) would be much higher when considering the price difference for different quality categories due to high-quality yield improvement. This portion will not be addressed here because it is mostly treated as the benefit of applying APC.

Additional cost per year due to handling VM false alarms and missed detections (Cost_Q) is considered as follows. Cost_Q is mainly caused by those VM values which are not as accurate as their corresponding actual metrology values. This

 $^{^{1}}$ The benefit from ΔCT_{P} generally only applies to critical process, i.e., processes for which cycle time will impact overall line cycle time.



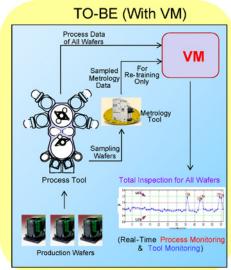


Fig. 2. Tool and process monitorings without and with VM.

accuracy issue may cause false alarms and missed detections as shown in Fig. 3.

Before determining the false alarm rate, the required VM solution accuracy should be defined first. In general, the acceptable-measurement-error bound of actual metrology is 10% of the tolerance spec. Therefore, in this paper, the ideal 10% error bound is selected as the accuracy requirement when VM is applied. Assume that the process capability is 1.333, the tolerance spec is then $4\sigma[28]$. As shown in Fig. 3, if the value of the actual metrology is within the $(0.4\sigma = 4\sigma - 3.6\sigma)$ 10% error bound, then its corresponding VM value may cause a false alarm. This $(3.6\sigma \sim 4\sigma)$ 10% error bound is equivalent to 0.02549%. The average annual salary of an engineer is about U.S. \$40K, then the hourly pay is 40000/(12 * 22 *8) = 18.94. It generally requires an hour for an engineer to handle an out-of-control action plan (OCAP) from a VM alarm report. On average, there are totally 30 VM operations for a generic logic process flow. Therefore, the false-alarm portion of $Cost_O = 360\,000 * 0.02549\% * 18.94 * 30 = U.S.$ \$52 140.

On the other hand, if the value of the actual metrology is within the other $(0.4\sigma=4.4\sigma-4\sigma)$ 10% error bound, then its corresponding VM value may cause a missed detection. This $(4\sigma\sim4.4\sigma)$ 10% error bound is equivalent to 0.00525%. As a result, the missed-detection portion of $Cost_Q=360\,000*0.00525\%*2400=U.S.$45\,360$.

In fact, VM solution accuracy depends on the prediction algorithm utilized [26], on-line model refreshing method applied [18], process and metrology data quality evaluation approaches adopted [20], and so on. It may not be easy to meet the ideal 10% VM accuracy requirement bound. If the actual VM accuracy is larger than 10% (such as 15% or 20%) of the tolerance spec (the false-alarm and miss-detection portions of) Cost_Q may be recalculated by the same approach as stated above.

Substituting all the parameter values mentioned above into (1), the benefit of VM yields U.S. \$63 458 792 per year for this fab model with capacity of 30K wafer starts plus 4.5K test wafers per month.

In conclusion, given the assumptions noted above, VM fab-wide implementation is expected to gain extra $\left[\frac{1}{1-(\Delta CT_P + \Delta CT_M)}\right] (=10.56\%) \text{ production volume output due to } (\Delta CT_P + \Delta CT_M = 9.55\%) \text{ cycle-time reduction. This extra production volume output contributes the major portion of VM total benefit. Note that the productivity improvement derived from this formula will be realized when the overall market demand is strong enough to support this capacity improvement. In other words, the first term (Wo multiplier) only provides benefit through the additional capacity realized. While the overall market demand is not strong such that the fab does not need the extra capacity provided with the improved cycle time, then this term has less or no impact.$

Based on the authors' experience of 300 mm foundry operations [30], generally, foundry's high-product-mix operation requires four to five times more of monitoring processes than those of DRAM's low-product-mix operation. From the actual manufacturing management experience, the total testwafer cost of a monthly 30K foundry could be easily over U.S. \$9M per year. Therefore, the benefit of deploying VM will be even better in the advanced foundry service facility. The cost saving mentioned here is purely the test-wafer-cost reduction. Besides test-wafer-usage reduction, if we also consider the corresponding FOUP-usage reduction, stocker-bin-storage reduction, and AMHS-investment cost saving, the benefit will be higher.

The authors have developed the so-called AVM system to implement and deploy the VM operations and functions in a fab automatically [20]. The AVM system is introduced and summarized in the following section.

IV. INTRODUCTION TO AUTOMATIC VIRTUAL METROLOGY

The AVM system consists of a model-creation (MC) server, a VM manager, several VM clients, and many VM servers. The MC server will generate the first set of data quality evaluation

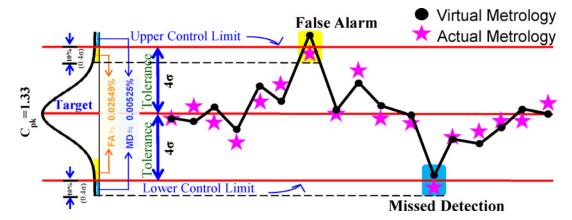


Fig. 3. Illustration of a false alarm and a missed detection.

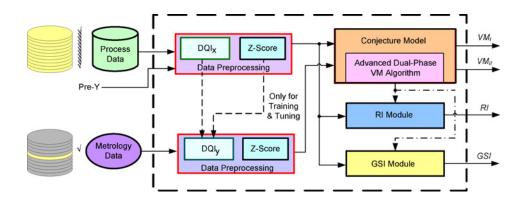


Fig. 4. VM server.

models, VM conjecture models, and VM reliability evaluation models of a certain tool type. Under fab-wide VM deployment, the VM manager can fan out the first set of models generated to all the VM servers of the same tool type. Also, the VM server of each individual fan-out-accepter can perform an automatic model refreshing process to promptly refresh its own model set. Consequently, the VM accuracy of each VM server can be maintained and the VM server is then ready to serve various VM applications.

The VM server, which contains data preprocessing [20], conjecture model with advanced dual-phase VM algorithm [18], [20], RI module [19], and GSI module [19], is shown in Fig. 4. Besides the fundamental functions of VM on-line conjecturing and VM quality evaluation, the VM server also possesses the functions of automatic data quality evaluation and automatic model refreshing [20]. The inputs of a VM server include process data of the current tool and premetrology (Pre-Y) data of the previous tool as well as the metrology data of the current tool. The Pre-Y data is also called Type-2 data in [24] and [25] and may be either actual or virtual metrology data. The outputs are Phase-I VM (VM_{II}), Phase-II VM (VM_{II}), RI, and GSI values. The kernel of the AVM system is the advanced dual-phase VM algorithm that will be briefly introduced next.

As mentioned in [18], Phase I emphasizes promptness and Phase II improves accuracy. Observing the right-hand portion of Fig. 5, the Phase-I algorithm starts to collect the process data of each processing workpiece after the conjecture model is built.

The DQI_X algorithm [20] will be applied to evaluate the quality of the collected process data once process data collection of the said workpiece is completed. If an abnormality is detected, a warning signal will be sent to the process engineer for analysis and confirmation to make sure whether it is an abnormality or a clean outlier. If it is an abnormality, this process data should be discarded.

The workpiece's VM_I and its accompanying RI and GSI values are computed once the DQI_X evaluation is completed and no matter what the evaluation result is. This computation takes about a second only; therefore, promptness is assured. With this VM_I accompanying RI and GSI values for gauging its reliance level, appropriateness for adopting this VM_I value (such as for W2W control) can be checked.

As shown in the left-hand portion of Fig. 5, the Phase-II algorithm starts to collect the metrology data of the prespecified workpiece in a cassette after the conjecture model is built. Correlation between the metrology data and the process data is checked via the workpiece ID once a complete set of metrology data is collected.

If correlation check is successful, the set of process data and metrology data with the same workpiece ID will be checked by the DQI_y algorithm. The DQI_y algorithm [20] is used to do on-line and real-time evaluation for ensuring that both the metrology datum and its corresponding process data are

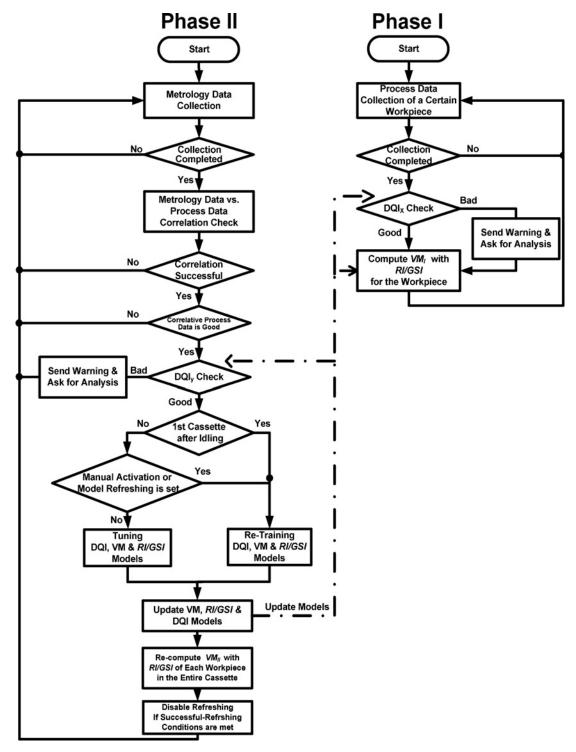


Fig. 5. Advanced dual-phase VM algorithm.

normal before this metrology datum can be considered for tuning or re-training the VM models. If an abnormality is detected, a warning signal will be sent to process engineers for analysis and confirmation. If abnormality is confirmed, the metrology data will be deleted to avoid deteriorating the VM conjecture models. The normal metrology datum verified by DQI_y is then sent to the conjecture model for re-training or tuning usage.

Model refreshing is essential if the first set of DQI_X/DQI_y and VM & RI/GSI models is not generated from its own

historical process and metrology data. The DQI_X/DQI_y and VM & RI/GSI models will be updated once they are retrained or tuned. Subsequently, VM_{II} and its accompanying RI/GSI values of each workpiece in the entire cassette are recomputed. After updating the DQI_X/DQI_y and VM & RI/GSI models in Phase II, these updated models should also be adopted to compute the subsequent DQI_X/DQI_y, VM_I and its accompanying RI/GSI values. Finally, the conditions for a successful and complete refreshing procedure are checked [20]. If all of the conditions are met, which means the conjecture accu-

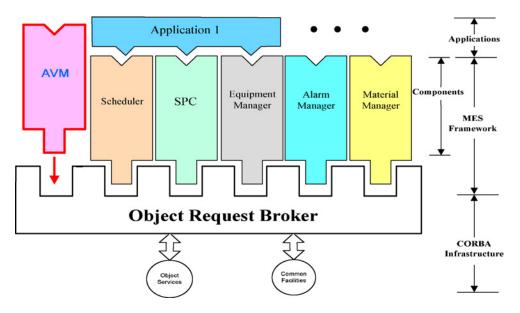


Fig. 6. Plugging AVM into the MES framework.

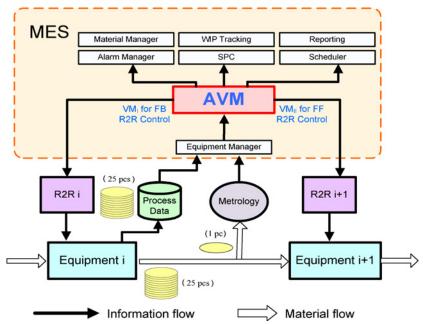


Fig. 7. Relationships among AVM, MES components, and R2R controllers.

racy of the VM server is assured, the refreshing request will be disabled and the system will enter the normal operation state.

From the descriptions above, it becomes clear how the AVM system and advanced dual-phase VM algorithm function. The VM_I and VM_{II} will be applied to support W2W control [18]. In the following section, the details of integrating AVM into the MES will be elaborated.

V. INTEGRATING AVM INTO THE MANUFACTURING EXECUTION SYSTEM

The MES is a shop floor control system which includes manual and/or automatic labor, production reporting, on-line inquiries, and links to tasks that take place on the production floor. The MES provides links to work orders, receipt of goods, shipping, quality control, maintenance, scheduling, and other related tasks [14]. The MES is one of the core components

of the advanced e-manufacturing model [21]. The mission of MES is to increase productivity and yield.

ISMT developed a SEMATECH computer integrated manufacturing (CIM) framework [11] to specify the common MES infrastructure and the software functions of MES applications, and incorporate those MES applications into a coherent system. By specifying the standard interfaces and functions of the common MES components, manufacturers can collect system components from multiple suppliers. Thus, manufacturers can develop systems by extending the common components and substituting old components with improved ones of the same interfaces and functions. The authors have also proposed a MES framework [12] and a holonic manufacturing execution system framework [13] by applying distributed and object-oriented technologies and the concepts of holon and holarchy.

Most of the current commercial MESs (such as IBM's SiView) contain SPC functional module to handle on-line quality monitoring. However, SPC can merely perform quality monitoring on those sampling products that are measured by real metrology tools. The AVM system presented in Section IV has the capability to convert sampling inspection with metrology delay into real-time and on-line total inspection of all products. Therefore, to enable the MES to have the capability of real-time and on-line total inspection, the AVM system should be integrated into the MES.

Based upon the frameworks of [11], [12], or [13], the AVM system can also be developed as a plug gable component of the MES framework shown in Fig. 6. The MES components include scheduler, SPC, equipment manager, alarm manager, material manager, and so on.

The capabilities of AVM include: 1) converting sampling inspection with metrology delay into real-time and on-line total inspection; 2) control/monitoring workpieces reduction /elimination; and 3) supporting W2W control. To bring the AVM's capabilities into full play in a novel manufacturing system, the relationships among AVM, MES components, and R2R controllers are depicted in Fig. 7. The AVM module is plugged into the MES. The AVM module collects process data of process equipment and metrology data of metrology tool via the equipment manager. The AVM outputs (including VM_I, VM_{II}, and their accompanying RI/GSI values) are sent respectively to the SPC module for W2W total quality inspection, to the alarm manager when RI and/or GSI values exceed their thresholds, and to the scheduler module for golden-route consideration, which dispatches important products to stable equipment so as to improve yield stability. The VM_I value is delivered to the R2R controller of the current equipment for feedback R2R control [18]. Finally, the VM_{II} value is dispatched to the R2R controller of the subsequent equipment for feedforward R2R control [18]. The detailed operating scenarios of a novel manufacturing system with AVM capabilities are presented next.

VI. OPERATING SCENARIOS AMONG AVM, MES COMPONENTS, AND R2R CONTROLLERS

A novel manufacturing system with AVM capabilities shall at least consist of a MES with an embedded AVM module and R2R controllers. The detailed operating scenarios among AVM, MES components, and R2R controllers are shown in Fig. 8 and are described below. Note that the operating scenarios should align with the advanced dual-phase VM algorithm shown in Fig. 5.

- 1.&2. Scheduler dispatches a lot via Equipment Manager to Process Equipment I (PE i).
- 3.&4. PE i delivers process data (PD) via Equipment Manager to AVM.
- 5. AVM calculates VM_I and its accompanying RI, GSI, & DQI_X; then checks if any alarm(s) occurs.
- 6. If any alarm(s) occurs, then AVM sends alarm(s) to Alarm Manager.
- AVM reports VM_I (with accompanying RI, GSI, & DQI_X) to SPC for W2W total inspection.

- 8. AVM reports VM_I (with accompanying RI) to R2R i for supporting feedback R2R control.
- 9. SPC triggers an out-of-control action plan (OCAP) to Alarm Manager if an alarm is detected.
- 10. Alarm Manager executes OCAP.
- 11. R2R i calculates control advice of PE i.
- 12.&13. R2R i sends control advice via Equipment Manager to PE i.
- 14. PE i checks if the whole lot is not completed then the procedure jumps to Step 3 for processing the subsequent wafer in the lot.
- 15.&16. PE i checks if the whole lot is completed then the job done message is sent via Equipment Manager to Scheduler.
- 17.&18. Scheduler dispatches a sampling wafer via Equipment Manager to Metrology Equipment (ME).
- 19. ME performs measurement on the sampling wafer.
- 20.&21. ME delivers metrology data (MD) via Equipment Manager to AVM.
- 22. AVM calculates VM_{II} and its accompanying RI, GSI, & DQI_v; then checks if any alarm(s) occurs.
- 23. If any alarm(s) occurs, then AVM sends alarm(s) to Alarm Manager.
- 24. AVM reports MD of the sampling wafer and the VM_{II} (with accompanying RI, GSI, & DQI_y) of the whole lot to SPC for W2W total inspection.
- 25. AVM reports VM_{II} (with accompanying RI) to R2R i+1 for supporting feedforward R2R control of the subsequent PE i+1.
- 26. R2R i+1 calculates control advice of PE i+1.
- 27. AVM reports MD of the sampling wafer and the VM_{II} (with accompanying RI, GSI, & DQI_y) of the whole lot to Scheduler for golden-route consideration.
- 28. Scheduler selects a golden route based on MD and $VM_{\rm II}$ results.

The major differences between the flow diagrams by adopting AVM versus high speed (e.g., integrated) metrology are as follows.

1) Besides VM_I and VM_{II}, AVM can also generate and send RI, GSI, DQI_X, & DQI_y to the SPC, alarm manager, scheduler, and so forth for gauging the VM reliability level, monitoring the equipment health status, and evaluating the process & metrology data qualities, respectively such that more applications (e.g., intelligent dynamic metrology and process schemes leading to further reduction in cycle time) may be developed; while integrated metrology can only provide actual metrology data.

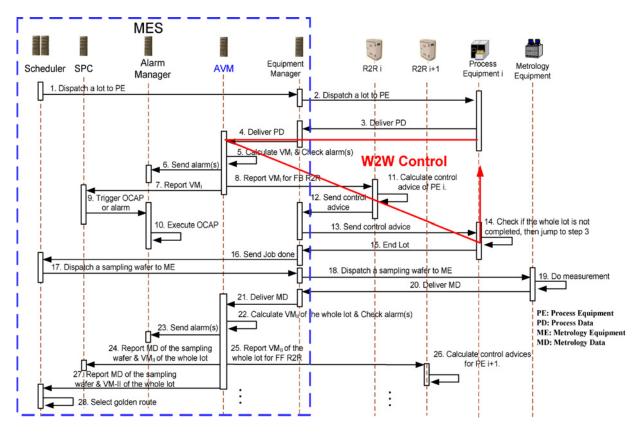


Fig. 8. Operating scenarios among AVM, MES components, and R2R controllers.

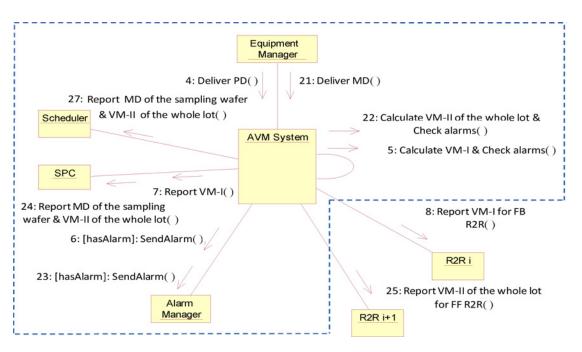


Fig. 9. Collaboration diagram for integrating AVM into MES.

 AVM needs sampled metrology data to re-train or tune the VM models; while integrated metrology requires calibration wafers to re-calibrate itself.

Observing the red triangle shown in Fig. 8, it explicitly shows the operating scenario of AVM supporting the W2W control. The corresponding collaboration diagram of the operating scenarios shown in Fig. 8 is depicted in Fig. 9. The framework messages shown in Figs. 8 and 9 are aligned (with the same sequence numbers). Both the operating-scenario diagram and the collaboration diagram are the essential developing guides for designing the framework messages [12], [13] among AVM, MES components, and R2R controllers. With these framework messages designed, the AVM module can be configured as a pluggable component of the MES and the AVM module can send VM_I and VM_{II} to the R2R controllers for supporting the W2W control. Observing Sequence 8 in Section VI: "AVM reports VM_I (with accompanying RI) to R2R i for supporting feedback R2R control," the purpose of reporting VM_I with accompanying RI to R2R i is to tune α 2 with $\alpha 2 = RI \times \alpha 1$ [29] when W2W control with VM_I is applied.

VII. SUMMARY AND CONCLUSION

A novel manufacturing system with AVM capabilities was proposed in this paper. This novel manufacturing system is composed of at least a MES with a pluggable AVM module and R2R controllers. The operating scenarios of the novel manufacturing system and the collaboration diagram of the AVM pluggable module were elaborated in this paper. Furthermore, a benefit equation was established to evaluate the profitability of applying VM fab-wide. The evaluation result shows that VM fab-wide implementation is expected to gain roughly 10% extra production volume output due to cycle-time reduction. In conclusion, applying the manufacturing system with AVM capabilities is one of the effective approaches to accomplish the requirements of both cycle-time and cost reductions of the next generation fab.

REFERENCES

- W. A. Shewhart, Economic Control of Quality of Manufactured Product. New York: Van Nostrand, 1931.
- [2] G. D. R. Hall, R. Young, M. Dunne, and M. Muro, "A quality-cost model of in-line inspections for excursion detection and reduction," in *Proc.* IEEE/SEMI Adv. Semiconductor Manuf. Conf., May 2008, pp. 273–277.
- [3] F. Bergeret and C. L. Gall, "Yield improvement using statistical analysis of process data," *IEEE Trans. Semiconductor Manuf.*, vol. 16, no. 3, pp. 535–542, Aug. 2003.
- [4] S.-B. Lee, T.-Y. Lee, J. Liao, and Y.-C. Chang, "A capacity-dependence dynamic sampling strategy," in *Proc. IEEE Int. Symp. Semiconductor Manuf.*, Oct. 2003, pp. 312–314.
- [5] S. J. Qin, G. Cherry, R. Good, J. Wang, and C. A. Harrison, "Semi-conductor manufacturing process control and monitoring: A fab-wide framework," *J. Process Control*, vol. 16, pp. 179–191, Mar. 2006.
- [6] C. J. Spanos, P. Jula, and R. C. Leachman, "The economic impact of choosing off-line, inline or in-situ metrology deployment in semiconductor manufacturing," in *Proc. IEEE Semiconductor Manuf. Symp.*, Oct. 2001, pp. 37–40.
- [7] A.-J. Su, C.-C. Yu, and B. A. Ogunnaike, "On the interaction between measurement strategy and control performance in semiconductor manufacturing," *J. Process Control*, vol. 18, pp. 266–276, Mar. 2008

- [8] J. Zhang, C.-C. Chu, J. Munoz, and J. Chen, "Minimum entropy based run-to-run control for semiconductor processes with uncertain metrology delay," *J. Process Control*, vol. 19, pp. 1688–1697, Dec. 2009.
- [9] K. L. Butler and R. Woods, "A methodology for determining capacity consumption due to the sampling of lots within the photolithography metrology sector in a multi-part number, multi-technology fabricator," in *Proc. IEEE/SEMI Adv. Semiconductor Manuf. Conf. Workshop*, Sep. 1999, pp. 113–116.
- [10] J. Moyne, "International technology road map for semiconductors (ITRS) perspective on AEC/APC," in *Proc. 21st ISMI AEC/APC Symp.*, Sep. 2009.
- [11] SEMATECH. CIM Framework Specification 2.0 [Online]. Available: http://www.sematech.org
- [12] F.-T. Cheng, E. Shen, J.-Y. Deng, and K. Nguyen, "Development of a system framework for the computer-integrated manufacturing execution system: A distributed object-oriented approach," *Int. J. Comput.-Integr. Manuf.*, vol. 12, no. 5, pp. 384–402, Sep.–Oct. 1999.
- [13] F.-T. Cheng, C.-F. Chang, and S.-L. Wu, "Development of holonic manufacturing execution systems," *J. Intell. Manuf.*, vol. 15, no. 2, pp. 253–267, Apr. 2004.
- [14] Manufacturing Execution Systems. (2007). TechTarget [Online]. Available: http://www.bitpipe.com/rlist/term/manufacturing-execution-systems.html
- [15] A. Weber, "Virtual metrology and your technology watch list: Ten things you should know about this emerging technology," *Future Fab Int.*, no. 22, section IV, pp. 52–54, Jan. 2007.
- [16] O. Rothe, "ISMI next generation factory," in *Proc. e-Manufacturing Workshop, SEMICON West*, Jul. 2008 [Online]. Available: http://www.sematech.org/meetings/archives/emanufacturing/8546/01-NGF.pdf
- [17] D. Stark, "Data usage," in Proc. e-Manufacturing Workshop, SEMICON West, 2008 [Online]. Available: http://www.sematech.org/meetings/ archives/emanufacturing/8546/06-%20PPM%20and%20VM%20and%20 EEQA.pdf
- [18] F.-T. Cheng, H.-C. Huang, and C.-A. Kao, "Dual-phase virtual metrology scheme," *IEEE Trans. Semiconductor Manuf.*, vol. 20, no. 4, pp. 566–571, Nov. 2007.
- [19] F.-T. Cheng, Y.-T. Chen, Y.-C. Su, and D.-L. Zeng, "Evaluating reliance level of a virtual metrology system," *IEEE Trans. Semiconductor Manuf.*, vol. 21, no. 1, pp. 92–103, Feb. 2008.
- [20] Y.-T. Huang, H.-C. Huang, F.-T. Cheng, T.-S. Liao, and F.-C. Chang, "Automatic virtual metrology system design and implementation," in *Proc. IEEE Int. Conf. Autom. Sci. Eng.*, Aug. 2008, pp. 223–229.
- [21] F.-T. Cheng, W.-H. Tsai, T.-L. Wang, J. Y.-C. Chang, and Y.-C. Su, "Advanced e-manufacturing model," *IEEE Robot. Autom. Mag.*, vol. 17, no. 1, pp. 71–84, Mar. 2010.
- [22] J. Moyne, "Providing APC input to the factory integration chapter of the international technology road map for semiconductors (ITRS)," in Proc. 9th Eur. AEC/APC Conf., Mar. 2008.
- [23] J. Moyne, "PCS mechanisms for fab-wide development and latest trends, new directions in PCS: Virtual metrology," in *Proc. 21st ISMI AEC/APC Symp.*, Sep. 2009.
- [24] A. A. Khan, J. R. Moyne, and D. M. Tilbury, "An approach for factory-wide control utilizing virtual metrology," *IEEE Trans. Semiconductor Manuf.*, vol. 20, no. 4, pp. 364–375, Nov. 2007.
- [25] A. A. Khan, J. R. Moyne, and D. M. Tilbury, "Virtual metrology and feedback control for semiconductor manufacturing process using recursive partial least squares," *J. Process Control*, vol. 18, no. 10, pp. 961–974, Dec. 2008.
- [26] Y.-C. Su, T.-H. Lin, F.-T. Cheng, and W.-M. Wu, "Accuracy and real-time considerations for implementing various virtual metrology algorithms," *IEEE Trans. Semiconductor Manuf.*, vol. 21, no. 3, pp. 426– 434, Aug. 2008.
- [27] N. S. Patel, G. A. Miller, and S. T. Jenkins, "In situ estimation of blanket polish rates and wafer-to-wafer variation," *IEEE Trans. Semiconductor Manuf.*, vol. 15, no. 4, pp. 513–522, Nov. 2002.
- [28] M. P. Groover, Automation, Production Systems, and Computer-Integrated Manufacturing, 2nd ed. London, U.K.: Prentice-Hall, 2001.
- [29] F.-T. Cheng, C.-A. Kao, and W.-M. Wu, "Advanced process control system and method utilizing virtual metrology with reliance index," U.S. Provisional Patent Pending Under Application 61/369 761, Aug. 2010.
- [30] J. Chang and F.-T. Cheng, "Application development of virtual metrology in semiconductor industry," in *Proc. 31st IEEE Annu. IECON*, Nov. 2005, pp. 124–129.
- [31] S. Imai, N. Sato, M. Kitabata, and S. Yasuda, "Fab-wide equipment monitoring and FDC system," in *Proc. IEEE Int. Symp. Semiconductor Manuf.*, Sep. 2006, pp. 114–117.

[32] A. A. Khan, J. R. Moyne, and D. M. Tilbury, "On the quality of virtual metrology data for use in the feedback process control," in *Proc. 19th AEC/APC Symp.*, Sep. 2007.



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