Factoring Variability in the Design/Technology Co Optimisation (DTCO) in advanced CMOS

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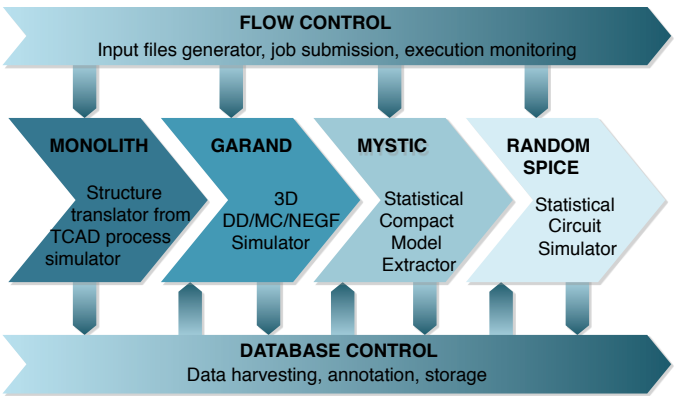
I. INTRODUCTION

This paper describes the fully automated GSS tool flow, which bridges the gap between Technology Computer Aided Design (TCAD) at the transistor level, and circuit simulations and verification. The purpose of the tool flow is twofold: (i) to allow rapid simulation-based Design-Technology Co-Optimisation (DTCO) and (ii) to allow generation of accurate compact models for Preliminary Design Kit (PDK) development at the early stages of new technology development. The aim is to capture accurately process, statistical and time dependent variability in the DTCO and early PDKs. The operation of the automated tool flow is exemplified in the comprehensive PDK compact model development for a 14 nm SOI FinFET process, and the corresponding transistor / SRAM cell co-optimisation.

II. TOOLL FLOW AND AUTOMATIONS

The block diagram of the automated tool flow is illustrated in Fig. 1. It includes the GSS 'atomistic' device simulator GARAND, the statistical compact model extractor Mystic and the statistical circuit simulation engine Random Spice.



The tool flow allows simulation of process and statistical variability and statistical reliability. The simulations capture the correlations between different sources of process variability, the interplay between process and statistical variability and the impact of both on statistical reliability associated with discrete charge trapping. The script-based flow control system parses and generates input files for all simulators and extractors, automatically submits jobs to a large cluster of processors and monitors the job execution. The database control system harvests, annotates and stores data which can be readily accessed by the different components of the tool flow.

The FLOW CONTROL SYSTEM (FCS) allows automated simulation of process-induced variability, statistical variability and time-dependent variability and their full interactions using the GSS 'atomistic simulator' GARAND Process-induced variability is captured using a Design of Experiment (DOE) approach that superimposes the different sources of process variations including critical dimensions, layer thicknesses and doping variations. Statistical variability sources can be superimposed on each combination of process variability sources. The FCS automatically generated input files for the above simulations. Then it submits the corresponding jobs on compute clusters supporting Grid Engine or LSF. The job execution is monitored and corrective action can be performed including resubmission of jobs due to hardware failure. FCS also controls the extraction of nominal, process variability, statistical variability and time-dependent variability compact models using the GSS statistical compact model extractor MYSTIC Finally the FCS automatically performs large-scale statistical simulation and verification using the GSS statistical circuit simulator RANDOM SPICE. The FCS allows a script-based definition of a workflow, automatically linking the different tools in the GSS tool chain.

The DATABSE CONTROL SYSTEM (DCS) performs data harvesting, annotation and storage. It allows automated seamless flow of data between the different tools of the tool chain during the workflow execution. It also stores data for post-processing, data analysis and visualisation using different R-based statistical analysis tools and Paraview-based visualisation.

III. CONCLUSIONS

We have developed and presented an automated tool flow that greatly enhances the productivity of the circuit design process in the presence of acute variability.

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