Tutorial T5

# The World beyond DRC: Design for Manufacturing (DFM) - *Impact on Yield & Reliability for Advanced Technology Nodes and Their Elucidations*

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## Abstract

As we pace towards advanced technologies there is an assorted increase in design intricacies and accurate layout requirements. To meet the demanding specifications without compromising the time to market, designers look for precise first-pass silicon with first-class yield.

The traditional Design Rule Checks (DRCs) cannot capture all the layout related issues that degrade the circuit yield and reliability. The rule-based DRCs considered as the mainstay of the layout verification have been augmented by latest DFM techniques in the last few years.

In the first part of our tutorial, we will present various yield limiting layout issues arising from lack of DFM uses, such as how DFM issues lead to yield and reliability impacts on advance technology nodes like 28nm and below. This forces industry to think beyond DRC and mandate DFM for better yield and reliability. We will also discuss different degrees of DFM and its scoring used in industry.

In the second part we will discuss Litho Process Checking (LPC): what are the challenging layout limiting configurations, how to detectclassify and fix them. We will cover cutting-edge approaches from EDA tools and foundries ranging from full process simulation based hotspots detection kits, to fast pattern matching based kits.We will discuss our analysis of these techniques in terms of finding hotspots, efforts to implement & use, and improvement in speed of execution as compared to traditional rule or simulation-based checks.Next we will discuss Chemical Mechanical Polishing (CMP) techniques and their elucidations. Further we will talk about Critical Area Analysis (CAA) and other yield enhancement approaches. In the concluding part we will discuss opportunities of different DFM design flows and collateral to be used in design process for better yield and reliability.

## Speaker Biography

**Yadav Preet**, has been involved in diversified VLSI domains of, CAD, AMS design & verification, and core technology development throughout his 12+ years hands-on experiences. He received his B. Tech. degree in ECE from Kurukshetra University and M. Tech. degree in VLSI Design & CAD from Thapar University.

He worked at Semiconductor Complex Ltd. and, Cadence Design Systems. In 2008, he joined Freescale Semiconductor (now NXP Semiconductor), worked on Process Design Kits, leading handful of technologies from matured to advance nodes. Presently he is working on Analog and Mixed Signal SOC in Automotive Microcontrollers and Processors (AMP) group.

He has received President Award in Scouts & Guides, and various certifications of merit. He has 15+ publications in international/national conferences, with two best paper awards on his name. He has delivered several invited talks & tutorials at Institutes and international conference. He has acted as member of review committee for international conference in the area of VLSI. He is lifetime member of Indian Microelectronics Society (IMS) and The Institution of Electronics Telecommunication Engineers (IETE).