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WLCSP Package and PCB Design for Board Level Reliability

Jason Chiu, K.C. Chang, Steven Hsu, Pei-Haw Tsao and M. J. Lii
Taiwan Semiconductor Manufacturing Company, Ltd.
6, Creation Rd. 2, Hsinchu Science Park, Hsinchu, Taiwan 300-77, R.O.C.
Email: sschiud@tsmc.com

***Abstract*—WLCSP packaging is wildly use in portable electronic products such as phone, watch, and intelligent bracelet. The advantages of WLCSP package are parasitic inductance minimized, reduced package size, and enhanced thermal conduction characteristics. To enable these benefits regardless of the die's functional complexity, we adopted Cu with ELK (extreme Low-K) material as inter-metal-dielectric native to advanced silicon fabrication technology, and WLCSP packing with large die size, thus fulfilling requirements for high speed & low power consumption. Investigating WLCSP package board level reliability is essential and critical for product launch and reducing field return risk. Test vehicles were used with combinations in PBO2 opening, PCB thickness, and PCB metal gradient, to understand stress on ELK behavior and potential impact on board level reliability.**
Liquid-to-liquid thermal shock (LLTS) 75 cycles of -65^{0}C~150^{0}C will be a quick stress methodology which have ~1.9x acceleration factor compared with TCB stress and used for shortening experiment cycle time. A 6x6 mm^2 test vehicle was used for different WLCSP package PBO2 opening, PCB thickness and PCB metal design to assess board level reliability impact. LLTS 75cycles result showed larger PBO2 opening will get die edge ELK delamination defects. Higher PCB metal gradient board (more than 50%) & more thick (1mm) also got higher fail rate. For better WLCSP board level reliability structure, smaller WLCSP package PBO2 opening, thinner PCB thickness and uniform PCB metal distribution are recommended.

Keywords-WLCSP; WLCSP PBO openingl; WLCSP PCB metal density; WLCSP package reliability

I. INRODUCTION

As WLCSP packaging is wildly use in portable electronic products such as phone, watch, and intelligent bracelet. The advantages of WLCSP package are parasitic inductance minimized, reduced package size, and enhanced thermal conduction characteristics. Not only the numbers of WLCSP device used were increased, the WLCSP package size was also obviously increased due to higher level of functional requirement. Larger than 5x5 mm^2 WLCSP size becomes unavoidable in fulfilling high-end product performance demands. Knowing the WLCSP structure, shown in Fig. 1, has few thin dielectric layers on chip surface as stress buffer between chip and printed-circuit-board (PCB). The large WLCSP chip's board level reliability will be very challenge due to high coefficient of thermal expansion (CTE) mismatch between the package and PCB. To improve the reliability performance of large chip WLCSP, best WLCSP package design and PCB board design was used as important practices in the industry. To manage the potential side effect and effectiveness of action taken for advanced WLCSP is quite important. Typical on-board defect modes of larger WLCSP package reported recently, are package edge ELK delamination defect, shown in Fig. 2. Therefore, this study was to understand PCB thickness/PCB metal distribution/WLCSP package PBO2 opening effect and potential impact on the board reliability performance of WLCSP using advanced wafer technology.

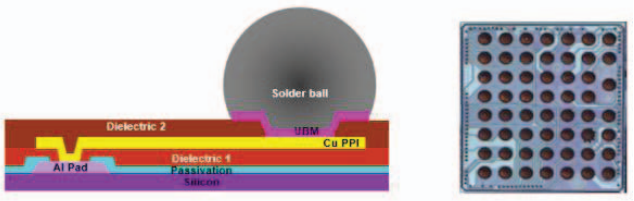

Figure 1. A WLCSP package schematic.

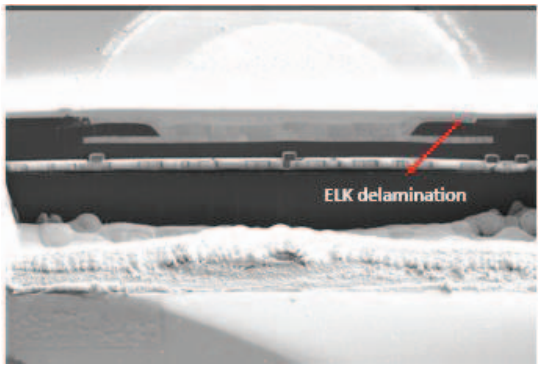

Figure 2a. WLCSP package edge ELK delamination post board level reliability test.

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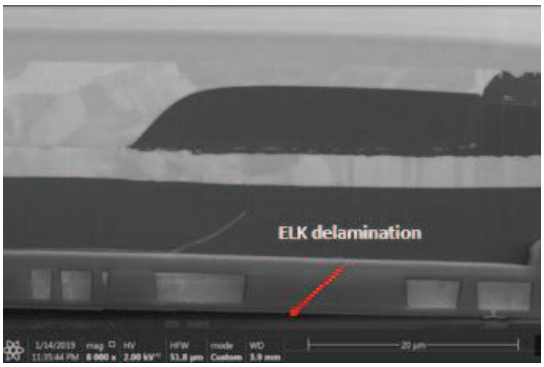


Figure 2b. WLCSP package edge ELK delamination post board level reliability test.

II. EXPERIMENT

Test vehicle, with 6x6 mm^2 die size and consisting of full backend interconnection Cu metal layers, were processed by advanced wafer fabrication technology using ELK IMD material. The WLCSP packages were built in 270um die thickness using the standard production process flow of assembly house with 2 WLCASP package design PBO2 opening 130um, 190um. The PCB design were designed 3 thickness including 0.65mm, 1.0mm, and 1.2mm. The 0.65mm PCB was designed non-uniform Cu distribution design, as named "High metal gradient" PCB in this study. And the 1.0mm/1.2mm PCB were designed uniform Cu distribution, as named "Low metal gradient" PCB. In order to simulate real portable devices PCB behavior having multi chips on top and bottom side, the test samples were mounted on the top side and bottom side of JEDEC PCB without underfill which can have higher stress, as shown in Fig3. The samples were processed by standard SMT process with 3x260^{0}C reflow in representing the worse SMT condition. There were 6 DOE legs for WLCSP package PBO2 opening, PCB thickness and PCB Cu distribution as shown in Table II. Each leg sample size is 45ea.

In order to shorten the experiment cycle time, liquid-to-liquid thermal shock test (LLTS) was used as quick stress method by its wider temperature range and short cycle time compared with in-situ temperature cycle test, Table I. Based on Coffin Manson equation and the Coffin Manson exponent of 3 for ductile material, 1.9 acceleration factor is expected to allow to obtain TCB200 equivalent results in one day. The on boarded samples were subjected to perform LLTS75x stress.

6x6mm^2 test vehicle mounted on the JEDEC board samples were used for quick stress method validation by benchmark with in-situ monitored board level TCB reliability stress test.

TABLE I. QUICK TEST OF LIQUID-TO-LIQUID THERMAL SHOCK CONDITION VS. TEMPERATURE CYCLE TEST

	Liquid-to-liquid Thermal Shock test	Temperature Cycle Test
Temperature range	-65^{0}C ~ 150^{0}C	-50^{0}C ~ 125^{0}C
Cycle time (minute)	10	30

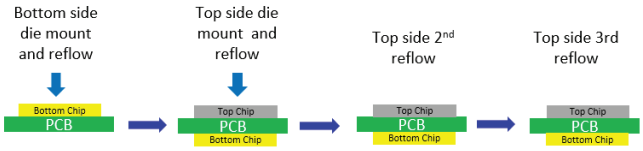
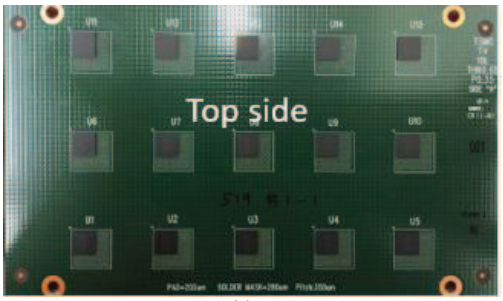
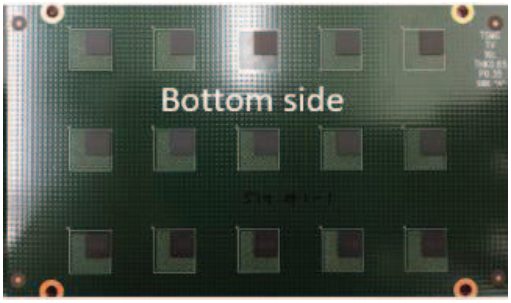


Figure 3. SMT die attachment sequence including top die (test die) bottom die (more stress) then perform reflow



(a)



(b)

Figure 4. A picture of board mounted 6x6 mm2 test samples
(a) PCB top side (real test dies)
(b) PCB bottom side (stress enhancement dies)

TABLE II. DOE OF SPLIT LEGES INCLUDING PBO2 OPENING, PCB THICKNESS AND PCB DESIGN METAL GRADIENT (EACH LEG TEST 45EA SAMPLES)

Leg	PM2 CD opening(um)	PCB thickness(mm)	PCB metal gradient
1	130	0.65	High
2	130	1.0	Low
3	130	1.2	Low
4	190	0.65	High
5	190	1.0	Low
6	190	1.2	Low

III. EXPERIMENTAL RESULTS

This research intended to deliver a WLCSP board level reliability assessment methodology with minimum test chip and test board constraint, and also not being limited by using electrical open/short measurement as pass/fail criteria. So the pass/fail criterial will be judged by CSAM.

LLTS75x test results with different PCB thickness (1.0mm vs. 1.2mm) & PBO2 opening (130um vs. 190um) were shown in Fig5. Thicker PCB thickness will have higher fail rate than thinner PCB thickness. Larger PBO2 opening will have higher fail rate also. LLTS75x test results with different PCB thickness (0.65mm, 1.0mm & 1.2mm) & PCB metal gradient (high vs. low) were shown in Fig6 (a) & (b). In thinner PCB thickness condition less than 1.0mm, PCB design with higher metal gradient have higher fail rate. If PCB thickness is more than 1.0mm(ex:1.2mm), the major contribution will be PCB thickness than PCB metal gradient.

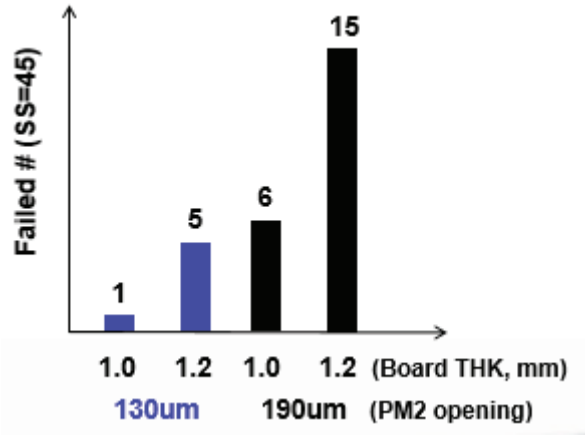


Figure 5. CSAM check result of 6x6mm^2 die split with different PCB thickness & PBO2 opening.

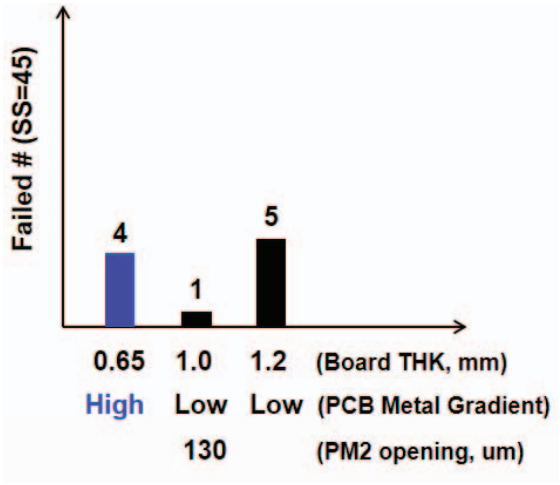


Figure 6a. CSAM check result of 6x6mm^2 die split with different PCB thickness & PCB metal gradient with 130um PBO2 opening design.

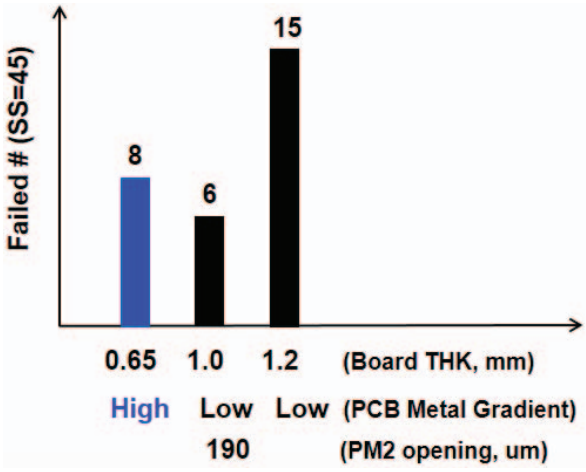


Figure 6b. CSAM check result of 6x6mm^2 die split with different PCB thickness & PCB metal gradient with 190um PBO2 opening design.

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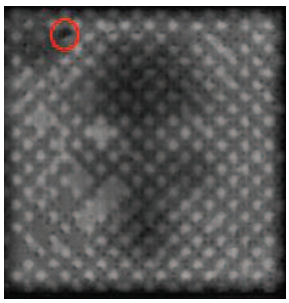

Figure 7a. CSAM fail images which showed ELK delamination defect.

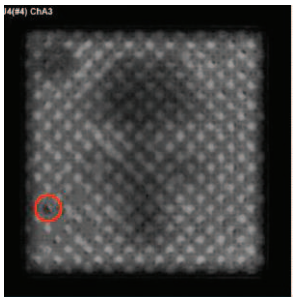

Figure 7b. CSAM fail images which showed ELK delamination defect.

IV. DISCUISSION

Small PBO2 opening showed better board level reliability performance in same PCB thickness condition with 6x6 mm^2 test vehicle. The major technical reason is PBO is a good stress buffer dielectric material. With more PBO material (small PBO2 opening), the stress from PCB board side (through solder ball) can be reduced by PBO thus less stress transferred into die interior.

Thinner PCB thickness with same PBO2 opening showed better board level reliability. The technical reason is thicker PCB thickness will have larger stiffness between die & PCB which induce more stress.

Higher PCB metal gradient (50%) showed higher ELK fail rate after board level reliability in PCB thickness under 1.0mm. The PCB metal gradient definition means in small area (4x4 $mm^{2)}$, the PCB metal uniformity (max-mini). In general PCB design rule, more uniform is better. Higher PCB metal gradient will generate loading effect when performing board level reliability.

To have better understanding on PBO2 opening stress behavior on WLCSP board level reliability performance, besides performing the experiment. Stress modeling with different PBO2 opening was shown in Table III. The modeling temperature loading is from SMT reflow 220^0C(stress) to 25^0C (stress calculated). The Modeling results showed smaller PBO2 opening have less ELK stress. ELK stress decrease 8% from PBO2 opening 190um to 130um. The 3-D modeling focused on ELK layer at die edge, Fig. 9. Stress modeling with different PCB thickness was shown in Table IV. If the PCB thickness is increase from 1.0mm to 1.3mm, the stress will increase 15%. 3-D stress simulation of thicker PCB and chip interaction was shown in Fig. 8 and Fig. 9. Stress modeling with 2 PCB Cu layout design was shown in Table V. PCB with 25% metal gradient got 11% ELK stress reduce than PCB with 50% metal gradient design. 3-D stress simulation of thicker PCB and chip interaction was shown in Fig. 10.

The simulation result showed good agreements with experiment data that small PBO2 opening of package, thinner PCB thickness and more uniform PCB metal distribution (means less metal gradient) can have best CPBI (chip package board interaction) for ELK layer.

TABLE III STRESS MODELING WITH DIFFERENT PBO2 OPENING

Leg	1	2	3	4	5	6	7
UBM (um)	220	220	220	220	220	220	220
PBO2 (um)	190	170	150	130	110	90	70
PBO2/UBM size ratio	0.86	0.72	0.68	0.59	0.50	0.41	0.32
RDL pad (um)	240	240	240	240	240	240	240
PBO Stress (RDL edge)	1.00	0.99	0.98	0.97	0.96	0.96	0.96
PBO Stress (UBM edge)	0.75	0.71	0.71	0.71	0.71	0.71	0.71
ELK Stress	1.00	0.98	0.95	0.92	0.90	0.88	0.87

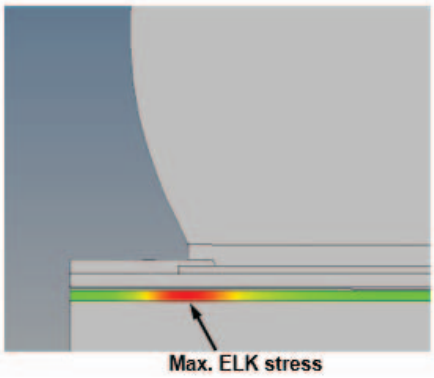

Figure 7. 3-D package model for stress simulation.

TABLE IV STRESS MODELING WITH DIFFERENT PCB THICKNESS

Simulation	Condition-1	Condition-2
Die size (mm^2)	7.2x7.2	7.2x7.2
Die thickness (um)	325	325
Ball pitch (um)	400	400
Ball size (um)	250	250
Ball material	SAC405	SAC405
PCB thickness (mm)	1.0	1.3
Normalized die ELK stress	1.00	1.15

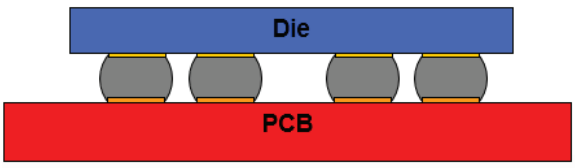

Figure 8. Thicker PCB thickness will have larger stiffness between die & PCB which induce more stress.

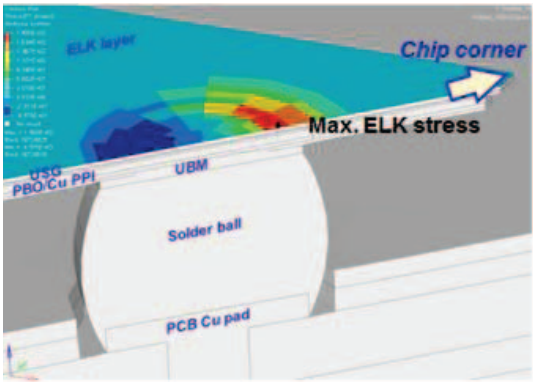

Figure 9. 3-D package model for Thicker PCB

TABLE V STRESS MODELING WITH DIFFERENT PCB METAL GRADIENT DESIGN

Simulation	Condition-1	Condition-2
Die size (mm^2)	7.2x7.2	7.2x7.2
Die thickness (um)	325	325
Ball pitch (um)	400	400
Ball size (um)	250	250
Ball material	SAC405	SAC405
PCB thickness (mm)	1.0	1.0
PCB metal gradient (%)	25%	50%
Normalized die ELK stress	1.00	1.11

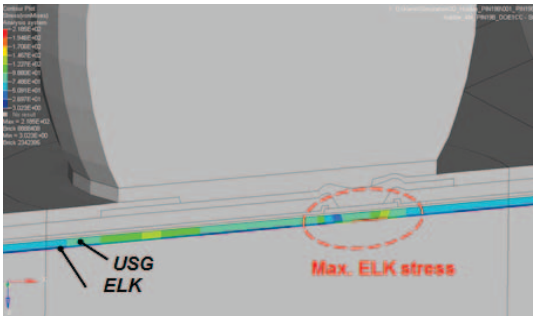

Figure 10. 3-D package model for High PCB Metal Gradient

V. CONCLUSION

Since the trend of WLCSP package towards large chip size with advanced wafer process using ELK as inter metal dielectric material, the assessment of WLCSP board level reliability is very critical and need to be carefully investigated. Two major key factors, package design and PCB design, impacting WLCSP board level reliability performance were studied.

For WLCSP with ELK die, the package design of PBO2 opening was shown having significant impact on board level reliability due to inducing potential ELK delamination defect. Larger PBO2 opening design will have higher ELK fail rate since the less PBO material under UBM which will have less stress buffer. The minimum PBO2 opening need to check the process capability and current requirement. For portable devices, thinner PCB thickness will be a toward trend. High PCB thickness also have higher ELK fail since the mismatch between die and PCB. For PCB design, more uniform metal design is recommended. Since the stress loading effect will occur when performing board level reliability.

A quick WLCSP board level reliability test methodology, SMT 3x 260^0C plus liquid-to-liquid thermal shock test (LLTS) 75 cycles with CSAM check, was demonstrated as an effective way for reliability assessment with less constrain on test vehicle and test board and much shorter time. Then we can base on the result to enhance the WLCSP package or PCB design. The results of this study provide a reference for WLCSP package board level reliability enhancement.

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