Design for Manufacturability: A Key to Semiconductor Manufacturing Excellence

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Abstract – This paper reviews measures of manufacturing excellence and presents a design-for-manufacturability (DFM) program organized around early design and manufacturing teamwork and the economic analysis of design options. Typical measures of manufacturing excellence for a semiconductor fabricator are expressed in terms of either operational or economic results. Those expressed in terms of operational results are independent of the product mix in the fabricator while those expressed in terms of economic results integrate both fabricator and product design attributes into a single parameter like revenue/wafer. Improvements in the operational measures of manufacturing excellence focus upon increases in capacity and throughput, defect density reductions, and cost containment. Improvements in the economic measures of manufacturing excellence must focus on both fabricator processing efficiency and the productivity of the design. Design-for-manufacturability practices can improve design productivity, time-to-market, and product performance and reliability by closely coupling semiconductor fabrication knowledge with product requirements during the initial phase of a product design. Every design decision produces both technical and economic consequences; understanding these consequences and using this knowledge in the design process to optimize product productivity and profitability is key to achieving manufacturing excellence for that product.

INTRODUCTION

During the past several years, many major business enterprises have been under tremendous competitive pressure to streamline operations and better direct the expenditure of finite organization resources toward achieving enterprise objectives. In the semiconductor industry, these competitive pressures drive more efficient fabricators, faster design cycles, and new function in each design generation. The people working in the semiconductor industry understand better than most that these competitive pressures will not disappear from the business landscape. These marketplace realities fuel the relentless drive toward manufacturing excellence within semiconductor development and manufacturing enterprises.

This drive to manufacturing excellence touches every aspect of semiconductor manufacturing operations. Every tool, every raw material, every environmental condition, every process setting, and every routing is carefully studied for inefficiency or interactions which might limit throughput, cycle time or wafer-test yields. When a new fabricator is built every process condition and tool configuration is copied exactly from the previous fabricator so that yield learning will not have to be repeated [1].

There is one other "raw material" that impacts throughput, cycle time, wafer-test yield, and asset utilization, that is often overlooked in the drive towards "manufacturing excellence." This raw material is the design of the product being manufactured. Normalizing yield by die area or number of gates reveals that manufacturing productivity is strongly modulated by the design attributes of the products being fabricated. Figure 1 shows the relationship between good cm^2 of silicon/wafer and die size for a number of products.

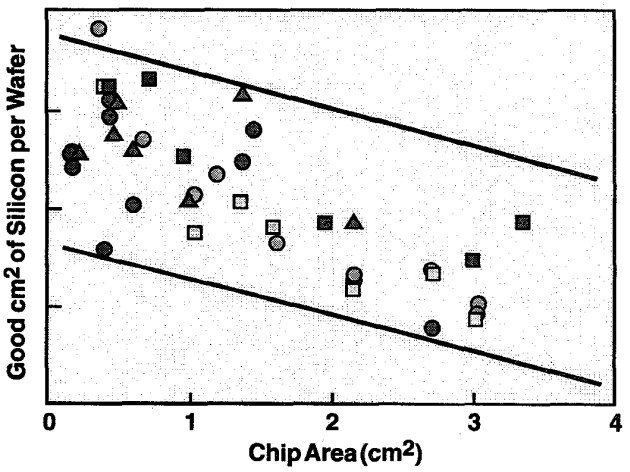

Figure 1. Good cm^2 of silicon/wafer vs chip area in cm^2

After observing the range in productivity, for any given die size, between the highest- and lowest-yielding designs, it is recognized that all designs do not process and yield the same. It is reasonable to conclude,

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therefore, that product design is a very significant raw material, and that design attributes which have a significant impact upon manufacturing excellence must be understood and optimized.

With leading-edge fabricator costs exceeding $2B, a significant portion of manufacturing costs are incurred from fabricator and tooling depreciation. The drive toward manufacturing excellence must also recognize the contribution of depreciation to manufacturing costs and respond with product designs that improve asset utilization. Product developers must be aware of the impact of their design decisions on asset utilization and capacity. For example, designing a six-level metal product for manufacturing in a fabricator that has been tooled for four-level metal will detract significantly from the fabricator's total capacity and overall potential for profit.

MEASURES OF MANUFACTURING EXCELLENCE

The semiconductor industry measures and reports manufacturing excellence using a number of parameters. Typically these parameters document a significant processing activity in quantitative terms and allow fabricator-to-fabricator comparisons and the determination of productivity changes over time for various tooling and line-loading conditions. There are two types of manufacturing excellence parameters: those that document fabricator capabilities in terms of operational results and those that document these capabilities in terms of economic results.

Manufacturing excellence parameters based upon operational results are internal in nature because they depend entirely upon the fabricator elements of tooling and personnel and not on the products being processed. Tool cost of ownership, sector outs, fabricator throughput, fabricator cycle time, process yield, and defect density are typical examples of operational measures of manufacturing excellence. These operational (or internal) parameters provide valuable technical information to the engineering and management teams responsible for the fabricator's operation, and often form the basis for management decisions that allocate scarce engineering resources to the tasks of optimizing fabricator wafer starts and output, and reducing defect levels.

Semiconductor manufacturers must allocate finite capital resources to either upgrade existing fabricators or plan new ones. These decisions require key manufacturing excellence parameters expressed in economic terms so that a return-on-investment calculation can be made for each investment option and investment priorities set based upon economic factors. Manufacturing excellence parameters that express fabricator capabilities in terms of economic results integrate both fabricator capability and product design attributes. This is obvious for revenue/wafer because the strong linkage between product function and selling price is easily understood, however it may be less obvious for other manufacturing excellence parameters like good modules/wafer, production cost/good cm^2, and yield learning rate, etc. Simply stated, any manufacturing excellence parameter determined by using wafer final-test yield as an element in the calculation, integrates both fabricator capability and design attributes into the result.

Revenue/wafer is the product of good modules/wafer and the average selling price per module.
Good modules/wafer is the product of die-per-wafer and five yield ratios:

Good modules/wafer = available die-per-wafer X
process yield X die yield X
module-build yield X
module-test yield X
module burn-in yield.

A careful examination of the variables that drive each of the components of this equation reveals that those controlled by the fabricator: process yield, defect density, parametric yield, and module-build yield, combined with the design attributes of die size, layout critical area, fault tolerance, circuit-limited yield, binning yield, and test guardbands, drive this measure of manufacturing excellence. A similar analysis shows that the rate of yield learning is driven by the defect density learning rate and cycle time of the fabricator as well as the product's wafer start volume, wafer-to-package traceability and diagnosability. These analyses establish that design attributes strongly modulate those manufacturing excellence parameters which are expressed in economic terms.

Every design decision produces an economic consequence which is realized in the fabricator, in the marketplace, or in both. The challenge is to make the economic consequences of design decisions upon product productivity and profitability easily discernible at the time design decisions are made. To maximize fabricator productivity and organizational profitability, a product design must tradeoff product functionality and performance requirements with time-to-market and fabricator productivity opportunities. Hence, a detailed technical exchange between manufacturing and product development is required, and a robust design methodology that assures analysis of the tradeoffs between factors is essential.

DFM Within the Semiconductor Industry

Design-for-manufacturability philosophy and practices are used in many industries because it is recognized that 70% to 90% of overall product cost is determined before a design is ever released into manufacturing [2]. For non-semiconductor industries, these practices teach that the interface between design and manufacturing activities is very complex, and that an accurate cost model must be available at the time of each design iteration [3, 4]. The semiconductor industry recognizes that a technical dialogue between the design and manufacturing organizations is necessary for at least some product types [5]. However, the economic impact of design decisions upon product productivity and profitability has generally not been determined at the time design decisions must be made. Historically, the rapid gains in productivity driven by technology advances have largely obscured the need for design-driven productivity gains. The semiconductor industry will need a much stronger focus on DFM, or design-driven productivity gains, if the rate of technology-driven productivity improvements slows (as predicted) for future technologies [6]. Stated another way, a comprehensive DFM program can become a semiconductor supplier's competitive edge.

Many authors are surveying and advancing the state of DFM activities within the semiconductor industry [7, 8, 9]. Conferences like the IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems, the International Symposium on Physical Design, the SEMI/IEEE Advanced Semiconductor Manufacturing Conference and Workshop, and others are producing a large body of knowledge devoted to advancing the state of semiconductor-related DFM philosophy and practice [10, 11, 12].

Essential Elements of a Semiconductor DFM Program

Design-for-manufacturability activities asks the question: What are the consequences of each design decision upon the productivity of the design and asset utilization? Design activities which seek to optimize the profitability of a product, design-for-profitability activities, expand these questions to include: What is the impact of each design decision upon time-to-market, marketplace acceptance, and price of the product? A DFM program must be broad enough to consider both of these questions because the ultimate goal is to optimize the productivity and profitability of the entire design-manufacturing enterprise.

Figure 2 shows the elements of a semiconductor DFM program and relationships between the DFM program and manufacturing experience, observed market conditions, and product definition and design. The key elements of this program are: obtaining and assimilating knowledge from manufacturing and market sources, formulating and deploying detailed DFM-based design recommendations, developing and deploying DFM-based analysis and design tools as needed, and measuring the results in terms of implementation level and economic benefit.

The first task of a formal DFM program is the establishment of a process to continuously obtain the best knowledge available on productivity and profitability limiters from manufacturing and market sources. Manufacturing characterization and yield modeling activities can identify, in pareto chart format, those design attributes which systematically limit productivity. Design attributes which drive rework, limit tool throughput, slow the rate of yield learning, limit

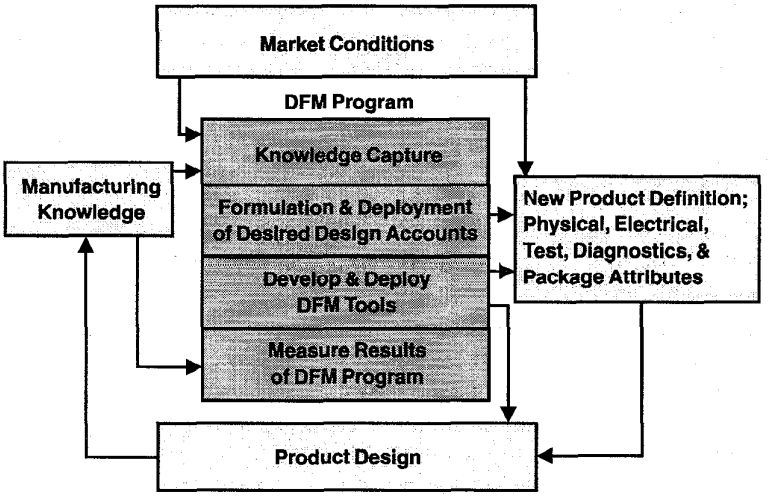

Figure 2. Elements of a DFM program

ultimate yield levels, or cause unnecessary nonrecurring engineering expenses are all correctable productivity inhibitors. Unnecessarily high critical area, inefficient redundancy schemes, inefficient chip aspect ratios, circuit and binning yield loss, lack of diagnostics, unique package and test requirements are additional examples of productivity inhibitors. Marketing sources identify those aspects of the design which limit market acceptance and depress market prices for the product. The design attributes which drive these profitability inhibitors may relate to product function, performance level, or time-to-market issues. Identifying design attributes which limit productivity and profitability is the easy part of a DFM program; this is simply a series of case studies of what has been vs what could have been achieved. Formulating and deploying a detailed set of DFM-based design recommendations and developing and deploying DFM-based tools is the real creative work of a DFM program.

The task of formulating DFM-based design recommendations is the second key element in a DFM program. This task starts with the productivity and profitability inhibitor charts described above and ends by identifying very specific changes to existing design practices and methodologies which affect the desired improvements in product productivity and profitability. DFM-based design recommendations can affect the physical, electrical, test, diagnostics, and packaging attributes of a product's design. In some cases, implementing these recommendations may not fit within the perceived mission of the design team (Figure 3), so the ultimate deployment plan for these DFM recommendations must also be considered during their formulation.

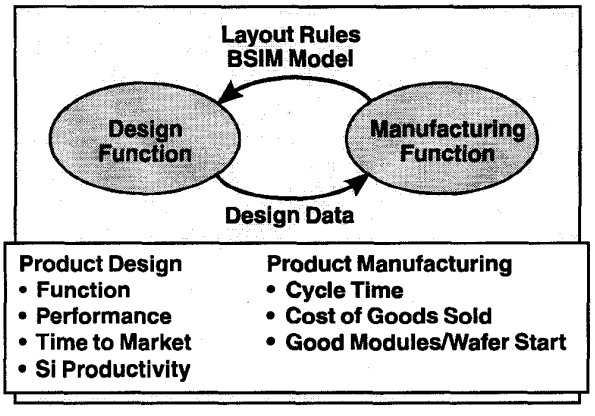

Figure 3. The design-manufacturing environment

Every recommended action must have a high perceived value to the design team or the prospects for its implementation will be slim. Reduced development expense, shortened time-to-market, improved product performance and reliability, and reduced product costs are the benefits of DFM actions which accrue to the design team. A DFM deployment team comprised of manufacturing and design engineers is best able to enumerate the full range of DFM-based design recommendations and their benefits to the product design audience. Implementation of some of the DFM recommendations will be contingent upon the availability of suitable design and analysis tools within the design organization.

The development and deployment of tools to support the objectives of the DFM program is the third key element of a DFM program. The DFM-based design recommendations will identify the need for a number of design-support tools which can provide detailed yield and performance modeling, measurements of the critical area of a layout at macro and chip level, layout modifications for yield enhancement, high levels of circuit simulation prior to fabrication, and detailed economic analysis of many DFM options. An accurate cost model was identified as a critical item in non-semiconductor DFM programs (as noted above). A cost model which provides the design team with a real time analysis capability of the economic impact of the technology, die size, wiring levels, packaging, and the many other design decisions which a design team must make, is an absolutely essential tool in a semiconductor industry DFM program. Providing the means to develop and integrate each of these analysis and modeling tools into the mainstream design methodology of the design organizations is a key challenge to the DFM program.

Ultimately the value of a DFM program must be "sold" to management. Sizing the overall opportunity for DFM-related productivity improvements, predicting the expected DFM benefits to a specific product, and measuring actual results is the fourth important element of a DFM program. The total value of the yield loss identified in the pareto charts created in element one is relatively easy to determine, and this represents the overall DFM opportunity for the organization. The economic benefits from DFM actions implemented in a specific product design will be realized either as the market value of the additional good product produced for an elastic market or as the cost avoided by processing

fewer wafers to produce a fixed volume of product for an inelastic market. Measurements of DFM progress may be expressed simply as the level of incorporation of DFM recommendations into designs over time, as productivity gains predicted from yield modeling, or as a measured level of productivity gain on individual products where data from split-lot experiments is available.

MEASURING AND MANAGING DFM IMPROVEMENTS

A 19-item DFM checklist has been deployed to the design organizations within IBM. A management review of the level of implementation of these items on new products is held before release to manufacturing, however the DFM philosophy recognizes that each of these productivity enhancement solutions will not fit all product design methodologies and goals. Overall implementation levels vary between product design groups, and span the range from 30% to 85%. Tools for back-end-of-the-line (BEOL) critical area analysis and layout modification are being developed and deployed by our EDA team and productivity increases on the order of 2% to 8% are being modeled for product designs that use these design tools. Performance modeling on these modified designs show performance improvements due to reduced BEOL capacitive loading of critical circuits. BEOL layout modification tools are also being employed to produce physical interconnect structures with improved reliability attributes.

Productivity enhancements of 10% to 97% have been demonstrated with split lots on specific products in production as a result of the application of DFM updates to existing product designs. Productivity enhancements on the order of 14% to 45% have been demonstrated by DFM designs using multichip reticles during prequalification hardware build on new product designs.

A characterization engineering team focused exclusively on improving good modules/wafer on selected products in high-volume production has achieved a 25% productivity gain that has been sustained over a period of two years. The correlation of in-line process and wafer-final test yield data with module yield data using electronic chip identification and other correlation means has justified process and product specification adjustments that are responsible for this productivity gain.

CONCLUSIONS

Manufacturing excellence is increasingly being measured in financial terms such as revenue per wafer and the production cost/good cm^2 of silicon. Significant and sustained productivity gains can be realized as the result of a systematic DFM program which focuses upon improving product productivity as measured by good modules/wafer. In practice, these design-driven productivity improvement activities improve yield learning rates, ultimate yield levels, reduce time-to-market, and can also enhance product performance and reliability.

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