Experimental Validation of Process-Induced Variability Aware SPICE Simulation Platform for Sub-20 nm FinFET Technologies

Amita Rawat, *Member, IEEE*, Neha Sharan, Doyoung Jang, Thomas Chiarella, Fabian M. Bufler, Francky Catthoor, Bertrand Parvais, and Udayan Ganguly, *Senior Member, IEEE*

***Abstract*— We propose an experimentally validated physics-based process-induced variability (PIV) aware SPICE simulation framework–enabling the estimation of performance variation due to line-edge-roughness (LER), metal-gate-granularity (MGG), random-dopant-fluctuation (RDF), and oxide-thickness-variation (OTV) at sub-20 nm technology node devices. The framework utilizes LER, RDF, OTV, and MGG defining parameters such as fin-edge correlation coefficient (ρ), autocorrelation length (Λ), grain-size (GS), σ[EOT], etc. as the inputs, and produces I_d–V_g distribution of ensemble size 250 as an output. We have validated the framework against 14 nm FinFET experimental data for I_d–V_g trends as well as for the threshold-voltage (V_T), ON-current (I_{ON}), and subthreshold slope (SS) distributions for a range of device dimensions with a reasonably good match. The worst and the best case R square errors are 0.64 and 0.98, respectively, for the validation. The very nature of the proposed framework allows the designers to use it for a vast range of process technologies. Such models are of dual importance, as it enables a PIV aware prediction of circuit-level performance, and provides a platform to estimate PIV parameters efficiently, on-par with sophisticated structural characterization tools.**

***Index Terms*— BSIM-CMG, design technology co-optimization (DTCO), experimental validation, FinFET, line-edge-roughness (LER), metal-gate-granularity (MGG), SPICE simulation, variability modeling.**

I. Introduction

OF ALL the process-induced-variability (PIV) sources, metal-gate-granularity (MGG) and line-edge-roughness (LER) are the two most dominant sources at sub-20 nm technology nodes [1] as shown in Fig. 1(b). The LER variation is further categorized into two forms; the fin-edge roughness (FER), which results in fin-width (W_{fin}) variation [i.e.,linewidth-roughness (LWR)], and the gate-edge-roughness (GER) results in channel length variation [i.e., gate-length-roughness (GLR)]. The LER parameters, specially the fin-edge-correlation coefficient (ρ), significantly vary from one lithography technology to another, and cause significant modulation in the effective fin-width ($W_{\text{fin-eff}}$). For various lithography technologies, such as the state-of-the-art extreme ultraviolet (EUV: $\rho \sim 0$), self-aligned-double patterning (SADP: $\rho \sim 0.9$) [2], etc. the LER and LWR relation as a function of ρ is shown in Fig. 1(c). Similarly, in the case of MGG, titanium nitride (TiN) is the most common work function (WF) metal being used in the high-κ metal gate (HKMG) gate-stack technology. Possible grain orientation and associated WF for TiN are listed in Table I [3].

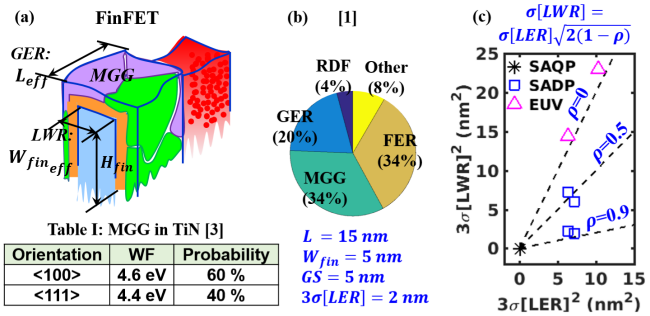


Table I: MGG in TiN [3]

Orientation	WF	Probability
<100>	4.6 eV	60 %
<111>	4.4 eV	40 %

Fig. 1. (a) Schematic of FinFET with PIVs. (b) % contribution of PIVs on V_T variability [1] for FinFET. (c) σ[LER], σ[LWR], and ρ for popular patterning techniques [2]. Table I: MGG parameters for TiN [3].

A physics-based analytical model is essential to enable an accurate and efficient computation of device-to-device performance variation due to PIVs. Impact of PIVs such as LER [4]–[6] (FER and GER) and MGG [1], [7]–[10] on device performance has been extensively explored using TCAD simulations as well as analytical models. Analytical models are better appreciated in predicting device-to-device performance variation as opposed to the computationally expensive TCAD simulations. The analytical models reported so far show good correlation with the TCAD simulations. However, none of the models show an experimental validation for advanced logic devices.

Manuscript received November 16, 2020; revised January 11, 2021 and January 14, 2021; accepted January 15, 2021. Date of publication February 8, 2021; date of current version February 24, 2021. This work was partially funded by Indian Institute of Technology Nano Fabrication Lab (IITBNF Lab), Ministry of Human Resource Development (MHRD), and Department of Science and Technology (DST). The review of this article was arranged by Editor Y. Chauhan. *(Corresponding author: Amita Rawat.)*

Amita Rawat and Udayan Ganguly are with the Department of Electrical Engineering, IIT Bombay, Mumbai 400076, India (e-mail: amitaiitb@ee.iitb.ac.in).

Neha Sharan, Doyoung Jang, Thomas Chiarella, and Fabian M. Bufler are with IMEC, 3001 Leuven, Belgium.

Francky Catthoor is with IMEC, 3001 Leuven, Belgium, and also with the Department of Electronics and Communication, Katholieke Universiteit Leuven (KU Leuven), 3000 Leuven, Belgium.

Bertrand Parvais is with IMEC, 3001 Leuven, Belgium, and also with the Department of Electronics and Communication, Vrije Universiteit Brussel, 1050 Brussel, Belgium.

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TED.2021.3053185.

Digital Object Identifier 10.1109/TED.2021.3053185

In our previous work, a compact model for LER [6] and an analytical model for MGG [8] are reported. In the LER model, Λ, σ[LER], and ρ are utilized to accurately mimic the fin-edge profile. Further, the short channel and quantum confinement (QC) effects are modeled in the form of threshold voltage as a function of fin-width (W_{fin}), such as $V_T(W_{\text{fin}})$. Finally, a percolation-based model is used to estimate the effective V_T by building a local width-dependent resistive network. Similarly, in the case of MGG model, Voronoi algorithm is used to assign a realistic grain position, and a binary distribution is used to model grain occurrence probability, using which random work-function boundary condition is estimated. Finally, an electrostatic potential (EP) profile is obtained by solving 3-D Laplace equation using previously estimated boundary conditions for the fin. Doing so, the grain-position-dependent potential perturbation is accurately captured in the EP profile in the fin [8]–the variation in the barrier height due MGG is accurately captured.

In this work, the previously presented LER and MGG models along with random-dopant-fluctuation(RDF) and oxide-thickness-variation (OTV) effects are incorporated in the BSIM-CMG [11] platform, and a PIV aware SPICE simulation framework is presented. At first, all the relevant PIV sources are categorized on the basis of their impact on the device performance parameters; for example, variation in the subthreshold slope (SS) is an outcome of LER, RDF, and OTV like PIV sources. Further, the contribution of each PIV sources in defining the device-to-device variability, and respective PIV parameters are estimated. These PIV parameters are fixed for a process-technology. Finally, the estimated parameters are used to predict the V_T, I_{ON}, SS distributions for W_{fin}, and L scaling to show an agreement with respective experimental data–to demonstrate an experimentally validated predictive PIV aware SPICE simulation framework.

II. Methodology

A. Set of Assumptions

To simplify the estimation of PIV parameters from the experimental data, a few sets of assumptions, as follows, are made:

1) **Random dopant fluctuation (RDF):** The effect of RDF in the channel is considered to be negligible, as the channel is assumed to be undoped. However, the effect of the dopant diffusion from the source/drain into the channel is modeled as L modulation [12].
2) **Oxide thickness variation (OTV):** An oxide thickness variation is added as a tuning parameter to correctly estimate the SS variability.
3) The FER, GER, RDF, and OTVPIV sources are assumed to be independent of MGG.
4) Variability in SS is majorly governed by LER, RDF, and OTVPIV sources as opposed to MGG [13].

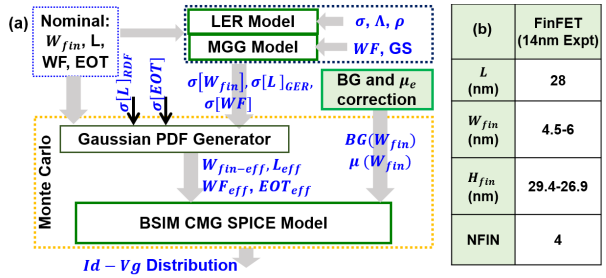
B. PIV Model

1) **LER (FER and GER) Model:** In LER model, the key LER parameters (i.e., Λ, 3σ[LER], and ρ) and the device dimensions, such as fin width (W_{fin}), channel length (L), and fin height (H_{fin}) are utilized as the inputs to generate the standard deviation of W_{fin} and L (i.e., $\sigma[W_{\text{fin}}]$, and $\sigma[L]$) as the outputs [6]. Equation(1) shows the $\sigma[W_{\text{fin}}]$ expression [6] used in the framework

$$\Delta W_{\text{avg}}(x) = \frac{C\sigma[\text{LER}]\sqrt{\Lambda(1-\rho)\sqrt{\pi}}}{L_G\sqrt{2}} \times \left[\text{erf}\left(\frac{\sqrt{2}}{\Lambda}\left(x+\frac{L_G}{2}\right)\right) - \text{erf}\left(\frac{\sqrt{2}}{\Lambda}\left(x-\frac{L_G}{2}\right)\right)\right]$$
$$\sigma[W_{\text{avg}}] = \text{std}\big(\Delta W_{\text{avg}}(x)\big). \quad (1)$$

2) **MGGModel:** In MGG model, the device dimensions, grain size (GS), and associated WFs are used as the inputs to generate the σ[WF] as an output [8]. The MGG model is implemented in the MATLAB and the estimated σ[WF] is used in the BSIM-CMG framework to perform MonteCarlo simulations.
Note: Impact of any other variability sources which can cause gate potential perturbation are cumulatively considered as an effective MGG, and based on which the effective GS is evaluated.
3) **Incorporating RDF effect:** The effect of RDF is modeled as channel length modulation (CLM) due to random diffusion of the dopant from the source/drain into the channel. The CLM effect due to RDF is realized by adding a $\sim 4\%$ L variability in addition to GER-induced L variation. The percentage variation in the L is chosen such that the resultant $\sigma[V_T]$ due to RDF is maintained $<= 10$ mV [12].
4) **Incorporating OTV effect:** A $\sim 5\%$ oxide thickness variation is added to address the oxide thickness variability [14], [15].

Out of all the PIV sources, only the impact of LER (FER and GER) and MGG is analytically modeled. A detailed description of the analytical models is reported in our previous work [6], [8]. The RDF and the OTV, not so dominant PIV sources [Fig. 1(b)], are modeled mathematically using Gaussian distribution. We have calibrated the BSIM-CMG for nominal performance, and for a range of width and length variation with respect to TCAD. The calibration of BSIM-CMG parameters is done, specific to the targeted technology node. To capture the QC effects, QMFACTOR is enabled; DVT0 and DVT1 parameters are calibrated to incorporate short channel effects; saturation threshold voltage (VSAT) and VSAT1 parameters are calibrated to capture velocity saturation effects; PHIG is used to match the work-function of the device; UA and EU parameters are used to calibrate the model on phonon scattering; PCLM parameter is used to capture the channel length modulation effect; SS correction is done using DVT1SS parameter. Calibrating the core BSIM-CMG model file on fundamental device physics ground, bandgap (BG) [16] and mobility (μ) [17] corrections are also made to enable W_{fin} sensitivity and to accurately capture the QC physics in the BSIM-CMG using the empirically fitted (2) and (3), respectively, and fed in the BSIM-CMG model using U0 and



(b)	FinFET (14nm Expt)
L (nm)	28
W_{fin} (nm)	4.5-6
H_{fin} (nm)	29.4-26.9
NFIN	4

Fig. 2. (a) Flow of the PIV aware SPICE framework. (b) Device dimensions used in this work associated with 14 nm technology nodes. It is noted that the device dimensions presented here acts as a reference to 14 nm technology node are the dimensions experimentally measured for the FinFET devices [18].

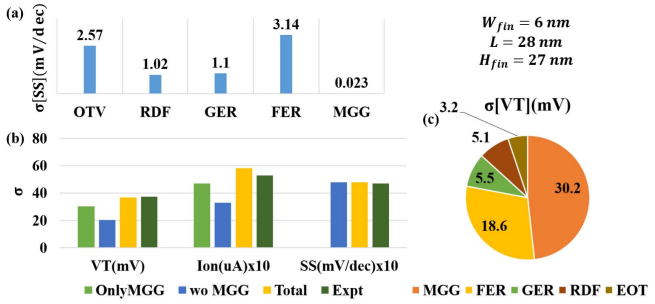


Fig. 3. (a) Comparison of $\sigma[SS]$ among all the PIV sources. (b) Comparison of $\sigma[V_T]$, $\sigma[I_{ON}]$, and $\sigma[SS]$ for with and without enabling MGG effects against the experimental data. (c) Bar plot defining the contribution of $\sigma[V_T]$ component corresponding to each PIV sources.

PHIG parameters, respectively

$$BG(W_{\text{fin}}) = 0.97 + \frac{24.34}{(W_{\text{fin}} + 1.16)^2} \tag{2}$$

$$\mu(W_{\text{fin}}) = 112.8 - \frac{632.5}{W_{\text{fin}}^2} \tag{3}$$

$$\frac{1}{\mu_{\text{new}}} = \frac{1}{\mu_{\text{old}}} + \frac{1}{\mu(W_{\text{fin}})}. \tag{4}$$

The $\sigma[W_{\text{fin}}]$, $\sigma[L]$, $\sigma[\text{WF}]$, and $\sigma[\text{EOT}]$ generated from the models are further used to generate Gaussian probability density functions (PDFs) of W_{fin}, L, effective oxide thickness (EOT), and WF. Finally, the generated PDFs are used to run MonteCarlo SPICE simulations using the BSIM-CMG model. The flow of the framework is summarized in Fig. 2(a). The device dimensions extracted experimentally for the 14-nm FinFET devices are listed down in Fig. 2(b).

III. Results and Discussion

At first, the framework is used to estimate PIV parameters associated with the process technology used to fabricate the FinFET devices for a given set of nominal device dimensions (e.g., $W_{\text{fin}} = 6$ nm, $L = 28$ nm, and $H_{\text{fin}} = 26.9$ nm). Further, using the estimated process-technology specific PIV parameters, the framework is validated for W_{fin} and L splits.

A. PIV Number Estimation Using Experimental Data

The framework is used to study the impact of each of the PIV sources independently on $\sigma[SS]$ variability as shown in Fig. 3(a). A negligible impact of MGGon $\sigma[SS]$ is observed as opposed to other PIV sources (i.e., FER, GER, RDF, and OTV). The subthreshold behavior, or the channel electrostatics in subthreshold region, is relatively more sensitive to the device geometry, and the gate-oxide thickness, as opposed to gate metal WF, which results in a weak impact of MGGon $\sigma[SS]$ [19], [20]. The interrelatedness of LER, RDF, and OTV has made the separation of these PIV sources from experimental data, practically infeasible. However, due to the targeted impact of MGGon I_{ON} and V_T variability, and insignificant impact of SS variation has enabled the MGG parameter extraction. Impact of PIV sources on $\sigma[V_T]$, $\sigma[I_{\text{ON}}]$, and $\sigma[SS]$ is compared for two hypothetical cases using the proposed framework against experimental data shown in Fig. 3(b). Case I: Only MGG effects are enabled; Case II: Only

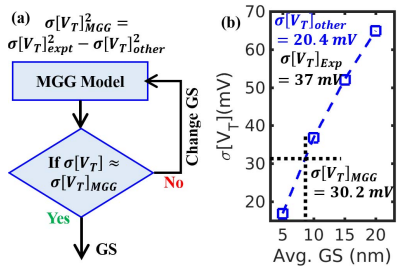


Fig. 4. (a) Methodology flow used to estimate the MGG contribution and respective GS. (b) Extraction of the GS using the $\sigma[V_T]$ versus Avg. GS trend.

MGG effects are disabled. In the case where only MGG effects are enabled, a negligible $\sigma[SS]$ is observed, as opposed to a significant $\sigma[SS]$ in the case II where only MGG effects are disabled (i.e., only FER, GER, RDF, and OTV are present). A significant $\sigma[SS]$ is observed in the experimental data, which can be assumed to be due to PIV sources like LER, RDF, and OTV. The LER (FER and GER) parameters for the targeted process technology (i.e., the process technology used in the 14-nm FinFET devices) are as follows: 1) $3\sigma[\text{LER}]$=2.5 nm; 2) $\Lambda = 80$ nm; and 3) $\rho = 0.7$ [21]. Keep the LER parameters fixed, the OTV and RDF parameters are adjusted such that the desired $\sigma[SS]$ is achieved. Once, the LER, RDF and OTV parameters are fixed, the $\sigma[V_T]_{\text{other}} = 20.2$ mV is used to calculate the $\sigma[V_T]_{\text{MGG}} = 31$ by subtracting the variance as shown in Fig. 4(a). Using the $\sigma[V_T]_{\text{MGG}}$, metal GS is back estimated as 9 nm from the MGG model as shown in Fig. 4(b). The estimated GS from the model is very-well aligned with GS extracted from the transmission electron microscopic (TEM) image of the gate-stack in 14-nm FinFET devices, as shown in Fig. 5. The estimated PIV parameters are well within the range of previously reported values [1]. The contribution of each PIV sources in deciding the net $\sigma[V_T]$, is plotted in Fig. 3(c). From the figure, it is evident that the major contributors of the V_T variability are MGG and LER (FER and GER) like variability sources. Going forward, we fix these PIV parameters, and further validate the framework for a range of device dimensions.

B. Validation

To validate the proposed framework, splits of W_{fin} and L from the 14-nm FinFET experimental data [18] are used.

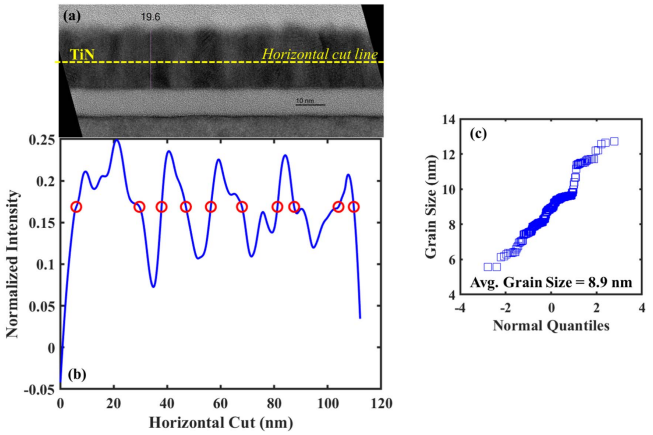


Fig. 5. (a) TEM image of the TiN used as gate metal as a part of gate-stack in the experimental FinFET devices. (b) Horizontal-cut RGB intensity mapping of the grain pattern arrangement in the TiN layer, where red circles are marking the grain-boundaries. (c) GS statistics extracted from the TEM image representing the GS distribution and average GS.

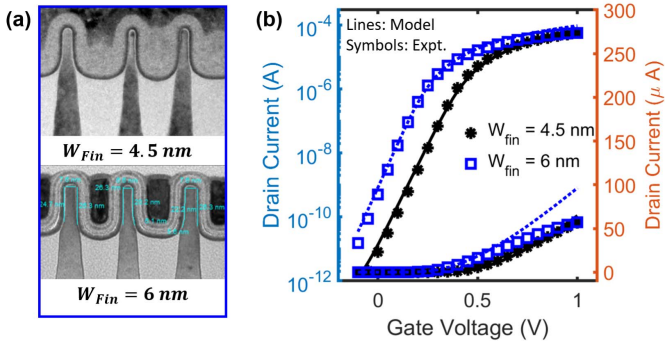


Fig. 6. (a) SEM images ($W_{\text{fin}} = 4.5$ and 6 nm) of 14 nm FinFET used for validating the platform [18] used for validation of the model. (b) Mean I_d–V_g trend generated using the SPICE simulation setup and compared against experimental I_d–V_g.

In Fig. 6(a), the scanning electron microscopic (SEM) images of $W_{\text{fin}} = 4.5$ nm and $W_{\text{fin}} = 6$ nm FinFET devices are shown. In Fig. 6(b) nominal I_d–V_g curves for $W_{\text{fin}} = 4.5$ nm and $W_{\text{fin}} = 6$ nm FinFET devices are plotted alongside with the I_d–V_g curves generated from the SPICE simulation to show an acceptable match. The observable mismatch in the ON-current is due to parasitic resistance, and the mismatch in the SS is due to ignoring the band-to-band tunneling effects, that is the gate-induced-drain-leakage model, in the core BSIM-CMG file. The ensemble size of the I_d–V_g distribution estimated from the framework is 250 devices. To eliminate the global variability in the experimental data, we have used ΔVT_{sat} ($\Delta VT_{\text{sat}} = V_{T-\text{device1}} - V_{T_{\text{device2}}}$), instead of absolute V_T, where device1 and device2 are two side-by-side fabricated FinFET [18].

In Fig. 7, we have shown a quantitative comparison between experimentally measured I_d–V_g distribution, against that of estimated from the proposed framework. The ΔVT_{sat} distributions generated from the SPICE simulation platform is validated against their experimental counterpart to show a good agreement. The comparison is made for three different cases-Fig. 7(a) $W_{\text{fin}} = 6$ nm and $L = 28$ nm; Fig. 7(b) $W_{\text{fin}} = 4.5$ nm and $L = 28$ nm; Fig. 7(c) $W_{\text{fin}} = 6$ nm and $L = 34$ nm so that the framework can be validated for a range

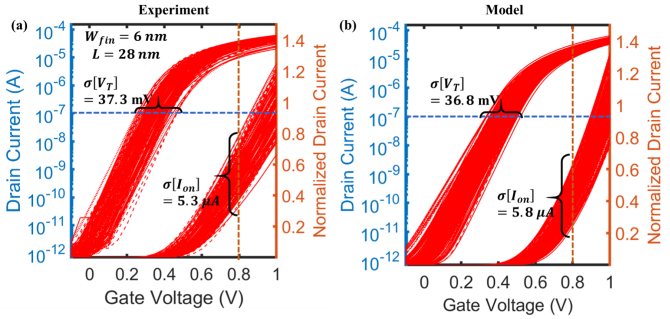


Fig. 7. Distribution of the I_d–V_g trends (a) experimentally measured and (b) estimated using the proposed framework for device with $W_{\text{fin}} = 6$ nm, $L = 28$ nm, and $H_{\text{fin}} = 27$ nm, and extracted variability parameters.

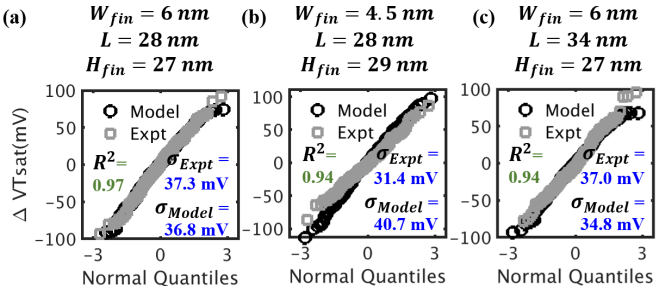


Fig. 8. ΔVT_{sat} distributions estimated from the framework are compared against the 14 nm FinFET experimental data for (a) $W_{\text{fin}} = 6$ nm and $L = 28$ nm. (b) $W_{\text{fin}} = 4.5$ nm and $L = 28$ nm to show width scaling. (c) $W_{\text{fin}} = 6$ nm and $L = 34$ nm to show channel length scaling.

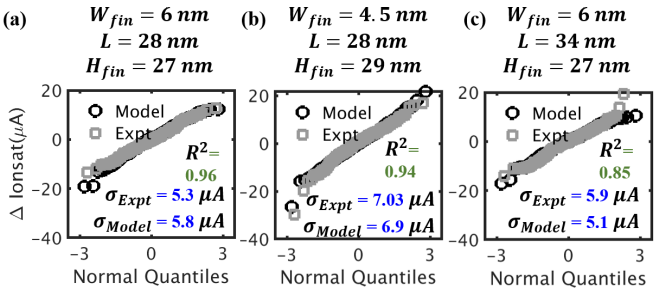


Fig. 9. $\Delta I_{\text{ON,sat}}$ distributions estimated from the framework are compared against the 14 nm FinFET experimental data for (a) $W_{\text{fin}} = 6$ nm and $L = 28$ nm. (b) $W_{\text{fin}} = 4.5$ nm and $L = 28$ nm to show width scaling. (c) $W_{\text{fin}} = 6$ nm and $L = 34$ nm to show channel length scaling.

of L as well as in the strong QC regime, as shown in the Fig. 8. In Fig. 8(b), where strong QC is expected, the estimated $\sigma[V_T]$ is significantly off as opposed to respective experimental data, which is to be investigated further.

Further, we have presented a validation for the ON-current ($\Delta I_{\text{ON,sat}}$) in each of the above-mentioned case. The respective ion distributions are estimated from the framework and compared against the experimental data, as shown in Fig. 9. The framework captures the distribution reasonably well in all the three cases with worst case R^2 error as 0.85.

Next, a comparison of SS distributions for all the three cases are presented against its experimental counterpart to show a decent match with worst case R^2 error as 0.64, as shown in Fig. 10. Finally, we have generated a Pelgrom plot and compared it against the experimental data [18] to show the capture of area-scalability in the proposed framework, as shown in Fig. 11.

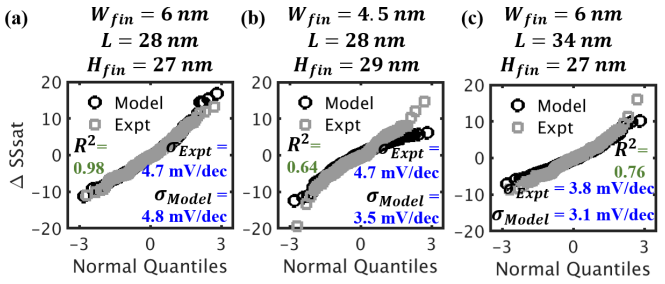


Fig. 10. ΔSS distributions estimated from the framework are compared against the 14-nm FinFET experimental data for (a) $W_{fin} = 6$ nm and $L = 28$ nm. (b) $W_{fin} = 4.5$ nm and $L = 28$ nm to show width scaling. (c) $W_{fin} = 6$ nm and $L = 34$ nm to show channel length scaling.

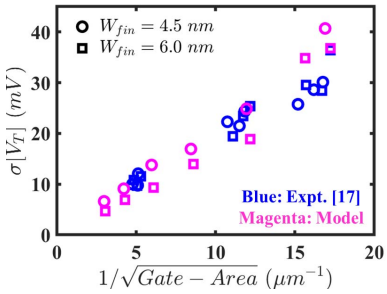


Fig. 11. Pelgrom plot reflecting the area scalability of the PIVs comparing the model with the experimental data.

By doing such extensive validation, we have established that the model is capable of predicting the performance parameter distributions over a range of device dimensions, that is the framework is compatible with device dimension scaling. The PIV aware SPICE simulation framework shows good match with the worst and the best cases R^2 errors as 0.64 and 0.98, respectively. It is to be noted that during the entire course of validation, the PIV parameters are fixed to the values estimated from the electrical data. Because, even if the nominal device dimensions have changed, PIV parameters, the process-dependent entities, must not change.

IV. Conclusion

A PIV aware SPICE simulation framework uses our in-house LER and MGG models, and a well-calibrated BSIM-CMG model is proposed. A methodology to estimate PIV parameters using the proposed framework from the 14-nm FinFET experimental I_d–V_g data is demonstrated. The estimated PIV parameters are on par with the equivalent results estimated from sophisticated structural characterization tools. Further, a detailed validation of the simulation setup for a range of device dimensions against the experimental data is presented to show good agreement with R^2 error ranging from 0.64 to 0.98. The proposed framework eliminates the dependence on TCAD simulators, which are time-consuming, and computationally complex, while studying the impact of PIVs on device-to-device performance variation. Despite all the positive aspects, the proposed framework is not yet self-sufficient, and requires MGG inputs externally from the MATLAB. Such a framework provides a direct technological insight to the circuit designers, and assists the process engineers to better decide the fabrication steps–facilitates a platform for design-technology–cooptimization.

References

[1] X. Wang, A. R. Brown, B. Cheng, and A. Asenov, "Statistical variability and reliability in nanoscale FinFETs," in *IEDM Tech. Dig.*, Dec. 2011, pp. 5.4.1–5.4.4.

[2] A. Rawat, S. Mittal, and U. Ganguly, "An analytical model to estimate V_T distribution of partially correlated fin edges in FinFets due to fin-edge roughness," *IEEE Trans. Electron Devices*, vol. 64, no. 4, pp. 1708–1715, Apr. 2017.

[3] H. Nam and C. Shin, "Study of high-*k*/metal-gate work-function variation using Rayleigh distribution," *IEEE Electron Device Lett.*, vol. 34, no. 4, pp. 532–534, Apr. 2013.

[4] K. Patel, "Intrinsic and systematic variability in nanometer CMOS technologies," Ph.D. dissertation, Dept. Electron. Commun., UC Berkeley, Berkeley, CA, USA, 2010.

[5] X. Jiang, X. Wang, R. Wang, B. Cheng, A. Asenov, and R. Huang, "Predictive compact modeling of random variations in FinFET technology for 16/14 nm node and beyond," in *IEDM Tech. Dig.*, Dec. 2015, pp. 28.3.1–28.3.4.

[6] A. Rawat, S. Mittal, and U. Ganguly, "The first compact model to determine V_T distribution for DG-FinFET due to LER," *IEEE Trans. Electron Devices*, vol. 65, no. 11, pp. 4772–4779, Nov. 2018.

[7] H. Dadgour, K. Endo, V. De, and K. Banerjee, "Modeling and analysis of grain-orientation effects in emerging metal-gate devices and implications for SRAM reliability," in *IEDM Tech. Dig.*, Dec. 2008, pp. 1–4.

[8] P. H. Vardhan, S. Mittal, S. Ganguly, and U. Ganguly, "Analytical estimation of threshold voltage variability by metal gate granularity in FinFET," *IEEE Trans. Electron Devices*, vol. 64, no. 8, pp. 3071–3076, Aug. 2017.

[9] S. Agarwal *et al.*, "Ab initio study of metal grain orientation-dependent work function and its impact on FinFET variability," *IEEE Trans. Electron Devices*, vol. 60, no. 9, pp. 2728–2733, Sep. 2013.

[10] G. Indalecio, A. J. Garcia-Loureiro, M. Aldegunde, and K. Kalna, "3D simulation study of work-function variability in a 25 nm metal-gate FinFET with curved geometry using Voronoi grains," in *Proc. 17th Int. Conf. Simulation Semiconductor Devices (SISPAD)*, 2012, pp. 149–152.

[11] Y. S. Chauhan *et al.*, *FinFET Modeling for IC Simulation and Design: Using the BSIM-CMG Standard*. New York, NY, USA: Academic, 2015.

[12] S. Markov, A. S. M. Zain, B. Cheng, and A. Asenov, "Statistical variability in scaled generations of n-channel UTB-FD-SOI MOSFETs under the influence of RDF, LER, OTF and MGG," in *Proc. IEEE Int. SOI Conf. (SOI)*, Oct. 2012, pp. 1–2.

[13] Z. Zhang, X. Jiang, R. Wang, S. Guo, Y. Wang, and R. Huang, "Extraction of process variation parameters in FinFET technology based on compact modeling and characterization," *IEEE Trans. Electron Devices*, vol. 65, no. 3, pp. 847–854, Mar. 2018.

[14] A. Veloso *et al.*, "Gate-last vs. gate-first technology for aggressively scaled EOT logic/RF CMOS," in *Symp. VLSI Technol., Dig. Tech. Papers*, 2011, pp. 34–35.

[15] K. Endo *et al.*, "Variability analysis of TiN metal-gate FinFETs," *IEEE Electron Device Lett.*, vol. 31, no. 6, pp. 546–548, Jun. 2010.

[16] H. Yoshioka, N. Morioka, J. Suda, and T. Kimoto, "Bandgap shift by quantum confinement effect in (100) Si-nanowires derived from threshold-voltage shift of fabricated metal-oxide-semiconductor field effect transistors and theoretical calculations," *J. Appl. Phys.*, vol. 109, no. 6, 2011, Art. no. 064312.

[17] K. Uchida, H. Watanabe, A. Kinoshita, J. Koga, T. Numata, and S. Takagi, "Experimental study on carrier transport mechanism in ultrathin-body SOI NAND p-MOSFETs with SOI thickness less than 5 nm," in *IEDM Tech. Dig.*, 2002, pp. 47–50.

[18] M. S. Bhoir, T. Chiarella, L. A. Ragnarsson, J. Mitard, N. Horiguchi, and N. R. Mohapatra, "Variability sources in nanoscale bulk FinFETs and TiTaN-a promising low variability WFM for 7/5 nm CMOS nodes," in *IEDM Tech. Dig.*, Dec. 2019, pp. 36.2.1–36.2.4.

[19] Z. Zhang, R. Wang, X. Jiang, X. Wang, Y. Wang, and R. Huang, "A comprehensive extraction method to decompose different random variation impacts in bulk FinFET technology," in *Proc. 14th IEEE Int. Conf. Solid-State Integr. Circuit Technol. (ICSICT)*, Oct. 2018, pp. 1–3.

[20] X. Jiang *et al.*, "A device-level characterization approach to quantify the impacts of different random variation sources in FinFET technology," *IEEE Electron Device Lett.*, vol. 37, no. 8, pp. 962–965, Aug. 2016.

[21] G. F. Lorusso, O. Inoue, T. Ohashi, E. A. Sanchez, V. Constantoudis, and S. Koshihara, "Line width roughness accuracy analysis during pattern transfer in self-aligned quadruple patterning process," *Proc. SPIE*, vol. 9778, Mar. 2016, Art. no. 97780V.