Process Enabler and Design Opportunities for Fully Safeguarding Against the Massive Presence of Reliability Defects

Lieyi Sheng
ON Semiconductor
2300 Buckskin Road, Pocatello, ID 83201, USA
Lieyi.Sheng@onsemi.com

2021 32nd Annual SEMI Advanced Semiconductor Manufacturing Conference (ASMC) | 978-1-7281-8645-0/20/$31.00 ©2021 IEEE | DOI: 10.1109/ASMC51741.2021.9435679

***Abstract* — We have simultaneously addressed two major challenges in semiconductor reliability engineering. One is how to characterize a genetically defective component with a massive presence of reliability defects. The other is how to passivate all the defects for measuring up to our ultimate goal of zero failures in the field. This paper highlights a decade-long case study and follow-up on many millions of IC (integrated circuit) shipments. Our insightful characterizations of defects have enabled the process maturation and the discovery of a novel design-for-reliability (DfR). Correspondingly, the mitigating measures have suppressed defects by several orders of magnitude and resulted in zero returns from a broad range of customers. Furthermore, our collective approach promises the narrative of our Road to Zero Defects, where the sky is the limit.**

Keywords* — *Reliability defects, defect characterization, process improvement, design for reliability, case studies, and zero defects

I. Introduction

Defects are common in manufacturing. They can come from various sources and in different forms and sizes. The most common type of defects is particles. In a Class 3 cleanroom for wafer-manufacturing, a cubic meter of air is allowed to contain 1,000 particles that are 0.1 micron or larger in diameter. For example, a ball-like particle from an air filtration system can become a defect after it falls and gets trapped between metal lines. Meanwhile, defects do not necessarily originate from environments. For example, a whisker-like defect can extrude from an aluminum surface. A wafer-manufacturing process often requires several hundreds of operations over a span of several weeks or months. Furthermore, a variety of materials and chemicals are extensively used in many of the complex tools. Consequently, defects are essentially unavoidable during the fabrication of semiconductor products.

Often, manufacturing defects can cause yield losses. Some defects can also escape functionality tests at product sort, but later incur reliability liability due to failures at customers. Starting from PPM (parts per million) in product failure rates a decade ago, every semiconductor company is now striving and competing at quality levels of PPB (parts per billion).

This paper presents, in the narrative of zero defects as our ultimate goal of quality and reliability, a decade-long exploration and confirmation of effectively safeguarding against massive defects in achieving zero customer returns.

II. Genetically Massive Presence of Defects

Due to their simple integration into backend-of-line (BEOL) processing, polysilicon-insulator-polysilicon capacitors (PIPCs) (Fig. 1) have been widely used in integrated circuit (IC) products. However, a polysilicon (poly-Si) surface is genetically very defective, if not the most defective, in the presence of numerous and variable grains, grain boundaries, and projections (Fig. 2). It was first demonstrated [1] that the bottom oxide-polysilicon interface, formed with the conformity of inter-poly oxide, was rougher and more defective than the top interface. Both poly-Si plates were heavily doped with phosphorus. Deposited using PECVD (plasma enhanced chemical vapor deposition), the dielectric oxide layer was 400 Å in thickness.

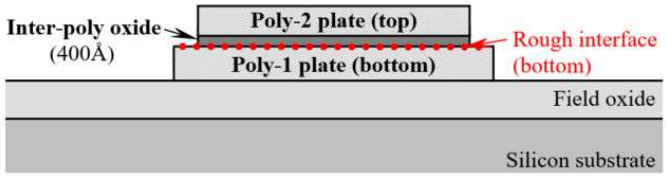
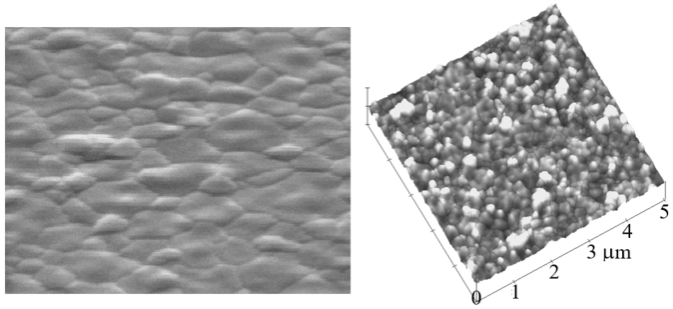


Fig. 1. Cross-sectional schematic of PIPC with a rough interface at the bottom.



(a) In-line SEM picture (b) 3D AFM picture

Fig. 2. Pictures of a poly-silicon surface using (a) in-line SEM (scanning electron microscopy), and (b) 3D AFM (atomic force microscopy).

For assessing the PIPC robustness in reliability, three test structures (Fig. 3), in a single capacitor or in an array of capacitor units, were available for mimicking various designs and uses in IC products. In a common or default setting, a positive voltage is applied at the poly-2 plate (top) while the poly-1 plate (bottom) is grounded. Such a use or test configuration is called a normal bias or in normal terminals.

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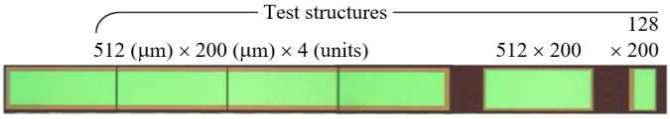


Fig. 3. Three test structures were available for assessing the PIPC robustness.

The PIPCs were extensively proven to be robust enough for a typical use voltage (V_{use}) at 5.0V. However, the long tails along the breakdown voltage (V_{bd}) distributions raised significant concern over their reliability at higher use voltages (incl., 12V and 20V; often used for automotive products) (Fig. 4). Meanwhile, the TDDB (time dependent dielectric breakdown) data showed poor distributions (Fig. 5). The Weibull slopes (β) were flat at only 0.52, which indicated reliability risks at lower failure percentiles (in PPM or PPB).

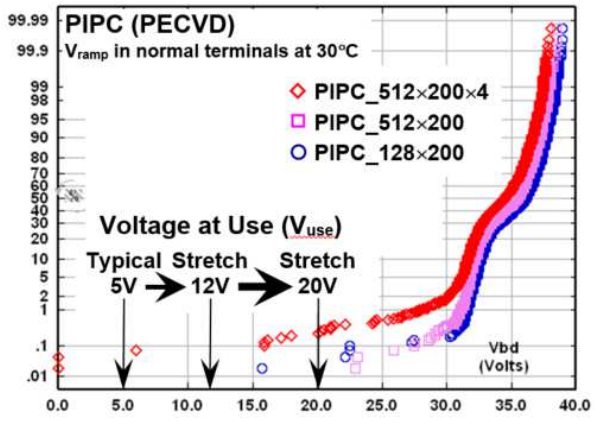


Fig. 4. Breakdown voltage distributions for the PIPCs with PECVD. The long tailing in the breakdown voltage (V_{bd}) was a significant reliability concern for higher use voltages (such as 12V and 20V) than a typical V_{use} at 5.0V.

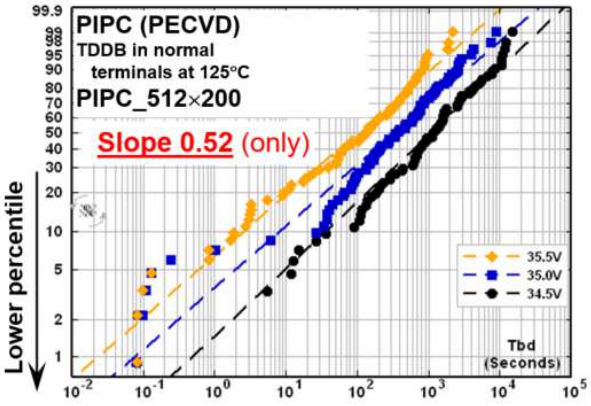


Fig. 5. TDDB plot for the PIPC with PECVD: Very flat Weibull slopes raised concerns over reliability. For a typical 400-Å-thick dielectric without a defectivity issue, the Weibull slope is expected to be more than 3.0.

III. Process Improvement

From a failure analysis, a defect was found to be enclosed by the PECVD oxide layer, where local oxide-thinning was observed along the sidewalls of the defect (Fig. 6). Having suspected that the PECVD process might be too directional and less conformal in step coverage, we experimented with LPCVD (low pressure chemical vapor deposition) for depositing the inter-poly oxide.

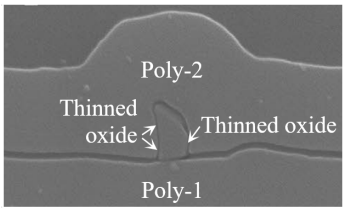


Fig. 6. SEM picture of a PIPC defect enclosed by the PECVD oxide layer. A local thinning of oxide was observed along the sidewalls of the defect.

For the LPCVD, testing large samples (>10,000) on the three PIPC structures confirmed that there were zero reliability defects ($5V<V_{bd}<30V$) along the V_{bd} distributions (Fig. 7). Therefore, the use of LPCVD oxide appeared to have significantly passivated the massive presence of defects along the bottom interface.

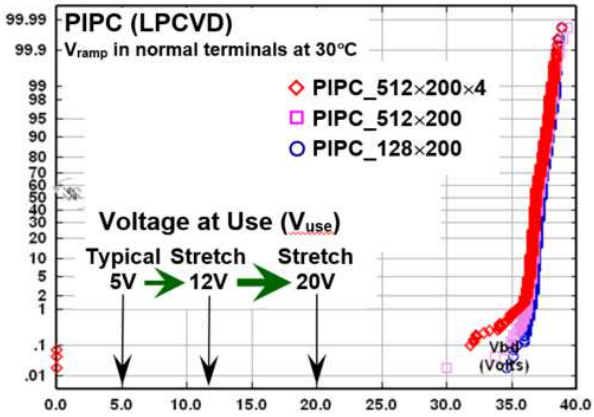


Fig. 7. Breakdown voltage distributions for the PIPCs with LPCVD. The PIPCs with LPCVD were free of reliability defects from 5V up to 30V.

Meanwhile, the Weibull slope β in TDDB was also improved to 1.17 (Fig. 8), which more than doubled the 0.52 associated with the PECVD oxide (Fig. 5). Such a drastic improvement in process robustness has clearly eased reliability concerns over stretching the use voltage beyond the typical 5.0V. As illustrated in Fig. 9, an improved Weibull slope β can have a drastic impact on the failure rate. For example, for a β ratio of 2.0 (i.e., 1.0/0.5), the failure rate is improved by four orders of magnitude; or equivalently from 100 PPM to 10 PPB.

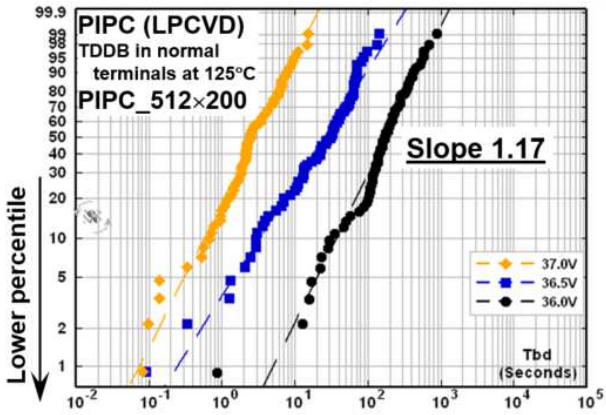


Fig. 8. The clearly improved Weibull slopes on the TDDB plot for the PIPC with LPCVD.

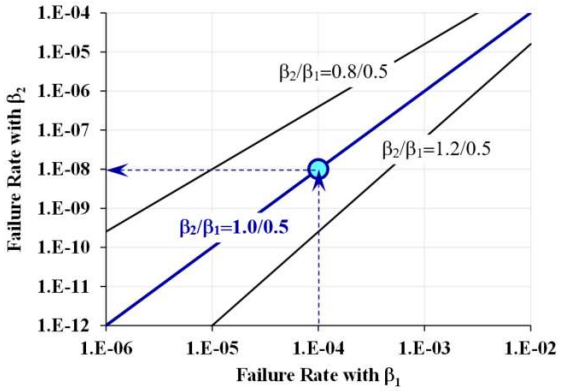
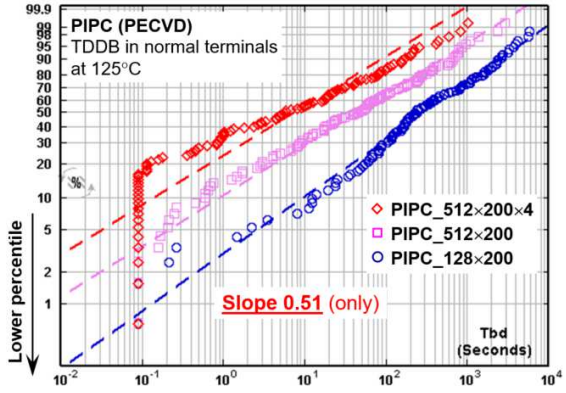


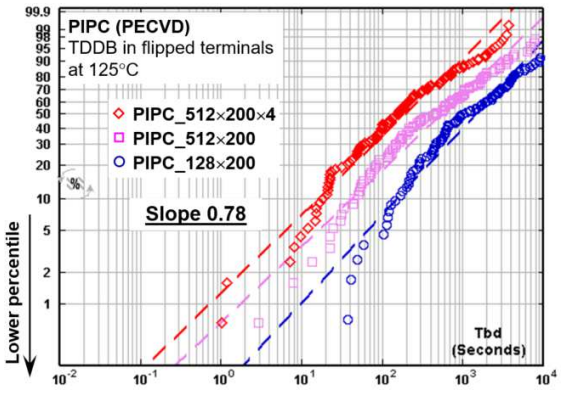
Fig. 9. An improved Weibull slope β can have a profound impact on the failure rate (F). Weibit W=ln(-ln(1-F)), where F is the failure rate, is proportional to the Weibull slope β. For example, for a β ratio β_2/β_1 at 1.0/0.5, the failure rate is improved from 100 PPM (with β_1) to 10 PPB (with β_2).

IV. Polarity Dependence in Defectivity

When applied on poly-2 with poly-1 grounded, a positive voltage is called a normal bias. On the contrary, a positive voltage applied on poly-1 with poly-2 grounded is called a flipped bias. Figure 10 compares the TDDB results of PIPCs with PECVD under the two different test polarities. Consistently for all the three test structures, much steeper Weibull slopes were observed under the flipped bias [Fig. 10(b)] than under the normal bias [Fig. 10(a)].



(a) Normal bias (Poly-2 plate at "+")



(b) Flipped bias (Poly-1 plate at "+")

Fig. 10. PIPC with PECVD: Much steeper Weibull slopes were observed under the flipped bias (b) than under the normal bias (a). The stress voltage was 34V.

For the PIPCs with LPCVD (Fig. 11), similar differences in TDDB were also observed under the different test polarities. In general, steeper slopes were achieved for the PIPCs using LPCVD.

Both poly plates were heavily doped with phosphorus (i.e., n-type dopant), so a normal bias induced a charge accumulation along the bottom interface, which embossed the existence of defects there. Meanwhile, a flipped bias caused a depletion and masked the defects to some extent. Clearly, we have demonstrated that a simple flip of device terminals significantly improves TDDB distributions. As a result, the low-percentile failure rates can be reduced by orders of magnitude.

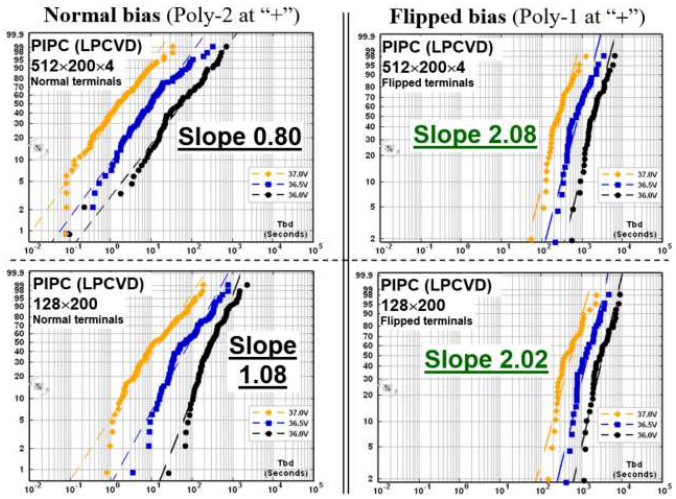


Fig. 11. PIPCs with LPCVD: Much steeper Weibull slopes in flipper terminals. The best β value was realized in the PIPCs with LPCVD under the flipped bias.

V. Discussion

Figure 12 lists in detail the options in developing IC products with a reliable PIPC implementation. For example, the use of LPCVD (❶) has ensured a quality level of 100 PPB (⑥) for an extended 12V usage, and an additional design-for-reliability (❷DfR) with the flipped bias is expected to achieve the virtual zero PPB [i.e., 0.1 PPB (⑦)]. Meanwhile, the use of two capacitors in series (❸DfR) divides a higher voltage (e.g., 20V) into half (i.e., 10V for each), thus making either capacitor much less exposed to the heavily defective V_{bd} tailing (Fig. 4). Such a design has also been further utilized as a redundancy for drastically reducing failure rates. For example, when the early failure probability of a capacitor is 100 PPM (①; due to the manufacturing limitation), the chance for two serial capacitors both to fail earlier than an expected lifetime can be minimized to 10 PPB (i.e., ③ at 100 PPM × 100 PPM). Some of the options have been used in designing and manufacturing IC products for a broad range of customers. After many millions of parts were delivered and used in potentially life-threatening environments (including medical, automotive, and military/aerospace applications), we have achieved the goal of zero customer returns due to the early lifetime failures of PIPC in the field.

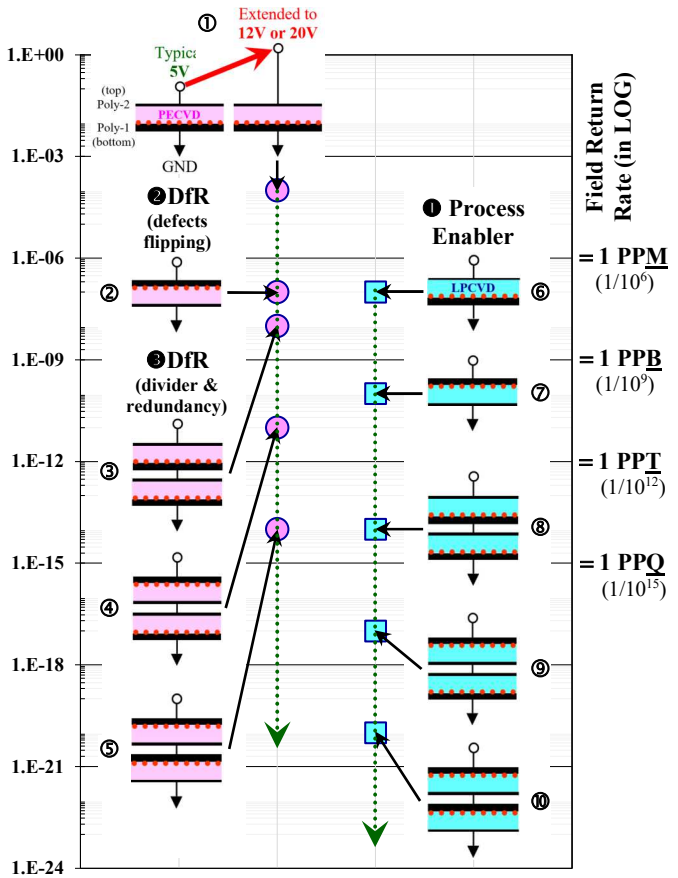


Fig. 12. The narrative of Road to Zero Defects collectively from process enablement to design optimization for fully safeguarding against the manufacturing defects.

VI. Summary

We have fully safeguarded against the massive reliability defects genetically present in manufacturing PIPC. In order to comprehensively passivate these defects, our collective approach includes process improvement and circuit design optimization with innovation and redundancy. This decade-long study and follow-up has vividly demonstrated, in the narrative of zero defects, that the sky is the limit.

Reference

[1] L. Y. Sheng, E. De Backer, D. Wojciechowski, J. Greve, Kurt Dhont, S. Boonen, D. Malschaert, E. Snyder, "Surface roughness enhanced current stressing: its correlation to double-poly capacitor breakdown and beyond", Proc. of Intl. Integrated Reliability Workshop (IIRW), 2006, pp. 205-208.