An Accurate Process-Induced Variability-Aware Compact Model-Based Circuit Performance Estimation for Design-Technology Co-Optimization

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***Abstract*— In sub-10-nm fin field-effect transistors (FinFETs), line-edge roughness (LER) and metal-gate granularity (MGG) are the two most dominant sources of variability and are mostly modeled semi-empirically. In this work, compact models of LER and MGG are used. We show an accurate process-induced variability (PIV)-aware compact model-based circuit performance estimation for design-technology co-optimization (DTCO). This work is carried out using an experimentally validated Berkeley Short-channel IGFET Model–Common Multi-Gate (BSIM-CMG) model on a 7-nm FinFET node. First, we have shown performance benchmarking of LER and MGG models with the state of the art and shown $\sim$4$\times$ ($\sim$2.3$\times$) accuracy improvement for nMOS (pMOS) in the estimation of device figure of merits (DFoMs). Second, ring oscillator (RO) and static random-access memory (SRAM) circuit's performance estimation is carried out for LER and MGG variability. Furthermore, $\sim$22% more optimistic estimate of $(\sigma/\mu)_{SHM}$ (static hold margin) compared to the state-of-the-art model with V_{DD} variation is shown. Finally, we demonstrate our improved DFoM accuracy translated to more accurate circuit figure of merits (CFoMs) performance estimation. For worst-case SHM ($3(\sigma/\mu)_{SHM}$@ $V_{DD} = 0.75$ V) compared to state of the art, dynamic (standby) power reduction by $\sim$73% ($\sim$61%) is shown. Thus, our enhanced variability model accuracy enables more credible DTCO with significantly better performance estimates.**

***Index Terms*— Berkeley short-channel igfet model–common multi-gate (BSIM-CMG), design-technology co-optimization (DTCO), fin field-effect transistor (FinFET), line-edge roughness (LER), metal-gate granularity (MGG), process-induced variability (PIV), simulation program with integrated circuit emphasis (SPICE) simulation, static random-access memory (SRAM), technology computer-aided design (TCAD).**

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I. Introduction

AGGRESSIVE scaling improves performance but aggravates process-induced variability (PIV). Statistical device-to-device variation caused by undesirable PIV sources produce circuit-level variations. To meet all specifications simultaneously for the distribution of devices, peak performance is compromised [1], [2].

In fin field-effect transistors (FinFETs), line-edge roughness (LER) and metal-gate granularity (MGG) have been shown to be the two most dominant sources of variability (see Fig. 1) [4]. In most advanced nodes, titanium nitride (TiN) is the most commonly used gate metal in high-k metal-gate (HKMG) stack technology. The MGG variation in TiN is due to the presence of two different workfunctions 4.4 and 4.6 eV with the probability of occurrence as 40% and 60% in $\langle 111 \rangle$ and $\langle 100 \rangle$ orientation, respectively (see Table I) [3]. The LER arises from fabrication-induced fin shape variation. It is further categorized in two forms: 1) gate-edge roughness (GER) and 2) fin edge roughness (FER). GER and FER account the variation in gate length and fin width, respectively. The LER variability is characterized using input process-dependent parameters such as the auto-correlation length (Λ), correlation coefficient (ρ), and root mean square (RMS) roughness (σ).

To introduce these LER variability information in circuit simulation, earlier, a semi-empirical model to capture the impact of LER on device performance has been reported in the literature [6]. However, it does not account for fin-edge correlation (ρ) which is significant in self-aligned quadruple patterning (SAQP). For MGG, the model in [7] depends on grain statistics without detailed positional dependence. Recently, a compact model for LER [8] that is physics-based and accounting for all the critical variability parameters is proposed by our group. Furthermore, a physics-based analytical model for MGG [9] considering the grain size and positional dependence work function is also proposed. Table II summarizes the model's comparison with state of the art. A simulation program with an integrated circuit emphasis (SPICE) platform including [8], [9] was experimentally validated on 14-nm node [10] in our earlier work.

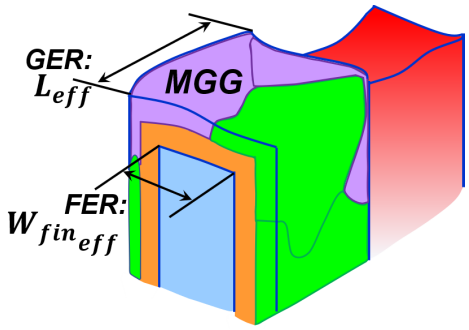

Fig. 1. Schematic of the fin field-effect transistor (FinFET) with PIVs, that is, line-edge roughness (LER) and metal-gate granularity (MGG). Workfunctions of titanium nitride (TiN) used for σV_T calculation are shown in Table I.

TABLE I
MGG IN TIN [3]

Orientation	WF	Probability
<100>	4.6 eV	60 %
<111>	4.4 eV	40%

In this work, we have extended the previously proposed PIV-aware SPICE framework for the state-of-the-art 7-nm CMOS technology FinFET to study the translation of device model accuracy to improvement in circuit performance estimation. At first, to ensure the accuracy of the results, we have calibrated the technology computer-aided design (TCAD) deck against the experimental data presented in [11] by Global Foundries for their 7-nm FinFET technology. The calibrated TCAD deck is used to perform an elaborate calibration of the Berkeley Short-channel IGFET Model–Common Multi-Gate (BSIM-CMG) model [12]. Second, we implement our model and compare it against the state-of-the-art semi-analytical model [6]. Finally, we demonstrate our improved accuracy translated to significantly different and hence more accurate performance estimation in the typical circuits—ring oscillator (RO) and static random-access memory (SRAM) using our PIV-aware SPICE framework [13].

This article is organized as follows. The device details and simulation parameters are discussed in Section II. The TCAD and SPICE calibration are shown in Sections III-A and III-B followed by benchmarking of PIV-aware simulation framework with TCAD in Section III-C. Impact of PIVs on typical circuits performance—RO and SRAM are discussed in Section IV-A and the comparison of accuracy in performance estimation with state-of-the-art is discussed in Section IV-B. The impact of improved accuracy in device variability estimation on circuit performance is discussed in Section IV-C followed by conclusion in Section V.

II. Device Details and Simulation Parameters

Fig. 1 shows the schematic of the FinFET with PIVs. The device dimensions [5] used in this work are mentioned in Table III. An industry standard BSIM-CMG model is adopted for SPICE simulation. The BSIM-CMG is calibrated with the experimental data and elaborate calibration is done using

TABLE II
BENCHMARKING OF OUR GROUP LER AND MGG MODELS WITH STATE-OF-THE-ART

	Models	Fin statistics		V_T	Input Parameter
		σ_W	μ_W		
LER	X.Jiang [6]	Semi-analytically calculated		LUT (SPICE)	Λ, σ
	Amita [8]	Compact form equation derived			Λ, σ, ρ

	Models	Type	Size dependence/ Grain position
MGG	S. H. Rasouli [7]	Physical model	Yes/No
	H. Vardhan [9]	Analytical model	Yes/Yes

TABLE III
DEVICE DIMENSION DETAILS [5]

Type/Parameter	L_G (nm)	W_{fin} (nm)	H_{fin} (nm)
NMOS	12	5	60
PMOS	12	5	60

statistical simulation data from an experimentally calibrated TCAD deck. σV_T values for process variation-induced average grain size of 4 nm and σ_{LER} of 2 nm are considered in SPICE simulation unless specified. Typical circuit—RO and SRAM circuits—performance analysis is carried out across variation of different LER parameters: ρ, Λ and σ. Similarly, for MGG, σV_T values corresponding to different TiN grain sizes are calculated using the analytical model presented in [9] for the device dimensions mentioned in Table III. Furthermore, the σV_T values are used in the SPICE simulation.

III. Calibration and Benchmarking of the Device Variability Model

In this section, the TCAD and SPICE calibration is discussed, followed by the validation of the SPICE framework against calibrated TCAD deck using statistical simulation. The design-technology co-optimization (DTCO) flow is summarized in Fig. 2.

A. TCAD Calibration

In TCAD Sentaurus [14] test bench, the following device physics models are used. To capture the current transport, the drift-diffusion model is used with the density gradient (DG) model. The DG model captures quantum correction at advanced nodes [15]. The mobility model includes thin layer in conjunction with IALMOB, high field saturation, and BALMOB. SRH recombination, trap-assisted tunneling (TAT),

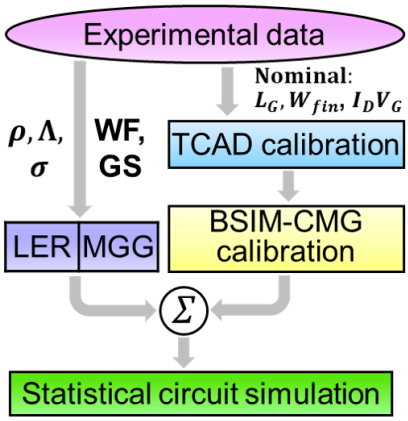

Fig. 2. Flowchart for model calibration, validation, and circuit simulation methodology adopted is shown.

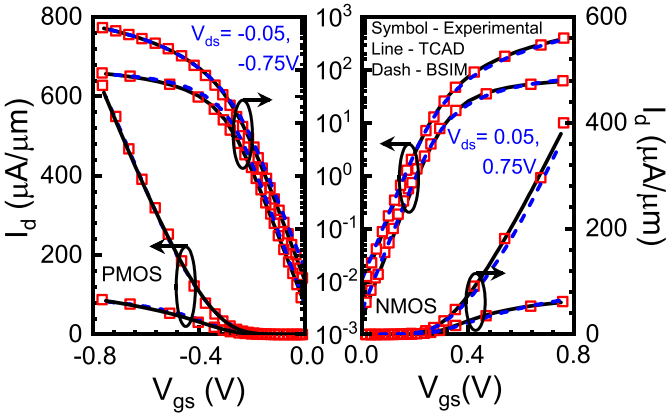

Fig. 3. Comparison of experimental data with the well-calibrated TCAD deck and SPICE model of nominal device for pMOS and nMOS.

and band-to-band tunneling models are used to capture the recombination and generation current. Using the above models, the TCAD deck is calibrated with the experimental data and the excellent matching is shown for the nominal device in Fig. 3 for both nMOS and pMOS. Furthermore, the calibrated 2-D simulation deck is used to generate the gate length (L_G) and fin width (W_{fin}) splits corresponding to σL and σW generated from the LER model for $\rho/\Lambda/\sigma = 0.7$ nm/50 nm/2 nm and σV_T from the MGG model for grain sizes of 4 nm for the elaborate calibration and validation of BSIM-CMG model as discussed below.

B. SPICE Calibration

We have calibrated the BSIM-CMG model with the experimental data of the nominal device for nMOS and pMOS. The model parameters used for calibration are discussed below. First, device physical parameters are fixed to define device geometry, and threshold voltage is captured by work function tuning. Second, U0 and UA parameters for low field mobility and phonon/surface roughness scattering, respectively, are used to capture the mobility degradation. The velocity saturation effects are captured using VSAT and VSAT1 parameters. Third, the short-channel effects are captured using DVT0 and DVT1, and product cost and life cycle management (PCLM)

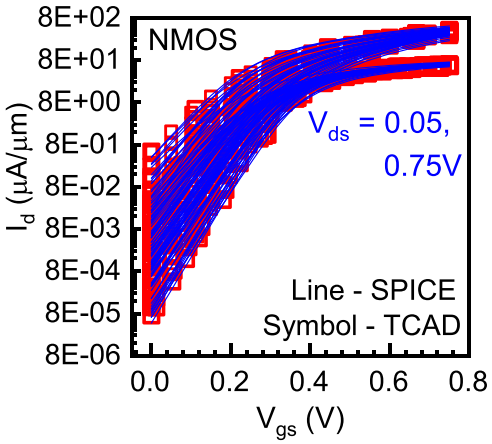

Fig. 4. Comparison of I_d–V_{gs} data of statistical TCAD simulation against SPICE simulation. Good consistency between the two confirms the PIV-aware framework capability to capture the LER and MGG variations well.

are used to capture the channel length modulation. In the sub-10-nm regime, small geometry-induced effect, that is, quantum confinement, became severe. QMFACTOR is enabled in the model for quantum correction. DVT1SS, U0, and VSAT are used for subthreshold swing, mobility, and saturation velocity correction, respectively, for calibration across different device geometries. The BSIM-CMG model calibration for the nominal device data is shown in Fig. 3 and benchmarking of the SPICE framework is discussed in the following section.

C. Benchmarking of the Device Variability Model

Using the calibrated BSIM-CMG model, statistical simulations are performed on the developed PIV-aware framework in the SPICE. SPICE simulation shows well consistency with the statistical data from calibrated TCAD as shown in Fig. 4. The statistical TCAD and SPICE simulations are performed using σL and σW generated from the LER model for $\rho/\Lambda/\sigma = 0.7$ nm/50 nm/2 nm and σV_T from the MGG model for grain sizes of 4 nm. Furthermore, to compare the accuracy in estimation of device figure of merits (DFoMs): SS_{lin}, SS_{sat}, $V_{\text{th,lin}}$, $V_{\text{th,sat}}$, I_{ON}, I_{OFF}, and DIBL due to PIVs, the standard deviation (σ) is calculated from the statistical data of TCAD and SPICE. Comparison of calculated σ of DFoMs for both nMOS and pMOS with respect to TCAD is shown using the spider plot in Fig. 5(a) and (b). All σ's are normalized with the respective σ_{TCAD}.

This work shows ~4× (~2.3×) σ_{error} reduction for nMOS (pMOS) when compared to the referenced model [6]. This developed framework is used for the performance estimation of RO and SRAM circuits, as discussed in the following section.

IV. Results and Discussion

A. RO and SRAM Circuit Performance Analysis

To study the impact of variability and fabrication aspects, (a) RO and (b) 6T SRAM cells are used as shown in Fig. 6, along with the RO characteristics and static hold margin (SHM) of SRAM. The performance of RO and 6T SRAM

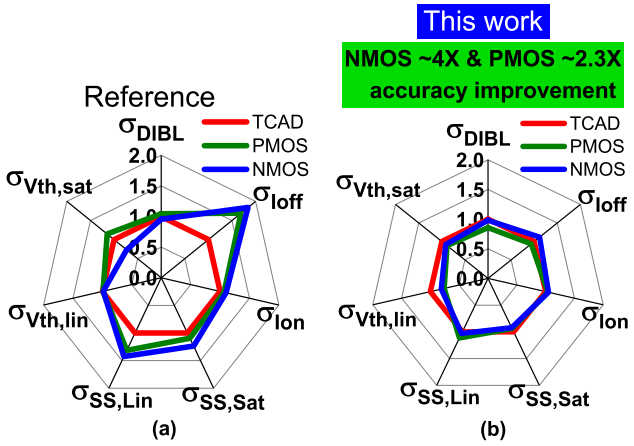

Fig. 5. Benchmarking of PIV-aware framework accuracy in estimation of PIV impact on device figure of merits (DFoMs) with respect to TCAD is shown. All σ's are rationalized with the respective σ_{TCAD}. This work shows ~74% (~54%) $\rho_{accuracy}$ improvement for nMOS and pMOS when compared to referenced model [6].

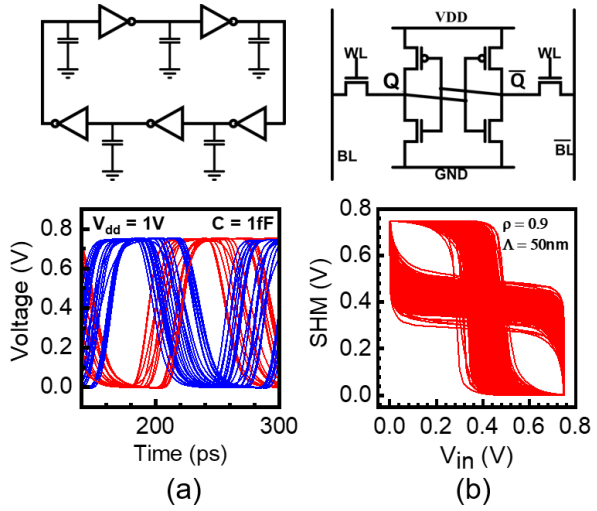

Fig. 6. Circuits (a) five-stage RO with a capacitor of 1 fF and (b) 6T SRAM are used for demonstration. The outputs are shown for statistical simulation using the developed PIV-aware framework.

TABLE IV
TiN Grain Size-Dependent σV_T Calculation [9]

Grain size (nm)	3	3.5	4	4.5	5
σV_T (mV)	25	27.5	33	39	47

cells is analyzed across different lithography techniques such as fin edge correlation coefficient $\rho = 0$ for EUV, $\rho = 0.5$, 0.9 for SADP [10], and across different $\Lambda = 5$, 10, 15, 20, 25, 35, 50 nm, and $\sigma = 1.4$, 1.7, and 2 nm. Similarly, for MGG, different TiN grain sizes of 3, 3.5, 4, 4.5, and 5 nm are considered for σV_T calculation (see Table IV) [9].

RO: Fig. 7(a) shows a negligible (~2%) decrease in RO delay for $\rho = 0.9$ compared to $\rho = 0$. But there is a significant decrease in variability for higher ρ. Also, $(\sigma/\mu)_{RO}$ analysis is carried out across ρ, Λ, and σ for constant grain size of 4 nm as shown in Fig. 7(b). It is observed that $(\sigma/\mu)_{RO}$ decreases with increase in ρ and decrease in σ. Also, the $(\sigma/\mu)_{RO}$ peak when Λ/L_G tends to ~1.

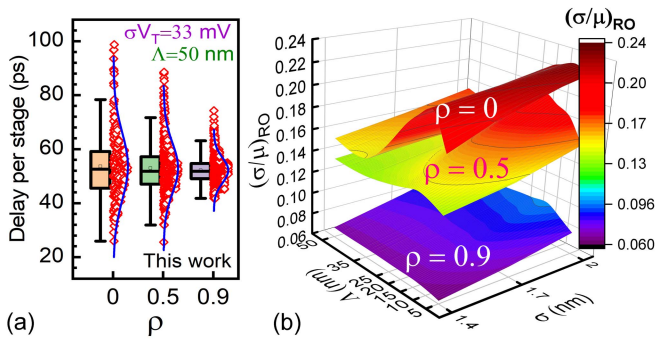

Fig. 7. (a) RO delay comparison (at fixed $\Lambda = 50$ nm) across different ρ. With the increase in ρ ($\rho = 0.9$ when compared to $\rho = 0$), delay shows a negligible (~2%) decrease. While $(\sigma/\mu)_{RO}$ decreases by ~61%. (b) $(\sigma/\mu)_{RO}$ comparison across different LER parameters: ρ, Λ, and σ variation for fixed $\sigma V_T = 33$ mV. With an increase in ρ, $(\sigma/\mu)_{RO}$ decreases at fixed Λ and σ. While decrease in σ shows monotonic decrease in $(\sigma/\mu)_{RO}$.

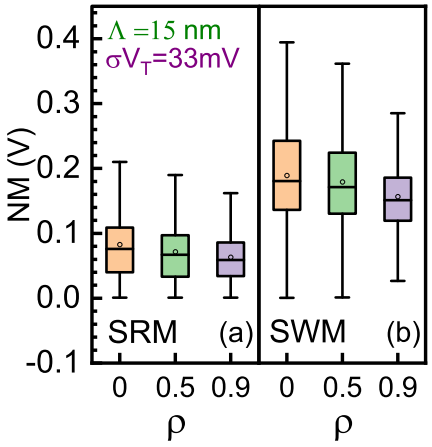

Fig. 8. SRAM static read margin (SRM) and static write margin (SWM) comparison across different ρ. With the increase in ρ, SRM (SWM) degrades by ~23% (~17%) for $\Lambda =$ 15 nm. While the increase in ρ shows the decrease in variability.

SRAM: Fig. 8 shows the SRAM (a) the static read margin (SRM) and (b) static write margin (SWM) degrade by ~23% (~17%) at $\Lambda = 15$ nm for $\rho = 0.9$ when compared to $\rho = 0$. Fig. 9 shows the dependence of $(\sigma/\mu)_{SHM}$ on Λ/L_G for different ρ. $(\sigma/\mu)_{SHM}$ increases with decrease in Λ and peaks as Λ/L_G tends to ~1 and reduces on further reduction of Λ/L_G, and the results are qualitatively consistent with the referenced model [6]. The SHM is further analyzed across different LER parameters as shown in Fig. 10. It has been observed that $(\sigma/\mu)_{SHM}$ decreases for higher ρ, due to an increase in correlation between edges (reduced LER), leading to lower variability. It also reduces with the decrease in σ.

The RO and SRAM analyses show the $(\sigma/\mu)_{RO}$ and $(\sigma/\mu)_{SHM}$ peaks as Λ/L_G tends to 1. This is because the initial increment in Λ makes the fin edges more regular, which increases the σ and μ, however, the incremental rates are different for σ (faster) and μ (lower). Moreover, as $\Lambda/L_G > 1$,

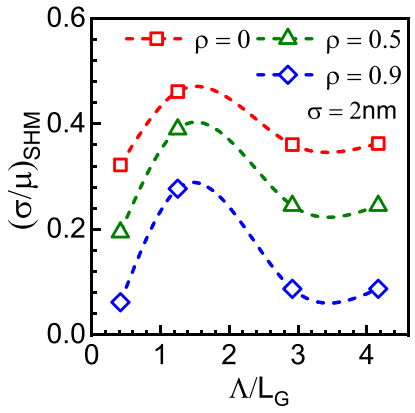

Fig. 9. Dependence of $(\sigma/\mu)_{SHM}$ on Λ/L_G is shown for different ρ. $(\sigma/\mu)_{SHM}$ increases with decrease in Λ and peaks as Λ/L_G tends to $\sim$1 and reduces on further reduction of Λ/L_G. Also, $(\sigma/\mu)_{SHM}$ decreases with ρ, due to increasing correlation between edges, leading to lower variability (results are qualitatively consistent with the referenced model [6]).

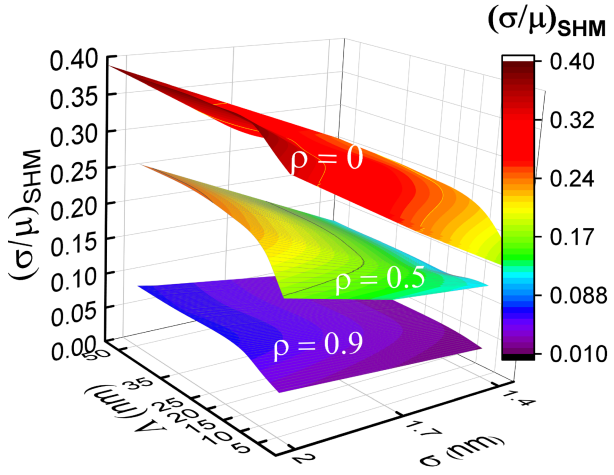

Fig. 10. Dependence of $(\sigma/\mu)_{SHM}$ on Λ and σ for different ρ. Variation is highest as $\Lambda/L_G \sim 1$ while it decreases with increase in ρ. It helps in establishing the design technology co-optimization (DTCO) strategy to choose suitable Λ and use lithography techniques with higher ρ and lower σ to improve SRAM performance.

the sigma saturates while μ saturates as $\Lambda/L_G \approx 3$ [8]

$$\Delta\left(\frac{\sigma}{\mu}\right)_{SRM}\% = \frac{\left(\frac{\sigma}{\mu}\right)_{SRM}|_{\sigma V_T} - \left(\frac{\sigma}{\mu}\right)_{SRM}|_{\sigma V_T=0}}{\left(\frac{\sigma}{\mu}\right)_{SRM}|_{\sigma V_T=0}}. \quad (1)$$

To study the impact of MGG variability, SRM is analyzed for σV_T variation (Table IV) across different LER parameters as shown in Fig. 11. The inset shows with the increase in σV_T and $\Delta(\sigma/\mu)_{SRM}$ % given by (1) increases. It is noteworthy to mention that the contribution due to MGG variation in $(\sigma/\mu)_{SRM}$ is not significant ($\sim$10% as compared to $\sigma V_T = 0$). Hence, LER is acting as a dominant source of variability. Thus, DTCO strategy by using lithography techniques with higher ρ and Λ, and lower σ to improve RO and SRAM performance is quantitatively established. In the next section, comparison of accuracy difference in performance estimation with state of the art is discussed.

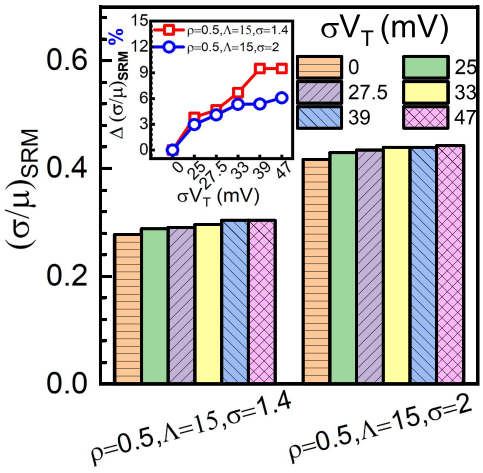

Fig. 11. Dependence of $(\sigma/\mu)_{SRM}$ on σV_T for fixed ρ and Λ and for $\sigma = 1.4$ and 2 nm is shown. Increase in σV_T leads to increase in $(\sigma/\mu)_{SRM}$ for both cases as shown in the inset. The contribution due to MGG variation in $(\sigma/\mu)_{SRM}$ is not significant ($\sim$10% as compared to $\sigma V_T = 0$). Hence, LER is acting as a dominant source of variability.

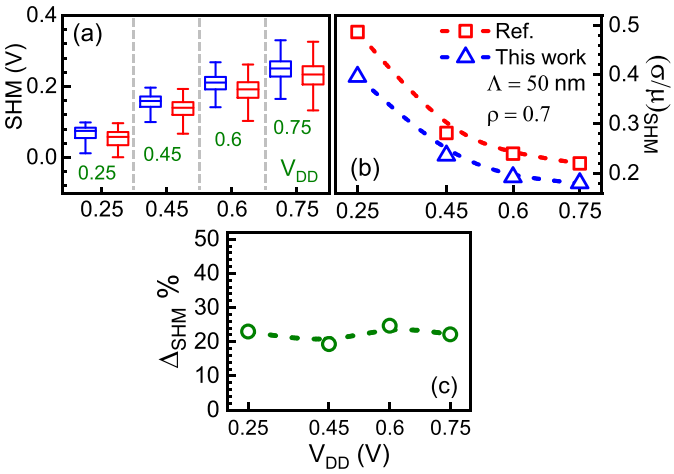

Fig. 12. (a) SHM comparison is shown with the referenced model [6] across V_{DD} variation. (b) $(\sigma/\mu)_{SHM}$ comparison is shown with the referenced model [6] and (c) $\sim$22% more optimistic estimate of $(\sigma/\mu)_{SHM}$ is observed with V_{DD} variation.

B. Circuit Performance Estimation Accuracy Comparison

To check the accuracy in performance estimation when compared to the referenced model [6], SHM is analyzed for V_{DD} variation as shown in Fig. 12(a). The $(\sigma/\mu)_{SHM}$ for both cases is shown in Fig. 12(b) and $\sim$22% improvement in $\Delta(\sigma/\mu)_{SHM}$ % (2) estimation is observed using our setup as shown in Fig. 12(c). Furthermore, we quantify the operating conditions predicted by our model for the same performance as the referenced model [6]. We compared the worst-case SHM, that is, $3\sigma_{SHM}$ that we got from our model and the referenced model [6] as shown in Fig. 13. It shows a significant reduction in operating V_{DD} (-180 mV) is possible for the worst-case SHM window (for same $3\sigma_{SHM[6]}@V_{DD} = 0.75$ V)

$$\Delta\left(\frac{\sigma}{\mu}\right)_{SHM}\% = \frac{\left(\frac{\sigma}{\mu}\right)_{SHM[Ref]} - \left(\frac{\sigma}{\mu}\right)_{SHM[This\ work]}}{\left(\frac{\sigma}{\mu}\right)_{SHM[This\ work]}}. \quad (2)$$

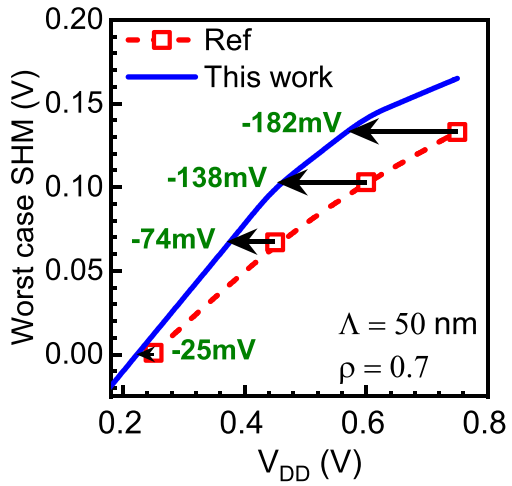

Fig. 13. Worst-case SHM ($3\sigma_{SHM}$) comparison of this work with the referenced model [6] is shown for V_{DD} variation. It is observed that this model enables significant V_{DD} reduction for same performance. It can lead to a significant reduction in dynamic power.

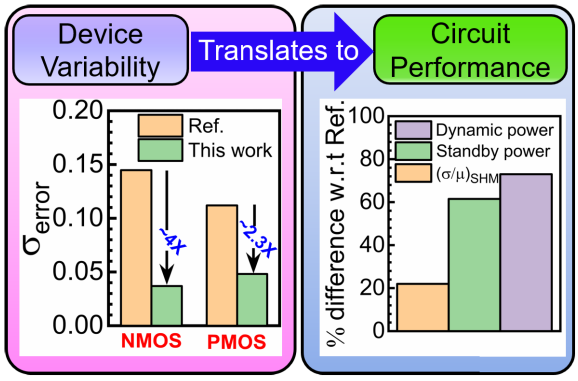

Fig. 14. Relative difference in comparison to referenced model [6] prediction is shown for DFoMs accuracy estimation translating to more optimistic CFoMs performance estimation, enabling the scope for circuit designers to further optimize performance.

C. Model Accuracy Translation to Circuit Performance

Fig. 14 shows the relative difference benchmarking in the DFoM and circuit figure of merits (CFoMs): $(\sigma/\mu)_{SHM}$, standby, and dynamic power benchmarked to the referenced model [6]. More accurate DFoM estimation leads to the significant difference in CFoM performance. Our model predicts a ∼22% more optimistic estimate of SHM compared to the referenced model [6], which enables more aggressive circuit design. Furthermore, it allows the SRAM to operate at lower V_{DD} (−180 mV) for $3(\sigma/\mu)_{SHM\,[6]}@V_{DD} = 0.75$ V, leading to dynamic power reduction by ∼73%. Also, ∼61% reduction in average standby power is observed.

V. Conclusion

To summarize, we demonstrated the relative improvement in DFoMs estimation using our PIV-aware SPICE simulation framework using in-house LER and MGG models compared from state of the art [6]. The DFoMs accuracy enhancement leads to significantly more accurate circuit performance estimation in RO and SRAM that improves CFoM estimates. Furthermore, the impact of variability is studied across different technological parameters (LER: ρ, σ, Λ, and MGG: Grain size). Our platform enables accurate DTCO for optimized circuit performance based on the earlier validated variability models against the experimental data from IMEC [10]. The experimental validation of the circuit's performance will be further explored and presented elsewhere.

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