Extended Scale Length Theory for Low-Dimensional Field-Effect Transistors

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***Abstract*— Low-dimensional (low-D) semiconductors such as carbon nanotubes (CNTs) and 2-D materials are promising channel materials for nanoscale field-effect transistors (FETs) due to their superior electrostatic control. However, classical scale length theory (SLT) does not incorporate the effect of channel extensions, which becomes crucial for thin channels (<10 nm) and short gate lengths. Here, we extend the classical SLT by introducing two boundary coupling parameters, which describe the impact of gate and drain biases on the source- and drain-channel junction potentials. Moreover, we introduce a general expression for the scale length specifically for low-D FETs. This extended SLT accurately describes electrostatic short-channel effects (SCEs) of low-D FETs, with <5% error in subthreshold slope over a wide range of parameters versus >2× error using the classical SLT. The extended SLT is based on three parameters (scale length, gate, and drain boundary coupling parameters) which can be extracted from potential profiles or FET transfer characteristics. In addition, the extended SLT uses analytical closed-form expressions that can be easily included in a compact model to facilitate design-technology co-optimization (DTCO) with low-D FETs to leverage the crucial role of their extensions.**

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I. Introduction

THE classical scale length theory (SLT) [1]–[5] has facilitated the design of bulk 3-D semiconductor field-effect transistors (FETs) by introducing a single electrostatic scale length, Λ, which quantifies the distance that lateral electric fields penetrate into the FET channel [1]. Short-channel effects (SCEs), including drain-induced barrier lowering (DIBL), threshold voltage (V_t) roll-off, and subthreshold swing (SS) degradation, can be predicted for arbitrary gate lengths (L_g) using simple analytical expressions with L_g and Λ as the only parameters. Due to its accuracy and simplicity, the classical SLT has become ubiquitous in a device engineer's toolkit [4].

The electrostatic limitations of bulk 3-D-semiconductors have made low-dimensional (low-D) materials such as carbon nanotubes (CNTs) and 2-D materials promising channel materials for extremely scaled FETs for digital logic applications [6]–[10] because the intrinsically thin channels (~0.5–2 nm) enable excellent electrostatic control. Moreover, some low-D FETs [e.g., 1-D CNT FETs (CNFETs), 2-D FETs] also enable monolithic 3-D integration, due to the low temperature of fabrication [11], [12], bringing even larger benefits at the system level [13].

However, unlike their bulk 3-D counterparts, low-D FETs have depletion lengths in their extension regions that are comparable with Λ [14]–[16] due to the low dimensionality, as shown in Fig. 1(a). Consequently, the extension regions of low-D FETs partially sustain the potential drop between the channel and the source or drain, thereby improving the electrostatic control and reducing SCEs [6], [17]–[19]. However, classical SLT developed for bulk 3-D-semiconductor channels [1], [3] neglects this potential drop and, therefore, overestimates SCEs for low-D FETs. This limitation of the classical SLT precludes device engineers from realizing potential miniaturization opportunities and associated design and optimization of low-D FETs [see Fig. 1(b) and (c)]. For instance, a reduction of the extensions doping [17], [19] and the engineering of the spacer dielectric surrounding the source/drain extensions [20] lead only to a small improvement in the SCEs for bulk 3-D-semiconductors. However, the same techniques have a greater impact on low-D FETs SCEs, due

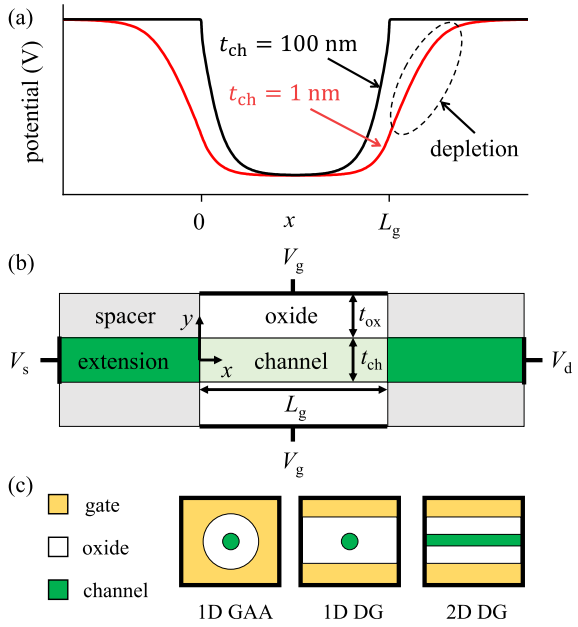

Fig. 1. (a) Channel potential profiles for $t_{ch} = 100$ nm and $t_{ch} = 1$ nm and (b) schematic of a generic DG FET, with the definitions of the device regions and geometrical parameters. L_g is chosen to show the same L_g/Λ for both t_{ch}. The relative dielectric constants for spacer and oxide are κ_{spa} and κ_{ox}, respectively. (c) Low-D FET geometries considered in this work: 1-D GAA, 1-D DG, and 2-D DG. Unless otherwise noted, the 1-D DG width is equal to $2t_{ox} + t_{ch}$.

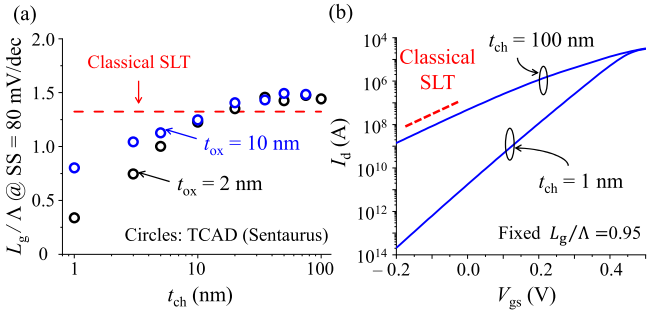

Fig. 2. (a) Minimum L_g/Λ ratio required to achieve SS = 80 mV/dec versus channel thickness. This ratio was extracted with Sentaurus for a 2-D DG FET with $t_{ox} = 2$ nm (black circles) and $t_{ox} = 10$ nm (blue circles), extension doping = 10^{20} cm^{-3}, and $\kappa_{ox} = \kappa_{spa} = 20$. The red dashed line shows the ratio of L_g/Λ required to achieve the same SS according to classical SLT. (b) Transfer characteristics of 2-D DG FETs simulated with Sentaurus for $t_{ch} = 1$ and 100 nm, $t_{ox} = 3$ nm, and other parameters as in (a). For each case, L_g is chosen to have the same L_g/Λ ratio. Red line indicates the slope predicted by classical SLT.

to their reduced dimensionality, and thus represent additional knobs to improve the performance of low-D FETs.

As an example of SCE overestimation, we plot the value of L_g/Λ required to obtain SS = 80 mV/dec in a 2-D double-gate (DG) FET, as predicted by Sentaurus [21], at various channel thicknesses (t_{ch}) in Fig. 2(a). While the classical SLT predicts that $L_g/\Lambda \approx 1.3$ should yield an SS = 80 mV/dec regardless of t_{ch} (red dashed line), we observe that much smaller values of L_g/Λ yield this SS as t_{ch} decreases below 10 nm. The subthreshold current of small-t_{ch} FETs (i.e., <10 nm) is likewise overestimated by classical SLT, as shown in Fig. 2(b).

This work is an extension of previous SLTs targeting low-D FETs (e.g., 2-D FETs [22], CNFETs [23]), because it simultaneously includes the impact of channel geometry, extension doping [18], [19], [24] and of the spacer dielectric constant [20], [25]. In our previous work [6], we introduced the boundary coupling parameters α_G and α_D and applied the theory to CNFETs. In contrast, here, we: 1) demonstrate that the extended SLT also works for 2-D FETs; 2) introduce a general expression for Λ in low-D FETs; and 3) introduce a new procedure to derive the boundary coupling parameters from potential profiles (similar to the conventional procedure used to extract the scale length Λ [22]) and from FET transfer characteristics.

The extended SLT abstracts the complexity of the specific device architecture to three physics-based parameters that uniquely determine electrostatic control and SCEs. Moreover, because the extended SLT is based on closed-form expressions, it is easily incorporated into compact models. The design space of low-D FETs, including both material selection and device architecture, makes such compact models crucial for enabling extensive design-technology co-optimization (DTCO) of emerging low-D FETs and projecting their benefits [6].

In Section II, after introducing the extended SLT and justifying the physical meaning of new coupling parameters, we describe a procedure to extract the extended SLT parameters, showing that the extended theory can accurately predict SCEs in low-D FETs. In Section III, we apply the extended SLT to 1-D and 2-D FETs and show the dependence of electrostatic control on device geometry, dimensionality, and technology parameters (such as extension doping and dielectric constants). Given their superior electrostatic control [6], [26]–[28], in this work, we consider three FET geometries: 1-D gate-all-around (GAA), 1-D DG-FETs, and 2-D DG-FETs [see Fig. 1(c)]. Finally, we conclude in Section IV with an outlook of how these findings will influence future designs of low-D FETs. Because the focus of this work is electrostatic control of the FET, we do not include the impact of direct source–drain tunneling [29] and band-to-band tunneling [30], [31]. However, we note that the extended SLT is representative of the analytical framework necessary to model band profiles, including the modeling of tunneling currents, as previously shown in [6]. As an additional example, the extended SLT can potentially be used in compact models for tunnel FETs [32] based on low-D materials, where the knowledge of the potential profile near the junction is crucial for the derivation of the tunneling currents.

II. Extended SLT

A. Formalism

Fig. 1(b) shows the schematic of device structures considered in this work. Source and drain terminals are separated from the intrinsic channel by doped extensions with a step-like profile so that the gate electrode is aligned with the edge of the extension regions (i.e., the gate length L_g and channel length L_{ch} coincide). In this section, we focus on 2-D DG to derive the extended SLT formalism. However, the extended SLT parameters are derived in an identical fashion for other geometries (see Section III).

In classical SLT, the potential profile along the channel is expressed as [33]

$$\Psi(x,y) = V_{gs} + \sum_{n=0}^{\infty} \frac{b_n \sinh\left(\pi \frac{L_g - x}{\Lambda_n}\right) + c_n \sinh\left(\pi \frac{x}{\Lambda_n}\right)}{\sinh\left(\pi \frac{L_g}{\Lambda_n}\right)} \times \sin\left(\frac{\pi y}{\Lambda_n}\right) \quad (1)$$

where V_{gs} is the gate-to-source voltage, and Λ_n are different orders of the electrostatic scale length. For the sake of simplicity, compared with [33, eq. 1], we consider $y = 0$ at the center of the channel. The coefficients b_n and c_n satisfy the boundary conditions at the junctions between the channel and the extensions. In classical SLT [1], [3], [5], b_n and c_n are derived by imposing a constant potential in the doped extensions, equal to Ψ_{bi} and $\Psi_{bi} + V_{ds}$ for the source- and drain-side extensions, respectively, where Ψ_{bi} is the built-in potential [5] and V_{ds} is the drain-to-source bias. In low-D FETs, where the vanishing thickness of the channel makes the potential drop along y-direction negligible, (1) can be further simplified as [33]

$$\Psi(x) = V_{gs} + \frac{b_1 \sinh\left(\pi \frac{L_g - x}{\Lambda}\right)}{\sinh\left(\pi \frac{L_g}{\Lambda}\right)} + \frac{c_1 \sinh\left(\pi \frac{x}{\Lambda}\right)}{\sinh\left(\pi \frac{L_g}{\Lambda}\right)} \quad (2)$$

$$b_1 = \Psi_{bi} - V_{gs} \quad (3)$$

$$c_1 = \Psi_{bi} + V_{ds} - V_{gs}. \quad (4)$$

While the assumption of constant potential in the extensions is appropriate for bulk 3-D-semiconductors FETs, low-D FETs are characterized by relatively large depletion lengths in their source and drain extensions, violating this assumption [see Fig. 1(a)] and, in turn, rendering classical SLT inappropriate for low-D FETs with doped extensions. Here, we aim to extend the classical SLT to low-D FETs by deriving an equation similar to (2) without imposing constant potentials throughout the source- and drain-side extensions.

To discern the role of extensions, we begin by modeling the potential near the junction as a piecewise function, similar to the derivation of [17] and [18]. Considering the potential at the source junction (i.e., $x = 0$) and for $L_g \gg \Lambda$, (2) can be simplified by noting that

$$\lim_{\Lambda/L_g \to 0} \left. \frac{b_1 \sinh\left(\pi \frac{L_g - x}{\Lambda}\right)}{\sinh\left(\pi \frac{L_g}{\Lambda}\right)} \right|_{x=0^+} = b_1 \exp\left(-\frac{\pi x}{\Lambda}\right) \quad (5)$$

$$\lim_{\Lambda/L_g \to 0} \left. \frac{c_1 \sinh\left(\pi \frac{x}{\Lambda}\right)}{\sinh\left(\pi \frac{L_g}{\Lambda}\right)} \right|_{x=0^+} = 0. \quad (6)$$

Therefore

$$\Psi(x) = V_{gs} + b_1 \exp\left(-\frac{\pi x}{\Lambda}\right) \quad x > 0. \quad (7)$$

We express the potential on the source side of the junction as

$$\Psi(x) = g(x) \quad x \le 0 \quad (8)$$

where $g(x)$ is a generic function that describes the potential drop in the extension. While general expressions for $g(x)$ can be complex [15], [34], a simple model for SCEs can be derived from the following equation, which is valid at $x = 0$:

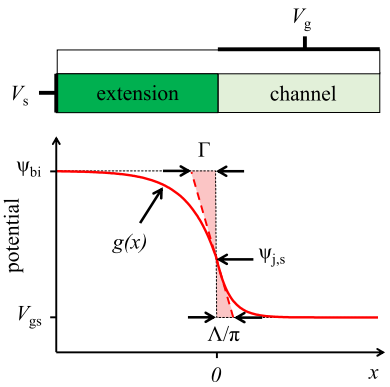

Fig. 3. Piecewise function used to model the potential near the junction between channel and extension and definitions of key modeling parameters used to derive the extended SLT.

$$\Psi_{bi} = -g'(0)\Gamma + g(0) \quad (9)$$

where Γ represents an effective depletion length, defined as the intercept between the prolongation of the derivative in $x = 0$ and $\Psi\ (x) = \Psi_{bi}$ (see Fig. 3). In principle, Γ in (9) is a function of V_{gs}, V_{ds}, and Ψ_{bi}. However, for the sake of simplicity, we keep only the 0^{th} order and consider two fixed values for the source and drain extensions (Γ_s and Γ_d, respectively). As we will demonstrate shortly, this approximation sufficiently captures the electrostatic behavior of low-D FETs. The assumption of constant Γ is furthermore justified by noting that the charge in the depletion tails of low-D junctions has a negligible impact on the potential and electric field near the junction [34]. Next, we impose continuity of the electrostatic potential and electric field at the source junction (see Fig. 3)

$$g(0) = \Psi(0) = V_{gs} + b_1 \quad (10)$$

$$g'(0) = \Psi'(0) = -\frac{\pi b_1}{\Lambda}. \quad (11)$$

Equations (9)–(11) can be solved to find

$$\Psi(0) = \Psi_{j,s} = \frac{\pi\Gamma_s}{\Lambda + \pi\Gamma_s} V_{gs} + \frac{\Lambda}{\Lambda + \pi\Gamma_s} \Psi_{bi} \quad (12)$$

which shows how the total potential difference $V_{gs} + \Psi_{bi}$ is partitioned between the extension and the channel. The above derivation can be repeated at the drain side to arrive at a similar expression for the drain junction potential

$$\Psi(L_g) = \Psi_{j,d} = \frac{\pi\Gamma_s}{\Lambda + \pi\Gamma_s} V_{gs} + \frac{\Lambda}{\Lambda + \pi\Gamma_s} \Psi_{bi} + \frac{\Lambda}{\Lambda + \pi\Gamma_d} V_{ds}. \quad (13)$$

Equations (12) and (13) represent a more generalized form of the boundary conditions used in classical SLT.

If $\Lambda \gg \pi\Gamma_s$ and $\pi\Gamma_d$, then $\Psi_{j,s} = \Psi_{bi}$ and $\Psi_{j,d} = \Psi_{bi} + V_{ds}$, restoring the classical SLT assumption. However, if $\Lambda \sim \pi\Gamma_s$ or $\pi\Gamma_d$ (as is the case of low-D FETs [15], [16]), this simple model captures the effect of the finite depletion length, thus extending classical SLT to low-D FETs.

The boundary coupling parameters introduced in [6], which describe how $\Psi_{j,s}$ and $\Psi_{j,d}$ respond to the applied gate and drain voltages, can be derived from (12) and (13) as

$$\alpha_G = 1 - \frac{\partial \Psi_{j,s}}{\partial V_{gs}} = \frac{\Lambda}{\Lambda + \pi\Gamma_s} \tag{14}$$

$$\alpha_D = \frac{\partial \Psi_{j,d}}{\partial V_{ds}} = \frac{\Lambda}{\Lambda + \pi\Gamma_d}. \tag{15}$$

With these definitions, we express the potential profile in the gate region as

$$\Psi(x) = V_{gs} + \frac{\left(-\alpha_G V_{gs} + \alpha_G \Psi_{bi}\right)\sinh\left(\pi\frac{L_g - x}{\Lambda}\right)}{\sinh\left(\pi\frac{L_g}{\Lambda}\right)} + \frac{\left(-\alpha_G V_{gs} + \alpha_G \Psi_{bi} + \alpha_D V_{ds}\right)\sinh\left(\pi\frac{x}{\Lambda}\right)}{\sinh\left(\pi\frac{L_g}{\Lambda}\right)}. \tag{16}$$

Given the definitions in (14) and (15), $\alpha_G \sim \alpha_D \sim 1$ for bulk 3-D-semiconductor FETs ($\Lambda \gg \Gamma$) and (16) becomes identical to the classical expression (2)–(4). However, in the general case, α_G and α_D are in the range of 0–1, incorporating the finite depletion length into the theory. Here, we note that the definition of Λ in the extended SLT is unchanged from that of classical SLT. However, we emphasize that Λ cannot univocally describe the electrostatics of low-D FETs because two low-D FETs might have equal Λ and different SCEs. These new parameters are thus crucial for predicting SCEs in low-D FETs.

B. Extended SLT Parameters Extraction Procedure

The extended SLT parameters (Λ, α_G, and α_D) can be extracted from potential profiles along the channel at different gate lengths and bias conditions (see Fig. 4). After simulating surface potential profiles for a device architecture of interest at various gate lengths [see Fig. 4(a)], we calculate Λ by plotting the change in the minimum of the potential Ψ as a function of L_g (as in [22]). For a small V_{ds}, the potential minimum is approximately at the center of the channel. Therefore

$$\Delta\Psi(L_g) = |\Psi_{\min,L_g=\infty} - \Psi_{\min,L_g}| = \left(2\alpha_G\Psi_{bi} - 2\alpha_G V_{gs} + \alpha_D V_{ds}\right)\frac{\sinh\left(\pi\frac{L_g}{2\Lambda}\right)}{\sinh\left(\pi\frac{L_g}{\Lambda}\right)}. \tag{17}$$

In the limit $L_g \gg \Lambda$

$$\ln\left(\Delta\Psi(L_g)\right) = \ln(f) - \pi\frac{L_g}{2\Lambda} \tag{18}$$

$$f = 2\alpha_G\Psi_{bi} - 2\alpha_G V_{gs} + \alpha_D V_{ds}. \tag{19}$$

Thus, Λ can be extracted from the slope of the linear fit of (18), as shown in Fig. 4(b). As α_G and α_D both appear in the intercept of (18), these parameters are likewise extracted by plotting f [defined in (19)] as functions of V_{gs} (with $V_{ds} = 0$) and V_{ds} (with $V_{gs} = 0$), respectively, and finding the slopes of the linear fits, as shown in Fig. 4(c) and (d) (note the factor 1/2 in the derivation of α_G). Here, we note that the linearity of the relation between f and the applied bias confirms that the 0^{th} order of Γ sufficiently captures the electrostatic behavior of low-D FETs. Finally, even though not necessary to derive SCEs, the effective value of Ψ_{bi} is found in a similar way from the limit of f for V_{gs} that tends to zero (assuming $V_{ds} = 0$).

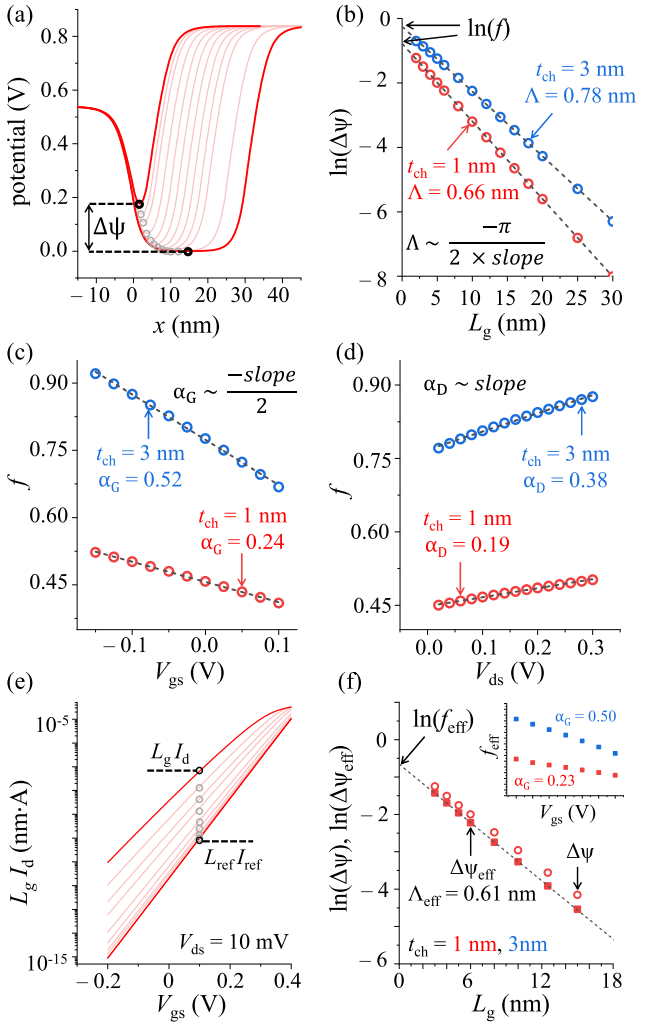

Fig. 4. Procedure used to extract extended SLT parameters. First, (a) $\Delta\Psi$ is measured at various L_g values for different V_{gs} and V_{ds} (e.g., $V_{gs} = 0$ V, $V_{ds} = 0.4$ V, L_g from 30 to 3 nm). Next, (b) we plot $\ln(\Delta\Psi)$ versus L_g and perform linear regression to find Λ using the inset equation. The intercept of this linear fit is defined as $\ln(f)$. Finally, we plot (c) f versus V_{gs} ($V_{ds} = 0$) and (d) f versus V_{ds} ($V_{gs} = 0$) and then perform similar linear fits to find α_G and α_D. For this example, we simulated a 2-D DG Si FET with Sentaurus ($t_{ox} = 3$ nm, extension doping 10^{20} cm^{-3}). Extended SLT parameters can also be derived from (e) transfer characteristics by extracting $\Delta\Psi_{eff}$ from $L_g I_d / L_{ref} I_{ref}$. The transfer characteristics are simulated with Sentaurus with the same parameters as in (a) for $t_{ch} = 1$ nm. The long-channel reference is $L_{ref} = 1$ μm, while L_g is swept from 15 to 3 nm. (f) Comparison between $\Delta\Psi$ and $\Delta\Psi_{eff}$ versus L_g with Λ_{eff} for $t_{ch} = 1$ nm and effective α_G for $t_{ch} = 1$ nm (red) and $t_{ch} = 3$ nm (blue) in the inset.

An approximation of the extended SLT parameters can be derived from FET I_d–V_{gs} transfer characteristics. A rigorous expression for the leakage current as a function of potential profile can be complex and involves numerical integrals. This is because, as noted in [33], the current continuity equation leads to a shift in the electron quasi Fermi level along the channel, making an analytical solution difficult to attain. As a result, the potential profile minimum Ψ_{min}, relative to the Fermi level in the source, overestimates the actual potential barrier.

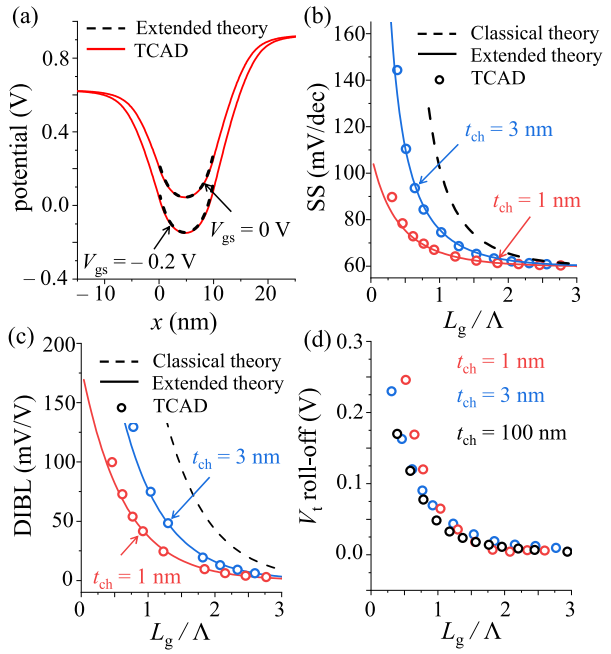

Fig. 5. (a) Potential profile of 2-D DG FETs as measured by Sentaurus (solid red) and as predicted by (16) (dashed black) using α_G and α_D extracted according to the procedure in Fig. 4. (b) SS and (c) DIBL versus L_g/Λ as measured by Sentaurus (circles) and as predicted using (22) and (23) (solid lines). SS is extracted averaging the slopes of the transfer curves over 3 orders of magnitude of current; DIBL is extracted at $V_{gs} = 0$. The dashed lines in (b) and (c) show the corresponding quantity as predicted by classical SLT. (d) V_t roll-off as measured with Sentaurus (using maximum transconductance method). Parameters used are highlighted in Fig. 4.

However, approximate values for extended SLT parameters can still be analytically derived by considering an effective barrier height Ψ_{eff}. Considering diffusive transport, the leakage current is

$$I_d = \frac{\beta}{L_g} \exp\left(-\frac{q\psi_{eff}(L_g, V_{gs}, V_{ds})}{k_B T}\right)\left(1 - \exp\left(-\frac{qV_{ds}}{k_B T}\right)\right) \tag{20}$$

where β is a prefactor independent of L_g and biasing conditions. In case of quasi-ballistic transport, (20) should be adapted considering L_g-dependent apparent mobility [35]. For $qV_{ds} \gg k_B T$, (20) leads to

$$\Delta\Psi_{eff}(L_g, V_{gs}, V_{ds}) = \frac{k_B T}{q} \ln\left(\frac{L_g I_d(L_g, V_{gs}, V_{ds})}{L_{ref} I_{ref}(V_{gs}, V_{ds})}\right) \tag{21}$$

where I_{ref} is the long-channel drain current at specific V_{gs} and V_{ds} [see Fig. 4(e)], L_{ref} is the reference long-channel length, and $\Delta\Psi_{eff}$ is the change of the effective potential barrier between the long-channel device and the device with L_g. The extended SLT parameters can then be derived following the procedure outlined in Fig. 4(b)–(d). Fig. 4(f) shows that, despite the introduction of an effective barrier height, the extended SLT parameters are in good agreement with those extracted from the potential profiles, with discrepancies in Λ, α_G, and α_D < 8% using parameters in Fig. 4.

C. Short-Channel Effects

Fig. 5(a) shows good agreement between the model and the profile simulated with Sentaurus for a 2-D DG FET, accurately reproducing the potential near the boundary conditions (i.e., the junction potentials) and at the minimum of the barrier. In this section, we leverage the extended SLT to analytically derive equations to predict SCEs in low-D FETs.

The SS quantifies the control of the gate over the channel. Without considering the impact of interface traps (which can be added subsequently), SS approaches ~60 mV/dec for a long-channel device (i.e., $L_g \gg \Lambda$) due to the small body thickness in low-D FETs [33]. As the gate length is reduced, the impact of source and drain fringe fields decreases the coupling between the gate and the channel, leading to an increase in SS. Assuming $L_g \gg \Lambda$ and in the limit of small V_{ds}, we derive SS from (11) as

$$SS = \frac{\ln(10) k_B T}{q}\left(\lim_{V_{ds}\to 0} \frac{\partial \Psi_{min}}{\partial V_{gs}}\right)^{-1} = \frac{\ln(10)(k_B T)/q}{1 - 2\alpha_G \exp\left(-\pi \frac{L_g}{2\Lambda}\right)}. \tag{22}$$

The reduction of the potential barrier as a function of V_{ds} is known as DIBL. Under the same assumptions

$$DIBL = \lim_{V_{ds}\to 0} \frac{\partial \Psi_{min}}{\partial V_{ds}} = \alpha_D \exp\left(-\pi \frac{L_g}{2\Lambda}\right). \tag{23}$$

Therefore, unlike bulk 3D-semiconductor FETs, whose SS and DIBL depend only on L_g/Λ, the SS and DIBL of low-D FETs are influenced by finite depletion lengths and hence also depend on α_G and α_D. On the contrary, we note that the V_t roll-off is invariant to α_G and α_D since the junction potentials are constant as L_g is reduced and, hence, the coupling parameters do not affect the roll-off. Accordingly, V_t roll-off of low-D FETs can still be described solely based on the L_g/Λ ratio [see Fig. 5(d)], just as is the case with bulk 3-D-semiconductors FETs. Therefore, low-D FETs can simultaneously show significant V_t roll-offs and yet have small DIBL (if $\alpha_D \sim 0$) or small SS deterioration (if $\alpha_G \sim 0$), unlike bulk 3-D-semiconductors FETs, whose SS, DIBL, and V_t roll-offs are all inherently coupled.

III. FET Design Impact on Extended SLT Parameters

Next, we apply the extended SLT to low-D FET geometries including 1-D GAA FETs, 1-D DG FETs, and 2-D DG FETs [cross sections in Fig. 1(c)]. We extract the extended SLT parameters from potential profiles simulated using both Sentaurus and Non-Equilibrium Green's Function (NEGF) simulators and compare SCEs predicted by the model to simulated SCEs. While NEGF intrinsically considers quantum effects, we do not include quantum corrections in Sentaurus. However, as demonstrated shortly, the extended theory accurately reproduces SCEs predicted from both Sentaurus and NEGF, suggesting that scale length and boundary coupling coefficients are dictated mainly by electrostatics.

When simulating with Sentaurus, we use generic materials with parameters in Table I. When simulating with NEGF, we use CNTs for 1-D FETs [36], and monolayer black phosphorous (BP) and monolayer HfS_2 for 2-D FETs (using in-house code [20], [37]). We consider equal t_{ch} and κ_{ch} for 2-D FETs (see Table I) to highlight the role of the different density of states (DOS). Although extended SLT can be applied to single gate (SG) FETs [6] by introducing

TABLE I
PARAMETER SPACE ANALYZED IN FIG. 6. THE CHIRALITIES CORRESPONDING TO CNTs WITH $t_{ch} = 1$, 1.35 nm ARE (13, 0) AND (17, 0), RESPECTIVELY

Parameters	Sentaurus	CNT NEGF	BP/HfS_2 NEGF
t_{ch} (nm)	0.5, 1, 2	1, 1.35	0.524
t_{ox} (nm)	2, 4, 6, 8	2, 3, 4, 5	2, 3, 4, 5
κ_{ch}	4, 8, 12	6.9	15.8
κ_{ox}	10, 15, 20	20	20

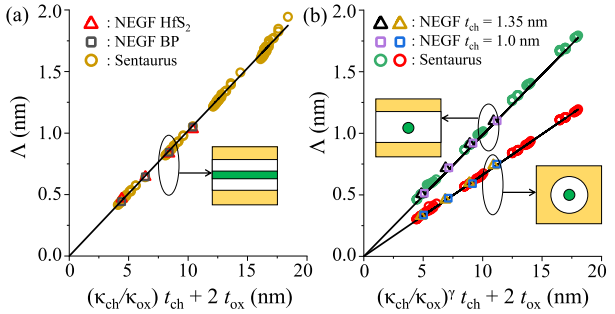

Fig. 6. Scale length Λ for (a) 2-D DG and (b) 1-D GAA and 1-D DG. Circles and squares/triangles represent values extracted from Sentaurus TCAD and NEGF, respectively, showing agreement between the solvers. Parameters used are highlighted in Table I.

an L_g-dependent Λ [38], we leave this application to future studies.

A. Scale Length

We extract Λ for three geometries [see Fig. 1(c)] with different combinations of t_{ch}, t_{ox}, κ_{ox}, and κ_{spa} across all combinations of variables shown in Table I (see Fig. 6).

A general expression for Λ in low-D FETs is

$$\Lambda_{low-D} = \pi \frac{[(\kappa_{ch}/\kappa_{ox})^{\gamma}]t_{ch} + 2t_{ox}}{A} \tag{24}$$

where A is a geometry-dependent coefficient and γ is a corrective factor that accounts for the different cross-sectional areas (normal to the source-to-drain direction) of planar (i.e., 2-D) and cylindrical (i.e., 1-D) channels

$$\gamma_{2-D} = 1, \quad \gamma_{1-D} = \left(\frac{\text{Area}_{ch}^{1-D}}{\text{Area}_{ch}^{1-D} + \text{Area}_{ox}^{1-D}}\right) \Big/ \left(\frac{\text{Area}_{ch}^{2-D}}{\text{Area}_{ch}^{2-D} + \text{Area}_{ox}^{2-D}}\right) \tag{25}$$

where Area_{ch} and Area_{ox} are the cross-sectional areas (normal to the source-to-drain direction) of channel and gate oxide, respectively.

Empirically, we find that for 1-D GAA, 1-D DG, and 2-D DG FETs, $A = 4.81$ (in agreement with [23]), 3.23, and 3.13 (close to the value proposed in [22]). We note that a higher A implies a smaller Λ and thus a stronger electrostatic control.

Critically, the concept of equivalent oxide thickness (EOT) is not applicable to low-D FETs, as Λ depends primarily on the physical thickness of the gate oxide t_{ox}, while the dielectric constants play only a minor role (also noted in [22]). This arises from the vanishing channel thickness; because only a small part of the source and drain fringe fields passes through the channel, the ratio between channel and oxide dielectric constants has minimal impact. The dielectric constant ratio is even less important in 1-D FETs, since the cross-sectional area of the channel is a smaller part of the total area due to the cylindrical channel geometry [see Fig. 1(c)]. As mentioned earlier, this effect is captured by γ. For 1-D GAA and DG, γ is given by, respectively,

$$\gamma_{1-D}^{GAA} = \frac{t_{ch}}{t_{ch} + 2t_{ox}}, \quad \gamma_{1-D}^{DG} = \frac{\pi}{4}\frac{t_{ch}}{t_{ch} + 2t_{ox}} \tag{26}$$

where the width of 1-D DG is $t_{ch} + 2t_{ox}$ [see Fig. 1(c)]. In this case, if γ tends to zero (as in 1-D with $t_{ox} \gg t_{ch}$), the dielectric constant ratio can be ignored altogether.

B. Boundary Coupling Parameters

Low-D FETs exhibit numerous tradeoffs between device geometry, extension doping, and dielectric constants. These tradeoffs are not present in bulk 3-D-semiconductor FETs and are likewise not captured by Λ [6]. We show that extended SLT and the new boundary coupling coefficients capture these effects (see Fig. 7) and, therefore, play a crucial role in the DTCO of low-D FETs (e.g., [6]).

We begin by considering α_G and α_D as functions of the extension doping concentrations in Fig. 7(a) for 1-D GAA, 1-D DG, and 2-D DG FETs. In order to capture only the impact of the different geometries, we consider the same channel material (Si, results obtained with Sentaurus). Regardless of the geometry, α_G and α_D increase as the extension doping increases. This behavior can be understood based on the definitions of α_G and α_D in (14) and (15), as Γ is known to decrease as doping increases [15], whereas Λ is unaffected by doping [6]. Moreover, as the dimensionality of the device goes from 3-D to 2-D and 1-D, the depletion length increases [15], leading to a decrease in the boundary coupling parameters. Given the qualitatively similar trends of α_G and α_D, we further simplify the discussion by only considering α_G for the remainder of this section (DIBL is shown in Fig. 7(f) for all the cases reported).

Next, we consider how α_G is influenced by the dielectric environment of low-D FETs. We plot α_G as a function of κ_{spa} (with fixed κ_{ox}) for different levels of doping in Fig. 7(b) for 1-D GAA CNFET. For higher doping, a high κ_{spa} increases the depletion in the extensions, reducing α_G. However, for low doping, where the depletion is already relatively long, the electrostatics is independent of the spacer relative dielectric constant.

The FET width also affects the electrostatics in 1-D DG. Indeed, a wider gate increases the fringe fields terminating in the 1-D extension, leading to an increase in the depletion and resulting in a decrease in α_G [see Fig. 7(c)].

Next, we consider whether the semiconductor material itself influences the extended SLT coupling parameters. We compare α_G for 2-D DG FETs with BP and HfS_2 channels because their electron DOS effective masses encompass those of other 2-D materials of interest (e.g., MoS_2 and WS_2 [39]). As shown in Fig. 7(d), the influence of a material's DOS on the coupling

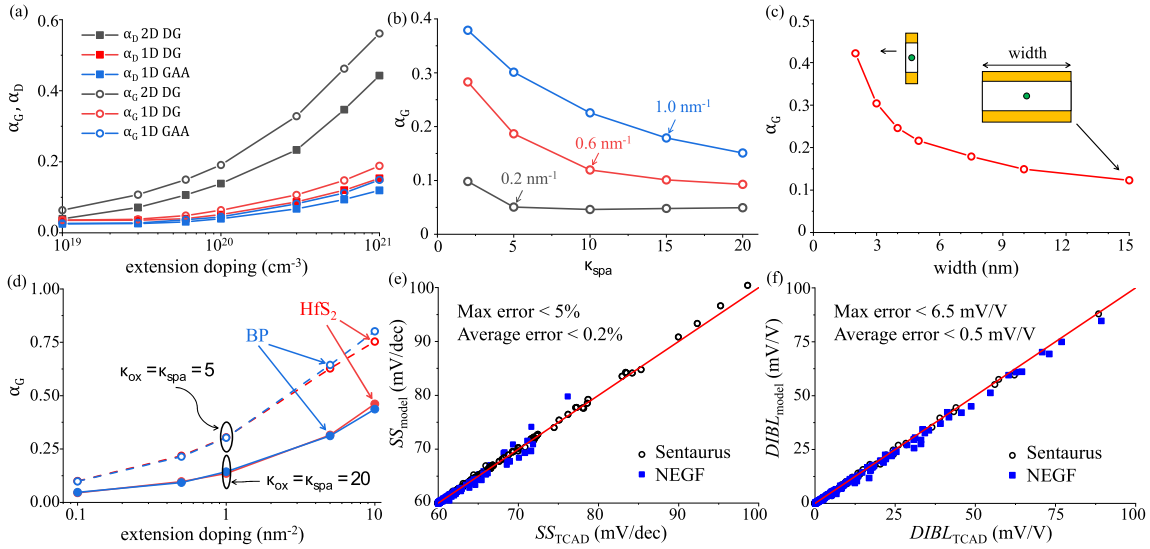

Fig. 7. (a) α_G and α_D versus extension doping for the low-D FET geometries shown in Fig. 1(c) for $\kappa_{ox} = \kappa_{spa} = 20$ for Si FET ($\kappa_{ch} = 11.7$, $t_{ox} = 2$ nm), extracted with Sentaurus. (b) α_G versus κ_{spa} for 1-D GAA (fixed $\kappa_{ox} = 20$) for three levels of extension doping (expressed in linear units), extracted with NEGF. (c) α_G versus device width for 1-D DG FET for $\kappa_{ox} = \kappa_{spa} = 20$, extracted with NEGF (fixed doping = 1.0 nm^{-1}). (d) α_G versus extension doping (expressed in areal units) for 2-D DG FETs using both BP and HfS_2 for $\kappa_{ox} = \kappa_{spa} = 5$ and 20, extracted with NEGF. (e) and (f) Comparison between SS and DIBL, respectively, for all cases considered in (a)-(d) (circles for Sentaurus, squares for NEGF). To avoid issues due to tunneling with the extraction of SS and DIBL from the transfer characteristics, we used the definitions based on the band profiles in (22) and (23).

parameters is negligible for a wide range of doping and relative dielectric constants.

Furthermore, boundary coupling parameters decrease as t_{ch} is reduced, as shown in Figs. 4(c) and (d). The extended SLT can therefore be applied to model the enhanced electrostatic control arising in bulk 3-D-seminconductor materials with few-nm-thin channels. For example, while not considered in this work, extended SLT might be applied to study the trade-off between electrostatic control and charge density in thin amorphous oxide materials, which are promising candidates for few-nm-thin channels [40], [41].

Finally, Fig. 7(e) and (f) shows the comparison between the model prediction and simulated values for SS and DIBL, respectively, for the cases in Fig. 7(a)–(d). The extended SLT has an average error <0.2% for SS (maximum error < 5%) and <0.5 mV/V for DIBL (maximum error < 6.5 mV/V).

IV. Conclusion

We extended the SLT to low-D FETs (e.g., 1-D and 2-D semiconductors) by including the impact of extensions on the channel's electrostatics. The extended SLT, based on three parameters, is fully analytical and accurately reproduces the channel potential and SCEs in low-D FETs. We provided a procedure to extract the new extended SLT parameters from potential profiles or FET transfer characteristics. The understanding gained from the boundary coupling parameters offers new opportunities to engineer low-D FETs. For example, SCEs are reduced by decreasing the extension doping or increasing the spacer dielectric constant. As a result, the extended SLT can be used in combination with DTCO to provide a path toward the introduction of low-D FETs in future technology nodes.

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