Performance & Stability Analysis of SRAM Cells Based on Different FinFET Devices in 7nm Technology

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***Abstract*—In this paper, the performances of 6T SRAM designs implemented by different FinFET devices are compared for different pull-up, pull down and pass gate transistor (PU:PD:PG) ratios to identify the best FinFET device for high speed and low power SRAM applications. Underlapped FinFETs (UF) and Design/Technology Co-Optimized FinFETs (DTCO_F) are used for the design and analysis. It is observed that with the PU:PD:PG ratios of 1:1:1 and 1:5:2 for the UF-SRAMs the read energy has degraded by 3.31% and 48.72% compared to the DTCO_F-SRAMs, respectively. However, the read energy with 2:5:2 ratio has improved by 32.71% in the UF-SRAM compared to the DTCO_F-SRAMs. The write energy with 1:1:1 configuration has improved by 642.27% in the UF-SRAM compared to the DTCO_F-SRAM. On the other hand, the write energy with 1:5:2 and 2:5:2 configurations has degraded by 86.26% and 96% in the UF-SRAMs compared to the DTCO_F-SRAMs. The stability and reliability of different SRAMs are also evaluated for 500mV supply.**

Keywords— SRAM, FinFET, Underlapped, Non-Underlapped, DTCO, Stability, Reliability.

I. Introduction

Scaling related challenges like the short channel effects (SCEs) in the bulk CMOS devices have led to the introduction of the FinFETs. FinFET offers better gate control, higher I_{ON}, better scalability and therefore, improved performance and reliability compared to the conventional CMOS designs. Among the double gate devices, the quasiplanar FinFET structure gained considerable attention because of the ease of the fabrication process [2]. In recent years, many Underlapped FinFET devices were proposed to have better control of the SCEs in the sub-nanometer technologies [1]-[4]. Underlap on either side of the gate increases effective channel length as seen by the charge carriers. Consequently, source-to-drain tunneling probability is improved. Moreover, edge direct tunneling leakage components can be reduced by controlling electric field at the gate-drain junction [3]. There is a limitation on the extent of underlap on drain or source sides because the I_{ON} is lower for larger underlap. Additionally, FinFET based designs have major width quantization issue. The width of a FinFET device increases only in quanta of silicon fin height (H_{FIN}) [2]. The width quantization issue becomes critical for ratioed designs like SRAMs, where proper sizing of the transistors is essential for fault-free operation. FinFETs based on Design/Technology Co-Optimization (DTCO_F) approach can overcome these issues [5]. DTCO_F follows the design rules illustrated in [6], which provides the specifications for the standard SRAM cells with special spacing rules and low leakages [6]. In this paper, 6T SRAM bit cells are designed using the UF and DTCO_F for high density, high performance and intermediate (trade-off between density and performance) applications. The performance and robustness of the SRAMs with different configurations of the transistors (PU:PD:PG = 1:1:1, 1:5:2 and 2:5:2) are evaluated at the 500mV supply voltage.

II. Characteristics of FinFET Devices

This section provides a comparison of the properties of the UF and DTCO_F devices. There are two types of UF devices available in the literature - the equal or symmetric underlapped FinFETs (SUF) and the unequal or asymmetric underlapped FinFETs (ASUF), where the unequal underlap on either side of the gate in FinFETs leads to different values of I_{ON} based on which ends of the device act as the source and drain terminals. The ASUFs offer better performance compared to the SUFs [4]. Moreover, the ASUFs with source side underlapped (SU) having long drain side underlapped (DU) achieves improved Drain Induced Barrier Lowering (DIBL) due to the better shielding of the channel potential barrier from the drain field lines by superseding drain underlap [4]. However, characteristics of the ASUFs with SU are worse because of the existence of the edge direct tunneling (EDT) [4]. Figure 1 shows the I-V characteristics of the n-type UF and DTCO_F. The n-type ASUF device with SU=1.09nm and DU= 1.635nm achieves the maximum I_{ON}-I_{OFF} ratio among the available n-type ASUFs. It is observed that the n-type DTCO_F has lower I_{ON} compared to the n-type UF. However, the DTCO_F offers higher I_{ON}-I_{OFF} ratio compared to the UF. TABLE 1 shows the device characteristics of the p-type FinFET devices. For our analysis, we have selected an n-type ASUF device with DU=1.635nm and SU=1.09nm, and a p-type SUF device illustrated in [2] and [4] to implement the design of the UF 6T SRAM. The following section explores different metrics of the UF and DTCO_F based SRAMs for different pull-up, pull-down and pass-gate configurations.

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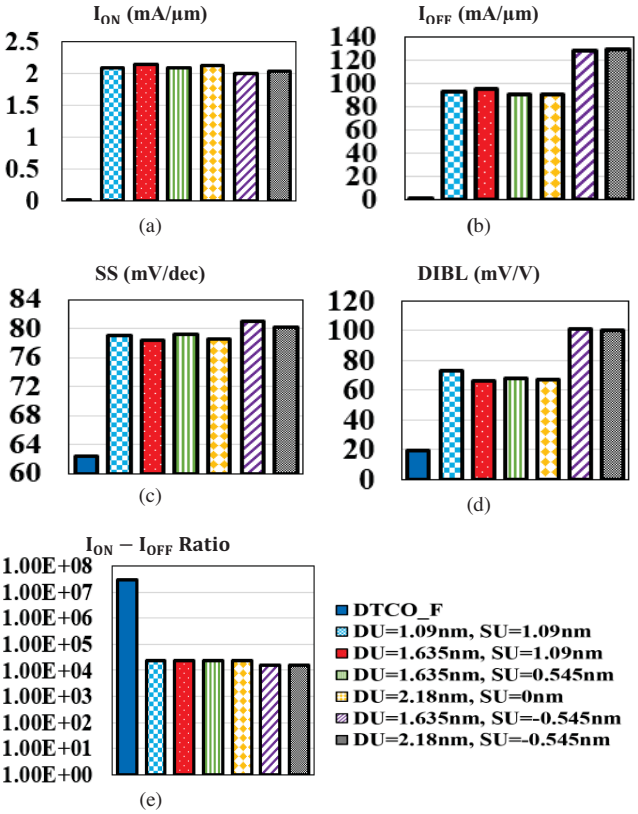

Figure 1: (a) I_{ON}; (b I_{OFF}; (c) SS (d) DIBL; (e) I_{ON}-I_{OFF} ratio of different existing n-type FinFET devices [2]-[6].

TABLE 1: EXISTING P-TYPE FINFETS DEVICE CHARACTERSITICS.

p-FinFET	I_{ON}	I_{OFF} (nA/μm)	SS (mV/dec)	DIBL (mV/V)	I_{ON}/I_{OFF}
SUF [2], [4]	1.99 mA/μm	100.44	78.4	74.9	$1.98\text{x}10^4$
DTCO_F [6]	26.90 μA/μm	0.004	64.34	24.1	$6.72\text{x}10^6$

III. BENCHMARKING OF UF-SRAMS VS. DTCO-F SRAMS

The 6T bit cell has been the industry standard from the beginning of the SRAM era. It consists of two bit-lines (BL, BLB) and one word-line (WL) as shown in Figure 2. The detail explanation of the 6T SRAM bit cell operation is available in [7].

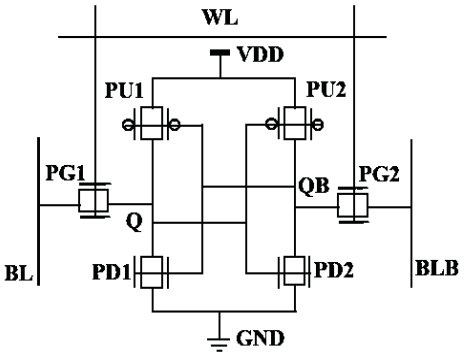

Figure 2: Schematic of FinFET based 6T SRAM cell [7].

Three different static noise margin (SNM) figures are essential to evaluate the robustness of the SRAM bit cell. These are the Hold Static Noise Margin (HSNM), the Write Static Noise Margin (WSNM) and the Read Static Noise Margin (RSNM). The reliability of the SRAM cells is investigated using the widely accepted methods [8]. Figure 3 and Figure 4 show the RSNM and the N-curve analysis of the UF-SRAM with a 500mV supply. It is observed that for the 1:1:1 configuration the UF-SRAM have the lowest robustness compare to the designs with other ratios. Monte Carlo simulation is also performed for the UF-SRAM with 1:1:1 ratio to evaluate the impact of the process variations. The threshold voltage (V_{TH}) is modeled as a ±10% Gaussian distribution with a variation of the ±3σ level. Figure 5 shows the Monte Carlo analysis of the UF-SRAM bit cell for 1:1:1 configuration with 3000 samples at the 500mV supply voltage. TABLE 2 provides the summary of the performance and stability of the UF and DTCO_F based SRAMs for different PU:PD:PG configurations.

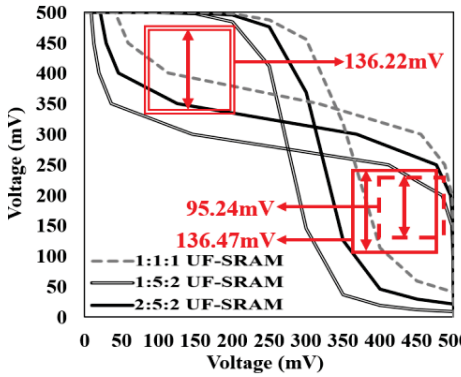

Figure 3: RSNM of different configuration UF-SRAMs.

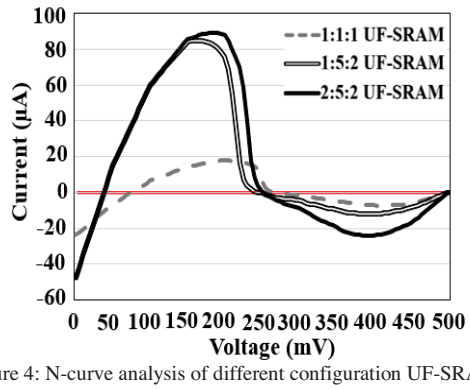

Figure 4: N-curve analysis of different configuration UF-SRAMs.

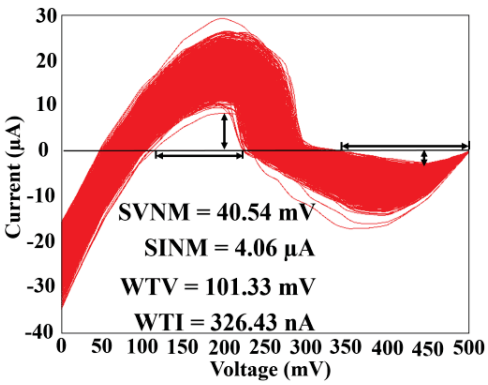

Figure 5: N-curve analysis of 1:1:1 UF SRAM under process variation.

TABLE 2: BENCHMARKING OF AUF SRAM DESIGNS.

Designs	6T UF-SRAM			6T DTCO_F-SRAM		
Technology	7 nm			7 nm		
Supply	500mV			500mV		
PU:PD:PG	1:1:1	1:5:2	2:5:2	1:1:1	1:5:2	2:5:2
Standby leakage power	852.34 pW	2.719 nW	3.07 nW	27.5 pW	27.5 pW	27.5 pW
Read Power (nW)	1.68	3.06	3.24	2.01	2.036	2.04
Write Power (nW)	1.34	58.63	118.8	5.1	5.09	5.09
Read Delay (ns)	2.68	0.161	0.179	2.77	1.97	2.11
Write Delay (ns)	0.092	0.064	0.187	0.179	0.043	0.174
HSNM (mV)	175.13	182.81	183.26	240.2	240.4	240.4
RSNM (mV)	95.24	136.22	136.47	174.8	175.2	175.3
WSNM (mV)	401.33	421.18	411.15	189.8	190.1	190.3
SVNM (mV)	195.76	204.33	212.88	202.57	202.6	202.62
SINM (µA)	17.96	89.27	84.79	9.60	9.62	9.66
WTV (mV)	229.58	253.64	248.53	232.79	233.01	233.2
WTI (µA)	7.201	23.96	11.92	2.40	2.43	2.44
Area (μm^2)	0.0114	0.0196	0.0218	0.0117	0.0212	0.0231

IV. CONCLUSION AND FUTURE WORK

It is observed that for the UF based SRAM designs, an ASUF with DU=1.635nm and SU=1.09nm offers the maximum I_{ON}/I_{OFF} ratio, which we selected to implement the SRAM for different configurations. The standby leakage power in the DTCO_F-SRAMs for 1:1:1, 1:5:2 and 2:5:2 configurations has improved by 31, 99 and 111.63 times compared to UF-SRAMs of the same configurations, respectively. Also, the DTCO_F-SRAMs consume less power. Therefore, the DTCO_F devices are better for the low power SRAMs. However, the UF-SRAMs offer 1.03, 12.23 and 11.78 faster read times compared to the DTCO_F SRAMs for 1:1:1, 1:5:2 and 2:5:2 configurations, respectively. Therefore, the UF-SRAMs are more suitable for the high speed SRAMs. The UF-SRAMs have lower stability compared to the DTCO_F-SRAMs. The RSNM of the UF-SRAMs degraded by 83.353%, 28.61% and 28.45% for 1:1:1, 1:5:2 and 2:5:2 configurations. Moreover, from the combined information of SVNM and SINM it is confirmed that the read stability of the UF-SRAMs is worse than that of the DTCO_F-SRAMs. However, the UF-SRAMs have better write ability. The WSNM of the UF-SRAMs has improved by 52.7%, 54.86% and 53.71% for 1:1:1, 1:5:2 and 2:5:2 configurations. From the combined information of WTV and WTI, we can conclude that the write ability of the UF-SRAMs is better than that of the DTCO_F-SRAMs. Further detail will be included in the extended journal version, where we will also include the analysis of SRAM array based on UF and DTCO_F devices.

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