# Monte Carlo Comparison of n-Type and p-Type Nanosheets With FinFETs: Effect of the Number of Sheets

F. M. Bufler, D. Jang, G. Hellings, *Senior Member, IEEE*, G. Eneman, *Member, IEEE*, P. Matagne, A. Spessot, and M. H. Na

***Abstract*— Analytic doping profiles and contact resistivities are adjusted to reproduce measured transfer characteristics of state-of-the-art n-type and p-type FinFETs by Monte Carlo device simulation. The results are used to compare the performance of nanosheets (NSs) and FinFETs at advanced-node device dimensions. It is found that the ON-current normalized by the effective gate width reduces for a higher number of sheets due to a higher access resistance of the lower-lying sheets. In order to reach the same absolute current level of FinFETs with a fin height of 55 nm, more than two sheets for n-type and about four sheets for the p-type NSs with a NS width of 16 nm are needed, respectively. This technology computer-aided design (TCAD) approach can serve as input for design-technology cooptimization (DTCO) of advanced devices.**

***Index Terms*— FinFET, Monte Carlo (MC), nanosheet (NS), technology computer-aided design (TCAD).**

## I. Introduction

AMONG gate-all-around devices with improved subthreshold characteristics reducing the short-channel effect, the nanosheet (NS) transistor [1] is a promising candidate as an alternative to the FinFET because the possibility to stack sheets and varying their width permits to adjust the drive current. Technology computer-aided design (TCAD) is an efficient way to optimize transistor performance and compare different device architectures. It has been employed to compare NS and nanowire transistors with FinFETs [2]–[4] and to investigate in NSs the effect of a parasitic bottom-channel [5], the impact of the sidewall high-$k$ layer [6] and issues related to the channel-release process [7]. So far, only n-type NS devices have been simulated.

It is the purpose of this work to provide an accurate and realistic comparison of both n-type and p-type NS devices with FinFETs. To this end, Monte Carlo (MC) device simulation [8] is used based on analytic doping profiles and contact resistivities which are adjusted to reproduce measured transfer characteristics of state-of-the-art FinFETs [9]. Thus, quasi-ballistic transport is directly incorporated without the need as in drift-diffusion simulation to adjust device-model parameters of unclear range of validity [7]. On the other hand, the adjustment of doping and contact resistance ensures that the comparison of n-type and p-type devices not only considers differences in intrinsic transport properties, but also in doping levels and resistivity values. Finally, we show that single-sheet device simulation [4] is inaccurate by investigating the influence of the number of sheets on performance.

Manuscript received August 7, 2020; revised September 3, 2020; accepted September 11, 2020. Date of publication September 23, 2020; date of current version October 22, 2020. The review of this article was arranged by Editor A. Schenk. *(Corresponding author: F. M. Bufler.)*

F. M. Bufler is with IMEC, 3001 Leuven, Belgium, and also with ETH Zürich, 8092 Zürich, Switzerland (e-mail: fabian.bufler@imec.be).

D. Jang, G. Hellings, G. Eneman, P. Matagne, A. Spessot, and M. H. Na are with IMEC, 3001 Leuven, Belgium.

Color versions of one or more of the figures in this article are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TED.2020.3024267

## II. Comparison With Measurements

Quantum-corrected MC device simulation is used for the simulation study. The silicon band structure is described by an analytic two-band model for electrons and the six-band $\mathbf{k} \cdot \mathbf{p}$ model for holes. We consider scattering by phonons, surface roughness, and ionized impurities with a calibrated doping-dependent prefactor of the scattering rate. As the focus is the investigation of the ON-current (ION) for a gate-last process, neither remote Coulomb nor remote phonon scattering is included. More details can be found in [3] and [8].

Stress engineering is important for performance improvement. Therefore, the theoretical stress-induced mobility enhancements have to be validated by experimental long-channel effective mobilities. For electrons, high tensile stress can be obtained in strained-silicon on-insulator (SSOI) Tri-Gate devices. Fig. 1 shows that MC simulation accurately reproduces the measured stress-induced electron mobility enhancements [10] without any parameter adjustment. For holes, only moderate uniaxial compressive stress can be achieved in long-channel MOSFETs, but MC simulation is also in agreement with measured hole mobility improvements [11].

Short-channel device simulation is based on analytic doping profiles and stress simulation [12]. Channel stress is governed by lattice mismatch between the source/drain (S/D) regions and the silicon substrate. For p-type devices, the S/D regions consist of $Si_{1-x}Ge_x$. In the case of n-type devices

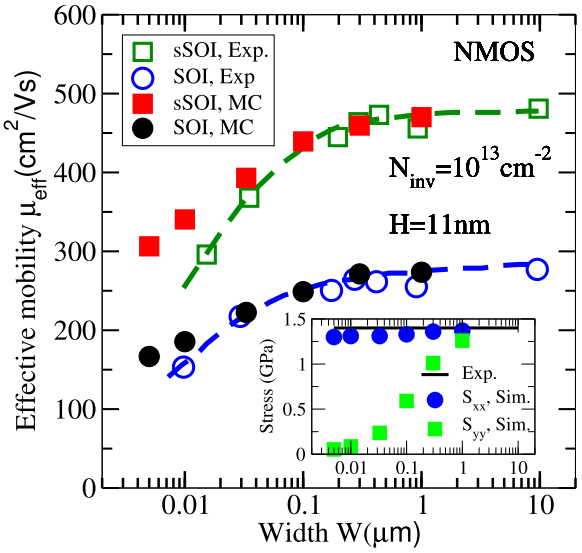


Fig. 1. Effective long-channel electron mobility of Tri-Gate silicon on-insulator (SOI)-FETs as a function of device width according to measurements [10] and MC simulations with and without mechanical stress [inset: corresponding stress components in channel direction ($S_{xx}$) and in width direction ($S_{yy}$)].

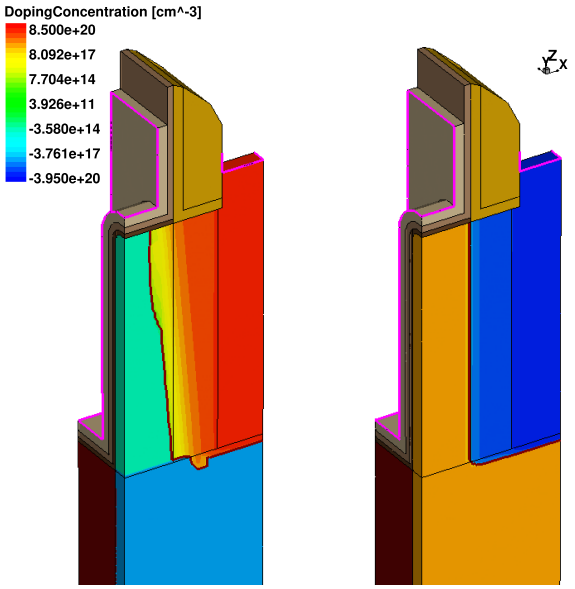


Fig. 2. Geometry and approximated doping profile of the n-type (left) and p-type (right) FinFETs. The gate oxide consists of 1.0 nm interfacial oxide and 1.3 nm $HfO_2$. The contacted poly pitch (CPP) is 57 nm and the FP is 30 nm. The diamond-shaped S/D regions (not visible) are only contacted from above. The channel orientation is in ⟨110⟩ direction.

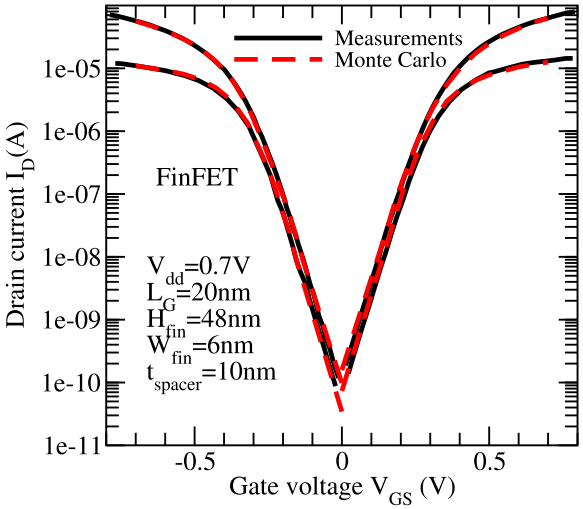


Fig. 3. Transfer characteristics at $V_{DS}$ = 0.7 V and $V_{DS}$ = 0.05 V according to MC simulations and measurements of the p-type and n-type FinFETs of [9] shown in Fig. 2, using in MC simulation a contact resistivity of $1.5 \times 10^{-9}$ Ω cm$^2$ for the p-type and $0.75 \times 10^{-9}$ Ω cm$^2$ for the n-type FinFET.

the lattice-mismatch induced by a high S/D phosphorus concentration is considered in terms of an equivalent $Si_{1-y}C_y$ epilayer [13]. Furthermore, the impact of the replacement metal gate process step on stress is taken into account. Besides considering the effect of the channel stress on the band structure, also the modifications of the conduction- and valence-band edges due to the stress and mole fraction profiles are used in the driving force during MC simulation.

The procedure to reproduce the measured short-channel FinFET transfer characteristics [9] basically comprises 1) the approximation of the doping profiles by error functions for S/D and extension regions and a constant channel doping as well as the adjustment of 2) the Ge-content $x$ for the $p$-FinFET and the equivalent C-content $y$ for the $n$-FinFET, respectively, and 3) the contact resistivities at the source/drain contacts. The resulting doping profiles for $n$-FinFET and $p$-FinFET are shown in Fig. 2 and the corresponding MC transfer characteristics in comparison to the measurements can be seen in Fig. 3.

While the channel of the $n$-FinFET is undoped and features a height-dependent small gate underlap, the $p$-FinFET has a doping concentration of $5 \times 10^{18}$ cm$^{-3}$ in the channel which is the same doping-level as in the silicon substrate. The Ge-content in the S/D region of the $p$-FinFET is $x = 0.5$ and the equivalent C-content in the S/D region of the $n$-FinFET is $y = 0.02$ resulting into respective channel stresses of $-1.14$ GPa for the $p$-FinFET and 583 MPa for the $n$-FinFET. The contact resistivities are $0.75 \times 10^{-9}$ Ω cm$^2$ and $1.5 \times 10^{-9}$ Ω cm$^2$ for $n$- and $p$-FET which are in the order of reported measurements [14], but on the lower side consistent with the reported optimization of contact process and S/D epitaxy [9]. It should be noted that the result of these approximations depends on the chosen framework in terms of doping functions, resistance, and transport model. For example, in the absence of a contact resistance our procedure permits a similar good agreement with measurements, but e.g., ION of the n-type FinFET at the smaller gate length ($L_G$) in Section III is then increased by 4%. However, achieving good agreement for both low and high drain bias with reasonable doping and contact resistivity values and without MC model parameter tuning reduces the ambiguity considerably.

A final aspect concerns the gate-stack where the insulator consists of $HfO_2$ as high-$k$ material and a thin silicon oxide interfacial layer at the interface to silicon. Theoretical first-principle [15] and experimental [16] investigations have shown that the permittivity of this thin interfacial silicon oxide

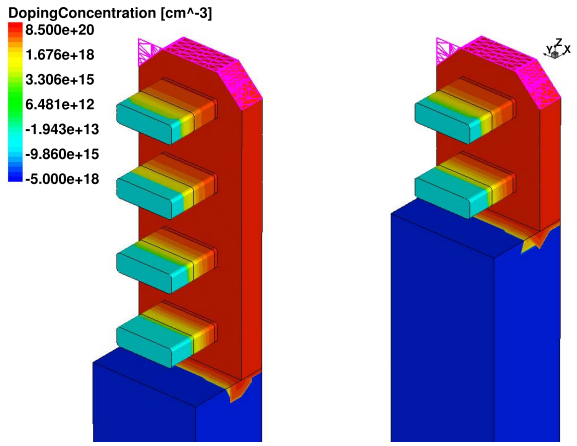


Fig. 4. Geometry and doping profile of the n-type NSs with 4 and 2 sheets. The CPP is 45 nm and the lateral pitch is 30 nm (the corresponding FP of the FinFET, the transfer characteristics of which are shown in Fig. 5, is 21 nm). The distance between sheets is 14 nm. The channel orientation is as in the case of FinFETs in ⟨110⟩ direction.

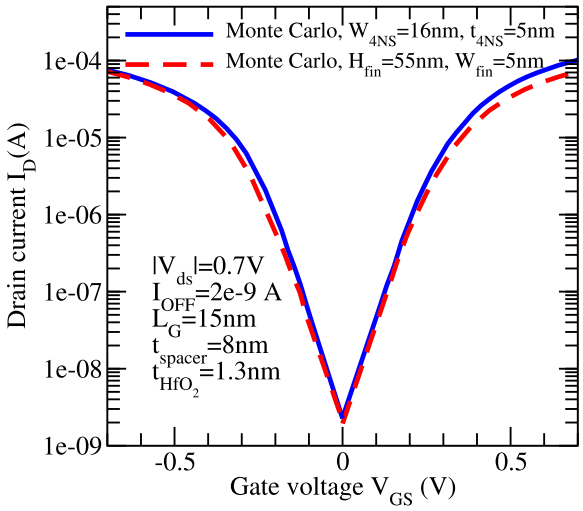


Fig. 5. MC transfer characteristics in logarithmic scale at the same OFF-current per device of $I_{OFF}$ = 2 nA for NSs with four sheets and FinFETs.

layer in the gate-stack deviates from its bulk value. This is related to the substoichiometric nature of the thin layer [15] and leads to a permittivity of $SiO_x$ between 6 and 7 in units of the vacuum permittivity $\varepsilon_0$ [15], [16]. Therefore, we have used an interfacial $SiO_x$ layer with a value of 7 $\varepsilon_0$ for the permittivity together with a layer thickness of 1 nm.

## III. Impact of the Number of Sheets

In this section, we apply the approach adopted in this work—using MC device simulation based on the adjustment of doping and contact resistance to state-of-the-art FinFET measurements to explore advanced technology nodes—to compare the performance of stacked NSs and FinFETs with a focus on the influence of the number of sheets. To enable a comparison of only the device architectures, the same S/D doping profiles are used, but due to a similar S/D process this is also a reasonable assumption. Fig. 4 shows the doping profiles of the n-type NS transistor with 4 and 2 sheets. Note that the height-dependence of the gate underlap in the FinFET corresponds in the NS to different underlaps in the different sheets. The largest underlap is, as in [1, Figs. 7 and 15], in the lowest sheet. In Fig. 5 the transfer characteristics of the n- and p-type NS transistors with four sheets are compared to those of the FinFETs. Device dimensions typical for advanced nodes as specified in Figs. 4 and 5 are used. In particular, the silicon film thickness is 5 nm and $L_G$ = 15 nm. Note that the definition of $L_G$ includes on both spacer sides 1.3 nm of $HfO_2$. The fin height is $H_{fin}$ = 55 nm and the NS width is $W_{NS}$ = 16 nm. For stress simulation, no formation of dislocations or voids is considered. Then the channel stress is governed by the volume ratio between the channel/extension regions on the one hand and the S/D regions on the other hand. In this case, the channel stress in NSs is similar to that in FinFETs (somewhat above 1 GPa compressive stress for the p-type devices and about 600 MPa tensile stress for the n-type devices). The workfunction is always adjusted such that the OFF-current per device is 2 nA. The NS transistors feature an improved subthreshold slope. ION of the p-type devices are similar, while the *n*- NS has a higher ION than the *n*-FinFET, but one has to keep in mind that the absolute values of ION in A are dominated by $H_{fin}$ and the number as well as $W_{NS}$ of the NSs.

We now turn to the investigation of the impact of the number of sheets on the performance of NS transistors. The NS ION as a function of the number of sheets is displayed in Fig. 6(a) in absolute values (i.e., in units of $\mu$A) and in Fig. 6(b) normalized with the effective gate width $W_{eff}$ (in units of $\mu$A/$\mu$m). For comparison, the corresponding ION of the FinFETs are shown. Fig. 6(a) demonstrates that beyond two sheets the absolute values of ION no longer increase linearly with the number of sheets. This also happens for p-type NS transistors where the gate underlap does not change for the different sheets. The conclusion is that the lower-lying sheets are affected by a higher access resistance as they are farther away from the S/D contacts and, therefore, contribute less to the total current than the higher-lying sheets. This is supported by Fig. 6(b) where one can see that ION normalized by $W_{eff}$ decreases with increasing number of sheets. For example, in the n-type NS transistor with four sheets the lowest-lying sheet carries less than half the current than the top-most sheet.

Finally, we compare ION per $W_{eff}$ between NS transistors and FinFETs in Fig. 6(b). In the case of FinFETs, n- and p-type devices involve about the same ION, while for NSs the p-type device has a significantly lower performance than its n-type counterpart and approaches for the 1-sheet device ION of the FinFETs. There are many different effects which contribute to ION of short-channel multigate devices. Favorable for transport in n-type NSs is the dominant (001) surface orientation compared to the (110) sidewall orientation in FinFETs with the opposite and stronger trend in p-type devices. The higher surface-to-volume ratio of narrow-width NSs involves a stronger impact of surface scattering [3] and the channel doping of p-type devices reduces their mobilities. On the other hand, the better gate-control in NSs involves a higher channel charge for the same gate-overdrive

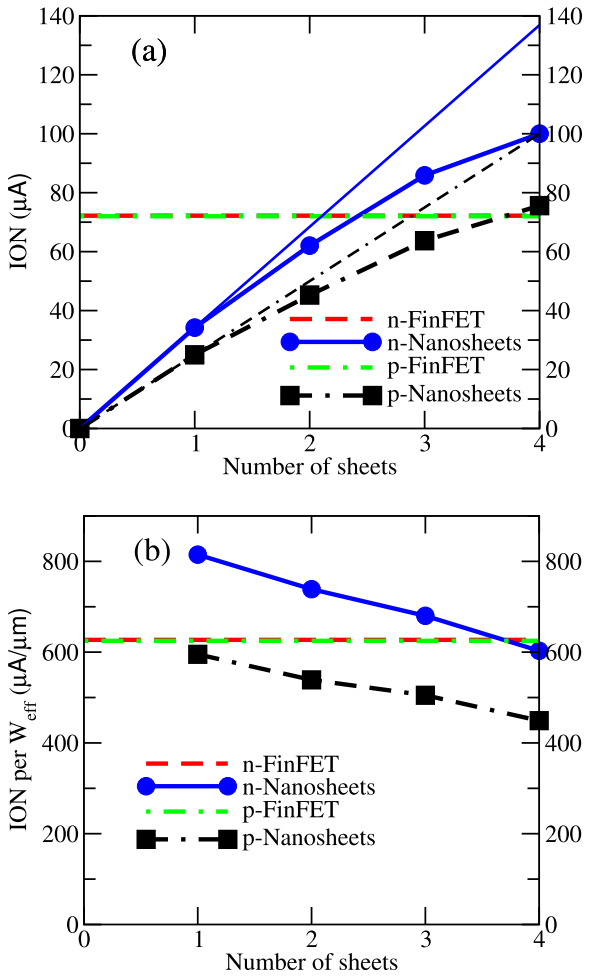


Fig. 6. ION of NSs as a function of the number of sheets $N_{sheet}$ in microampere (a) and normalized with $W_{eff}$ (b) according to MC device simulation. For comparison, also the ideal NS ION as obtained by multiplying the single-sheet ION by $N_{sheet}$ are shown (a) as well as ION of the FinFETs.

than in FinFETs. Together with a different importance of quasi-ballistic overshoot all these aspects determine ION in Fig. 6(b). However, for a comparison of the intrinsic performance between NS transistors and FinFETs the access resistance, which consists of the resistance of the S/D regions and the contact resistance, has to be the same. For a similar S/D resistance, the distance between the top of the highest sheet and the bottom of the lowest sheet should equal $H_{fin}$. This is approximately the case for an NS transistor with 3.5 sheets. On the other hand, the contact area of the FinFETs is smaller due to a smaller fin pitch (FP) which leads for the same contact resistivity to a higher contact resistance. Taking the same contact resistance as for the NS transistors increases ION of n-type and p-type FinFETs to 633 and 647 $\mu$A/$\mu$m, respectively. Therefore, for the same access resistance ION of n-type and p-type FinFETs is 1.3% smaller and 35.6% higher than their equivalent NS counterparts.

## IV. Conclusion

A TCAD approach has been presented which allows for an accurate and realistic comparison of short-channel multigate devices for future technology nodes. It is based on MC device simulation and the adjustment of analytic doping profiles and contact resistances to measurements of state-of-the-art FinFETs. As an application, it was shown that increasing the number of sheets only adds an increasingly smaller contribution to ION of NSs. The presented TCAD methodology can serve as a reference and an input to design-technology cooptimization (DTCO) for a complete assessment of technology options.

## References

[1] N. Loubet *et al.*, "Stacked nanosheet gate-all-around transistor to enable scaling beyond FinFET," in *Proc. Symp. VLSI Technol.*, Kyoto, Japan, Jun. 2017, pp. 230–231, doi: 10.23919/VLSIT.2017.7998183.

[2] S.-D. Kim, M. Guillorn, I. Lauer, P. Oldiges, T. Hook, and M.-H. Na, "Performance trade-offs in FinFET and gate-all-around device architectures for 7 nm-node and beyond," in *Proc. IEEE SOI-3D-Subthreshold Microelectron. Technol. Unified Conf. (S3S)*, Rohnert Park, CA, USA, Oct. 2015, pp. 1–3, doi: 10.1109/S3S.2015.7333521.

[3] F. M. Bufler, R. Ritzenthaler, H. Mertens, G. Eneman, A. Mocuta, and N. Horiguchi, "Performance comparison of *n*–type Si nanowires, nanosheets, and FinFETs by MC device simulation," *IEEE Electron Device Lett.*, vol. 39, no. 11, pp. 1628–1631, Nov. 2018, doi: 10.1109/LED.2018.2868379.

[4] D. Nagy, G. Espiñeira, G. Indalecio, A. J. García-Loureiro, K. Kalna, and N. Seoane, "Benchmarking of FinFET, nanosheet, and nanowire FET architectures for future technology nodes," *IEEE Access*, vol. 8, pp. 53196–53202, 2020, doi: 10.1109/ACCESS.2020.2980925.

[5] Y. Choi *et al.*, "Simulation of the effect of parasitic channel height on characteristics of stacked gate-all-around nanosheet FET," *Solid-State Electron.*, vol. 164, Feb. 2020, Art. no. 107686, doi: 10.1016/j.sse.2019.107686.

[6] D. Ryu, M. Kim, J. Yu, S. Kim, J.-H. Lee, and B.-G. Park, "Investigation of sidewall high-k interfacial layer effect in gate-all-around structure," *IEEE Trans. Electron Devices*, vol. 67, no. 4, pp. 1859–1863, Apr. 2020, doi: 10.1109/TED.2020.2975255.

[7] S. Kim *et al.*, "Investigation of electrical characteristic behavior induced by channel-release process in stacked nanosheet gate-all-around MOSFETs," *IEEE Trans. Electron Devices*, vol. 67, no. 6, pp. 2648–2652, Jun. 2020, doi: 10.1109/TED.2020.2989416.

[8] *Sentaurus Device Monte Carlo User Guide, Release O-2018.06*, Synopsys, Mountain View, CA, USA, 2018.

[9] S.-Y. Wu *et al.*, "Demonstration of a sub-0.03 um$^2$ high density 6-T SRAM with scaled bulk FinFETs for mobile SOC applications beyond 10 nm node," in *Proc. Symp. VLSI Technol.*, Honolulu, HI, USA, Jun. 2016, pp. 92–93, doi: 10.1109/VLSIT.2016.7573390.

[10] R. Coquand *et al.*, "Strain-induced performance enhancement of tri-gate and omega-gate nanowire FETs scaled down to 10nm width," in *Proc. Symp. VLSI Technol.*, Honolulu, HI, USA, Jun. 2012, pp. 13–14, doi: 10.1109/VLSIT.2012.6242437.

[11] F. M. Bufler, A. Tsibizov, and A. Erlebach, "Scaling of bulk pMOSFETs: (110) surface orientation versus uniaxial compressive stress," *IEEE Electron Device Lett.*, vol. 27, no. 12, pp. 992–994, Dec. 2006, doi: 10.1109/LED.2006.886706.

[12] *Sentaurus Process User Guide, Release O-2018.06*, Synopsys, Mountain View, CA, USA, 2018.

[13] M. Berti *et al.*, "Lattice parameter in $Si_{1-y}C_y$ epilayers: Deviation from Vegard's rule," *Appl. Phys. Lett.*, vol. 72, no. 13, pp. 1602–1604, 1998, doi: 10.1063/1.121127.

[14] H. Yu *et al.*, "$1.5\times10^{-9}$ Ωcm$^2$ contact resistivity on highly doped Si:P using Ge pre-amorphization and Ti silicidation," in *IEDM Tech. Dig.*, Washington, DC, USA, Dec. 2015, pp. 592–595, doi: 10.1109/IEDM.2015.7409753.

[15] F. Giustino, A. Bongiorno, and A. Pasquarello, "Equivalent oxide thickness of a thin oxide interlayer in gate insulator stacks on silicon," *Appl. Phys. Lett.*, vol. 86, no. 19, May 2005, Art. no. 192901, doi: 10.1063/1.1923185.

[16] C. M. Perkins, B. B. Triplett, P. C. McIntyre, K. C. Saraswat, S. Haukka, and M. Tuominen, "Electrical and materials properties of $ZrO_2$ gate dielectrics grown by atomic layer chemical vapor deposition," *Appl. Phys. Lett.*, vol. 78, no. 16, pp. 2357–2359, Apr. 2001, doi: 10.1063/1.1362331.