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Unit 19, Assignment 2

The Data Driver

Solihull College
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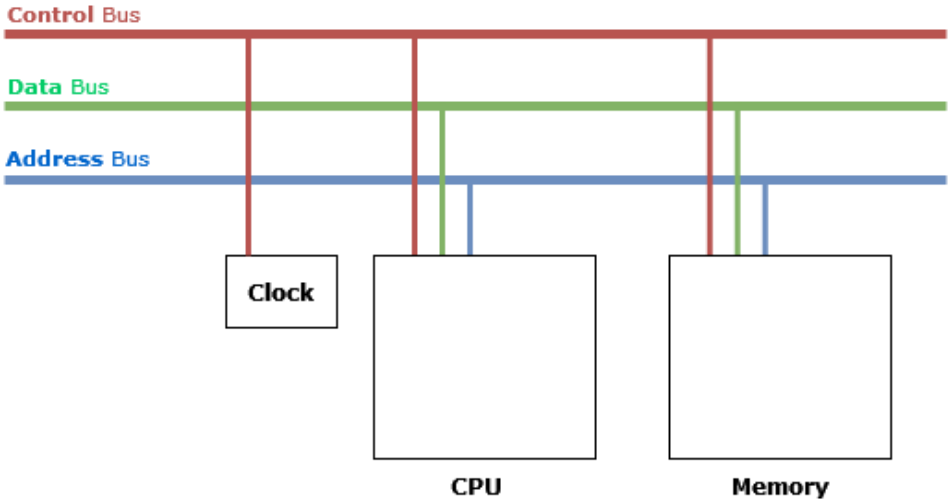
Task One P5

Key Components



CPU

The Central Processing Unit carries out instructions as part of the Fetch, Decode, Execute cycle. It is connected to all the system buses (Control, Data, Address).

Registers

Registers are tiny areas of memory within a CPU that store data being acted upon.

- **Program Counter** stores the address of the instruction to be executed
- **Instruction Register** stores the instruction to be executed.
- **Address Register** stores the address of memory to be acted upon
- **Accumulator** holds results of arithmetic operations
- **General Purpose Registers** are available for programs to use for any purpose

Memory

Memory is used to store instructions and data that the CPU will require. There are several types of memory, some integrated into the CPU itself, such as registers and cache. The CPU uses system memory to store information that it may need to access in the future—more frequently accessed than mass storage but not used for immediate access data.

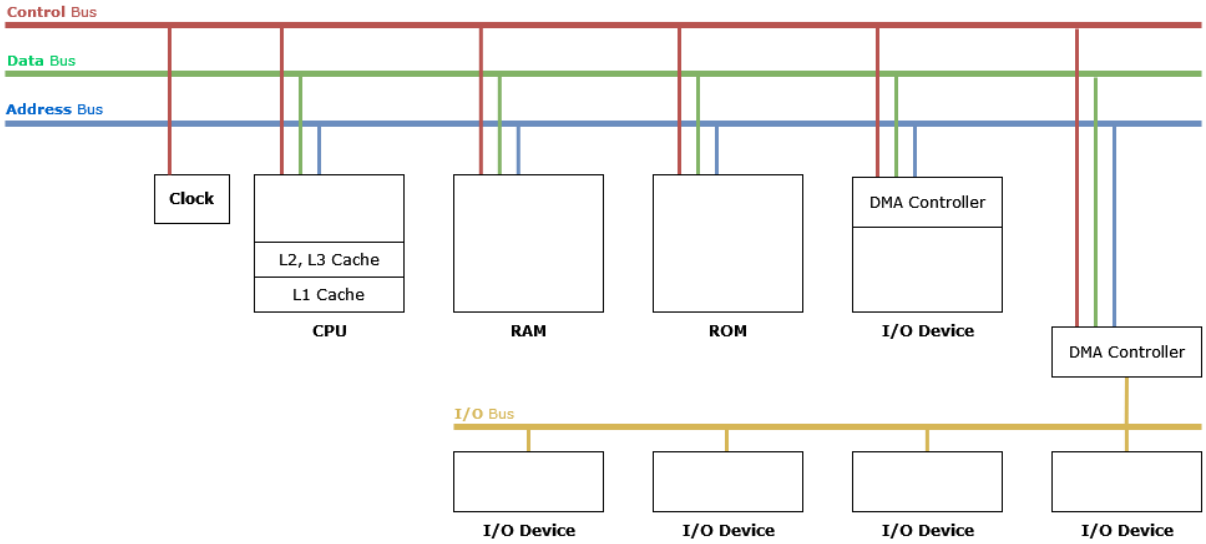
Clock

The clock is responsible for generating electrical pulses that other components in a CPU and in the system use for synchronising their operations. It is connected to a computer's clock bus circuit, a part of the control bus.
A CPU's control circuitry will 'multiply' a slower clock signal to allow itself to run faster. Changing this multiplier is referred to as 'overclocking' and allows a CPU to perform instructions faster however if the CPU cannot perform them fast enough, data will become corrupted, and the system will be unstable.

In some systems, the clock is integrated into the CPU rather than being a discreet component.

Task Two & Three P6, M2

Memory



Volatility

Volatile memory requires power for the stored data to be retained. When power is lost or interrupted, the stored information is also lost.

Non-volatile memory, in contrast, can retain information even when no power is applied.

Dynamic RAM (DRAM)

Dynamic RAM uses capacitors to store each bit of data. These need to be refreshed periodically, otherwise they will lose their charge and revert to representing a 0. DRAM is slower and cheaper than SRAM, so it is used for larger arrays of memory, such as main system RAM.

Static RAM (SRAM)

Static RAM makes use of transistors to store data. Unlike the capacitors used in DRAM, these transistors do not need to be periodically refreshed. Reading from and writing to SRAM is faster, so consequently it is used for small areas of memory that are frequently accessed, such as CPU cache.

Both DRAM and SRAM are examples of volatile memory.

Direct Memory Access (DMA)

Direct Memory Access is the process of allowing another device access to memory without the involvement of the CPU. It is used for connecting I/O devices as well as storage to a system.

Mass Storage

Mass storage is a large area of general-purpose storage. Solid State Drives and Hard Disk Drives are examples of mass storage mediums. Data such as the operating system, applications and user files will be stored here. The size of mass storage will be significantly greater than that of ROM, RAM or Cache but access time and transfer speeds are lower.

Read-Only Memory (ROM)

Read-Only Memory is memory that cannot be written to in general use. ROM chips are used for components such as the BIOS and firmware devices. These can be connected to a processor directly or through a storage or I/O bus. Read-only memory is non-volatile.

Random-Access Memory (RAM)

Random-Access Memory is memory that can be read from and changed at-will by the CPU and other components. Data can be read from and written to any part of the memory at any time, and it is used for storing working data. RAM is connected to a CPU via the system buses. On older computers, RAM was connected via a processor on the motherboard called the Northbridge. RAM is made up of DRAM modules and is volatile.

Cache

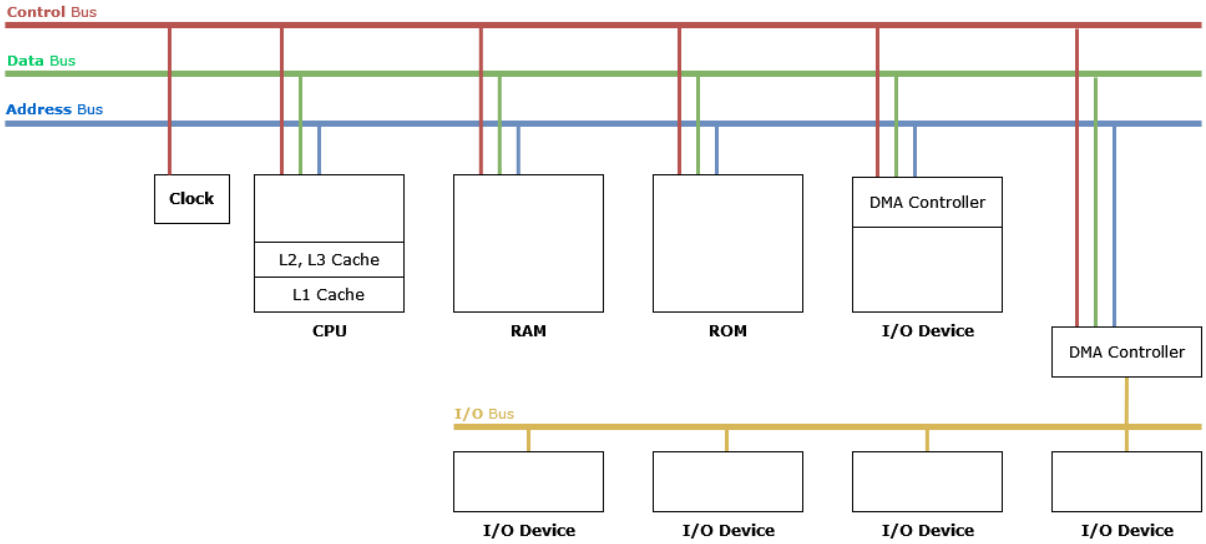
In a CPU, cache is a small area of fast memory that is located within the CPU. It stores copies of frequently accessed data from other memory to enable the CPU to work as fast as possible. The primary benefit of cache is latency (access time). This means the CPU needs to spend less time waiting for a data to be returned.

Modern CPUs feature multiple layers of cache. L1 is the fastest, typically less than a megabyte. L2 and beyond store more data—often several megabytes—but are slower for CPU cores to access.

Memory	Speeds	Latency	Average Capacity	Composition	Volatile?
CPU L1 Cache	Clock	~1ns	< 2MB	SRAM	Yes
CPU L2 Cache	Clock	~7ns	< 16MB	SRAM/DRAM	Yes
RAM (DDR5)	51.2GB/s per module, 7200 MT/s	~16ns	From 2GB to TBs	DRAM	Yes
ROM (Firmware)	Varies	~150,000ms	Several MBs	EPROM Flash	No
DMA Device (SSD)	~1GB/s	~150,000ms	< 2TB	NAND Flash	No

Task Four D1

System Buses



Buses

A bus is a shared connection between several components. Types of buses include multidrop and daisy-chain. The three system buses are the Control Bus, the Data Bus, and the Address bus. These are all multi-drop buses. Some components, however, may be point-to-point with direct connections to a CPU.

The terms below are general terms. Within a system, there may be several different control buses, address buses and data buses each performing a specific purpose. For example, a modern CPU will access RAM over a dedicated memory bus to reduce bottlenecks.

Control Bus

The Control Bus is used for control signals, such as sending interrupts to the CPU or requesting control of other buses. While the clock bus is typically separate, it can also be considered as part of the control bus.

Address Bus

The Address Bus is used for specifying addresses between devices. When the CPU or a DMA controller needs to read or write, it specifies the relevant memory locations on the address bus.

Data Bus

The Data Bus is a high bandwidth bus where data elements are transferred between components.

CPU

The CPU's control circuity is connected to the Control Bus; the Memory Buffer Register to the Data Bus; and the Memory Address Register to the Address Bus.

Memory Access

The CPU accesses system memory through the address bus and the data bus. The address bus is used to specify the address of memory to be read from or written to and the data bus is used for transferring the data elements.

Modern CPUs will have their Integrated Memory Controller and the Memory Management Unit connected to system RAM over a dedicated memory bus.

I/O Access & DMA

Direct Memory Access is the process wherein an I/O device transfers data to memory without the involvement of the CPU.

If a CPU were to perform the move operations itself, it would be unable to perform other operations while moving data. Additionally, each move operation is inefficient, taking two cycles: one to retrieve the data and one to send it where it needs to go.

A DMA Controller sends a hold request to the CPU via the control bus, which then acknowledges the request by tri-stating the control bus and allowing the DMA to take control of the data bus. While the DMA is moving data, the CPU continues executing instructions from its internal cache memory. When the data copy is finished, the DMA releases control of the bus back to the CPU.

A DMA Controller can be integrated into a device or manage its own I/O bus connecting an array of other devices.