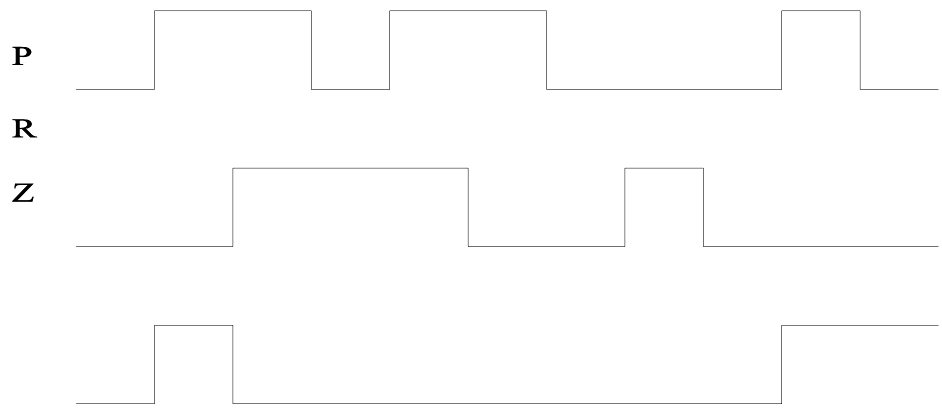
Fundamental Mode Design Example

Specification
2 inputs: Pulse (P) and Reset (R); 1 output: Z, normally 0
Z set to 1 when P changes 0 to 1 and R=0, Z is 0 when R=1

e.g.



Construct a primitive flow table (1 stable state per row).
States:

	P	R	Z	
IDLE	0	0	0	waiting for pulse
RES1	0	1	0	reset no pulse - new state
PLS1	1	0	1	pulse
RES2	1	1	0	reset after pulse
PLS2	0	0	1	pulse gone, output still 1, waiting for reset
PLSN	1	0	0	pulse, after R has gone to 1, then to 0

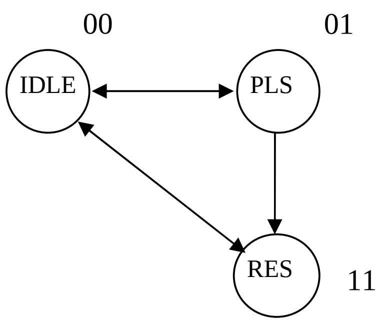
Primitive flow table:

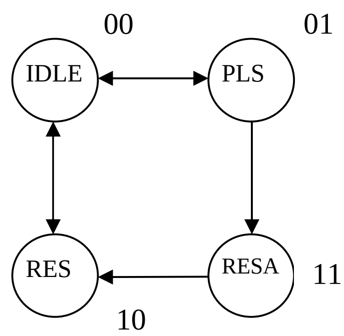
S	PR 00	01	11	10	Z
IDLE	IDLE	RES1	-	PLS1	0
RES1	IDLE	RES1	RES2	-	0
PLS1	PLS2	-	RES2	PLS1	1
RES2	-	RES1	RES2	PLSN	0
PLS2	PLS2	RES1	-	PLS1	1
PLSN	IDLE	-	RES2	PLSN	0
			S^*		

Minimise flow table By inspection, IDLE and RES1 are compatible, PLS1 and PLS2 are compatible, RES2 and PLSN are compatible. Can use formal techniques as for synchronous design.

			PR		
S	0	1	11	10	Z
IDLE	IDLE	IDLE	RES	PLS	0
PLS	PLS	IDLE	RES	PLS	1
RES	IDLE	IDLE	RES	RES	0
			S^*		

<u>Race free assignment</u> Three states require two boolean variables. However these variables are assigned to states, one transition will cause both variables to change. Therefore, we introduce a fourth state to avoid races.





Modified flow table

			PR		
S	00	01	11	10	Z
IDLE	IDLE	IDLE	RES	PLS	0
PLS	PLS	IDLE	RESA	PLS	1
RESA	-	-	RES	-	-
RES	IDLE	IDLE	RES	RES	0
			S^*		

<u>Transition Table</u>

			PR		
Y1 Y2	00	01	11	10	Z
00	00	00	10	01	0
01	01	00	11	01	1
11	-	-	10	-	-
10	00	00	10	10	0
			$Y1^* Y2^*$		

<u>Logic Equations</u> Include redundant terms to avoid hazards

$$Y1^* = P.R + P.Y1$$

$$Y2^* = Y2.\overline{R} + \overline{Y1}.Y2.P + \overline{Y1}.P.\overline{R}$$

$$Z = Y2$$